Multi-layer ceramic chip capacitors

MCH03 (0603 (0201) size, chip capacitor)

Features

- 1) Ultra miniature (0.6mm×0.3mm×0.3mm), Ultra light weight (0.3mg)
- 2) Suitable for mobile devices
- 3) Lead-free plating terminal
- 4) No polarity

Quick Reference

The design and specifications are subject to change without prior notice. Please check the most recent technical specifications prior to placing orders or using the product. For more detail information regarding packaging style code, please check product designation.

Thermal compensation

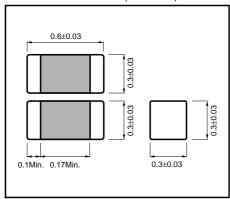
Part No.	Size code	Temperature characteristics code (ppm/°C)		Operating temp. range (°C)	Rated voltage (V)	Capacitance (pF)	Capacitance tolerance	Thickness (mm)
мсноз	MCH03 0603	A (AN)	0±250(CK) 0±120(CJ) 0±60(CH)	-55 to +125	25	0.5 to 2.7 (E12 Series) * 3.0 to 3.9 (E12 Series) * 4 to 5 (E12 Series) *	C(±0.25pF)	0.3 ± 0.03
						5.1 to 10 (E12 Series) * 11 to 100 (E12 Series)	D(±0.5pF) J(±5%)	

*: 0.5 pF/0.75 pF/2 pF/3 pF/4 pF/5 pF/6 pF/7 pF/8 pF/9 pF available

High dielectric constant

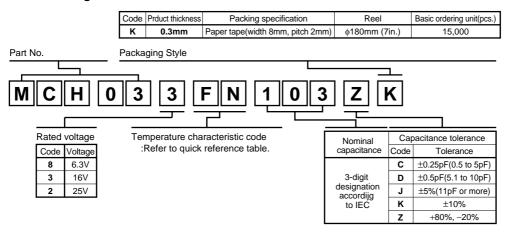
Part No.	Size code	Temperature characteristics code		Operating temp. range (°C)	Rated voltage (V)	Capacitance (pF)	Capacitance tolerance	Thickness (mm)
	0603		±10%(B)	-25 to +85	25	100 to 2,200 (E6 Series)		
			±10%(D)		16	4,700 (E3 Series)	K (±10%)	0.3 ± 0.03
		CN	±15%	-55 to +125	25	100 to 2,200 (E6 Series)		
			(R) (X7R)		16	4,700 (E3 Series)		
MCH03			±15%(X5R)	-55 to +85	6.3	10,000 (E6 Series)		
		FN	+30%, -80% (F)	-25 to +85	16	10,000 (E1 Series)	Z (+80%, -20%)	
		+22%, -82% (Y5V)		-30 to +85	16	10,000 (E1 Series)	2 (+00 /0, -20 %)	

●External dimensions (Unit : mm)





Product designation



●Product No.list

•Thermal compensation capacitors

Canacitanas	Te	mperature	A·AN(CG) (COG) (CH) Characteristic
Capacitance (pF)	Rated	d voltage (V)	25V
(pr)	Tolerance	Product thickness(mm)	Product No.
0.5			MCH032A (AN) 0R5CK
0.75			MCH032A (AN) R75CK
1.0			MCH032A (AN) 010CK
1.2		0.6 ± 0.03	MCH032A (AN) 1R2CK
1.5			MCH032A (AN) 1R5CK
1.8	C (±0.25pF)		MCH032A (AN) 1R8CK
2.0			MCH032A (AN) 020CK
2.2			MCH032A (AN) 2R2CK
2.7			MCH032A (AN) 2R7CK
3.0			MCH032A (AN) 030CK
3.3			MCH032A (AN) 3R3CK
3.9			MCH032A (AN) 3R9CK
4.0			MCH032A (AN) 040CK
4.7			MCH032A (AN) 4R7CK
5.0			MCH032A (AN) 050CK
5.6			MCH032A (AN) 5R6DK
6			MCH032A (AN) 060DK
6.8			MCH032A (AN) 6R8DK
7	D (±0.5pF)		MCH032A (AN) 070DK
8			MCH032A (AN) 080DK
8.2			MCH032A (AN) 8R2DK
9			MCH032A (AN) 090DK
10			MCH032A (AN) 100DK

0	Te	mperature	A·AN(CG) (COG) (CH) Characteristic		
Capacitance (pF)	Rate	ed voltage (V)	25V		
(ρι)	Tolerance	Product thickness(mm)	Product No.		
12			MCH032A (AN) 120JK		
15			MCH032A (AN) 150JK		
18			MCH032A (AN) 180JK		
22]		MCH032A (AN) 220JK		
27			MCH032A (AN) 270JK		
33	J (±5%)	0.6 ± 0.03	MCH032A (AN) 330JK		
39			MCH032A (AN) 390JK		
47			MCH032A (AN) 470JK		
56			MCH032A (AN) 560JK		
68			MCH032A (AN) 680JK		
82			MCH032A (AN) 820JK		
100			MCH032A (AN) 101JK		

•High dielectric constant capacitors

Conscitones	Te	mperature	CN (R) (B) (X7F	R) Characteristic	CN (X5R) Characteristic				
Capacitance (pF)	Rate	d voltage (V)	25V	16V	6.3V				
(ρι-)	Tolerance	Product thickness(mm)	Product No.	Product No.	Product No.				
100			MCH032CN101KK						
150			MCH032CN151KK						
220			MCH032CN221KK						
330				MCH032CN331KK					
470									MCH032CN471KK
680	K (±10%)	0.6 ± 0.03	MCH032CN681KK						
1,000			MCH032CN102KK						
1,500			MCH032CN152KK						
2,200			MCH032CN222KK						
4,700				MCH033CN472KK					
10,000					MCH038CN103KK				

Capacitance	Te	mperature	FN(F) (Y5V) Characteristic		
(pF)	Rate	ed voltage (V)	16V		
(ρι)	Tolerance	Product thickness(mm)	Product No.		
10.000	7 (+80% -20%)	0.6 ± 0.03	MCH033FN1037K		

•Performance and test method

No.	Items		Performance	Test Method (As per JIS C 5101-1, JIS C 5101-10)		
1	Appearance and dimensions	for appe	ons shall be as specified the	As per 4.4 of JIS C 5101-1. As per 4.5 of JIS C 5101-10 Using a Magnifier.		
2	Withstanding voltage	1	ctrical breakdown or other shall be allowed.	As per 4.6 of JIS C 5101-1. As per 4.6.4 of JIS C 5101-10 Voltage shall be applied as per Table1. Table 1 Characteristic A, AN 300% Rated voltage CN 250% Rated voltage Voltage shall be applied for 1 to 5s with 50mA charging and discharging curent.		
3	Insulation resistance	500MΩ • (For proof than 16\	than $10000 \text{M}\Omega$ or μF , whichever is less. ducts with rated voltage less \prime , it is not less than $10000 \text{M}\Omega$ $\Omega \cdot \mu\text{F}$, whichever is less.)	As per 4.5 of JIS C 5101-1. As per 4.6.3 of JIS C 5101-10 Measurements shall be made after 60+/-5s period of the rated voltage applied.		
4	Capacitance		ance shall be recified tolerance range.	As per 4.7 of JIS C 5101-1. As per 4.6.1 of JIS C 5101-10 Measurements shall be made under the conditions specified in Table 2.		
5	Dielectric loss tangent	A, AN	Capacitance < $30pF$ tan $\delta \le 100/(400+20C)\%$ Capacitance $\ge 30pF$ tan $\delta \le 0.1\%$ Rated voltage= $25V$ tan $\delta \le 3.0\%$ Rated voltage= $16V$ tan $\delta \le 5.0\%$ Rated voltage= $6.3V$ tan $\delta \le 10.0\%$	As per 4.8 of JIS C 5101-1. As per 4.6.2 of JIS C 5101-10 Measurements shall be made under the conditions specified in Table 2.		
		FN				



No.	Ite	ms		Performance	Test Method (As per JIS C 5101-1, JIS C 5101-10)		
6	Temperature characteristic			Capacitance C ≤ 2pF 0+/-250ppm/°C Capacitance C=3pF 0+/-120ppm/°C Capacitance C ≥ 4pF 0+/-60ppm/°C (-55°C to +125°C)	As per 4.24 of JIS C 5101-1. As per 4.7 of JIS C 5101-10 Temperature coefficient shall be calculated at 20°C and 85°C.		
				7R ·	As per 4.24 of JIS C 5101-1. As per 4.7 of JIS C 5101-10 If required, measurements shall be made at a given temperature.		
			F N 	+30%, -80% (-25°C to +85°C) +22%, -82% (-30°C to +85°C)			
7	Solderability			n 3/4 of each end on shall be covered with er.	As per 4.15.2 of JIS C 5101-1. As per 4.11 of JIS C 5101-10 The solder specified in JIS Z 3282 H63A shall be used. Ans the flux containing 25% rosin and ethanol solution shall be used. The specimens shall be immersed into the solder at 235+/–5°C for 2+/–0.5s So that both end terminations are completely under solder.		
8	Resistance to solderin heat	Appearance	Without m	nechanical damage.	As per 4.14 of JIS C 5101-1. As per 4.10 of JIS C 5101-10 The solder specified in JIS Z 3282. H63A		
		Change rate from initial value	A, AN	Within +/-2.5% or +/-0.25pF whichever is larger.	shall be used. The specimens shall be immersed into the solder at 260+/–5°C for 5+/–0.5s so that		
			CN	Within +/-7.5%	both end terminations are completely under the solder. Pre-heating at 150+/-10°C for 1 to 2min		
			FN	Within +/-20%	Initial measurements prior to test shall be performed after the thermal Pre-conditioning specified in Remarks (1). Final measurements shall be made after the		
		Dielectric loss tangent	Within spe	ecified initial value.	specimens have been left at room temperature as per Table3.		
		Insulation resistance	Within spe	ecified initial value.	Table3 Characteristic Time		
		Withstanding voltage	No defects	s shall be allowed.	A, AN 24+/-2 h CN, FN 48+/-4 h		
9	9 End termination adherence		peeling sh	eeling or sign of nall be allowed d terminations.	As per 4.13 of JIS C 5101-1. As per 4.8 of JIS C 5101-10 A 2N weight for 10+/-1s shall be applied to the soldered specimens as shown by the arrow mark in the below sketch. Applied pressure Substrate		

No.	lte	ems		Per	formance	(,	As p	er JIS	Test Method C 5101-1, JIS		
10	Bending strength	Appearance	Without mechanical damage.			As per 4.35 of JIS C 5101-1. As per 4.9 of JIS C 5101-10 Glass epoxy board with soldered specimens shall be bent till 1mm by 1.0mm/s.					
11	Vibration	Appearance	With	out mech	anical damage.		As per 4.17 of JIS C 5101-1 The specimens shall be soldered on the				
		Change rate from initial value	A,	AN w	apacitance shall be rithin specified blerance range.	spec Initia the	specified test jig. Initial measurements shall be made after the thermal pre-conditioning specified in Remarks(1). Final measurements shall be made after the specimens have been left at room			made after	
			С	N V	Vithin +/-7.5%	Fina					
			F	N V	Vithin +/-20%	temperature as per Table3. [Condition] Directions: 2h each X, Y and Z directions			Z directions		
		Dielectric loss tangent	With	in specifie	d initial value.	App	Total: 6h Frequency range: 10 to 55 to 10Hz(1min) Applitude: 1.5mm (shall not exceed acceleration196m/s²)			, ,	
						`	Table3				
							1	arac- eristic	Time		
							-	, AN	24+/–2 h	<u> </u>	
							CI	N, FN	48+/–4 h	1	
12	Temperature cycling	Appearance	With	out mech	anical damage.	As p	As per 4.16 of JIS C 5101-1 As per 4.12 of JIS C 5101-10 The specimens shall be soldered on the test jig shown in Remarks. Temperature cycle: 5cycles Initial				
		Change rate from initial value		A, AN	Within +/-2.5% or +/-0.25pF whichever is larger.	jig s					
			CN	Rated voltage 25V,16V	Within +/-7.5%	perf	orme	ed after	prior to test sh r the thermal g specified in F	Remarks (1).	
			CIV	Rated voltage 6.3V	Within +/-10.0%	spec	cime	ns hav	nents shall be e been left at i per Table3.	made after the room	
				FN	Within +/-20%	_		ndition	(-2)		
		D: 1				\sqcup	tep 1		emp. (°C) perating temp.	Time (min) 30+/-3	
		Dielectric loss	With	Within specified initial value.			2		oom temp.	≤ 3	
		Insulation	Within specified initial value.			┨	3	Max o	perating temp.	30+/-3	
		resistance	vviumi specineu initiai value.			4	Ro	oom temp.	≤ 3		
		Withstanding	No defects shall be allowed.		-			Table3			
		voltage	INO U	1616613 3116	all be allowed.		1	arac-	Time		
								eristic ., AN	24+/–2 h		
						CN, FN 48+/-4 h					

No.	Ite	ems		Per	formance		(As per JIS	Test Method S C 5101-1, JIS C 5	101-10)	
13	Humidity	Appearance	With	out mecha	anical damage.			f JIS C 5101-1		
	(Steady)	Change rate from initial value	Д	, AN	Within +/-5.0% or +/-0.5pF whichever is larger.	Te Re	IS C 5101-10 Fest temperature : 60+/-2°C Relative humidity : 90 to 95% Fest time : 500 +24/-0 h			
			CN	Rated voltage 25V,16V	Within +/-12.5%	Ini be	Initial measurements prior to test shall be made after the voltage pre-conditioning specified in Remarks (2). Final measurements have been left at room temperature as per Table3.			
				Rated voltage 6.3V	Within +/-25.0%	Re Fir				
				FN	Within +/-30.0%		·	·		
		Dielectric tangent	А	, AN	tan δ ≤ 0.3%			Table3		
		tangent		C N	Less than 200% of initial spec.		Charac- teristic	Time		
				FN	Less than 150% of initial spec.		A, AN	24+/–2 h		
		Insulation resistance	50Mg (For politage) than	Ω•μF, whi products v ge less tha	000MΩ or chever is less. vith rated an 16V, it is not less or 10MΩ • μF,	CN, FN 48+/-4 h				
14	Humidity	Appearance	With	out mecha	anical damage.	As per 4.22 of JIS C 5101-1				
	life test	Change rate from initial value	Α	, AN	Within +/-7.5% or +/-0.75pF whichever is larger.	Te Re	As per 4.14 of JIS C 5101-10 Test temperature: 60+/–2°C Relative humidity: 90 to 95% Voltage: Rated voltage			
			CN	Rated voltage 25V,16V	Within +/-12.5%	Te Ini	est time : 50 tial measur	00 +24/–0 h ements prior to test	shall	
			CN	Rated voltage 6.3V	Within +/-25.0%	Re	emarks (2).	ng specified in ements shall be mad	de after	
				FN	Within +/-30.0%	1		s have been left at r	oom	
		Dielectric loss	Α	, AN	tan δ ≤ 0.5%	ter	nperature a	as per Table3.		
		tangent		CN	Less than 200% of initial spec.			Table3		
				FN	Less than 150% of initial spec.		Charac- teristic	Time		
		Insulation resistance	than 16V, it is r		chever is less. with rated voltage less not less than 500mΩ		A, AN CN, FN	24+/-2 h 48+/-4 h		
			or 5N	112• μF, WI	hichever is less.)					

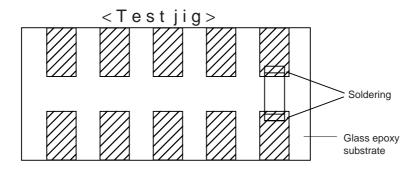
No.	Ite	ms	Performance				(As p	Test Ner JIS C 5101-	Method 1, JIS C 5	5101-10)	
15	Heat life test	Appearance Change		out mecha	anical damage. Within +/-3.0% or			.23 of JIS C 51 .15 of JIS C 51			
		rate from initial value			+/-0.3pF whichever is larger.			Test temperature(°C)	Voltage	Test time (h)	
				Rated voltage 25V,16V	Within +/-15.0%	A,	, AN	125	200%	1000	
		Rated Within +/-25.0%		CN	CN	85	Rated voltage 200%	+48/-0			
				6.3V F N	Within +/-30.0%			(B, X5R)	Rated voltage	+48/-0	
		Dielectric loss	A	A, AN	tan δ ≤ 0.3%			125 (R, X7R)	200% Rated voltage		
	tangent		ngent C N		Less than 200% of initial spec.		FN	85	200% Rated voltage	1000 +48/–0	
			FN		Less than 150% of initial spec.		Initial measurements prior to test shall be made after the voltage pre-conditioning				
		Insulation resistance	istance 50MΩ • μF, whi (For products when 16V, it is r		chever is less. vith rated voltage less oot less than 1000mΩ	$0 M\Omega$ or specified Final measured voltage less ess than $1000 m\Omega$ temperat			specified in Remarks (2). Final measurements shall be made after the specimens have been left at room temperature		
		or $10M\Omega \cdot \mu F$, whichever is less.)		villeriever is less.)			Table3				
								Charac- teristic	Time		
									24+/-2 h 48+/-4 h		
								, I			

[Remarks]

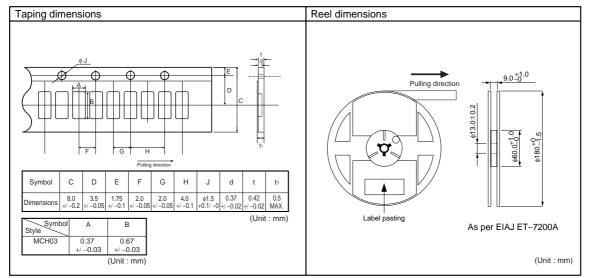
Pre-conditioning

If specified in test method of as per 3(Performance and test merhod), capacitors of CN, FN characteristics shall be pre-conditionded as follows.

- (1) Thermal pre-conditioning
 - Prior to initial measurements, specimens shall be conditioned at a temperature of 150 $\,$ 0/ -10° C for a period of 1hr., and shall be allowed to stabilize at room temperature for 48+/-4h
- (2) Voltage pre-conditioning



Packaging specifications



(1) The quantity for one reel is as bellows.

Kind of reel	Corios	Paper tape				
Kind of reel	Series	Quantity	Symbol			
φ180 reel	MCH03	15,000 pcs.	K			

- (2) When the tape is pulled out towards the operator with the cover tape facing upward, the feeding holes shall be found on the right portion of the tape.
- (3) Specification of beginning and ending of the tape are as follows.

Ending(reel's center) : Approx. 300mm (no chips) Beginning(reel's round) : Approx. 270mm (no chips)

: Approx. 30mm (no pasted tape) : Approx. 260mm (cover tape only)

- (4) No juncture of tape shall be allowed.
- (5) The share strength of tape shall be more than 5N at the break down strength.
- (6) The peel strength of the cover tape shall be 0.1 to 0.7(N) when the cover tape are peeled 0 to 15° degree from the surface.
- (7) The number of missing components shall not exceed 0.1% of the total number of components (marked number) or one whichever is the larger, and no consecutive missing exceeding two is allowed.
- (8) The reels made from resin shall be used, as per EIAJ ET-7200A.

Marking

No marking shall be performed on the chip.

Trademark, parts number, quantity, lot No., and country of origin shall be labeled on each reel, bulk case.

Numbering system for LOT No.

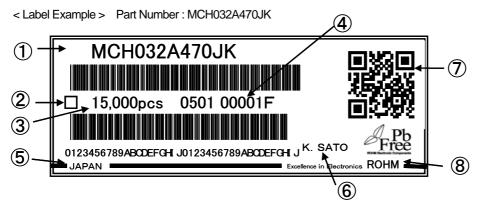
Example

03	01	_A0001	J
(1)	(2)	(3)	(4)

- (1) The end of the Christian Era < two digits> of production finish.
- (2) Week in completing part of production finish.
- (3) Manufacture continuity number.
- (4) The symbol of manufacturing plant.

Label expression

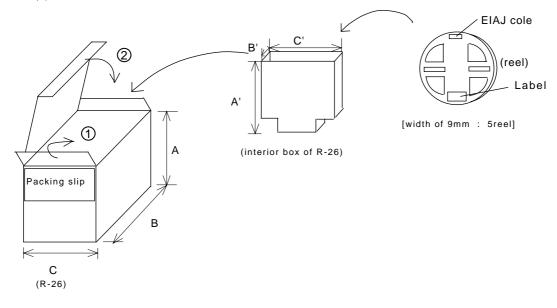
The Figure below is label expression



- 1 Part Number
- ② Division cord
- 3 Quantity
- 4 Lot No.
- (5) The Country of origin
- 6 Inspector
- ⑦ QR code
- 8 Trademark

Packing method

1) ϕ 180mm Reel



< Packaging unit >

Symbol	K
Quantity of reel in interior box	5
Quantity of reel in box of R-26	20

Dimensions	Packaging		
	R-26	interior box of R-26	
A (A')	195	185	
B (B')	255	60	
C (C')	190	185	

(Unit:mm)

< Appearance > Carton

< Accumulation >

You must do accumulation by ten boxes

< Packaging slip >

- 1. Customer
- 2. Parts number
- 3. Quantity
- 4. Box quantity
- 5. Trade mark

●Weight / Piece

(Unit : mg

				(Unit : mg)
Size	Item	Thickness	Characteristic	Weight / Piece
0603 (0201)	MCH03	0.3mm	A, AN	0.3
			CN	0.3
			FN	0.3

(Note) The measured values in the table are for reference only.

Actual weight of these chips may very slightly lot by lot.

•Electrical characteristics

■A (C0G) Characteristics

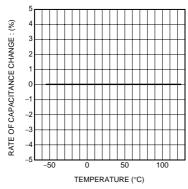


Fig.1 Capacitance-temperature characteristics

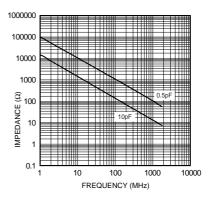


Fig.2 Impedance-frequency characteristics

■CN (X7R) Characteristics

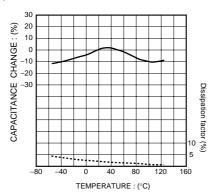


Fig.3 Capacitance-temperature characteristics

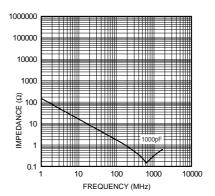


Fig.4 Impedance-frequency characteristics

■FN (Y5V) Characteristics

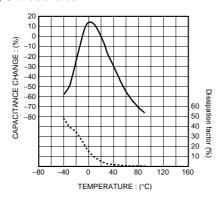


Fig.5 Capacitance-temperature characteristics



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 use and operation. Please pay careful attention to the peripheral conditions when designing circuits
 and deciding upon circuit constants in the set.
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