

Automotive-grade N-channel 40 V, 1.1 mΩ typ., 200 A STripFET™ F6 Power MOSFETs in H²PAK-2 and H²PAK-6

Datasheet - production data

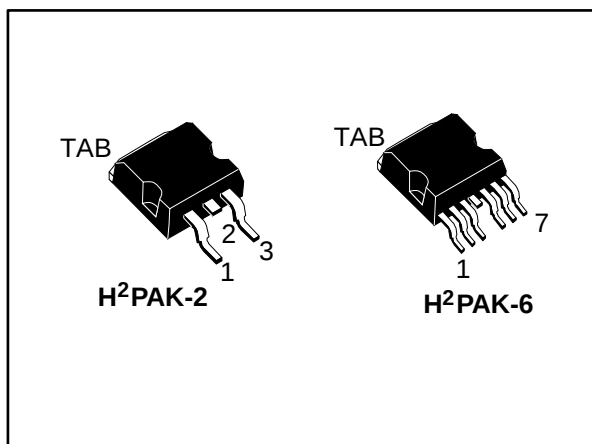
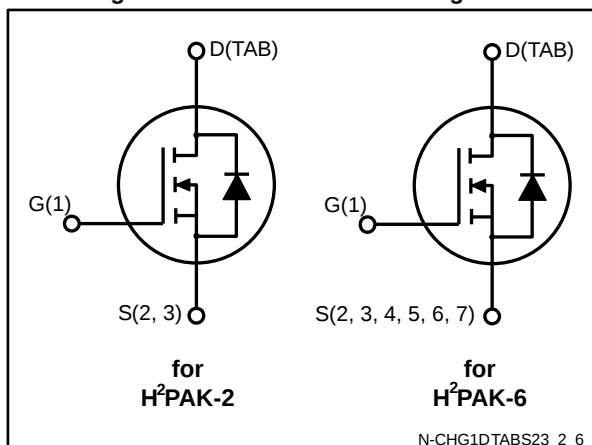


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max	I _D
STH320N4F6-2	40 V	1.3 mΩ	200 A
STH320N4F6-6			

- AEC-Q101 qualified
- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss



Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using the STripFET™ F6 technology with a new trench gate structure. The resulting Power MOSFETs exhibit very low R_{DS(on)} in all packages.

Table 1: Device summary

Order code	Marking	Package	Packaging
STH320N4F6-2	320N4F6	H ² PAK-2	Tape and reel
STH320N4F6-6		H ² PAK-6	

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	200	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	200	A
$I_{DM}^{(2)}$	Drain current (pulsed)	800	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	340	W
I_{AS}	Not-repetitive avalanche current	160	A
E_{AS}	Single pulse avalanche energy	920	mJ
T_{stg}	Storage temperature range	- 55 to 175	$^{\circ}\text{C}$
T_j	Operating junction temperature range		

Notes:

⁽¹⁾Current value is limited by package.

⁽²⁾Pulse width is limited by safe operating area.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.44	$^{\circ}\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	35	$^{\circ}\text{C/W}$

Notes:

⁽¹⁾When mounted on FR-4 board of 1 inch², 2 oz Cu.

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V, I _D = 250 μA	40			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 40 V			1	μA
		V _{GS} = 0 V, V _{DS} = 40 V, T _C = 125 °C ⁽¹⁾			100	μA
I _{GSS}	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2		4	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 80 A		1.1	1.3	mΩ

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 15 V, f = 1 MHz, V _{GS} = 0 V	-	13800	-	pF
C _{oss}	Output capacitance		-	1870	-	pF
C _{rss}	Reverse transfer capacitance		-	1095	-	pF
Q _g	Total gate charge	V _{DD} = 20 V, I _D = 160 A, V _{GS} = 0 to 10 V (see Figure 14: "Test circuit for gate charge behavior")	-	240	-	nC
Q _{gs}	Gate-source charge		-	59	-	nC
Q _{gd}	Gate-drain charge		-	75.2	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 20 V, I _D = 80 A, R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform")	-	28	-	ns
t _r	Rise time		-	98	-	ns
t _{d(off)}	Turn-off-delay time		-	190	-	ns
t _f	Fall time		-	95	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		200	A
$I_{SDM}^{(2)}$	Source-drain current (pulsed)		-		800	A
$V_{SD}^{(3)}$	Forward on voltage	$I_{SD} = 80\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 160\text{ A}$, $V_{DD} = 32\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 150\text{ }^{\circ}\text{C}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	58.7		ns
Q_{rr}	Reverse recovery charge		-	99.2		nC
I_{RRM}	Reverse recovery current		-	3.38		A

Notes:

⁽¹⁾Current value is limited by package.

⁽²⁾Pulse width is limited by safe operating area

⁽³⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

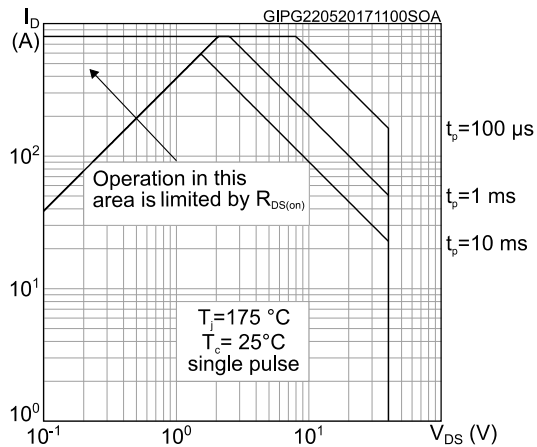


Figure 3: Thermal impedance

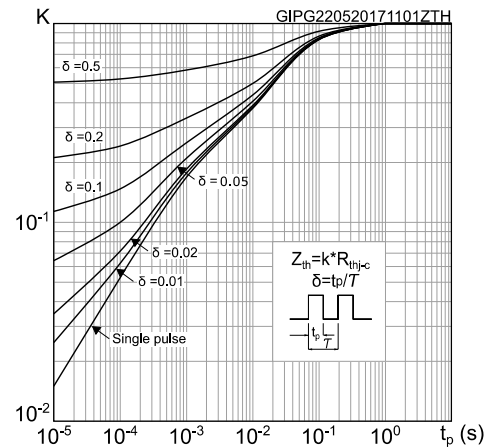


Figure 4: Output characteristics

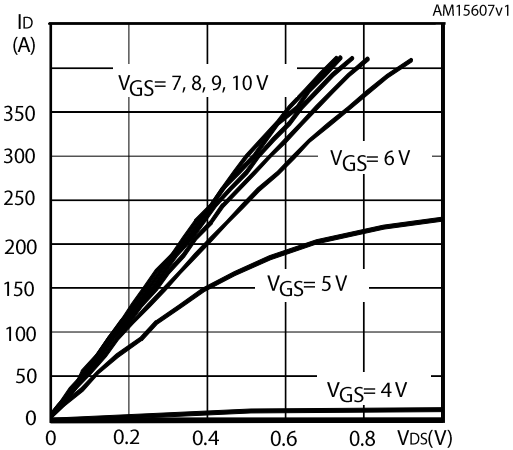


Figure 5: Transfer characteristics

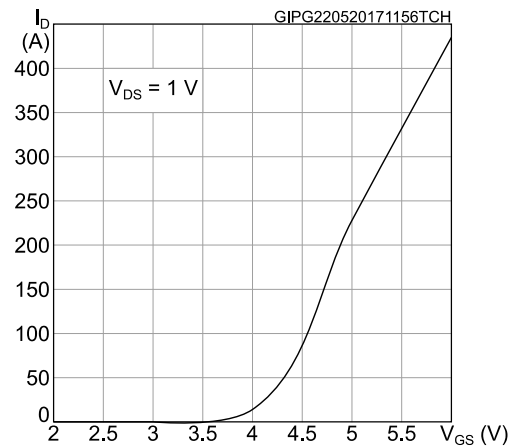


Figure 6: Gate charge vs. gate-source voltage

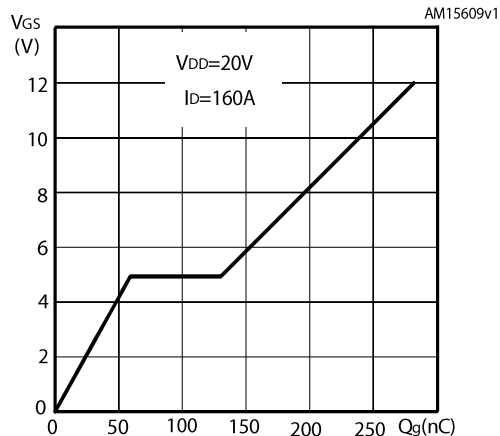


Figure 7: Static drain-source on-resistance

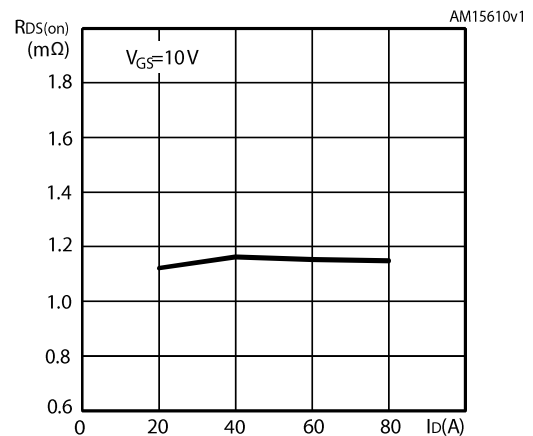


Figure 8: Capacitance variations

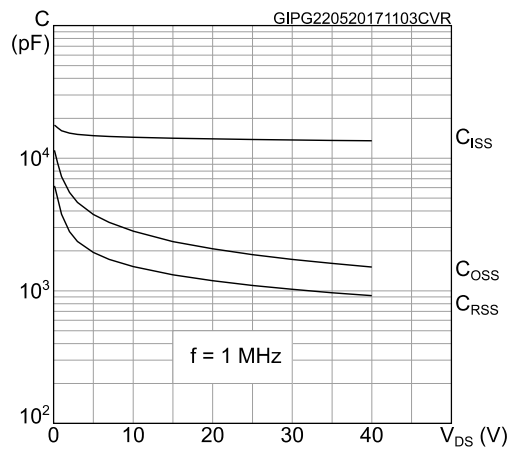


Figure 9: Drain-source diode forward characteristics

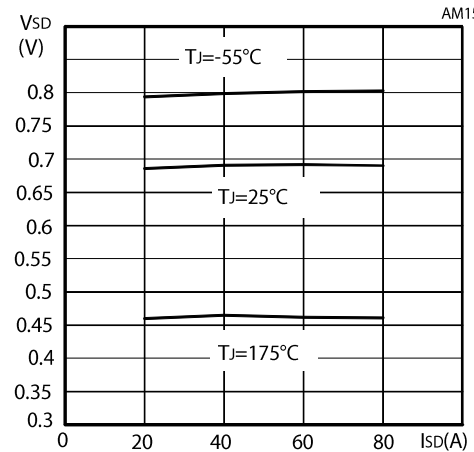


Figure 10: Normalized gate threshold voltage vs. temperature

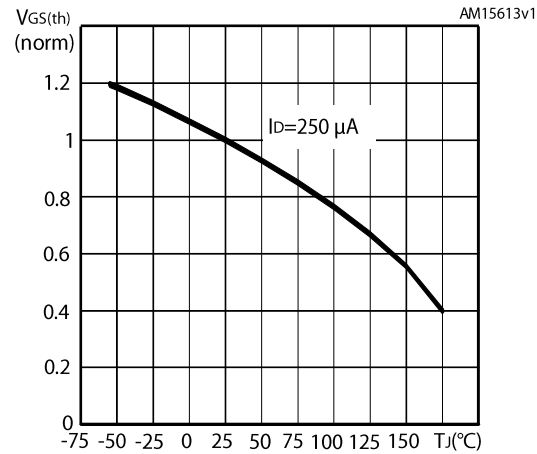


Figure 11: Normalized on-resistance vs. temperature

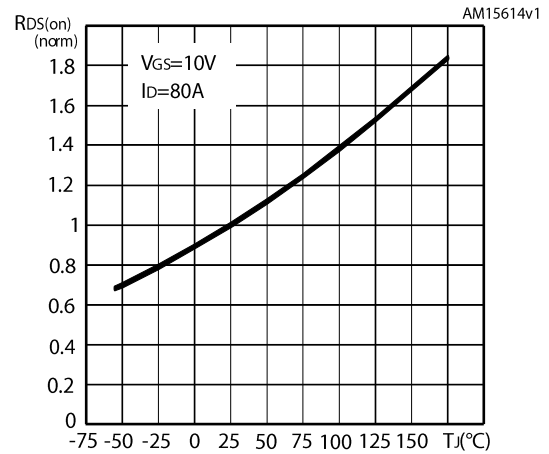
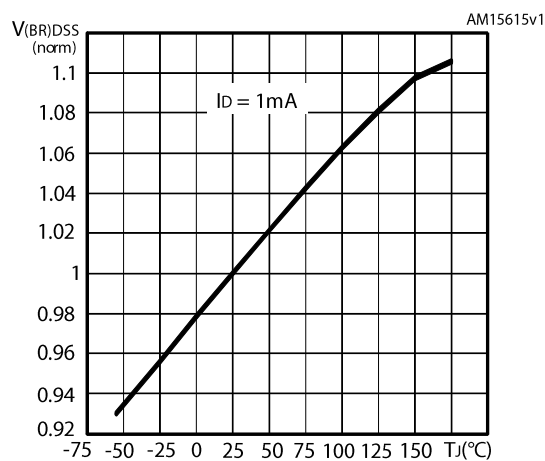


Figure 12: Normalized $V_{(BR)DSS}$ vs temperature



3 Test circuits

Figure 13: Test circuit for resistive load switching times

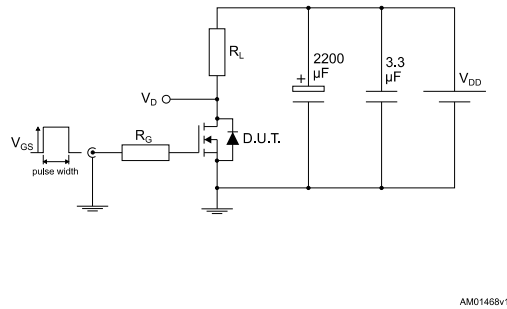


Figure 14: Test circuit for gate charge behavior

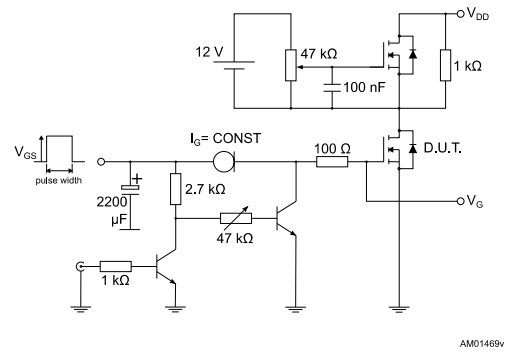


Figure 15: Test circuit for inductive load switching and diode recovery times

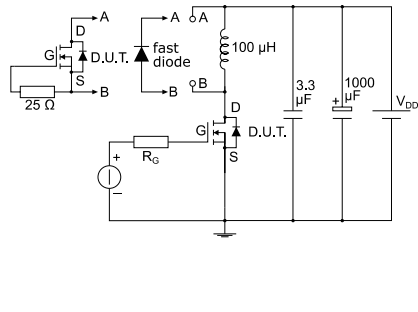


Figure 16: Unclamped inductive load test circuit

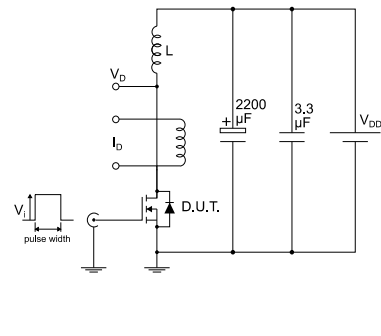


Figure 17: Unclamped inductive waveform

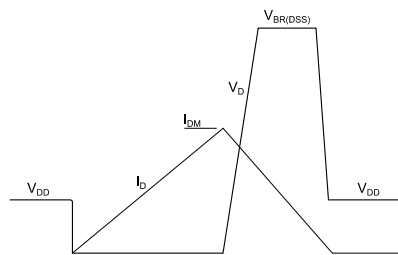
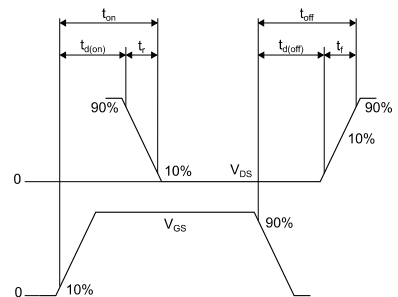


Figure 18: Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

4.1 H²PAK-2 mechanical data

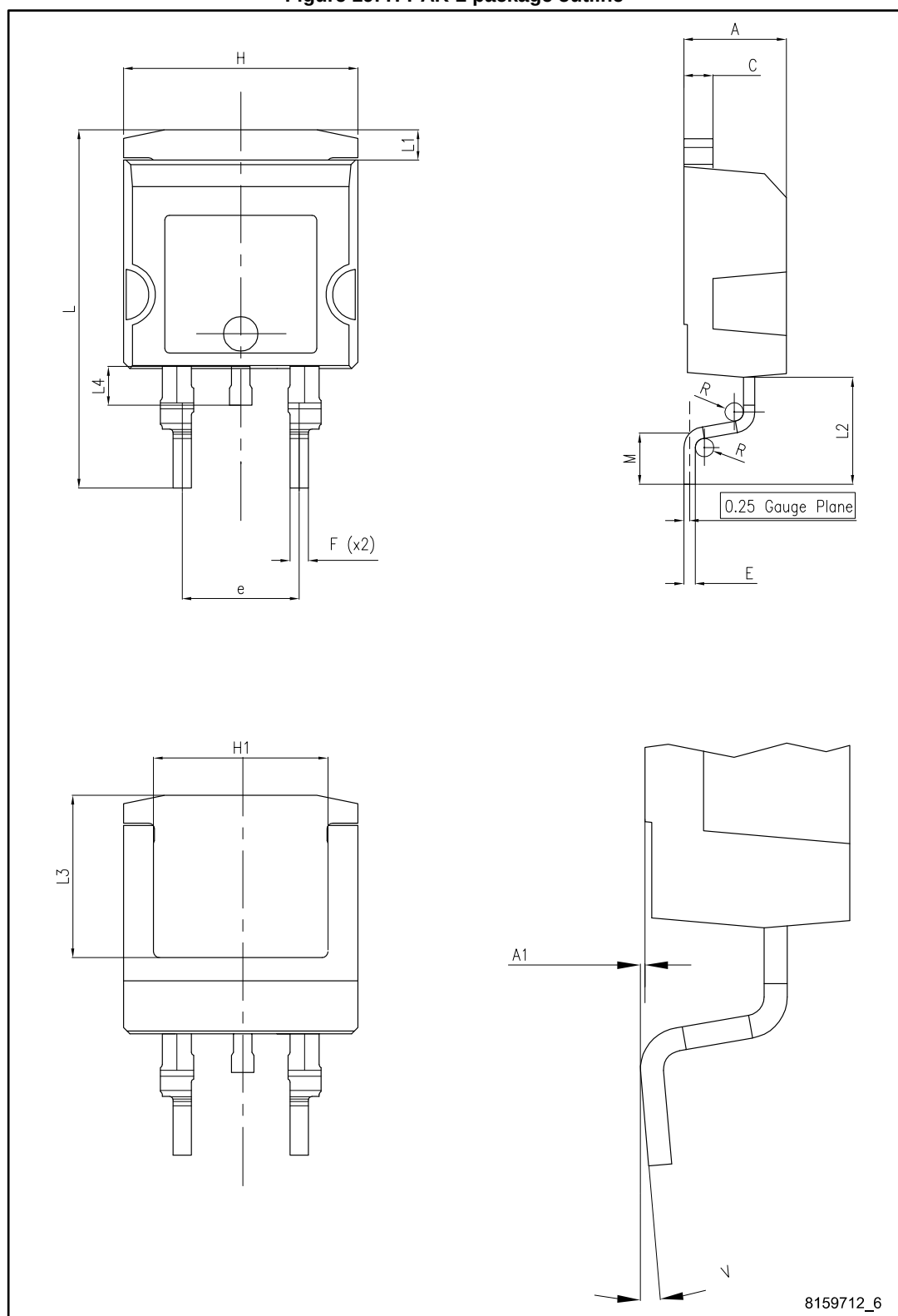
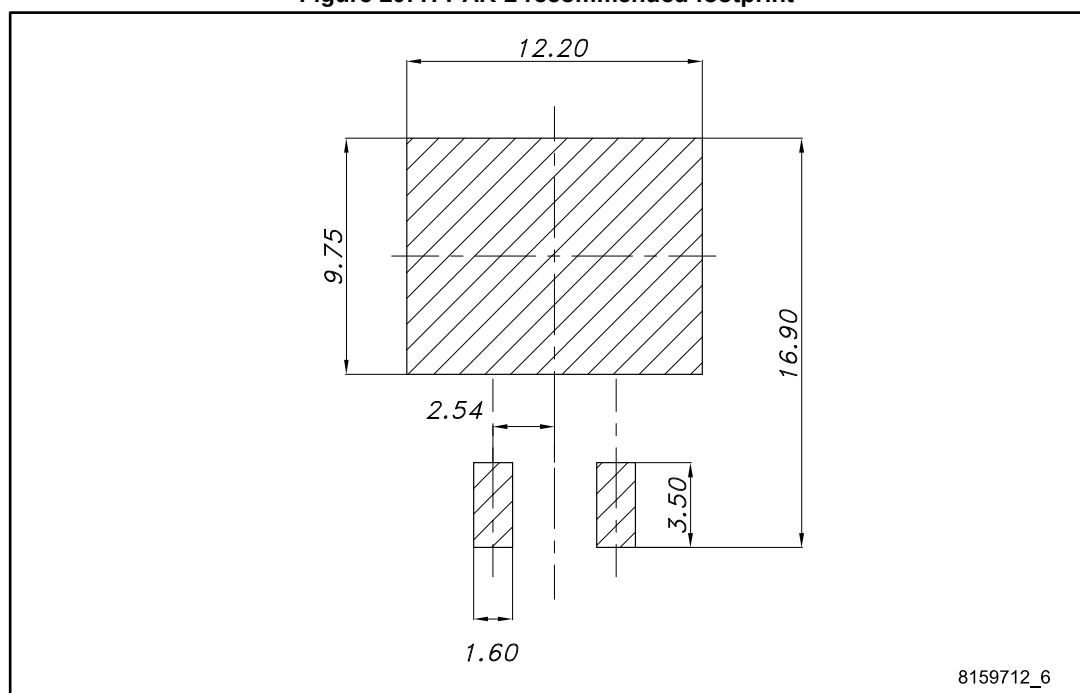
Figure 19: H²PAK-2 package outline

Table 8: H²PAK-2 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30	-	4.70
A1	0.03		0.20
C	1.17		1.37
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
H	10.00		10.40
H1	7.40		7.80
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.5		1.7
M	2.6		2.9
R	0.20		0.60
V	0°		8°

Figure 20: H²PAK-2 recommended footprint



4.2 H²PAK-6 mechanical data

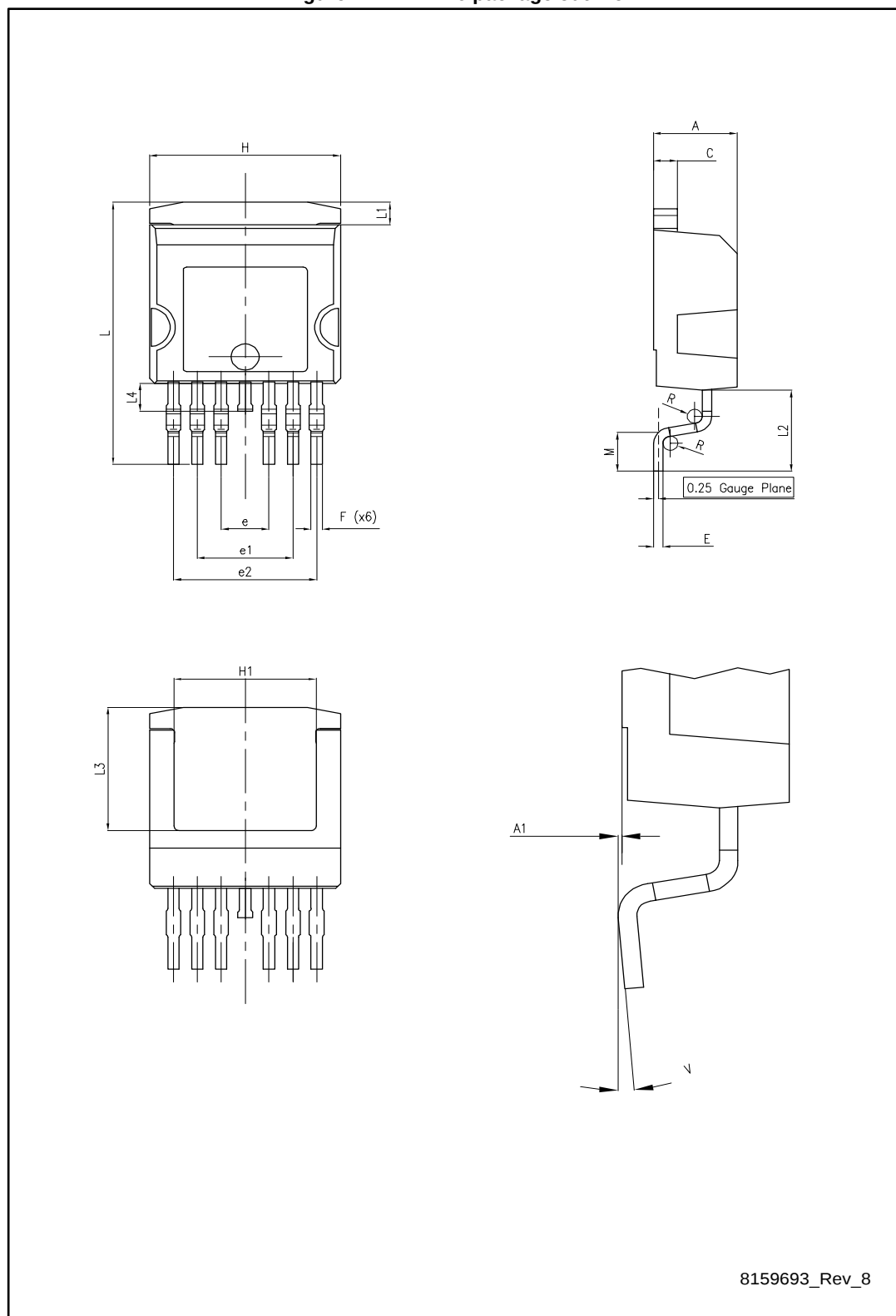
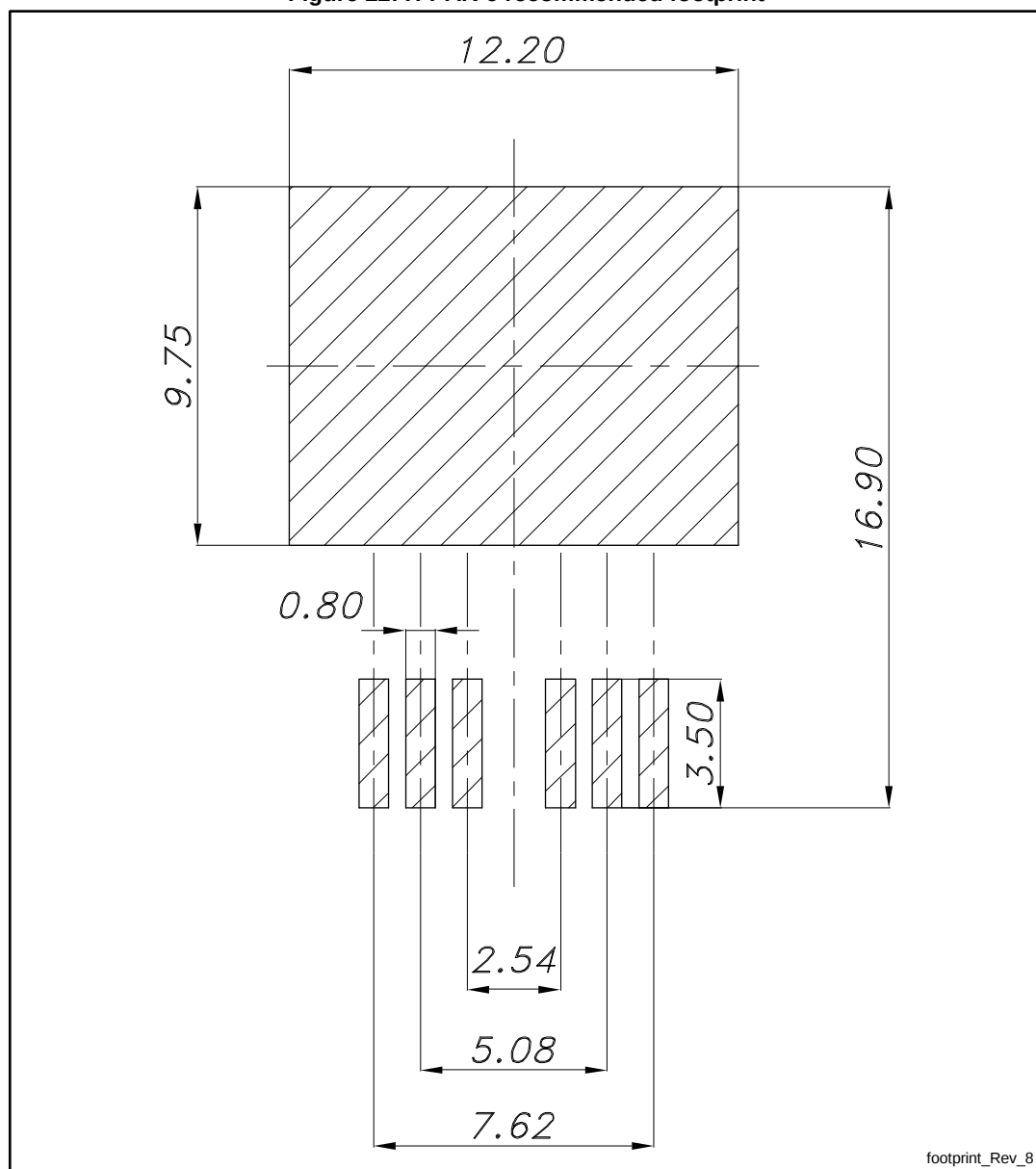
Figure 21: H²PAK-6 package outline

Table 9: H²PAK-6 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.70
A1	0.03		0.20
C	1.17		1.37
e	2.34	2.54	2.74
e1	4.88		5.28
e2	7.42		7.82
E	0.45		0.60
F	0.50		0.70
H	10.00		10.40
H1	7.40		7.80
L	14.75		15.25
L1	1.27		1.40
L2	4.35		4.95
L3	6.85		7.25
L4	1.50		1.75
M	1.90		2.50
R	0.20		0.60
V	0°		8°

Figure 22: H²PAK-6 recommended footprint

Dimensions are in mm.

4.3 Packaging information

Figure 23: Tape outline

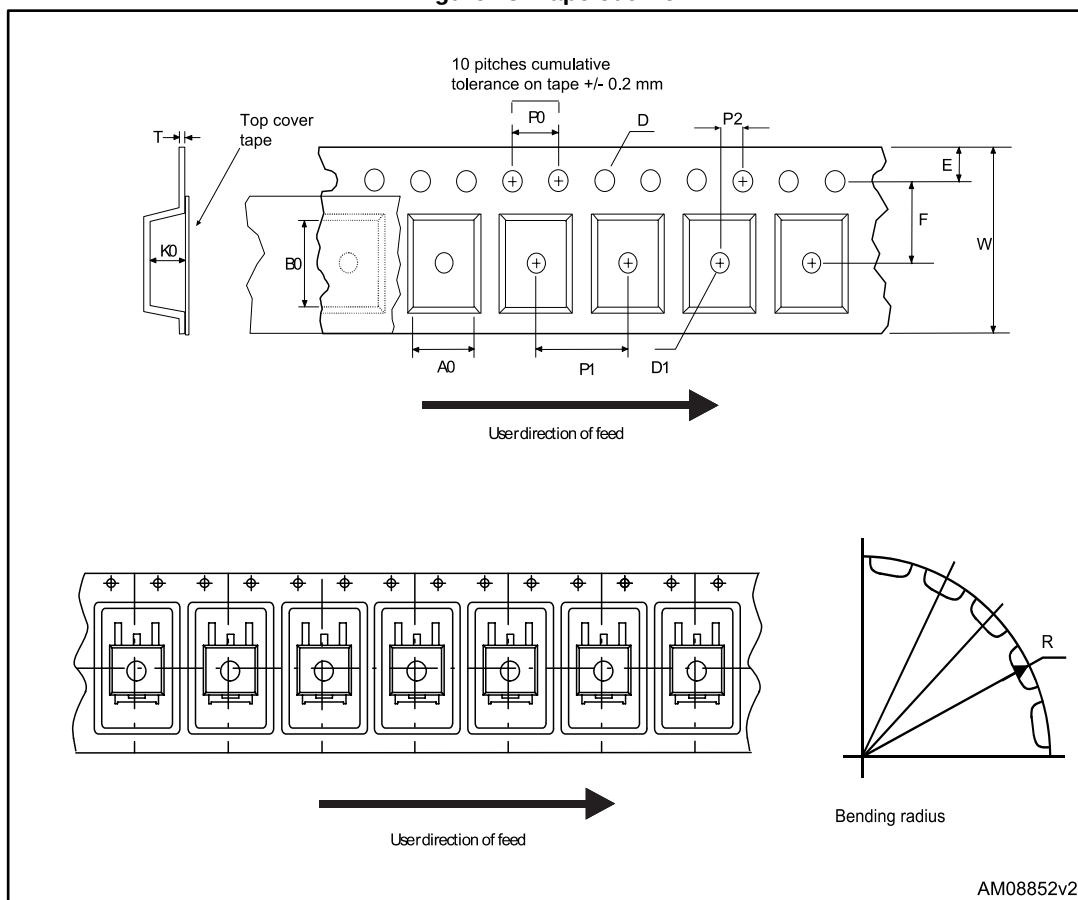


Figure 24: Reel outline

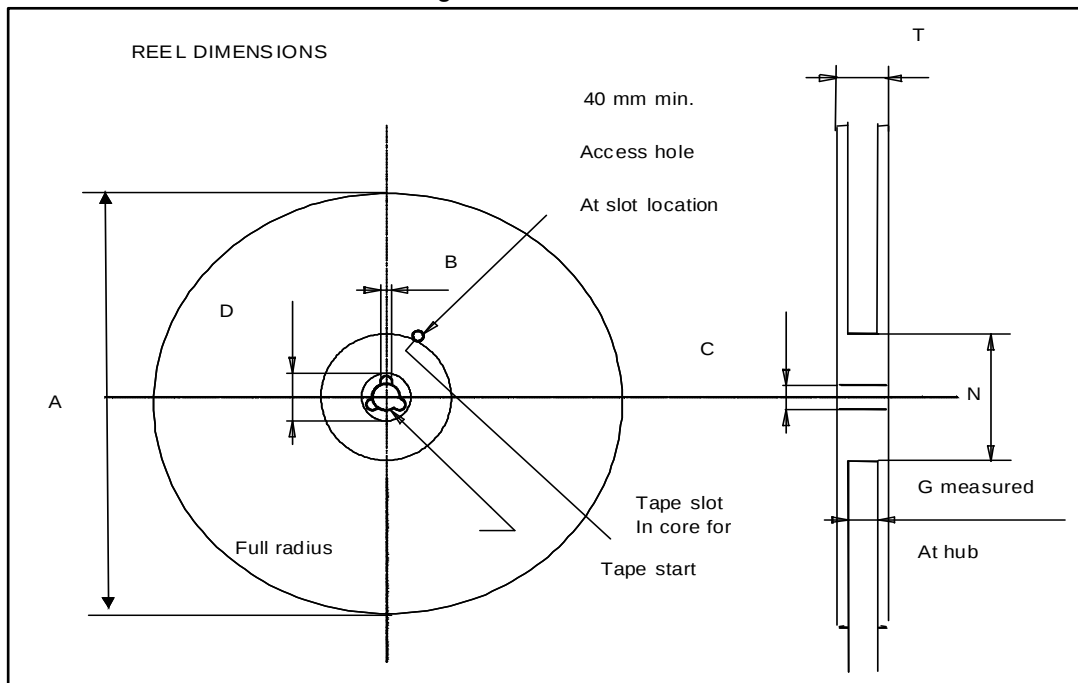


Table 10: Tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
01-Feb-2013	1	First release.
12-May-2017	2	Modified title and features on cover page. Updated Section 4: "Package mechanical data". Modified Figure 2: "Safe operating area", Figure 3: "Thermal impedance", Figure 5: "Transfer characteristics" and Figure 8: "Capacitance variations". Minor text changes.
29-May-2017	3	Modified Table 2: "Absolute maximum ratings" . Minor text changes.

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