



Rev. 1.0

AS7C316098B

1024K X 16 BIT HIGH SPEED CMOS SRAM

REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issued	June 2014



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FEATURES

- Fast access time : 10ns
- **low power consumption:**
Operating current : 70mA (TYP.)
Standby current : 4mA(TYP.)
- Single 3.3V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data byte control : LB# (DQ0 ~ DQ7)
UB# (DQ8 ~ DQ15)
- Data retention voltage : 1.5V (MIN.)
- **All parts are ROHS Compliant**
- Package : 54-pin 400 mil TSOP-II

GENERAL DESCRIPTION

The AS7C316098B is a 16M-bit high speed CMOS static random access memory organized as 1024K words by 16 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The AS7C316098B operates from a single power supply of 3.3V and all inputs and outputs are fully TTL compatible

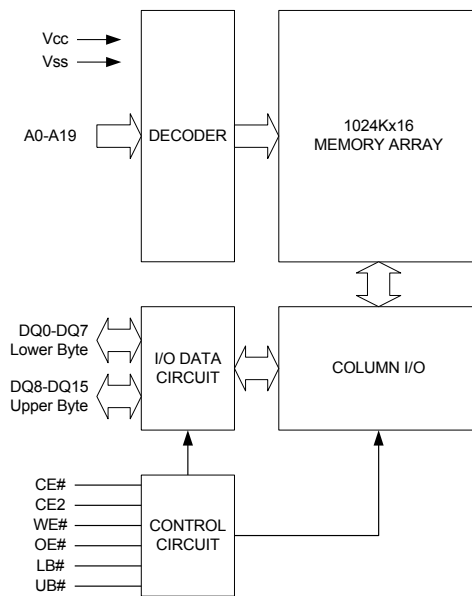
Table 1. Speed Grade Information

Product Family	Vcc Range	Speed	Power Dissipation	
			Standby(I_{SB1} , TYP.)	Operating(I_{CC} , TYP.)
AS7C316098B	2.7 ~ 3.6V	10ns	4mA	70mA

Table 2. Ordering Information

Product part No	Org	Temperature	Package
AS7C316098B-10TIN	1024K x 16	Industrial -40°C to 85°C	54-pin 400mil TSOP-II

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A19	Address Inputs
DQ0 – DQ15	Data Inputs/Outputs
CE#, CE2	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
LB#	Lower Byte Control
UB#	Upper Byte Control
Vcc	Power Supply
Vss	Ground

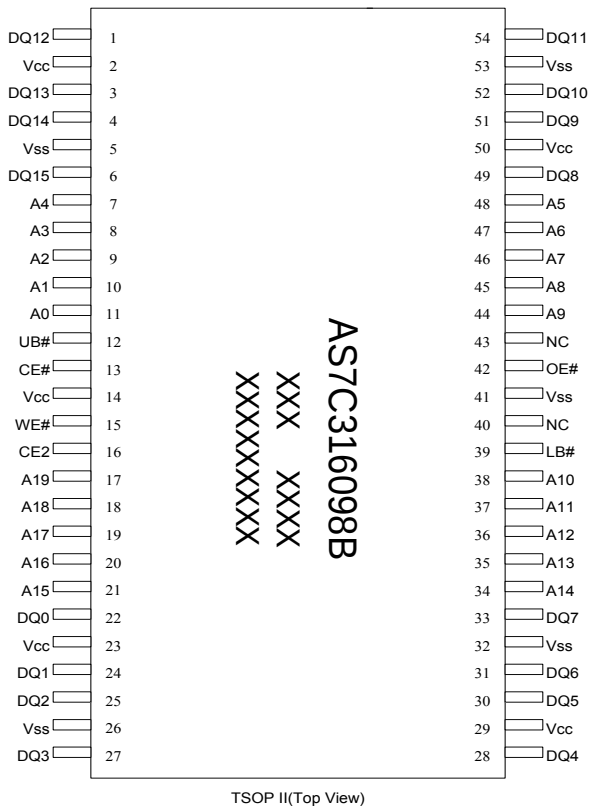


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PIN CONFIGURATION





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ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on Vcc relative to Vss	V_{T1}	-0.5 to 4.6	V
Voltage on any other pin relative to Vss	V_{T2}	-0.5 to Vcc+0.5	V
Operating Temperature	T_A	-40 to 85(I grade)	°C
Storage Temperature	T_{STG}	-65 to 150	°C
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	LB#	UB#	I/O OPERATION		SUPPLY CURRENT
							DQ0-DQ7	DQ8-DQ15	
Standby	H	X	X	X	X	X	High – Z	High – Z	I_{SB1}
	X	L	X	X	X	X	High – Z	High – Z	
Output Disable	L	H	H	H	L	X	High – Z	High – Z	I_{CC}
	L	H	H	H	X	L	High – Z	High – Z	
Read	L	H	L	H	L	H	D_{OUT}	High – Z	I_{CC}
	L	H	L	H	H	L	High – Z	D_{OUT}	
	L	H	L	H	L	L	D_{OUT}	D_{OUT}	
Write	L	H	X	L	L	H	D_{IN}	High – Z	I_{CC}
	L	H	X	L	H	L	High – Z	D_{IN}	
	L	H	X	L	L	L	D_{IN}	D_{IN}	

Note: H = V_{IH} , L = V_{IL} , X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYM.	TEST CONDITION		MIN.	TYP. ⁴	MAX.	UNIT
Supply Voltage	V _{CC}			2.7	3.3	3.6	V
Input High Voltage	V _{IH} ¹			2.2	-	V _{CC} +0.3	V
Input Low Voltage	V _{IL} ²			- 0.3	-	0.8	V
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}		- 1	-	1	μA
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled		- 1	-	1	μA
Output High Voltage	V _{OH}	I _{OH} = -4mA		2.4	-	-	V
Output Low Voltage	V _{OL}	I _{OL} = 8mA		-	-	0.4	V
Average Operating Power supply Current	I _{CC}	CE# ≤0.2V and CE2≥ V _{CC} -0.2V, other pins at 0.2V or V _{CC} -0.2V, I _{I/O} = 0mA; f=max.	-10	-	70	120	mA
Standby Power Supply Current	I _{SB1}	CE# ≥ V _{CC} - 0.2V; other pins at 0.2V or V _{CC} -0.2V.		-	4	40	mA

Notes:

- $V_{IH(MAX)} = V_{CC} + 2.0V$ for pulse width less than 6ns.
- $V_{IL(MIN)} = V_{SS} - 2.0V$ for pulse width less than 6ns.
- Over/Undershoot specifications are characterized on engineering evaluation stage, not for mass production test.
- Typical values are included for reference only and are not guaranteed or tested.
Typical valued are measured at $V_{CC} = V_{CC(TYP)}$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	8	pF
Input/Output Capacitance	$C_{I/O}$	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

speed	10ns
Input Pulse Levels	0.2V to $V_{CC}-0.2V$
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	$V_{CC}/2$
Output Load	$C_L = 30\text{pF} + 1\text{TTL}$, $I_{OH}/I_{OL} = -8\text{mA}/4\text{mA}$

AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	AS7C316098B-10		UNIT
		MIN.	MAX.	
Read Cycle Time	t_{RC}	10	-	ns
Address Access Time	t_{AA}	-	10	ns
Chip Enable Access Time	t_{ACE}	-	10	ns
Output Enable Access Time	t_{OE}	-	4.5	ns
Chip Enable to Output in Low-Z	t_{CLZ}^*	2	-	ns
Output Enable to Output in Low-Z	t_{OLZ}^*	0	-	ns
Chip Disable to Output in High-Z	t_{CHZ}^*	-	4	ns
Output Disable to Output in High-Z	t_{OHZ}^*	-	4	ns
Output Hold from Address Change	t_{OH}	2	-	ns
LB#, UB# Access Time	t_{BA}	-	4.5	ns
LB#, UB# to High-Z Output	t_{BHZ}^*	-	4	ns
LB#, UB# to Low-Z Output	t_{BLZ}^*	0	-	ns

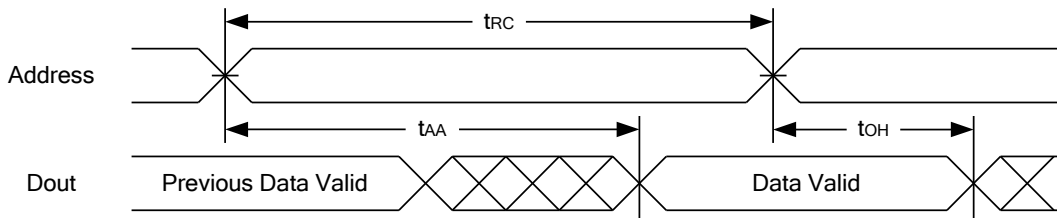
(2) WRITE CYCLE

PARAMETER	SYM.	AS7C316098B-10		UNIT
		MIN.	MAX.	
Write Cycle Time	t_{WC}	10	-	ns
Address Valid to End of Write	t_{AW}	8	-	ns
Chip Enable to End of Write	t_{CW}	8	-	ns
Address Set-up Time	t_{AS}	0	-	ns
Write Pulse Width	t_{WP}	8	-	ns
Write Recovery Time	t_{WR}	0	-	ns
Data to Write Time Overlap	t_{DW}	6	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	ns
Output Active from End of Write	t_{OW}^*	2	-	ns
Write to Output in High-Z	t_{WHZ}^*	-	4	ns
LB#, UB# Valid to End of Write	t_{BW}	8	-	ns

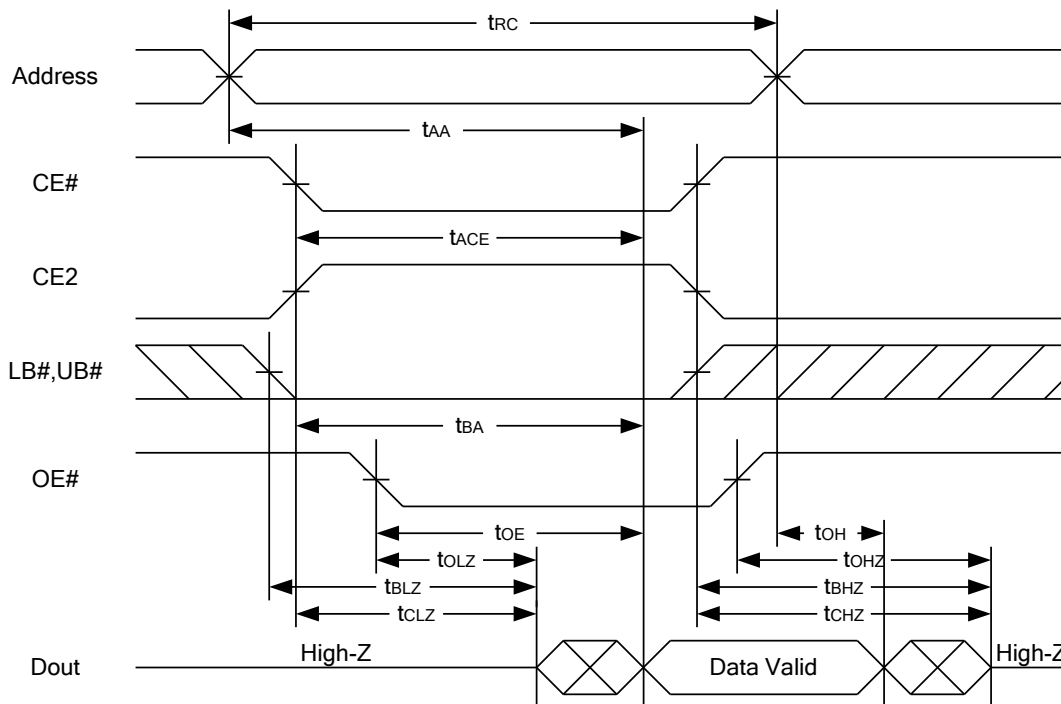
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



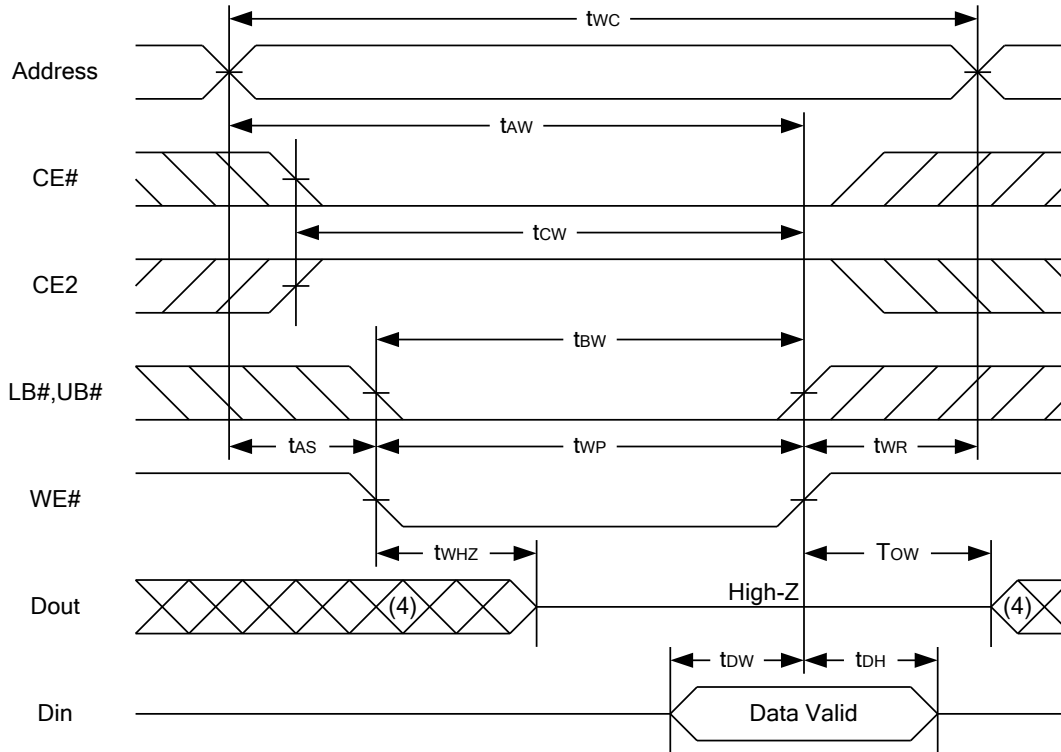
READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)



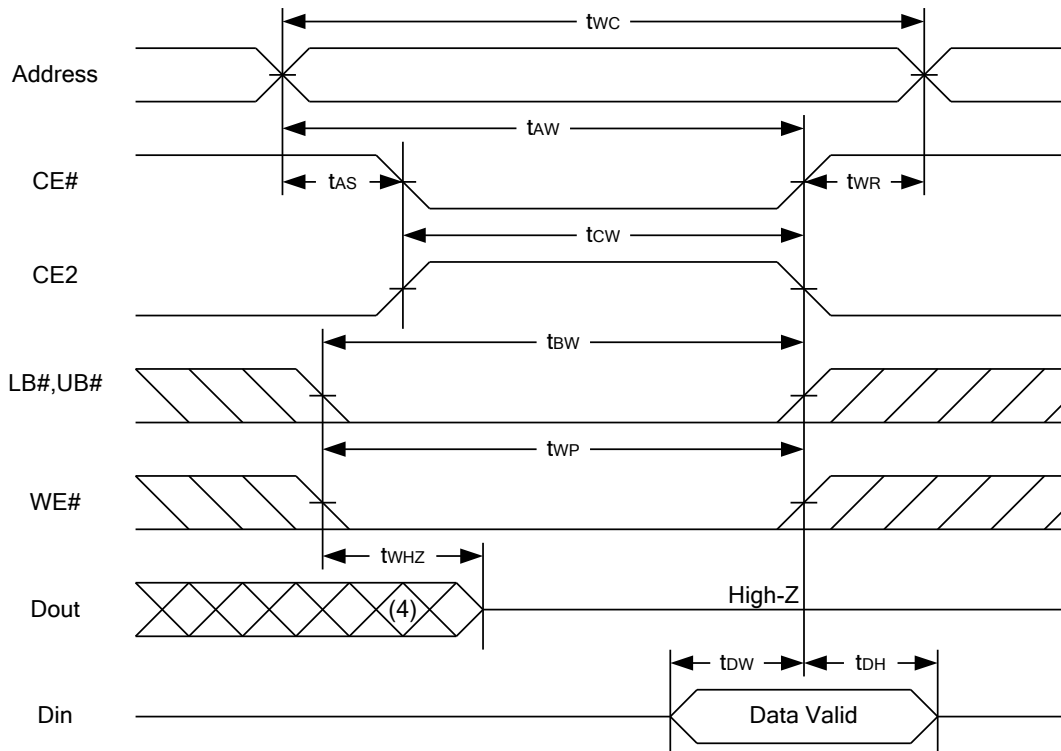
Notes :

- WE# is high for read cycle.
- Device is continuously selected OE# = low, CE# = low, CE2 = high, LB# or UB# = low.
- Address must be valid prior to or coincident with CE# = low, CE2 = high, LB# or UB# = low transition; otherwise tAA is the limiting parameter.
- tCLZ, tBLZ, tOLZ, tCHZ, tBHZ and tOHZ are specified with CL = 5pF. Transition is measured ±500mV from steady state.
- At any given temperature and voltage condition, tCHZ is less than tCLZ, tBHZ is less than tBLZ, tOHZ is less than tOLZ.

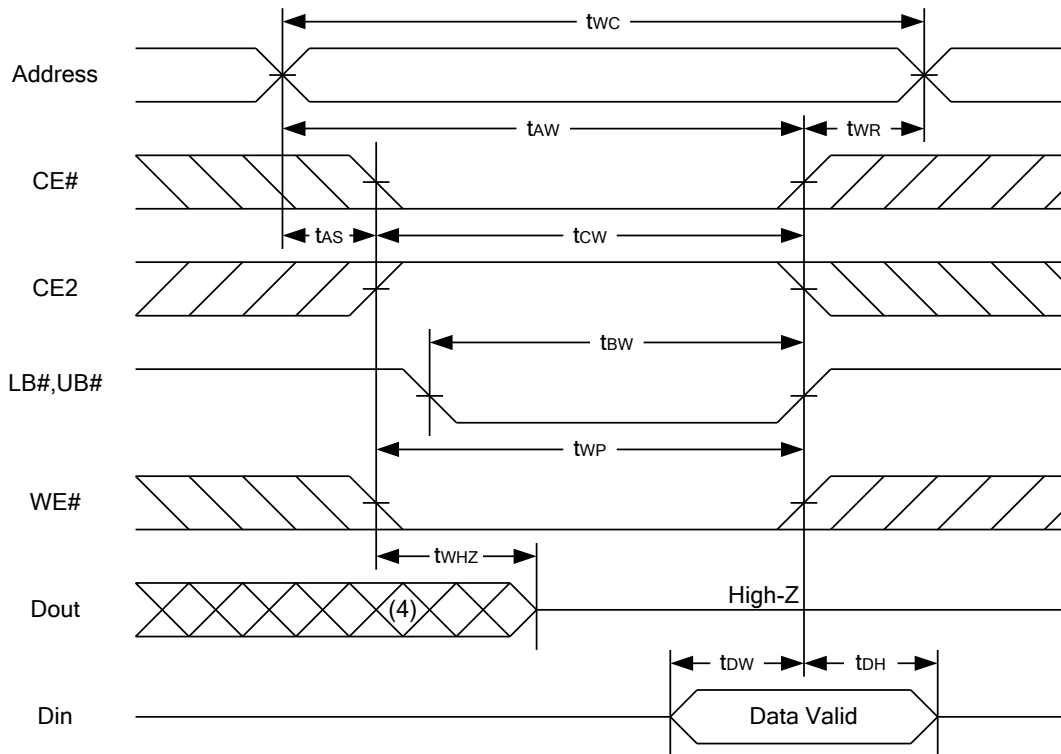
WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)



WRITE CYCLE 2 (CE# and CE2 Controlled) (1,2,5,6)



WRITE CYCLE 3 (LB#,UB# Controlled) (1,2,5,6)



Notes :

1. WE#, CE#, LB#, UB# must be high or CE2 must be low during all address transitions.
2. A write occurs during the overlap of a low CE#, high CE2, low WE#, LB# or UB# = low.
3. During a WE# controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE#, LB#, UB# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.

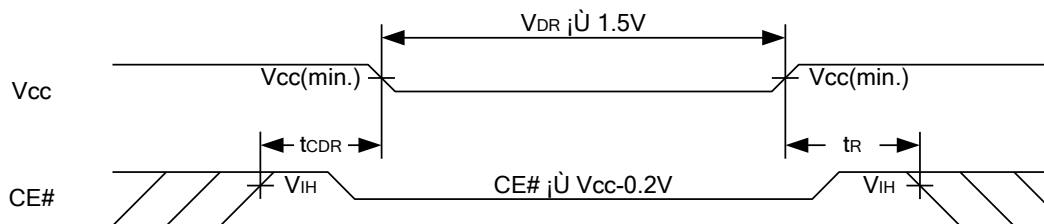
DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
VCC for Data Retention	V_{DR}	$CE\# \geq V_{CC} - 0.2V$ or $CE2 \leq 0.2V$	1.5	-	3.6	V
Data Retention Current	I_{DR}	$V_{CC} = 1.5V$ $CE\# \geq V_{CC} - 0.2V$ or $CE2 \leq 0.2V$ Other pins at 0.2V or $V_{CC}-0.2V$	-	4	40	mA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t_R		t_{RC}^*	-	-	ns

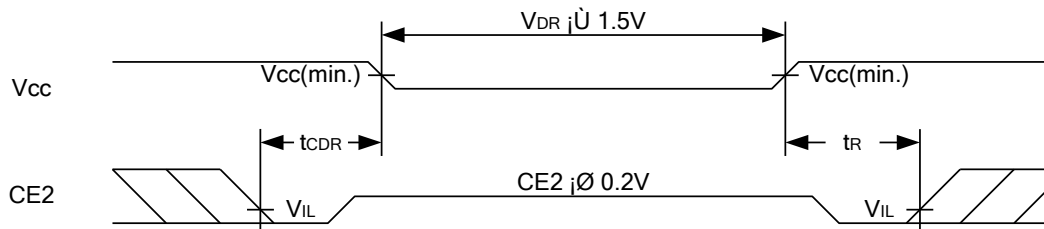
t_{RC}^* = Read Cycle Time

DATA RETENTION WAVEFORM

Low Vcc Data Retention Waveform (1) (CE# controlled)

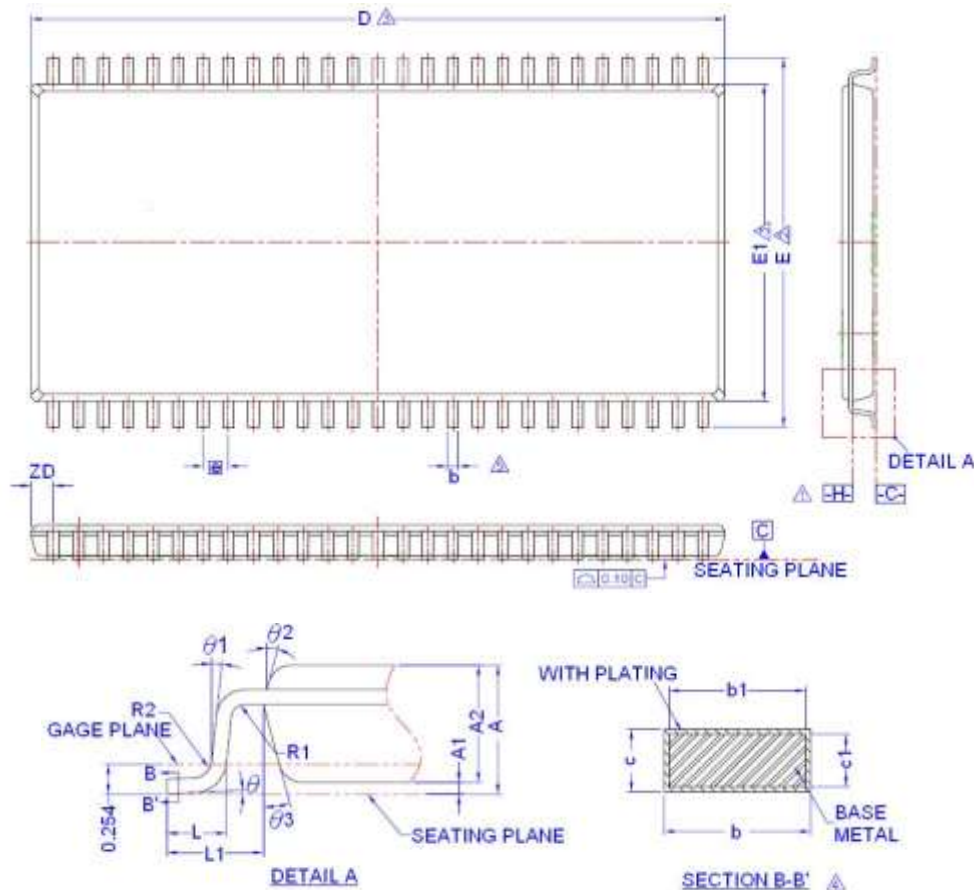


Low Vcc Data Retention Waveform (2) (CE2 controlled)



PACKAGE OUTLINE DIMENSION

54-pin 400 mil TSOP-II Package Outline Dimension



SYM.	DIMENSION (MM)			DIMENSION (INCH)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.20	—	—	0.047
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	—	0.45	0.012	—	0.018
b1	0.30	0.35	0.40	0.012	0.014	0.016
c	0.12	—	0.21	0.005	—	0.008
c1	0.10	0.127	0.16	0.004	0.005	0.006
D	22.22 BSC			0.875 BSC		
ZD	0.71 REF			0.028 REF		
E	11.76 BSC			0.463 BSC		
E1	10.16 BSC			0.400 BSC		
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.80 REF			0.031 REF		
(E)	0.80 BSC			0.031 BSC		
R1	0.12	—	—	0.005	—	—
R2	0.12	—	0.25	0.005	—	0.010
theta	0°	—	8°	0°	—	8°
theta1	0°	—	—	0°	—	—
theta2	10°	15°	20°	10°	15°	20°
theta3	10°	15°	20°	10°	15°	20°

NOTE:

1. DATUM PLANE $\square$ COINCIDENT WITH BOTTOM OF LEAD, WHERE LEAD EXITS BODY.
2. TO BE DETERMINED AT SEATING PLANE $\square$.
3. DIMENSION D AND E1 ARE DETERMINED AT DATUM $\square$.
DIMENSION D DOES NOT INCLUDE MOLD PROTRUSIONS OR GATE BURRS. MOLD PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
DIMENSION E1 DOES NOT INCLUDE INTERLEAD MOLD PROTRUSIONS. INTERLEAD MOLD PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE.
4. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.
6. CONTROLLING DIMENSION: MILLIMETER.
7. REFER TO JEDEC STD MS-024, FA.



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Alliance Memory Inc. reserves the rights to change the specifications and products without notice.

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