



DMP4051LK3

40V P-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

$V_{(BR)DSS}$	$R_{DS(on)}$	I_D $T_A = 25^\circ C$
-40V	51mΩ @ $V_{GS} = -10V$	-10.5A
	85mΩ @ $V_{GS} = -4.5V$	-8.4A

Description and Applications

This MOSFET has been designed to minimize the on-state resistance ($R_{DS(on)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

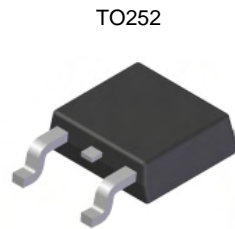
- Backlighting
- DC-DC Converters
- Power management functions

Features and Benefits

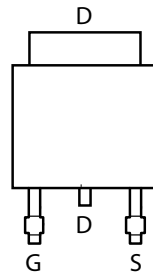
- 100% Unclamped Inductive Switch (UIS) test in production
- Low on-resistance
- Fast switching speed
- **“Green” component and RoHS compliant (Note 1)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

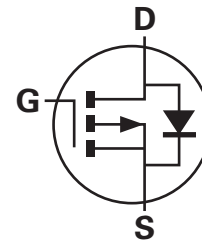
- Case: TO252
- Case Material: Molded Plastic, “Green” Molding Compound. UL Flammability Classification Rating 94V-0 (Note 1)
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Matte Tin Finish annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208
- Weight: 0.33 grams (approximate)



Top View



Top View
Pin-Out



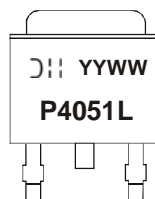
Equivalent Circuit

Ordering Information (Notes 1 & 2)

Product	Grade	Marking	Reel size (inches)	Tape width (mm)	Quantity per reel
DMP4051LK3-13	Commercial	P4051L	13	16	2,500
DMP4051LK3Q-13	Automotive	P4051L	13	16	2,500

- Notes:
1. Diodes, Inc. defines “Green” products as those which are RoHS compliant and contain no halogens or antimony compounds; further information about Diodes Inc.’s “Green” Policy can be found on our website. For packaging details, go to our website.
 2. Products with Q-suffix are automotive grade. Automotive products are electrical and thermal the same as the commercial, except where specified.

Marking Information



- ⌋⌋ = Manufacturer’s Marking
- P4051L = Product Type Marking Code
- YYWW = Date Code Marking
- YY = Year (ex: 09 = 2009)
- WW = Week (01 - 53)

Maximum Ratings @ $T_A = 25^\circ\text{C}$ unless otherwise specified

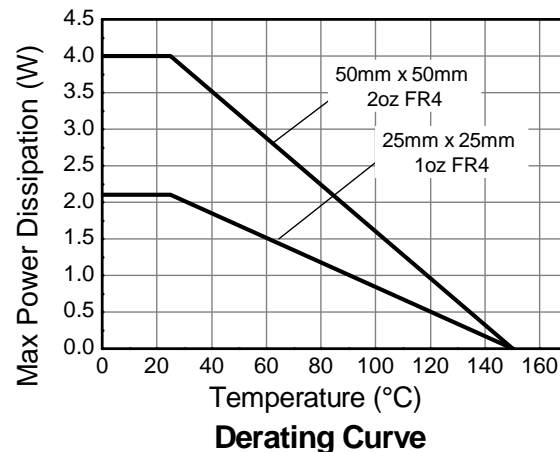
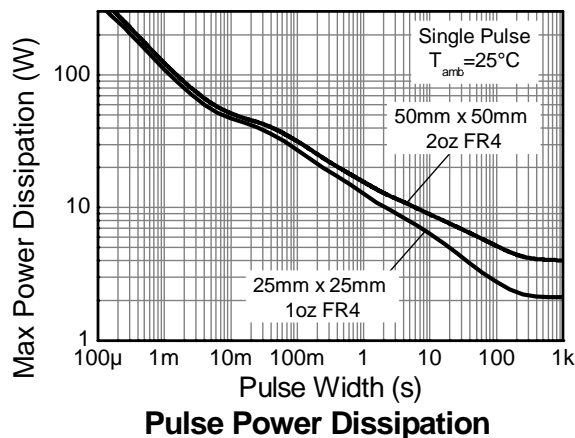
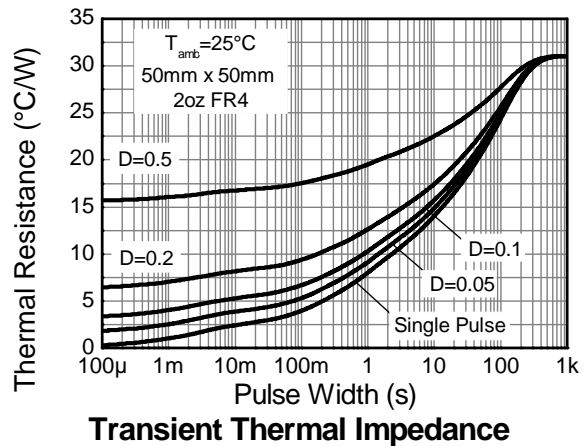
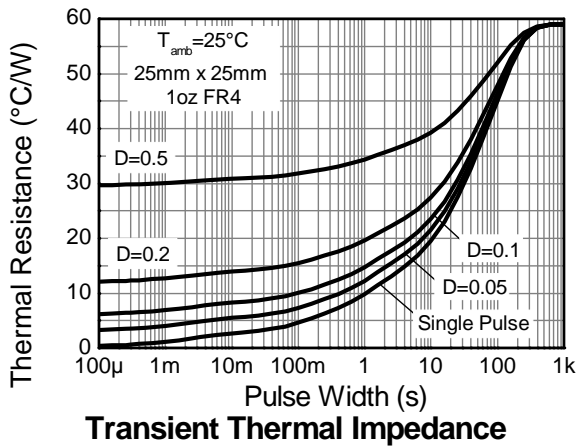
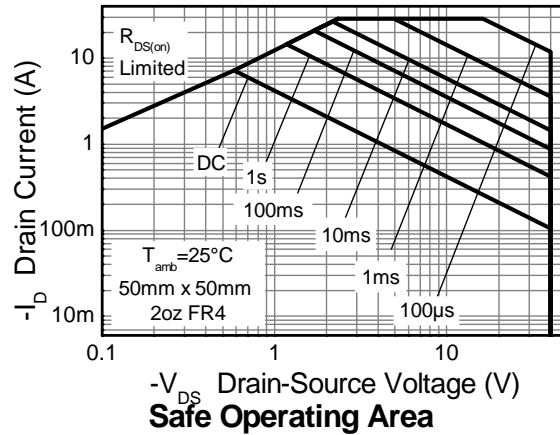
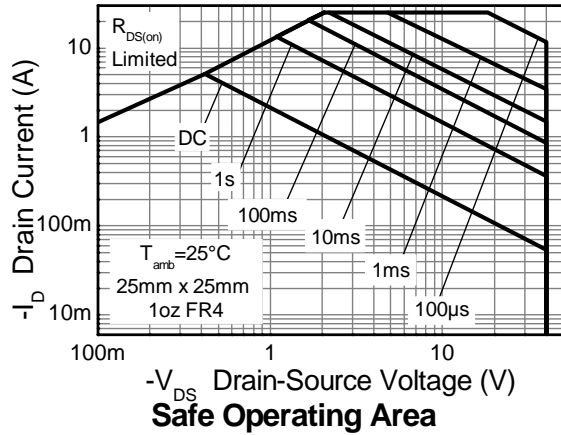
Characteristic			Symbol	Value	Unit
Drain-Source voltage			V_{DSS}	-40	V
Gate-Source voltage		(Note 3)	V_{GS}	± 20	V
Single Pulsed Avalanche Energy		(Note 9)	E_{AS}	50	mJ
Single Pulsed Avalanche Current		(Note 9)	I_{AS}	20.3	A
Continuous Drain current	$V_{GS} = 10\text{V}$	(Note 5)	I_D	-10.5	A
		$T_A = 70^\circ\text{C}$ (Note 5)		-8.40	
		(Note 4)		-7.2	
Pulsed Drain current	$V_{GS} = 10\text{V}$	(Note 6)	I_{DM}	-28.9	A
Continuous Source current (Body diode)		(Note 5)	I_S	-10.1	A
Pulsed Source current (Body diode)		(Note 5)	I_{SM}	-28.9	A

Thermal Characteristics @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic		Symbol	Value	Unit
Power dissipation Linear derating factor	(Note 4)	P_D	4.18	W mW/ $^\circ\text{C}$
	(Note 5)		33.4	
	(Note 7)		8.9	
	(Note 7)		71.4	
Thermal Resistance, Junction to Ambient	(Note 4)	$R_{\theta JA}$	2.14	$^\circ\text{C/W}$
	(Note 5)		17.1	
	(Note 7)		29.9	
Thermal Resistance, Junction to Lead	(Note 8)	$R_{\theta JL}$	14.0	$^\circ\text{C/W}$
Operating and storage temperature range		T_J, T_{STG}	2.46	$^\circ\text{C}$
			-55 to 150	

- Notes:
- AEC-Q101 V_{GS} maximum is $\pm 16\text{V}$.
 - For a device surface mounted on 50mm x 50mm x 1.6mm FR4 PCB with high coverage of single sided 2oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
 - Same as note 4, except the device is measured at $t \leq 10$ sec.
 - Same as note 4, except the device is pulsed with $D = 0.02$ and pulse width 300 μs . The pulse current is limited by the maximum junction temperature.
 - For a device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
 - Thermal resistance from junction to solder-point (at the end of the drain lead).
 - UIS in production with $L = 100\mu\text{H}$, $V_{DD} = -40\text{V}$.

Thermal Characteristics

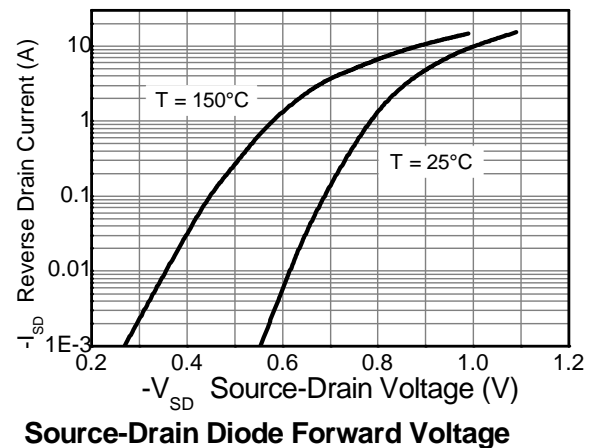
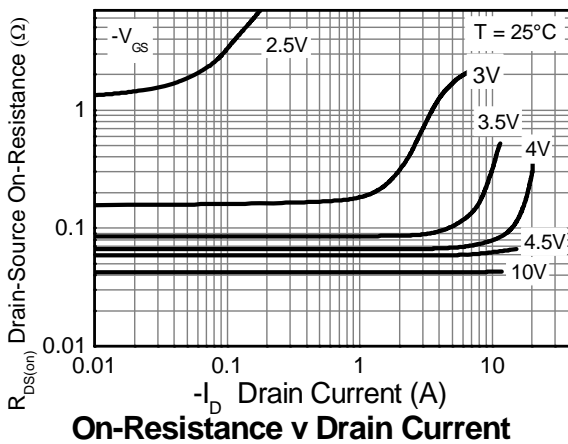
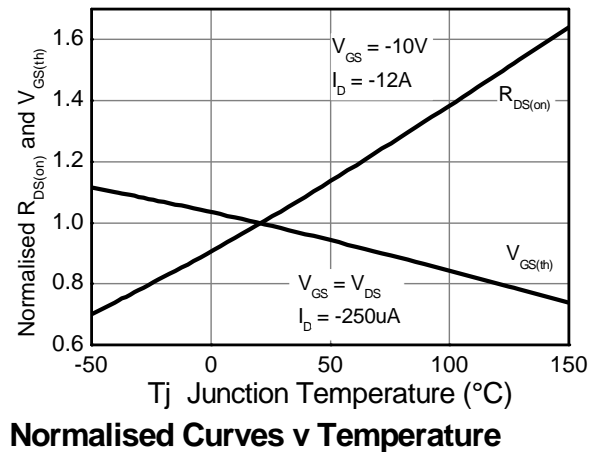
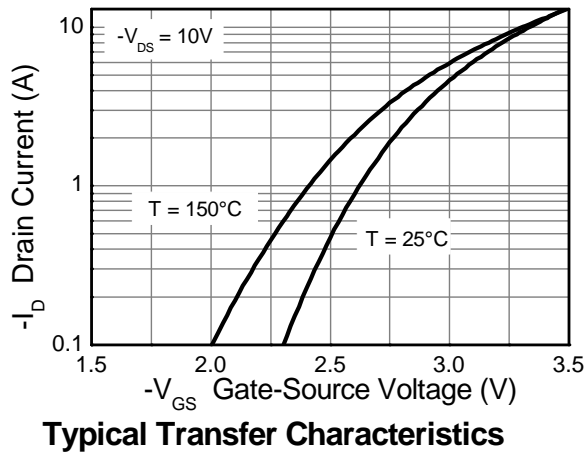
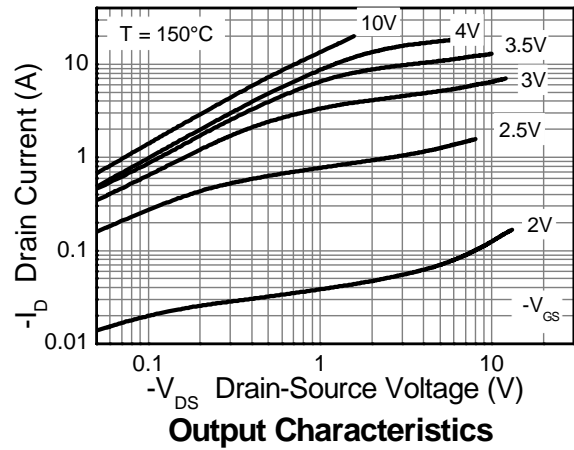
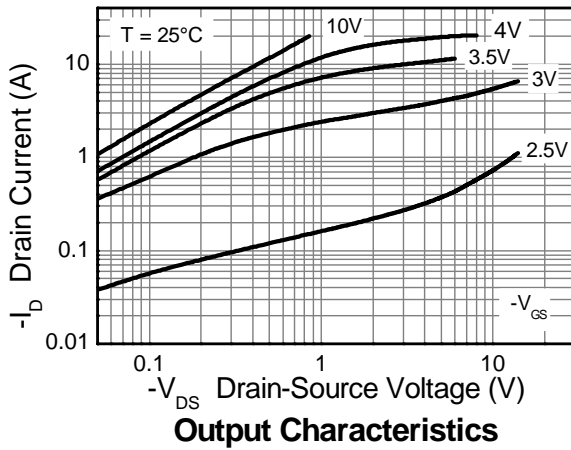


Electrical Characteristics @T_A = 25°C unless otherwise specified

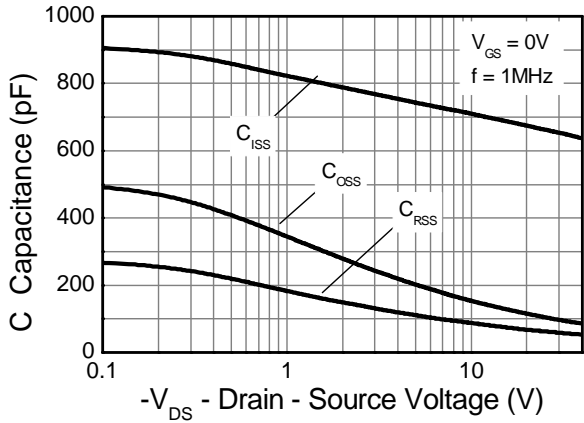
Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	-40	—	—	V	I _D = -250μA, V _{GS} = 0V
Zero Gate Voltage Drain Current	I _{DSS}	—	—	-0.5	μA	V _{DS} = -40V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±20V, V _{DS} = 0V
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(th)}	-1.0	—	-3.0	V	I _D = -250μA, V _{DS} = V _{GS}
Static Drain-Source On-Resistance (Note 10)	R _{DS(on)}	—	0.041	0.051	Ω	V _{GS} = -10V, I _D = -12A
			0.059	0.085		V _{GS} = -4.5V, I _D = -8A
Forward Transconductance (Notes 10 & 11)	g _{fs}	—	16.6	—	S	V _{DS} = -15V, I _D = -12A
Diode Forward Voltage (Note 10)	V _{SD}	—	-0.98	-1.2	V	I _S = -12A, V _{GS} = 0V
Reverse recovery time (Note 11)	t _{rr}	—	138	—	ns	I _S = -12A, di/dt = 100A/μs
Reverse recovery charge (Note 11)	Q _{rr}	—	841	—	nC	
DYNAMIC CHARACTERISTICS (Note 11)						
Input Capacitance	C _{iss}	—	674	—	pF	V _{DS} = -20V, V _{GS} = 0V f = 1MHz
Output Capacitance	C _{oss}	—	115	—	pF	
Reverse Transfer Capacitance	C _{rss}	—	67.7	—	pF	V _{GS} = -10V I _D = -12A
Total Gate Charge (Note 12)	Q _g	—	7.0	—	nC	
Total Gate Charge (Note 12)	Q _g	—	14	—	nC	V _{GS} = -10V I _D = -12A
Gate-Source Charge (Note 12)	Q _{gs}	—	2.2	—	nC	
Gate-Drain Charge (Note 12)	Q _{gd}	—	3.7	—	nC	V _{DD} = -20V, V _{GS} = -10V I _D = -12A, R _G ≅ 6.0Ω
Turn-On Delay Time (Note 12)	t _{D(on)}	—	2.3	—	ns	
Turn-On Rise Time (Note 12)	t _r	—	14.1	—	ns	
Turn-Off Delay Time (Note 12)	t _{D(off)}	—	25.1	—	ns	
Turn-Off Fall Time (Note 12)	t _f	—	14.3	—	ns	

Notes: 10. Measured under pulsed conditions. Pulse width ≤ 300μs; duty cycle ≤ 2%
 11. For design aid only, not subject to production testing.
 12. Switching characteristics are independent of operating junction temperatures.

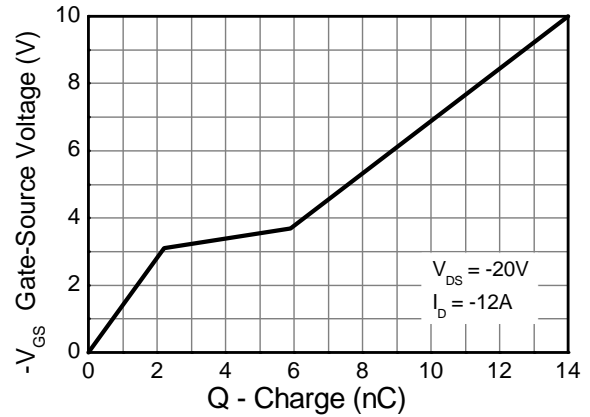
Typical Characteristics



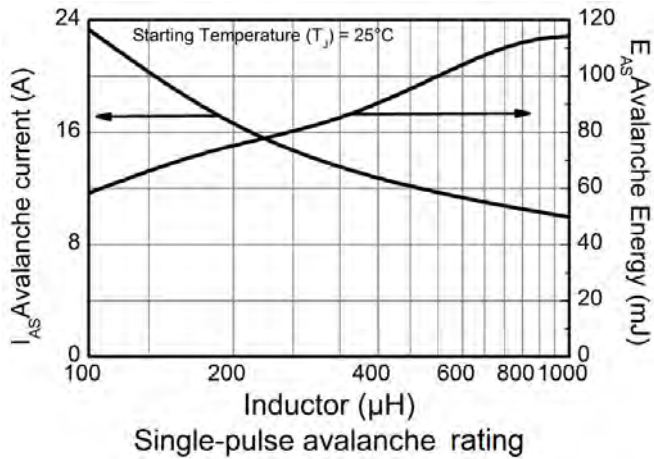
Typical Characteristics - continued



Capacitance v Drain-Source Voltage

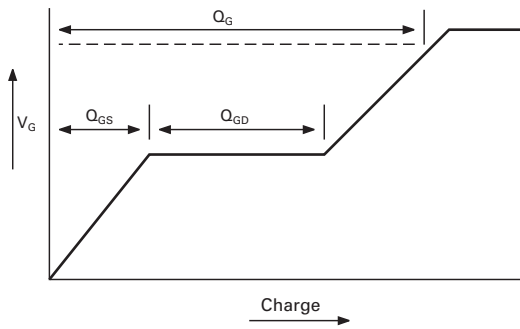


Gate-Source Voltage v Gate Charge

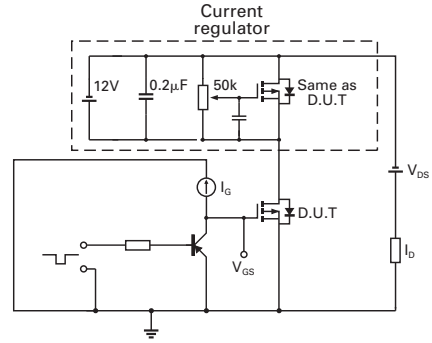


Single-pulse avalanche rating

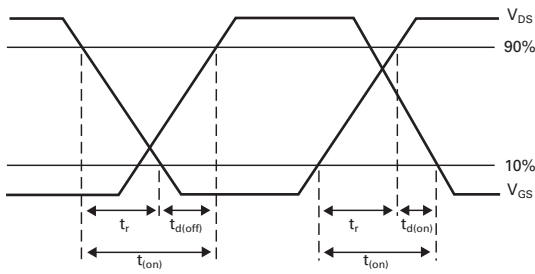
Test Circuits



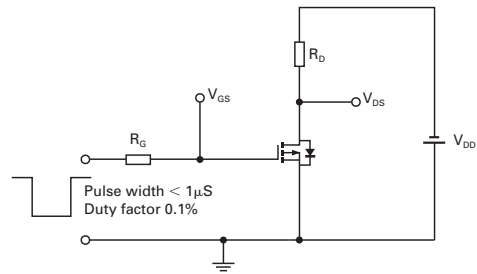
Basic gate charge waveform



Gate charge test circuit



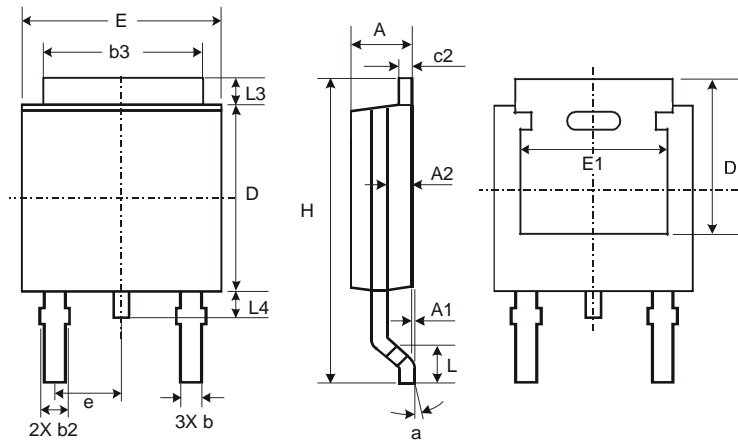
Switching time waveforms



Switching time test circuit

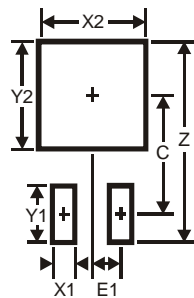
DMP4051LK3

Package Outline Dimensions



TO252			
Dim	Min	Max	Typ
A	2.19	2.39	2.29
A1	0.00	0.13	0.08
A2	0.97	1.17	1.07
b	0.64	0.88	0.783
b2	0.76	1.14	0.95
b3	5.21	5.46	5.33
c2	0.45	0.58	0.531
D	6.00	6.20	6.10
D1	5.21	-	-
e	-	-	2.286
E	6.45	6.70	6.58
E1	4.32	-	-
H	9.40	10.41	9.91
L	1.40	1.78	1.59
L3	0.88	1.27	1.08
L4	0.64	1.02	0.83
a	0°	10°	-
All Dimensions in mm			

Suggested Pad Layout



Dimensions	Value (in mm)
Z	11.6
X1	1.5
X2	7.0
Y1	2.5
Y2	7.0
C	6.9
E1	2.3

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