

## LVDS Interface ICs

# 35bit LVDS Transmitter 35:5 Serializer

**BU8254KVT**

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**●Description**

LVDS Interface IC of ROHM "Serializer" "Deserializer" operate from 8MHz to 150MHz wide clock range, and number of bits range is from 35 to 70. Data is transmitted seven times (7X) stream and reduce cable number by 3(1/3) or less. The ROHM's LVDS has low swing mode to be able to expect further low EMI.

**●Features**

- 35bits data of parallel LVCMOS level inputs are converted to five channels of LVDS data stream.
- 30bits of RGB data and 5bits of timing and control data(HSYNC, VSYNC, DE, CNTL1, CNTL2) are transmitted up to 784Mbps effective rate per LVDS channel.
- Support clock frequency from 8MHz up to 112MHz.
- Support consumer video format including 480i, 480P, 720P and 1080i as well.
- Clock edge selectable
- Power down mode
- Support spread spectrum clock generator.
- Support reduced swing LVDS for low EMI.
- 30bit LVDS receiver is recommended to use BU8255KVT.

**●Applications**

Flat Panel Display

**●Precaution**

- This chip is not designed to protect from radioactivity.
- The chip is made strictly for the specific application or equipment.  
Then it is necessary that the unit is measured as need.
- This document may be used as strategic technical data which subjects to COCOM regulations.

Status of this document

The Japanese version of this document is the official specification.

Please use the translation version of this document as a reference to expedite understanding of the official version.

If there is any uncertainty in translation version of this document, official version takes priority.

Jun.2008

●Block Diagram

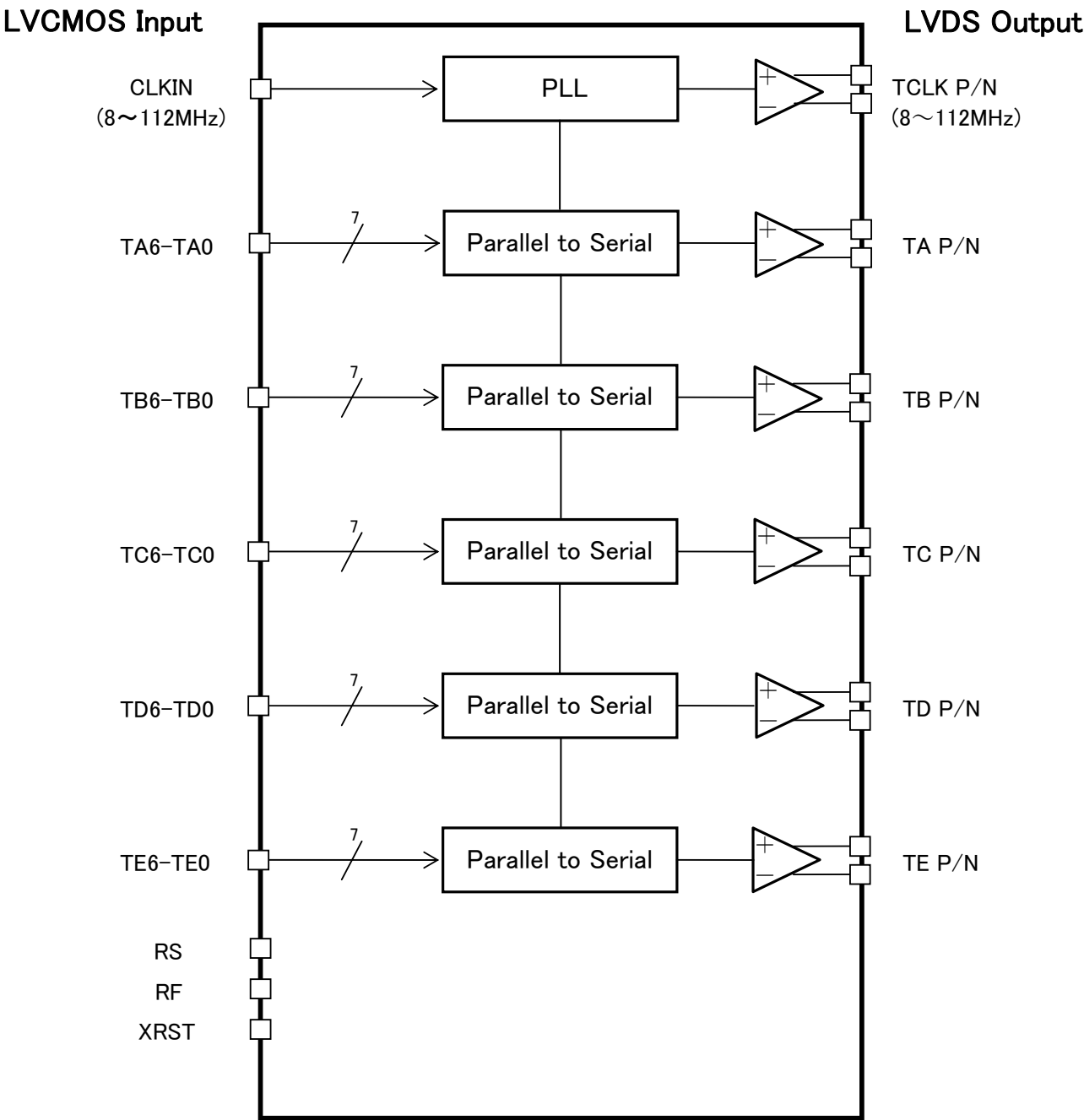
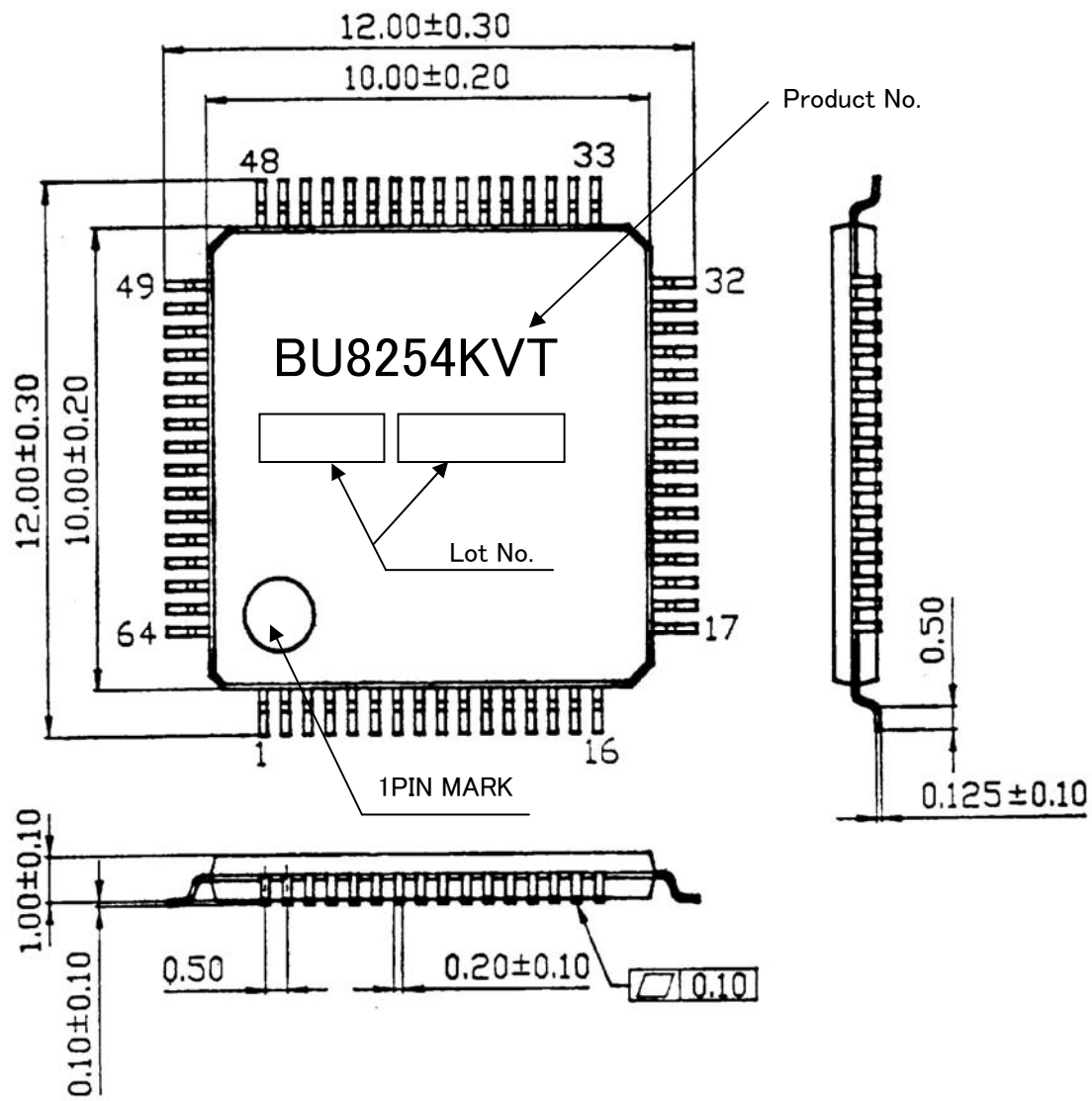


Figure-1 Block Diagram

●TQFP64V Package Outline and Specification



(UNIT: mm)

Figure-2 TQFP64V Package Outline and Specification

## ● Pin configuration

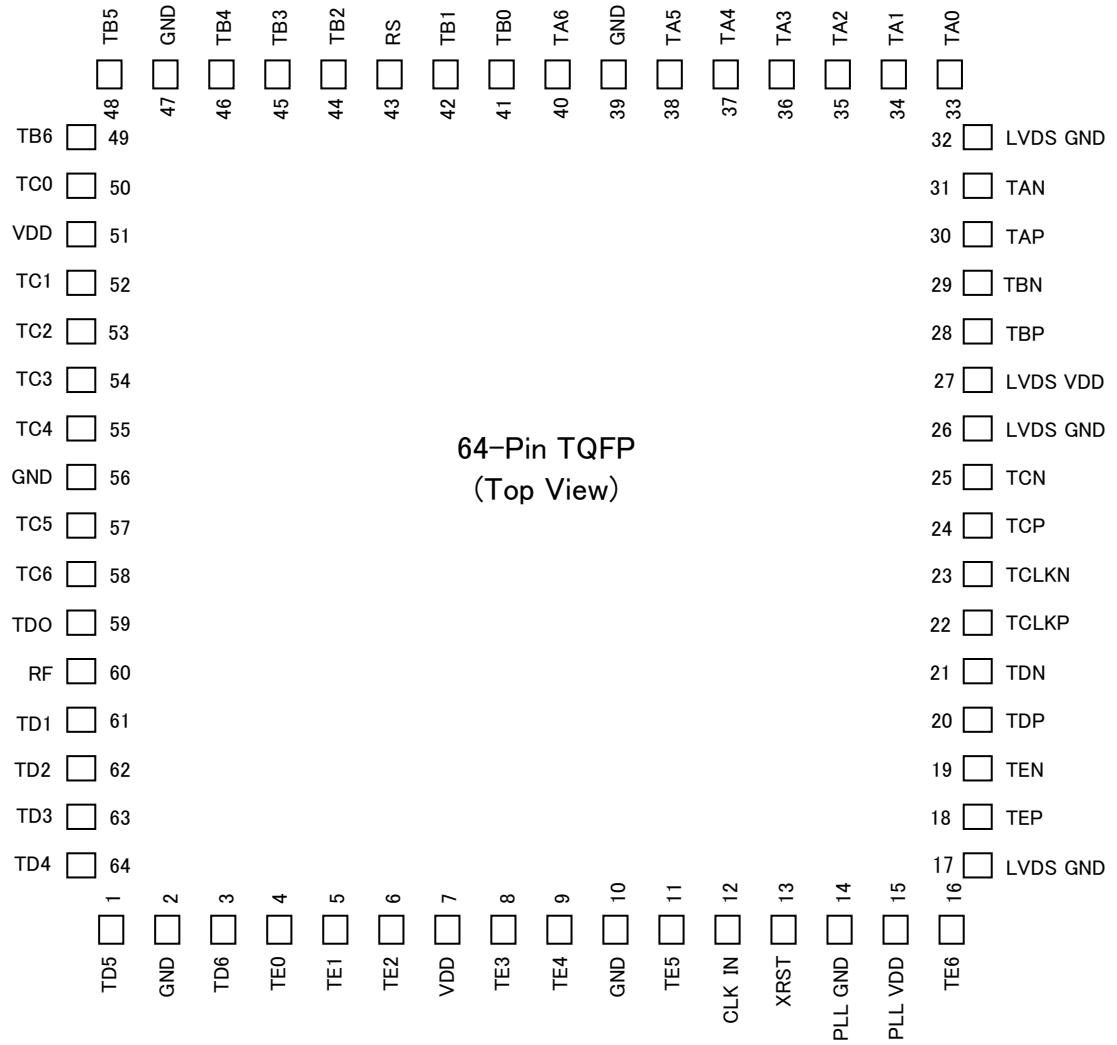


Figure-3 Pin Diagram (Top View)

## ●Pin Description

Table 1 : Pin Description

| Pin Name        | Pin No.              | Type                      | Descriptions                                                                                                                                                                                                                                                                                                                                                         |    |            |                           |                 |       |     |          |       |                     |     |       |     |
|-----------------|----------------------|---------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|------------|---------------------------|-----------------|-------|-----|----------|-------|---------------------|-----|-------|-----|
| TAP, TAN        | 30,31                | LVDS OUT                  | LVDS data out.                                                                                                                                                                                                                                                                                                                                                       |    |            |                           |                 |       |     |          |       |                     |     |       |     |
| TBP, TBN        | 28,29                | LVDS OUT                  |                                                                                                                                                                                                                                                                                                                                                                      |    |            |                           |                 |       |     |          |       |                     |     |       |     |
| TCP, TCN        | 24,25                | LVDS OUT                  |                                                                                                                                                                                                                                                                                                                                                                      |    |            |                           |                 |       |     |          |       |                     |     |       |     |
| TDP, TDN        | 20,21                | LVDS OUT                  |                                                                                                                                                                                                                                                                                                                                                                      |    |            |                           |                 |       |     |          |       |                     |     |       |     |
| TEP, TEN        | 18,19                | LVDS OUT                  |                                                                                                                                                                                                                                                                                                                                                                      |    |            |                           |                 |       |     |          |       |                     |     |       |     |
| TCLKP, TCLKN    | 22,23                | LVDS OUT                  | LVDS clock out.                                                                                                                                                                                                                                                                                                                                                      |    |            |                           |                 |       |     |          |       |                     |     |       |     |
| TA0~TA6         | 33,34,35,36,37,38,40 | IN                        | Pixel data inputs.                                                                                                                                                                                                                                                                                                                                                   |    |            |                           |                 |       |     |          |       |                     |     |       |     |
| TB0~TB6         | 41,42,44,45,46,48,49 | IN                        |                                                                                                                                                                                                                                                                                                                                                                      |    |            |                           |                 |       |     |          |       |                     |     |       |     |
| TC0~TC6         | 50,52,53,54,55,57,58 | IN                        |                                                                                                                                                                                                                                                                                                                                                                      |    |            |                           |                 |       |     |          |       |                     |     |       |     |
| TD0~TD6         | 59,61,62,63,64,1,3   | IN                        |                                                                                                                                                                                                                                                                                                                                                                      |    |            |                           |                 |       |     |          |       |                     |     |       |     |
| TE0~TE6         | 4,5,6,8,9,11,16      | IN                        |                                                                                                                                                                                                                                                                                                                                                                      |    |            |                           |                 |       |     |          |       |                     |     |       |     |
| XRST            | 13                   | IN                        | H : Normal operation,<br>L : Power down (all outputs are Hi-Z)                                                                                                                                                                                                                                                                                                       |    |            |                           |                 |       |     |          |       |                     |     |       |     |
| RS              | 43                   | IN                        | LVDS swing mode, V <sub>REF</sub> *1 select. <table><tr><td>RS</td><td>LVDS Swing</td><td>Small Swing Input Support</td></tr><tr><td>V<sub>DD</sub></td><td>350mV</td><td>N/A</td></tr><tr><td>0.6~1.4V</td><td>350mV</td><td>RS-V<sub>REF</sub></td></tr><tr><td>GND</td><td>200mV</td><td>N/A</td></tr></table><br>*1 V <sub>REF</sub> is Input Reference Voltage. | RS | LVDS Swing | Small Swing Input Support | V <sub>DD</sub> | 350mV | N/A | 0.6~1.4V | 350mV | RS-V <sub>REF</sub> | GND | 200mV | N/A |
| RS              | LVDS Swing           | Small Swing Input Support |                                                                                                                                                                                                                                                                                                                                                                      |    |            |                           |                 |       |     |          |       |                     |     |       |     |
| V <sub>DD</sub> | 350mV                | N/A                       |                                                                                                                                                                                                                                                                                                                                                                      |    |            |                           |                 |       |     |          |       |                     |     |       |     |
| 0.6~1.4V        | 350mV                | RS-V <sub>REF</sub>       |                                                                                                                                                                                                                                                                                                                                                                      |    |            |                           |                 |       |     |          |       |                     |     |       |     |
| GND             | 200mV                | N/A                       |                                                                                                                                                                                                                                                                                                                                                                      |    |            |                           |                 |       |     |          |       |                     |     |       |     |
| RF              | 60                   | IN                        | Input clock triggering edge select.<br>H : Rising edge, L : Falling edge.                                                                                                                                                                                                                                                                                            |    |            |                           |                 |       |     |          |       |                     |     |       |     |
| VDD             | 51,7                 | Power                     | Power supply pins for LVCMOS inputs and digital core.                                                                                                                                                                                                                                                                                                                |    |            |                           |                 |       |     |          |       |                     |     |       |     |
| CLKIN           | 12                   | IN                        | Clock input.                                                                                                                                                                                                                                                                                                                                                         |    |            |                           |                 |       |     |          |       |                     |     |       |     |
| GND             | 2,10,39,47,56        | Ground                    | Ground pins for LVCMOS inputs and digital core.                                                                                                                                                                                                                                                                                                                      |    |            |                           |                 |       |     |          |       |                     |     |       |     |
| LVDS VDD        | 27                   | Power                     | Power supply pins for LVDS outputs.                                                                                                                                                                                                                                                                                                                                  |    |            |                           |                 |       |     |          |       |                     |     |       |     |
| LVDS GND        | 17,26,32             | Ground                    | Ground pins for LVDS outputs.                                                                                                                                                                                                                                                                                                                                        |    |            |                           |                 |       |     |          |       |                     |     |       |     |
| PLLVD           | 15                   | Power                     | Power supply pin for PLL core.                                                                                                                                                                                                                                                                                                                                       |    |            |                           |                 |       |     |          |       |                     |     |       |     |
| PLLGND          | 14                   | Ground                    | Ground pins for PLL core.                                                                                                                                                                                                                                                                                                                                            |    |            |                           |                 |       |     |          |       |                     |     |       |     |

## ●Electrical characteristics

### ■Rating

Table 2 : Absolute Maximum Rating

| Parameter                 | Symbol    | Rating |              | Units |
|---------------------------|-----------|--------|--------------|-------|
|                           |           | Min    | Max          |       |
| Supply Voltage            | $V_{DD}$  | -0.3   | 4.0          | V     |
| Input Voltage             | $V_{IN}$  | -0.3   | $V_{DD}+0.3$ | V     |
| Output Voltage            | $V_{OUT}$ | -0.3   | $V_{DD}+0.3$ | V     |
| Storage Temperature Range | $T_{stg}$ | -55    | 125          | °C    |

Table 3 : Package Power

| PACKAGE | Power Dissipation (mW) | De-rating (mW/°C)*1 |
|---------|------------------------|---------------------|
| TQFP64V | 700                    | 7.0                 |
|         | 1000*2                 | 10.0*2              |

\*1:At temperature  $T_a > 25^{\circ}\text{C}$

\*2:Package power when mounting on the PCB board.

The size of PCB board :  $70 \times 70 \times 1.6 (\text{mm}^3)$

The material of PCB board :The FR4 glass epoxy board.(3% or less copper foil area)

(It is recommended to apply the above package power requirement to PCB board when the small swing input mode is used)

Table 4 : Recommended Operating Conditions

| Parameter                   | Symbol    | Rating |     |     | Units | Conditions                             |
|-----------------------------|-----------|--------|-----|-----|-------|----------------------------------------|
|                             |           | Min    | Typ | Max |       |                                        |
| Supply Voltage              | $V_{DD}$  | 3.0    | 3.3 | 3.6 | V     | VDD,LVDSVDD,PLLVD                      |
| Operating Temperature Range | $T_{opr}$ | -20    | -   | 85  | °C    | Clock frequency from 8MHz up to 90MHz  |
|                             |           | 0      | -   | 70  | °C    | Cock frequency from 90MHz up to 112MHz |

## ■ DC characteristics

**Table 5 : LVCMOS DC Specifications** ( $V_{DD}=3.0V\sim 3.6V$ ,  $T_a=-20^{\circ}C\sim 85^{\circ}C$ )

| Symbol         | Parameter                            | Rating                |             |                       | Units   | Conditions                    |
|----------------|--------------------------------------|-----------------------|-------------|-----------------------|---------|-------------------------------|
|                |                                      | Min                   | Typ         | Max                   |         |                               |
| $V_{IH}$       | High Level Input Voltage             | $V_{DD} \times 0.8$   | —           | $V_{DD}$              | V       | exclude RS pin                |
| $V_{IL}$       | Low Level Input Voltage              | GND                   | —           | $V_{DD} \times 0.2$   | V       |                               |
| $V_{IHRS}$     | High Level Input Voltage             | $V_{DD} \times 0.8$   | —           | $V_{DD}$              |         | RS pin                        |
| $V_{ILRS}$     | Low Level Input Voltage              | GND                   | —           | 0.2                   |         |                               |
| $V_{DDQ}^{*1}$ | Small Swing Voltage                  | 1.2                   | —           | 2.8                   | V       |                               |
| $V_{REF}$      | Input Reference Voltage              | —                     | $V_{DDQ}/2$ | —                     | —       | Small Swing( $RS=V_{DDQ}/2$ ) |
| $V_{SH}^{*2}$  | Small Swing High Level Input Voltage | $V_{DDQ}/2$<br>+200mV | —           | —                     | V       | $V_{REF}=V_{DDQ}/2$           |
| $V_{SL}^{*2}$  | Small Swing Low Level Input Voltage  | —                     | —           | $V_{DDQ}/2$<br>-200mV | V       | $V_{REF}=V_{DDQ}/2$           |
| $I_{INC}$      | Input Current                        | —                     | —           | $\pm 10$              | $\mu A$ | $0V \leq V_{IN} \leq V_{DD}$  |

\*1:  $V_{DDQ}$  voltage defines max voltage of small swing input. It is not an actual input voltage.

\*2: Small swing signal is applied to TA[6:0], TB[6:0], TC[6:0], TD[6:0], TE[6:0], CLKIN.

**Table 6 : LVDS Transmitter DC Specifications** ( $V_{DD}=3.0V\sim 3.6V$ ,  $T_a=-20^{\circ}C\sim 85^{\circ}C$ )

| Symbol          | Parameter                                         | Rating |      |          | Units   | Conditions                           |                           |
|-----------------|---------------------------------------------------|--------|------|----------|---------|--------------------------------------|---------------------------|
|                 |                                                   | Min    | Typ  | Max      |         |                                      |                           |
| $V_{OD}$        | Differential Output Voltage                       | 250    | 350  | 450      | mV      | RL=100Ω                              | Normal swing RS= $V_{DD}$ |
|                 |                                                   | 100    | 200  | 300      | mV      |                                      | Reduced swing RS=GND      |
| $\Delta V_{OD}$ | Change in VOD between complementary output states | —      | —    | 35       | mV      | RL=100Ω                              |                           |
| $V_{OC}$        | Common Mode Voltage                               | 1.125  | 1.25 | 1.375    | V       |                                      |                           |
| $\Delta V_{OC}$ | Change in VOC between complementary output states | —      | —    | 35       | mV      |                                      |                           |
| $I_{OS}$        | Output Short Circuit Current                      | —      | —    | -24      | mA      | $V_{OUT}=0V$ , RL=100Ω               |                           |
| $I_{OZ}$        | Output TRI-STATE Current                          | —      | —    | $\pm 10$ | $\mu A$ | XRST=0V,<br>$V_{OUT}=0V$ to $V_{DD}$ |                           |

## ■ Supply Current

**Table 7 : Supply Current**

| Symbol     | Parameter                             | Rating |     | Units   | Conditions                                                                                  |         |
|------------|---------------------------------------|--------|-----|---------|---------------------------------------------------------------------------------------------|---------|
|            |                                       | Typ    | Max |         |                                                                                             |         |
| $I_{TCCG}$ | Transmitter Supply Current            | 57     | –   | mA      | RL=100 $\Omega$ , CL=5pF<br>V <sub>DD</sub> =3.3V, RS=V <sub>DD</sub><br>Gray Scale Pattern | f=85MHz |
|            |                                       | 42     | –   | mA      | RL=100 $\Omega$ , CL=5pF<br>V <sub>DD</sub> =3.3V, RS=GND<br>Gray Scale Pattern             | f=85MHz |
| $I_{TCCW}$ | Transmitter Supply Current            | 62     | –   | mA      | RL=100 $\Omega$ , CL=5pF<br>V <sub>DD</sub> =3.3V, RS=V <sub>DD</sub><br>Worst Case pattern | f=85MHz |
|            |                                       | 45     | –   | mA      | RL=100 $\Omega$ , CL=5pF<br>V <sub>DD</sub> =3.3V, RS=GND<br>Worst Case pattern             | f=85MHz |
| $I_{TCCS}$ | Transmitter Power Down Supply Current | –      | 10  | $\mu$ A | XRST=L                                                                                      |         |

**Gray Scale Pattern**

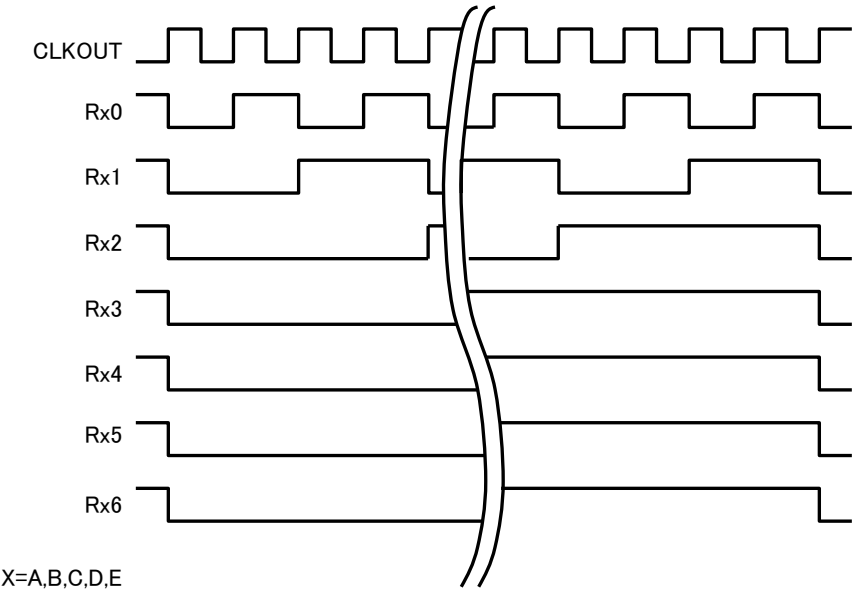


Figure-4 Gray scale pattern

**Worst Case Pattern (Maximum Power condition)**

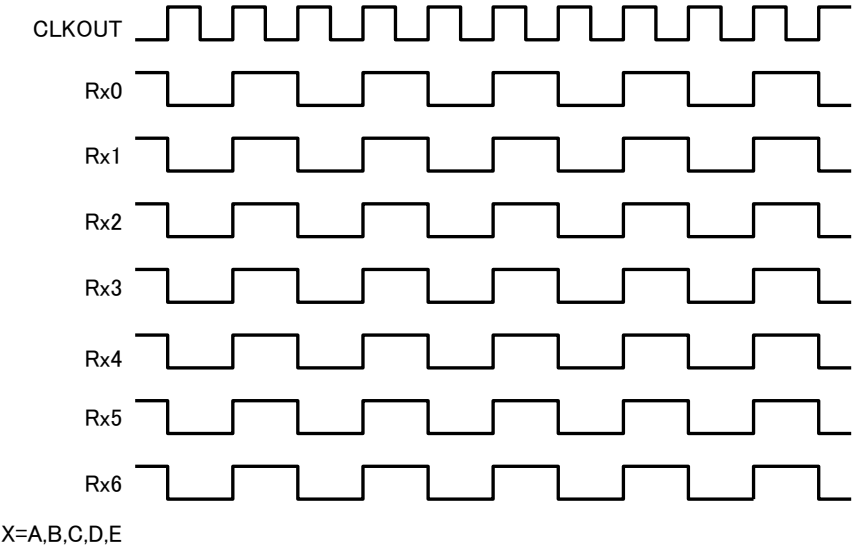


Figure-5 Worst Case Pattern

## ■ AC characteristics

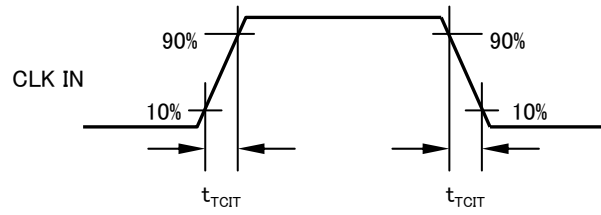
Table 8 : Switching Characteristics

| Symbol     | Parameter                     | Min                        | Typ                  | Max                        | Units |
|------------|-------------------------------|----------------------------|----------------------|----------------------------|-------|
| $t_{TCIT}$ | CLK IN Transition time        | –                          | –                    | 5.0                        | ns    |
| $t_{TCP}$  | CLK IN Period                 | 8.93                       | –                    | 125.0                      | ns    |
| $t_{TCH}$  | CLK IN High Time              | $0.35t_{TCP}$              | $0.5t_{TCP}$         | $0.65t_{TCP}$              | ns    |
| $t_{TCL}$  | CLK IN Low Time               | $0.35t_{TCP}$              | $0.5t_{TCP}$         | $0.65t_{TCP}$              | ns    |
| $t_{TCD}$  | CLK IN to TCLK+/-Delay        | –                          | $t_{TCP}$            | –                          | ns    |
| $t_{TS}$   | LVSMOS Data Set up to CLK IN  | 2.5                        | –                    | –                          | ns    |
| $t_{TH}$   | LVC MOS Data Hold from CLK IN | 0                          | –                    | –                          | ns    |
| $t_{LVT}$  | LVDS Transition Time          | –                          | 0.6                  | 1.5                        | ns    |
| $t_{TOP1}$ | Output Data Position 0        | –0.2                       | 0.0                  | +0.2                       | ns    |
| $t_{TOP0}$ | Output Data Position 1        | $\frac{t_{TCP}}{7} - 0.2$  | $\frac{t_{TCP}}{7}$  | $\frac{t_{TCP}}{7} + 0.2$  | ns    |
| $t_{TOP6}$ | Output Data Position 2        | $2\frac{t_{TCP}}{7} - 0.2$ | $2\frac{t_{TCP}}{7}$ | $2\frac{t_{TCP}}{7} + 0.2$ | ns    |
| $t_{TOP5}$ | Output Data Position 3        | $3\frac{t_{TCP}}{7} - 0.2$ | $3\frac{t_{TCP}}{7}$ | $3\frac{t_{TCP}}{7} + 0.2$ | ns    |
| $t_{TOP4}$ | Output Data Position 4        | $4\frac{t_{TCP}}{7} - 0.2$ | $4\frac{t_{TCP}}{7}$ | $4\frac{t_{TCP}}{7} + 0.2$ | ns    |
| $t_{TOP3}$ | Output Data Position 5        | $5\frac{t_{TCP}}{7} - 0.2$ | $5\frac{t_{TCP}}{7}$ | $5\frac{t_{TCP}}{7} + 0.2$ | ns    |
| $t_{TOP2}$ | Output Data Position 6        | $6\frac{t_{TCP}}{7} - 0.2$ | $6\frac{t_{TCP}}{7}$ | $6\frac{t_{TCP}}{7} + 0.2$ | ns    |
| $t_{TPLL}$ | Phase Locked Loop Set Time    | –                          | –                    | 10.0                       | ms    |

## ● AC Timing

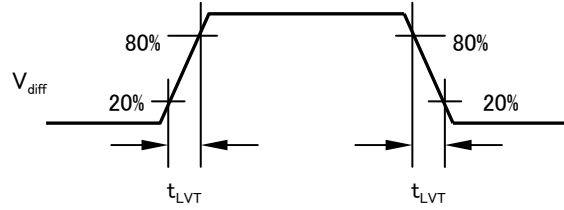
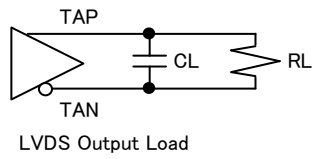
### ■ AC Timing Diagrams

LVC MOS Input



LVDS Output

$$V_{diff} = (TAP) - (TAN)$$



LVC MOS Input

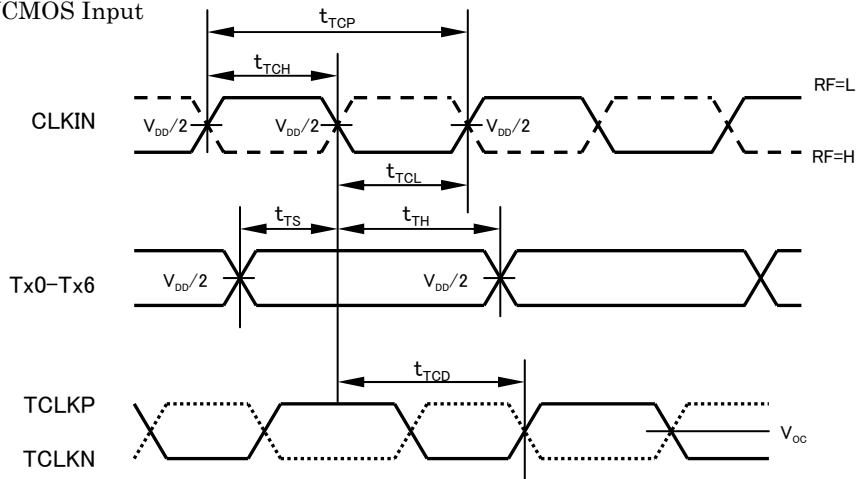


Figure-6 AC Timing Diagrams

## ■ Small Swing Inputs

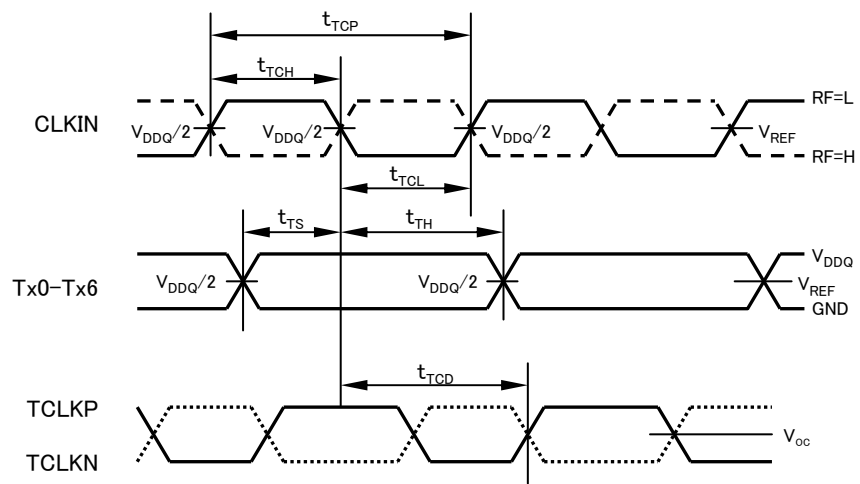


Figure-7 Small Swing Inputs

## ■ AC Timing Diagrams

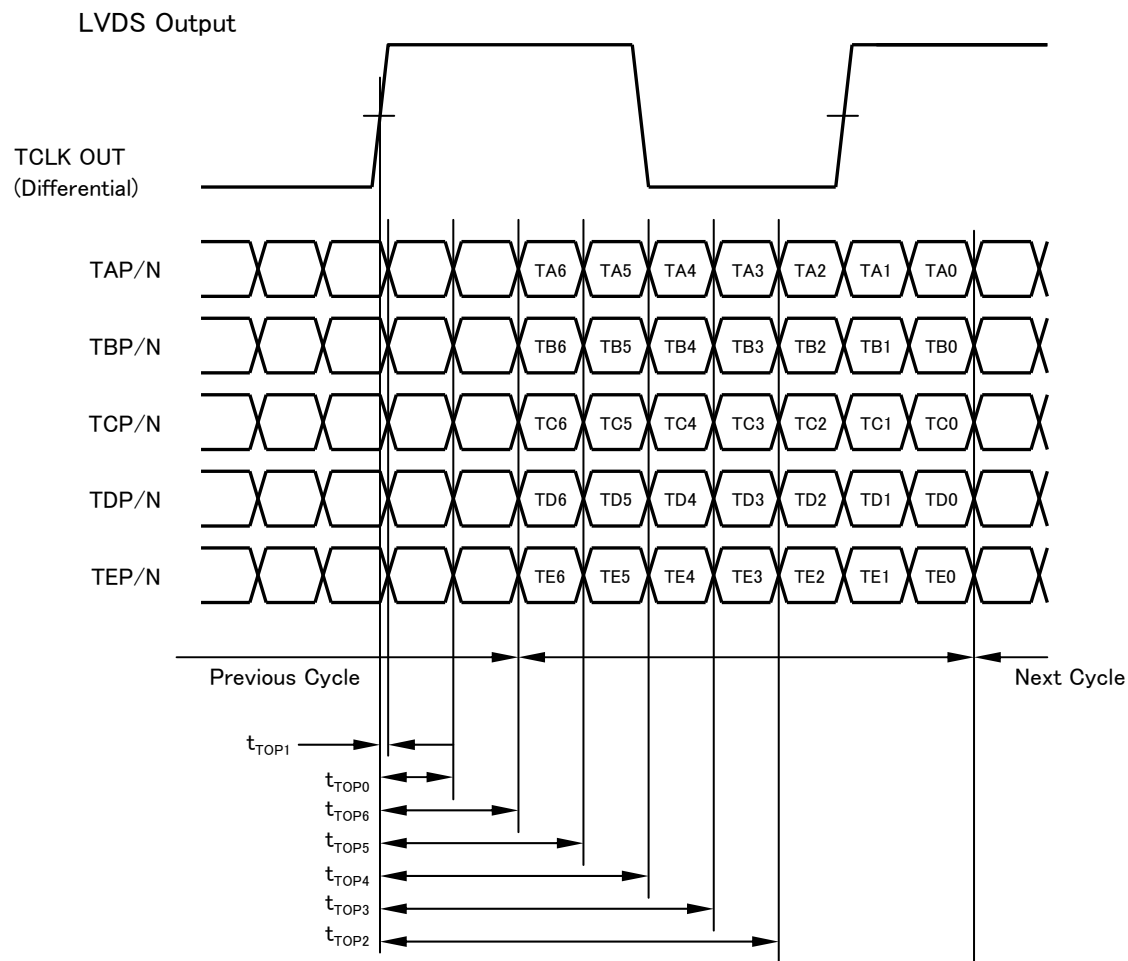


Figure-8 AC Timing Diagrams

## ■ Phase Locked Loop Set Time

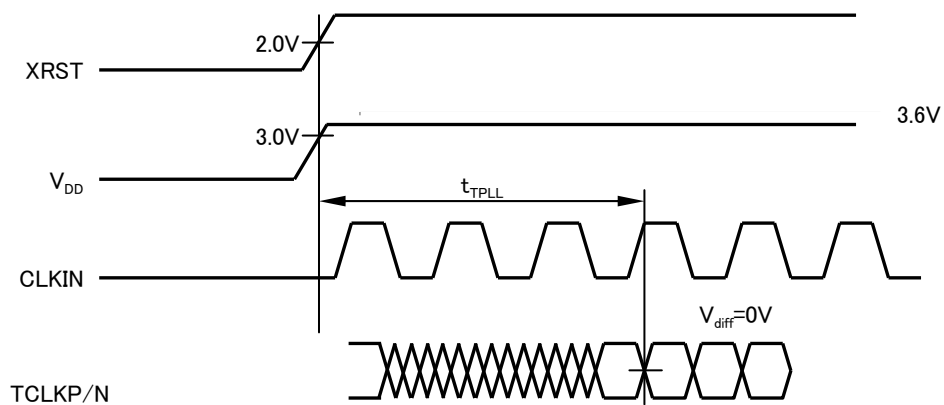


Figure-9 Phase Locked Loop Set Time

## ●About the Power On Reset

Power On Reset is not mandatory for this device.

(The PD pin should be set to high level when Power On Reset procedure is not used.)

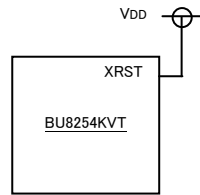


Figure-10 Terminal connection when Power On Reset is not used

However, Power On Reset procedure is strongly recommend for internal logic initialization by following two methods.

- ① The method of using CR circuit.
- ② The method of using external specific IC.

It is recommend to do enough examination for target application.

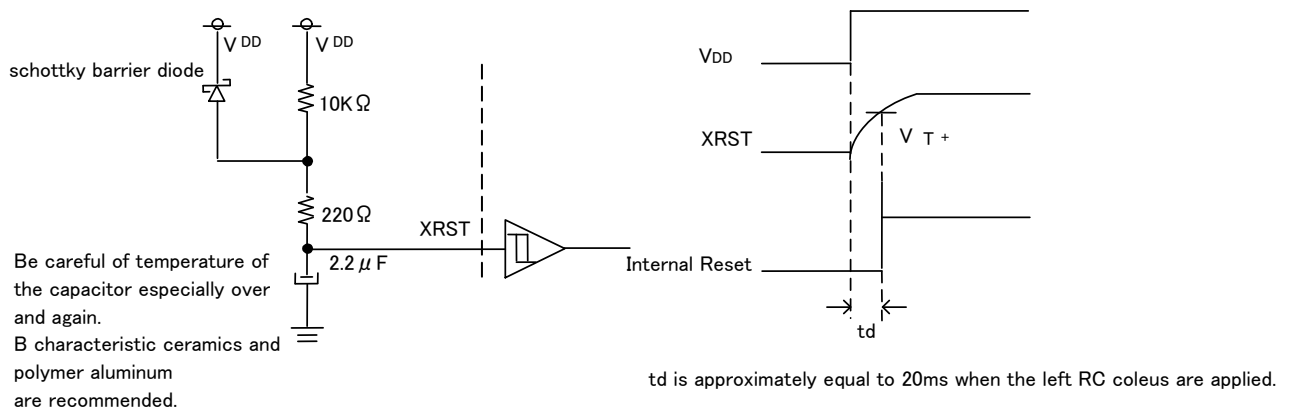


Figure-11 Power On Reset by external a CR circuit

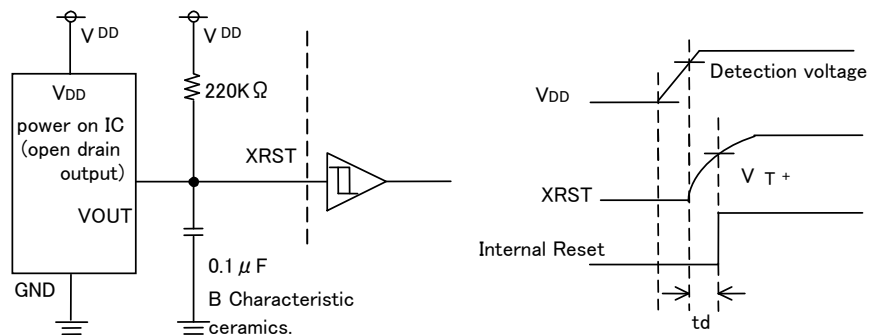


Figure-12 Power On Reset by specific IC

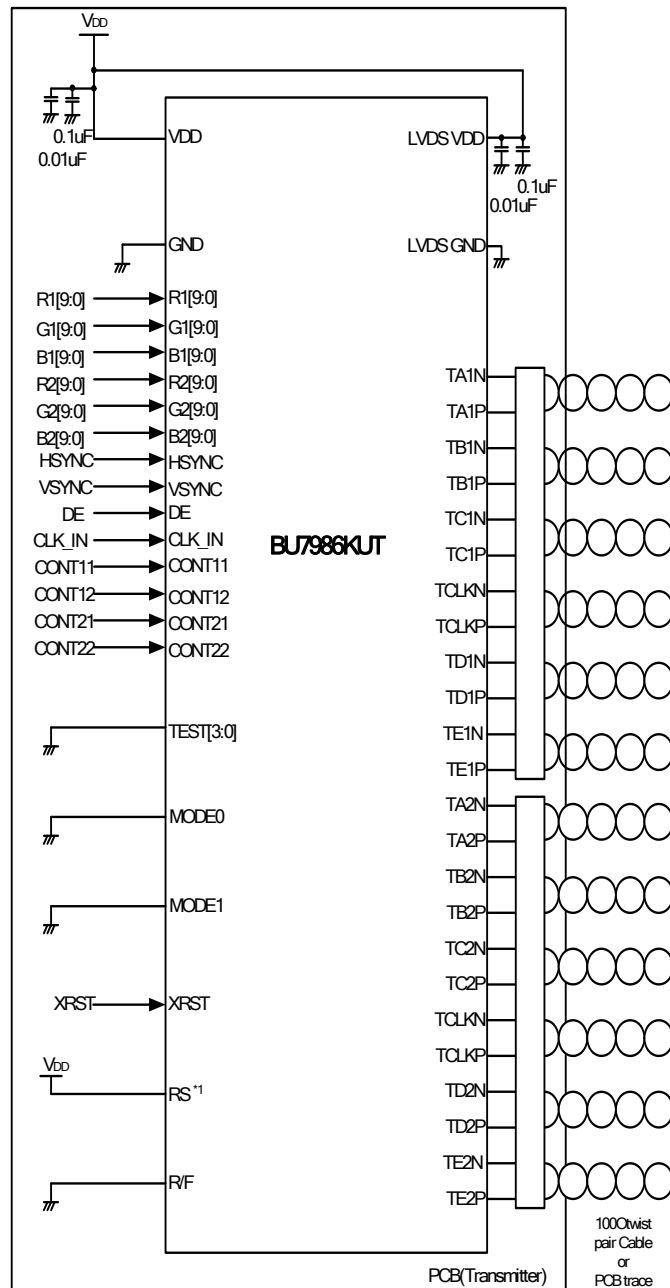
## ●10bit LVCMOS Level Input

Example:

BU7986KUT : Falling edge

Normal swing

Dual-in / Dual-out mode



\*1 : If RS pin is tied to  $V_{DD}$ , LVDS swing is 350m V.  
If RS pin is tied to  $GND$ , LVDS swing is 200m V.

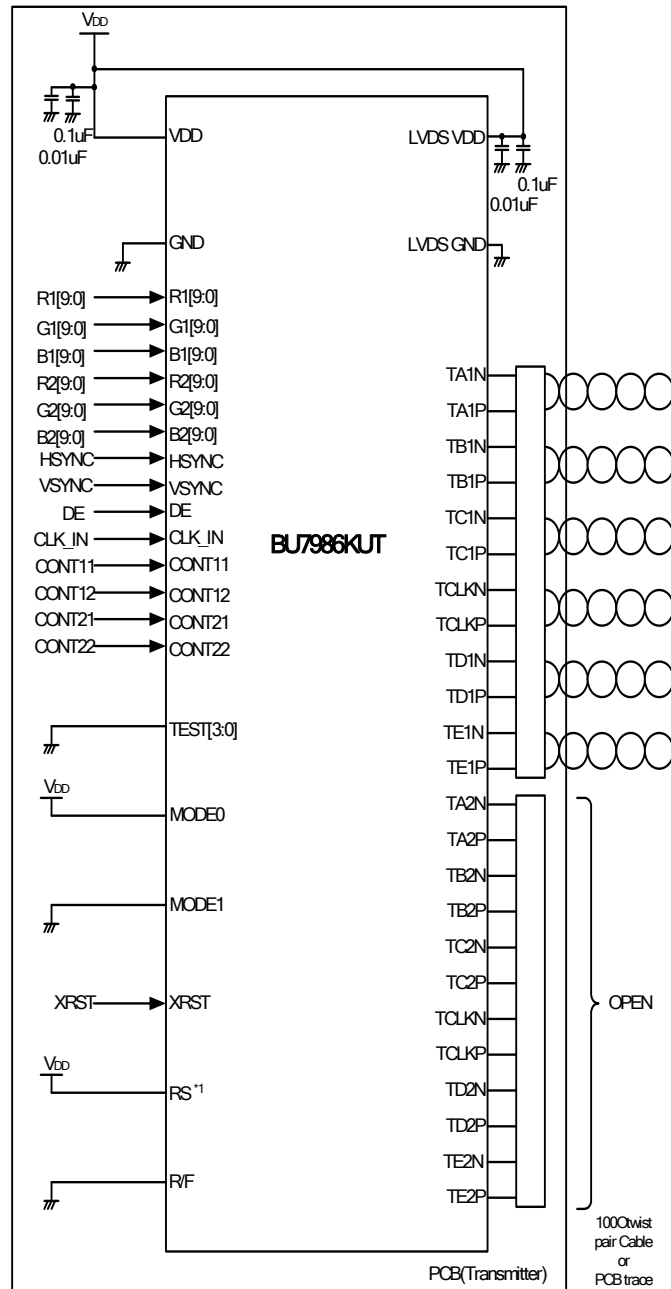
## ●10bit LVCMOS Level Input

Example:

BU7986KUT : Falling edge

Normal swing

Dual-in / Single-out mode



- \*1 : If RS pin is tied to  $V_{DD}$ , LVDS swing is 350m V.  
If RS pin is tied to GND, LVDS swing is 200m V.

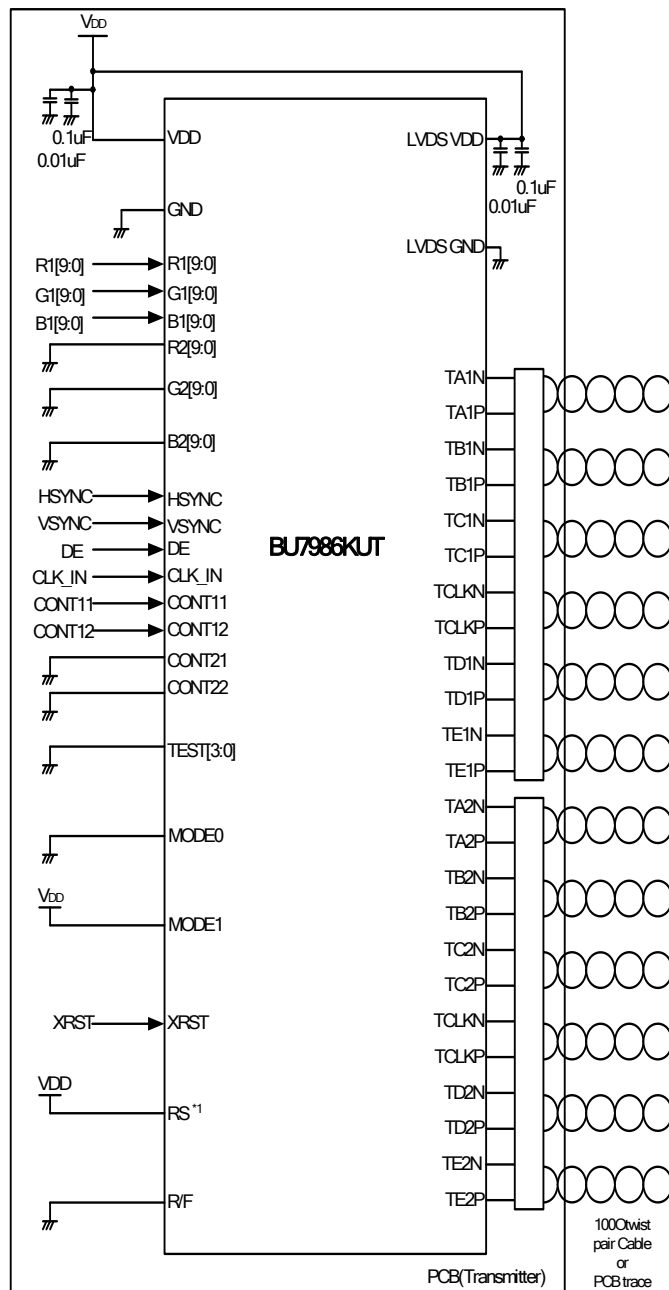
## ● 10bit LVCMOS Level Input

Example:

BU7986KUT : Falling edge

Normal swing

Single-in / Dual-out mode



- \*1 : If RS pin is tied to  $V_{DD}$ , LVDS swing is 350m V.  
If RS pin is tied to GND, LVDS swing is 200m V.

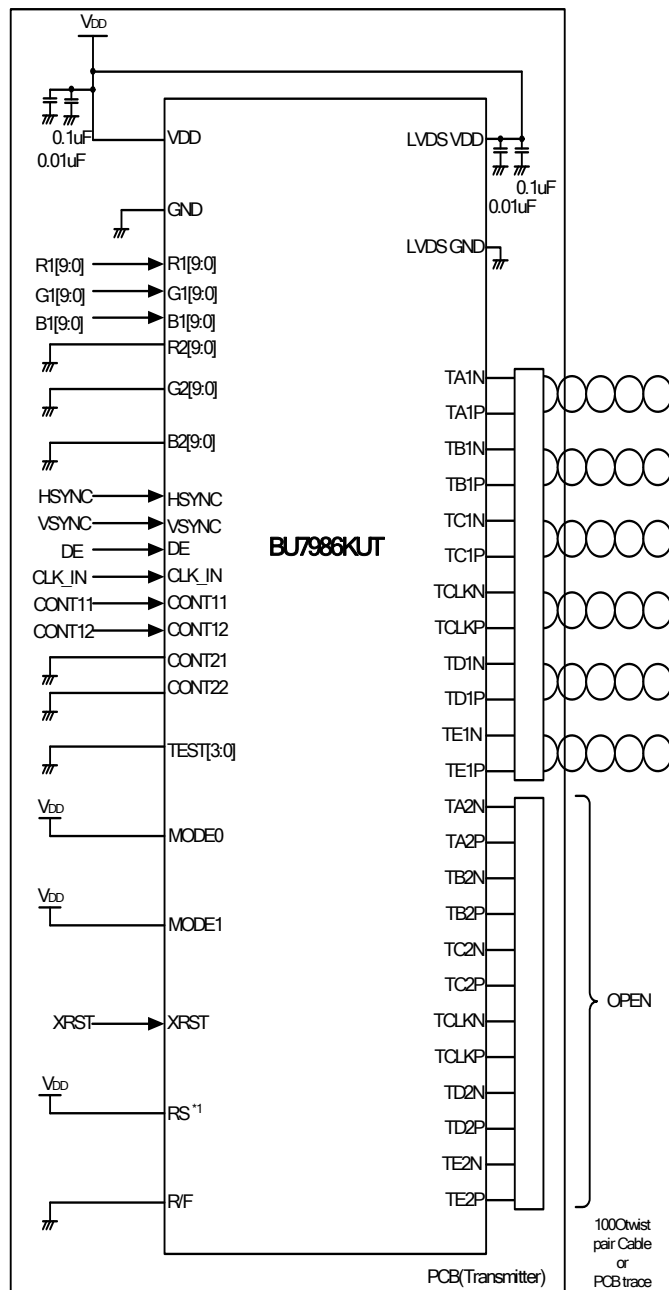
## ● 10bit LVCMOS Level Input

Example:

BU7986KUT : Falling edge

Normal swing

Single-in / Single-out mode



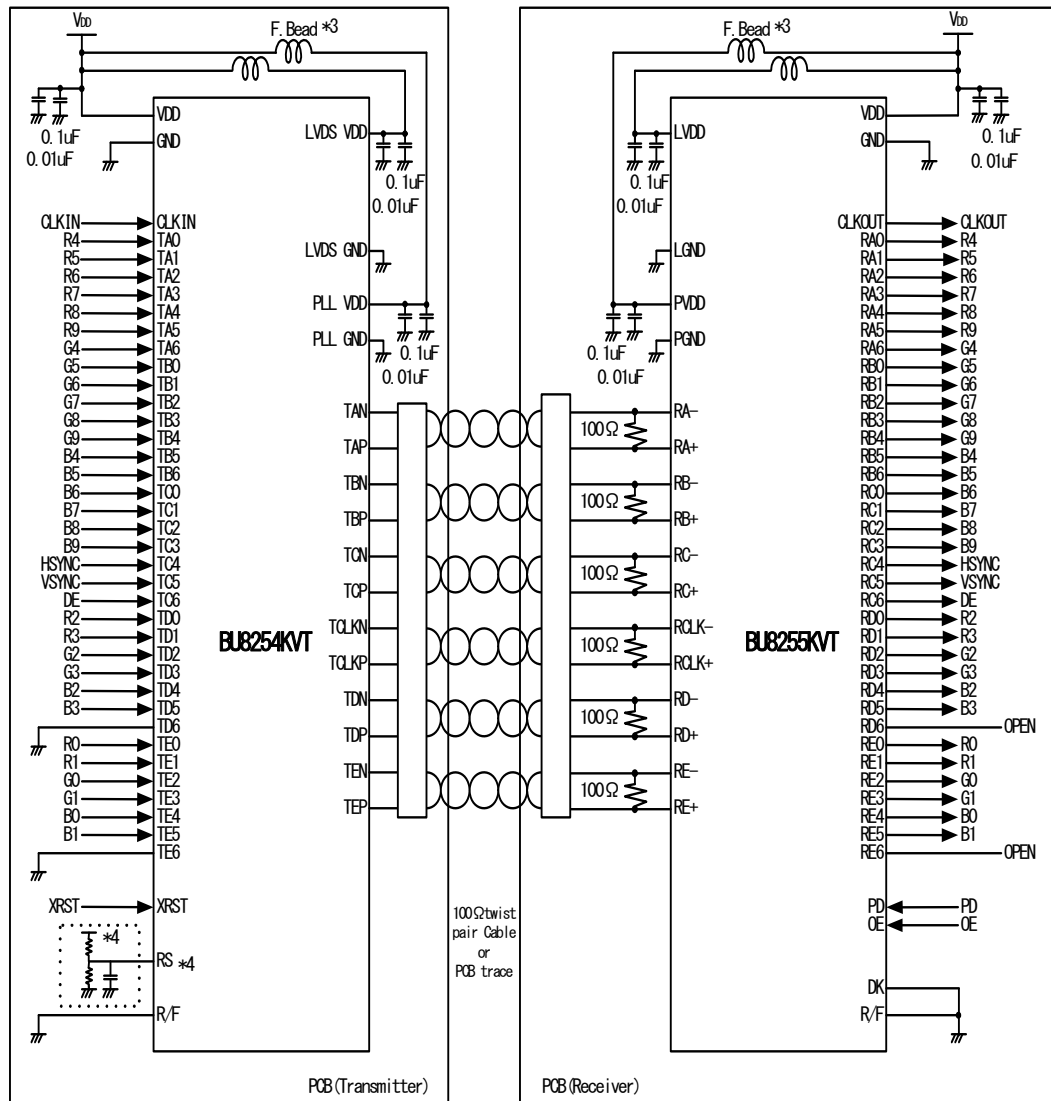
- \*1 : If RS pin is tied to  $V_{DD}$ , LVDS swing is 350m V.  
 If RS pin is tied to GND, LVDS swing is 200m V.

## ● 10bit Small Swing Input

Example:

BU8254KVT : LVCMOS level input/Falling edge/Normal swing

BU8255KVT : Falling edge

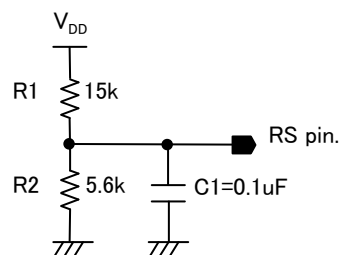


\*3 : Recommended Parts:

F.Bead : BLM18A-Series (Murata Manufacturing)

\*4 : RS pin acts as VREF input pin when input voltage is set to half of high level signal input.

We recommend to locate by-pass condenser near the RS pin.



Example for LVCMOS(1.8V input):(R1,R2)=(15kΩ,5.6kΩ)

# TOFP64V

<Dimension>

(Unit:mm)

<Packing information>

|                   |                                          |
|-------------------|------------------------------------------|
| Container         | Tray(with dry pack)                      |
| Quantity          | 1000pcs                                  |
| Direction of feed | Direction of product is fixed in a tray. |

※When you order , please order in times the amount of package quantity.

- The contents described herein are correct as of June, 2008
- The contents described herein are subject to change without notice. For updates of the latest information, please contact and confirm with ROHM CO.,LTD.
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