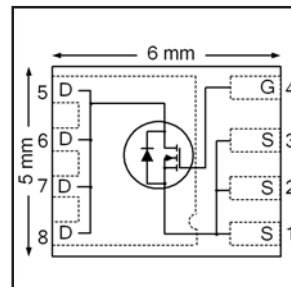


HEXFET® Power MOSFET

V_{DS}	100	V
R_{DS(on)} max (@ V _{GS} = 4.5V)	9.9	mΩ
Q_g (typical)	44	nC
R_G (typical)	1.2	Ω
I_D (@ T _{mb} = 25°C)	88⑥	A



Applications

- Secondary Side Synchronous Rectification
- Inverters for DC Motors
- DC-DC Brick Applications
- Boost Converters

Features

Low R _{DS(on)} (≤9.0mΩ)
Low Thermal Resistance to PCB (≤ 0.8°C/W)
100% R _g tested
Low Profile (≤ 0.9 mm)
Industry-Standard Pinout
Compatible with Existing Surface Mount Techniques
RoHS Compliant Containing no Lead, no Bromide and no Halogen
MSL1, Industrial Qualification

results in

⇒

Benefits

Lower Conduction Losses
Enable better thermal dissipation
Increased Reliability
Increased Power Density
Multi-Vendor Compatibility
Easier Manufacturing
Environmentally Friendlier
Increased Reliability

Base Part Number	Package Type	Standard Pack		Orderable part number
		Form	Quantity	
IRLH5030PBF	PQFN 5mm x 6mm	Tape and Reel	4000	IRLH5030TRPBF

Absolute Maximum Ratings

	Parameter	Max.	Units
V _{GS}	Gate-to-Source Voltage	±16	V
I _D @ T _A = 25°C	Continuous Drain Current, V _{GS} @ 10V	13	A
I _D @ T _A = 70°C	Continuous Drain Current, V _{GS} @ 10V	11	
I _D @ T _{mb} = 25°C	Continuous Drain Current, V _{GS} @ 10V	88⑥	
I _D @ T _{mb} = 100°C	Continuous Drain Current, V _{GS} @ 10V	56⑥	
I _{DM}	Pulsed Drain Current ①	400	
P _D @ T _A = 25°C	Power Dissipation ⑤	3.6	W
P _D @ T _{mb} = 25°C	Power Dissipation ⑤	156	
	Linear Derating Factor ⑤	0.029	W/°C
T _J	Operating Junction and	-55 to + 150	°C
T _{STG}	Storage Temperature Range		

Notes ① through ⑥ are on page 8

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.10	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	7.2	9.0	$m\Omega$	$V_{GS} = 10V, I_D = 50A$ ③
		—	7.9	9.9		$V_{GS} = 4.5V, I_D = 50A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.5	V	$V_{DS} = V_{GS}, I_D = 150\mu A$
$\Delta V_{GS(th)}$	Gate Threshold Voltage Coefficient	—	-5.9	—	mV/ $^\circ\text{C}$	
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 100V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 100V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 16V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -16V$
g_{fs}	Forward Transconductance	160	—	—	S	$V_{DS} = 50V, I_D = 50A$
Q_g	Total Gate Charge	—	94	—	nC	$V_{GS} = 10V, V_{DS} = 50V, I_D = 50A$
Q_g	Total Gate Charge	—	44	66	nC	$V_{DS} = 50V$ $V_{GS} = 4.5V$ $I_D = 50A$ See Fig.17 & 18
Q_{gs1}	Pre-V _{th} Gate-to-Source Charge	—	7.7	—		
Q_{gs2}	Post-V _{th} Gate-to-Source Charge	—	4.0	—		
Q_{gd}	Gate-to-Drain Charge	—	22	—		
Q_{godr}	Gate Charge Overdrive	—	10.3	—		
Q_{sw}	Switch Charge ($Q_{gs2} + Q_{gd}$)	—	26	—	nC	$V_{DS} = 16V, V_{GS} = 0V$
Q_{oss}	Output Charge	—	20	—		
R_G	Gate Resistance	—	1.2	—	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	21	—	ns	$V_{DD} = 50V, V_{GS} = 4.5V$ $I_D = 50A$ $R_G = 1.8\Omega$ See Fig.15
t_r	Rise Time	—	72	—		
$t_{d(off)}$	Turn-Off Delay Time	—	41	—		
t_f	Fall Time	—	41	—		
C_{iss}	Input Capacitance	—	5185	—	pF	$V_{GS} = 0V$ $V_{DS} = 50V$ $f = 1.0MHz$
C_{oss}	Output Capacitance	—	300	—		
C_{rss}	Reverse Transfer Capacitance	—	150	—		

Avalanche Characteristics

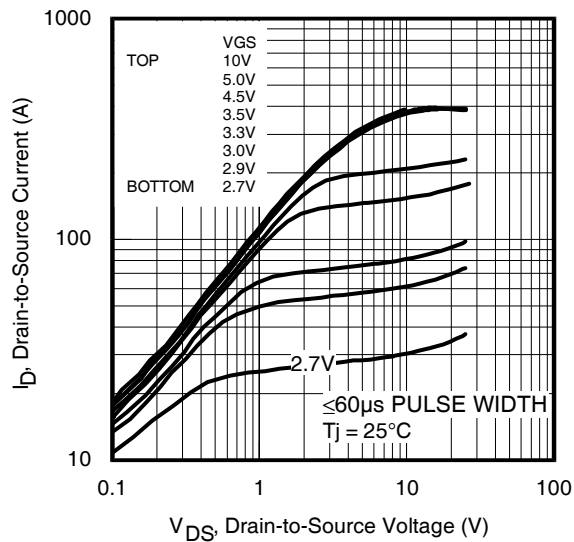
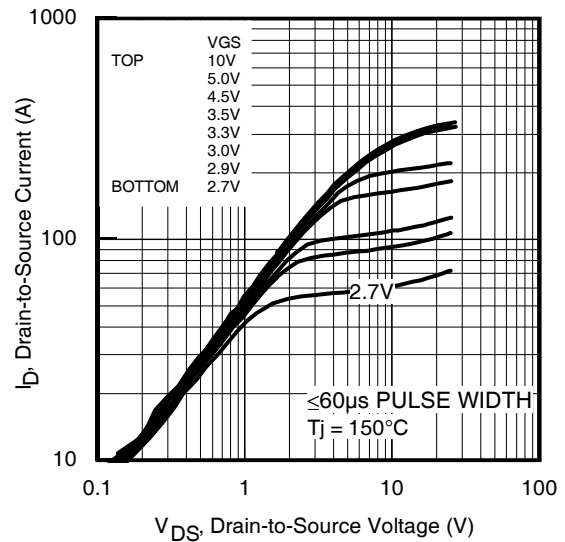
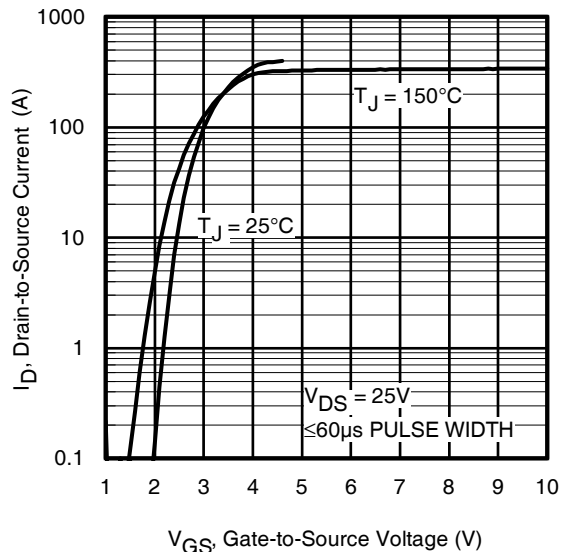
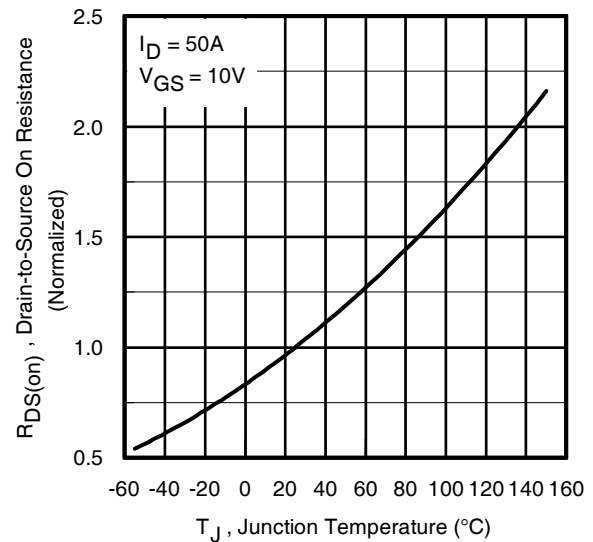
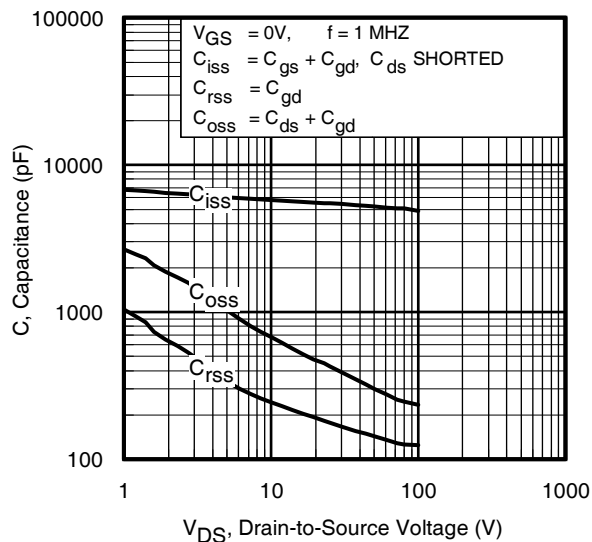
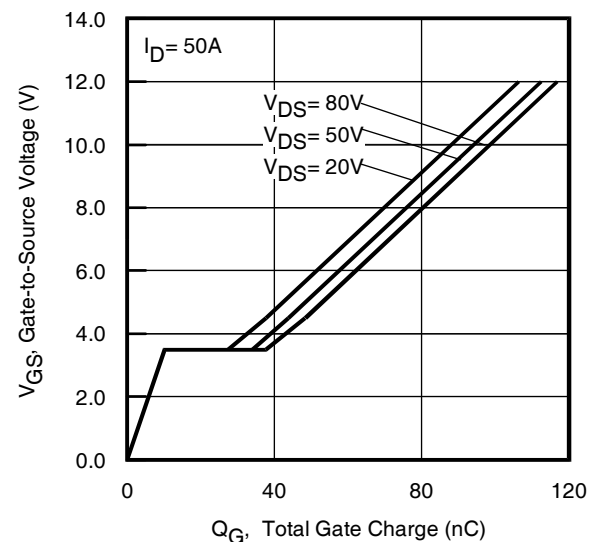
	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	230	mJ
I_{AR}	Avalanche Current ①	—	50	A

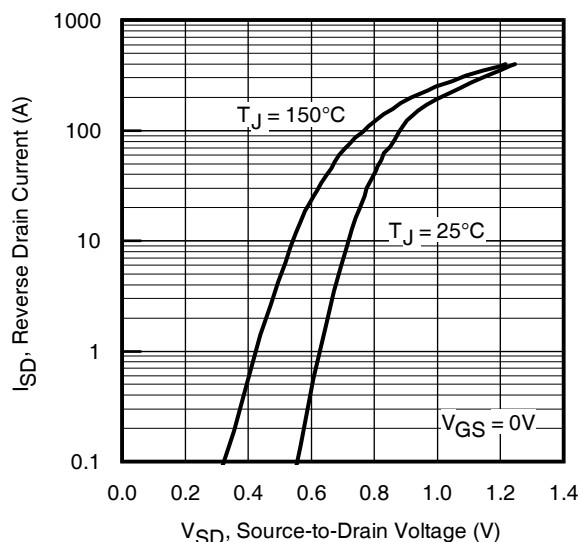
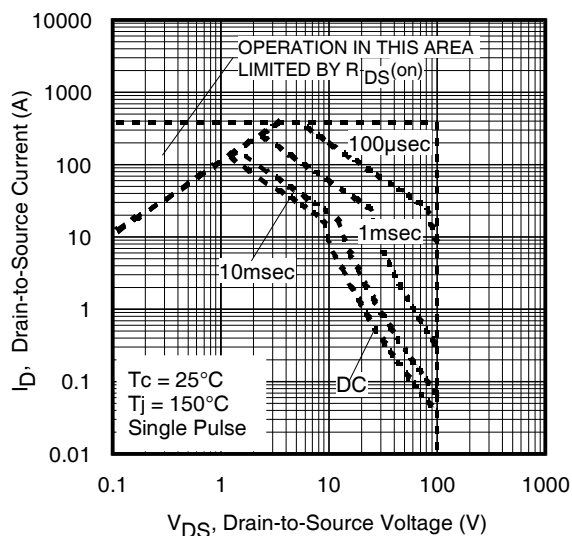
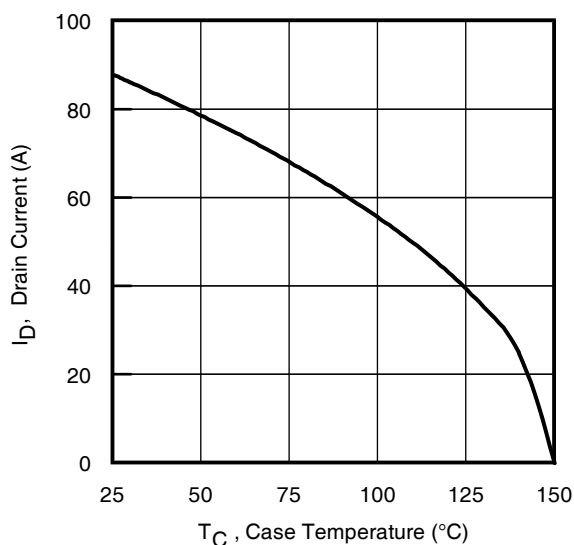
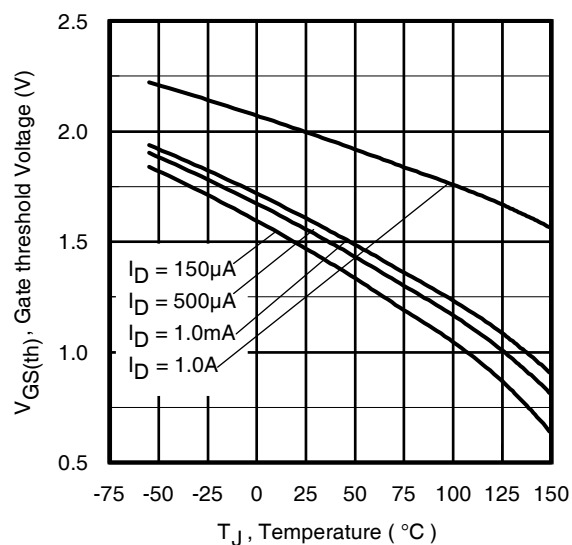
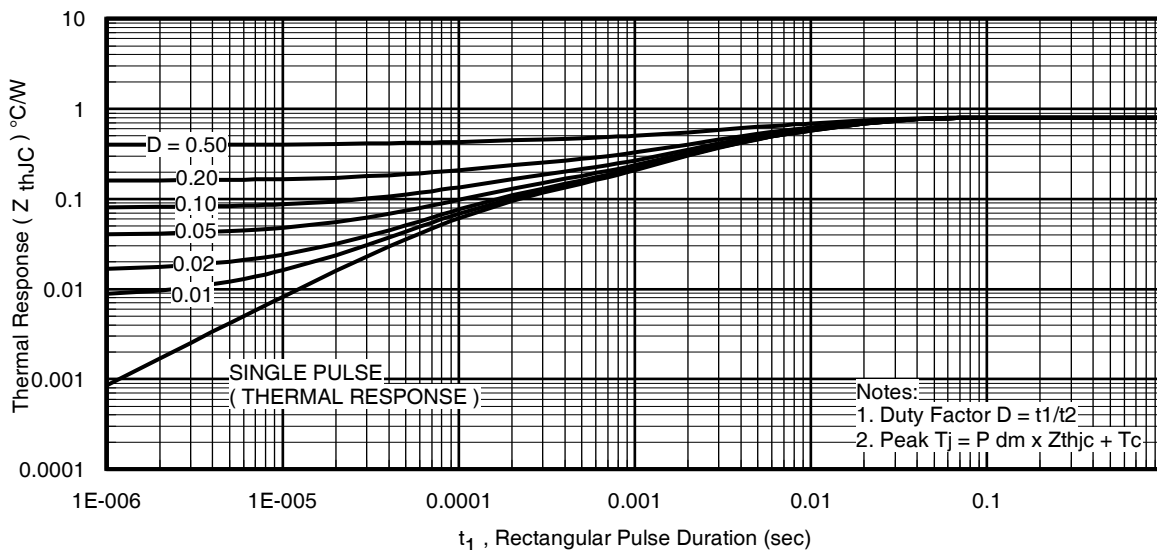
Diode Characteristics

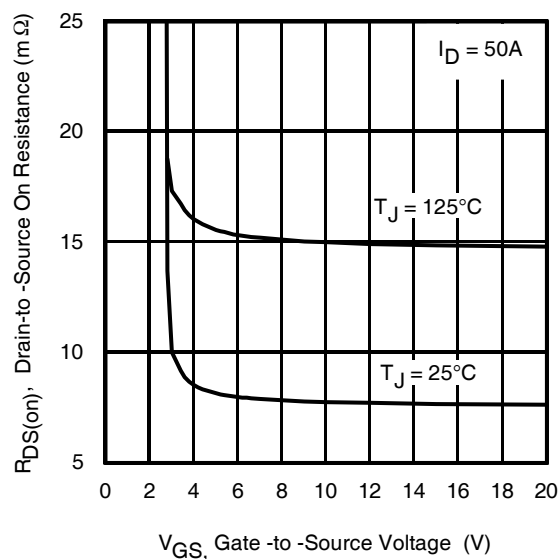
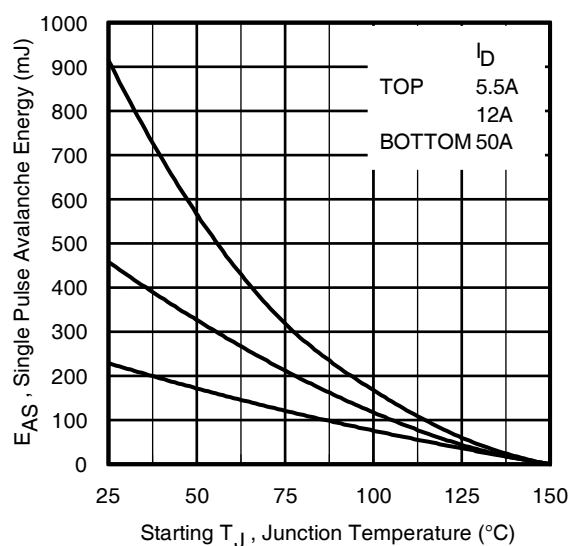
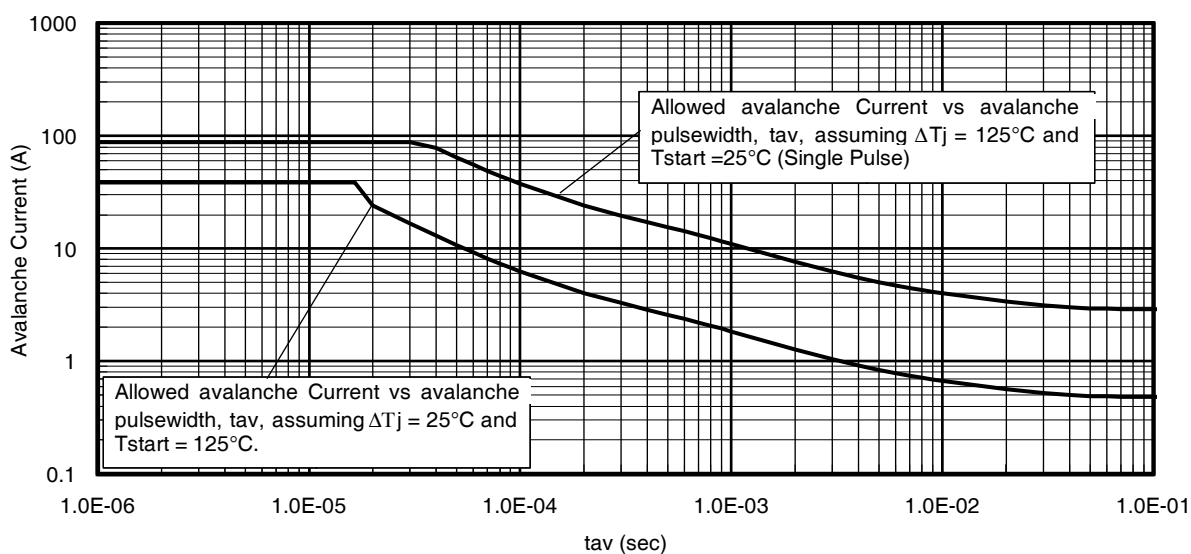
	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	100	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	400		
V_{SD}	Diode Forward Voltage	—	—	1.0	V	$T_J = 25^\circ\text{C}, I_S = 50A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	32	48	ns	$T_J = 25^\circ\text{C}, I_F = 50A, V_{DD} = 50V$
Q_{rr}	Reverse Recovery Charge	—	190	285	nC	$di/dt = 500A/\mu s$ ③
t_{on}	Forward Turn-On Time	Time is dominated by parasitic Inductance				

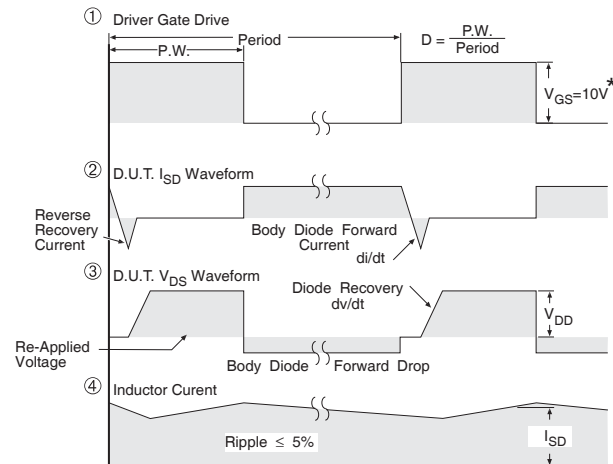
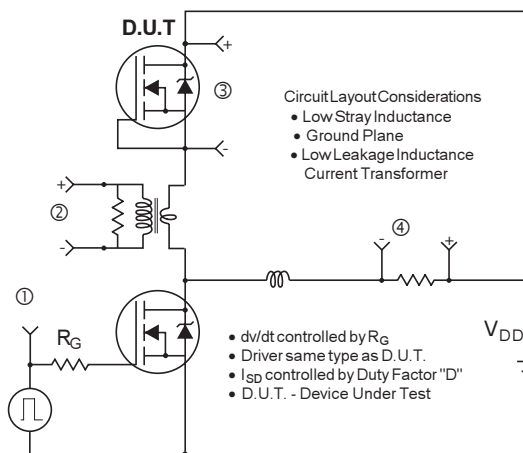
Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC-mb}$	Junction-to-Mounting Base	0.5	0.8	$^\circ\text{C/W}$
$R_{\theta JC}$ (Top)	Junction-to-Case ④	—	15	
$R_{\theta JA}$	Junction-to-Ambient ⑤	—	35	
$R_{\theta JA} (<10s)$	Junction-to-Ambient ⑤	—	33	


Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance vs. Temperature

Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage


Fig 7. Typical Source-Drain Diode Forward Voltage

Fig 8. Maximum Safe Operating Area

Fig 9. Maximum Drain Current vs. Case Temperature

Fig 10. Threshold Voltage vs. Temperature

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Mounting Base


Fig 12. On-Resistance vs. Gate Voltage

Fig 13. Maximum Avalanche Energy vs. Drain Current

Fig 14. Typical Avalanche Current vs. Pulsewidth



* $V_{GS} = 5V$ for Logic Level Devices

Fig 15. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

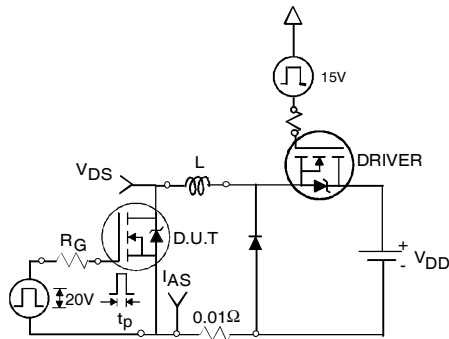


Fig 16a. Unclamped Inductive Test Circuit

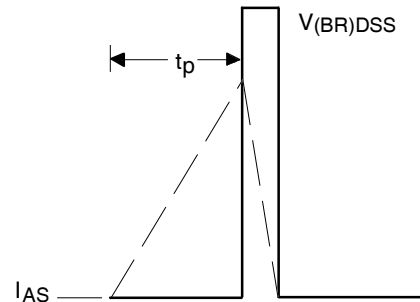


Fig 16b. Unclamped Inductive Waveforms

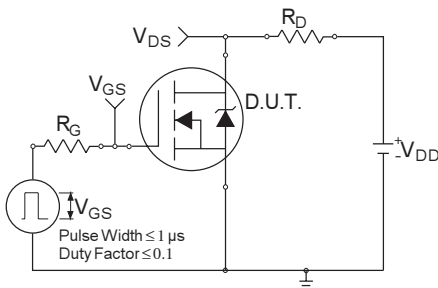


Fig 17a. Switching Time Test Circuit

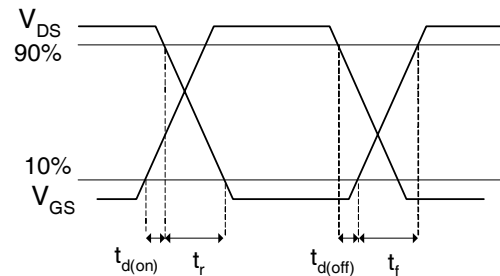


Fig 17b. Switching Time Waveforms

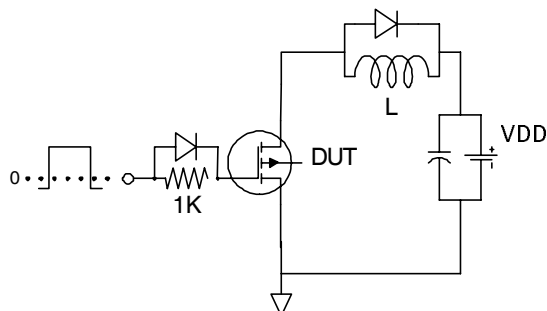


Fig 18a. Gate Charge Test Circuit

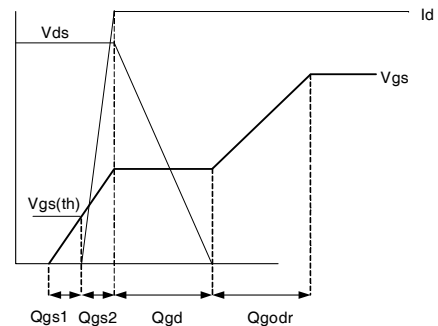
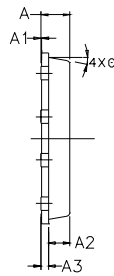
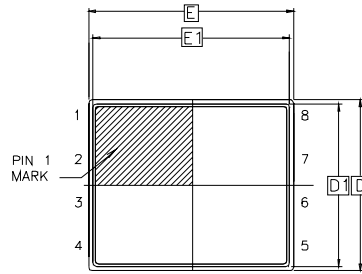


Fig 18b. Gate Charge Waveform

PQFN 5x6 Outline "B" Package Details

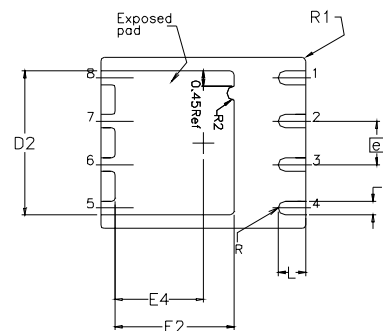


SIDE VIEW



TOP VIEW

DIM SYMBOL	MIN	NOM	MAX
A	0.800	0.830	1.05
A1	0.000	0.020	0.050
A2	0.580	0.630	0.680
A3		0.254 REF	
Ø	0"	10"	12"
b	0.350	0.400	0.470
D	4.850	5.000	5.150
D1	4.675	4.750	5.000
D2	3.700	4.210	4.300
e		1.270 BSC	
E	5.850	6.000	6.150
E1	5.675	5.750	6.000
E2	3.380	3.480	3.760
E4	2.480	2.580	2.680
L	0.550	0.800	0.900
R		0.200 REF	
R1		0.100 REF	
R2	0.150	0.200	0.250



BOTTOM VIEW

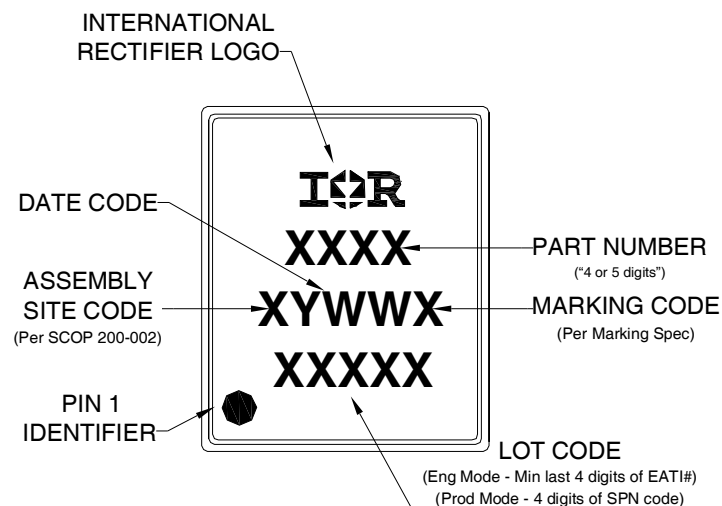
For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136:

<http://www.irf.com/technical-info/appnotes/an-1136.pdf>

For more information on package inspection techniques, please refer to application note AN-1154:

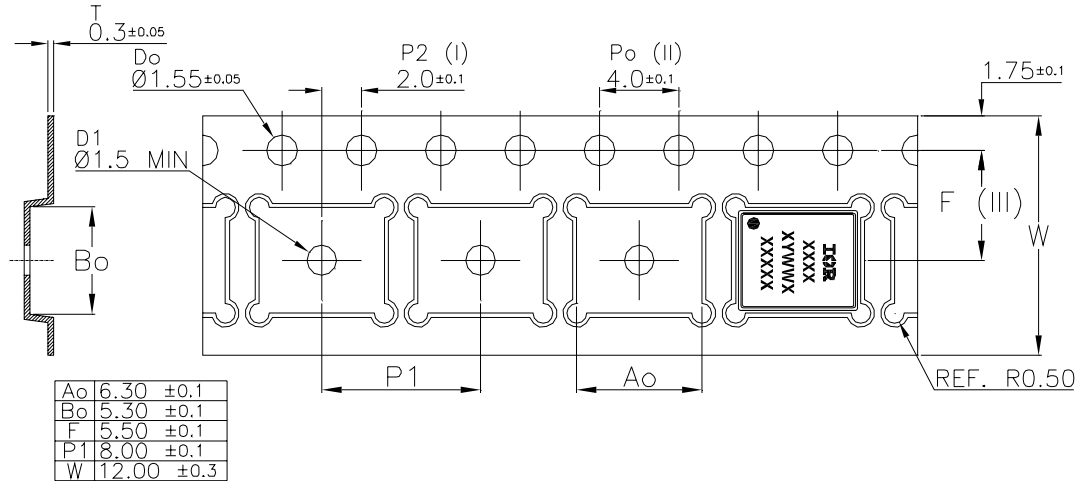
<http://www.irf.com/technical-info/appnotes/an-1154.pdf>

PQFN 5x6 Outline "B" Part Marking



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

PQFN 5x6 Outline "B" Tape and Reel



Qualification information[†]

Qualification level	Industrial ^{††} (per JEDEC JESD47F ^{†††} guidelines)	
Moisture Sensitivity Level	PQFN 5mm x 6mm	MSL1 (per JEDEC J-STD-020D ^{†††})
RoHS compliant	Yes	

[†] Qualification standards can be found at International Rectifier's web site

<http://www.irf.com/product-info/reliability>

^{††} Higher qualification ratings may be available should the user have such requirements.

Please contact your International Rectifier sales representative for further information:

<http://www.irf.com/whoto-call/salesrep/>

^{†††} Applicable version of JEDEC standard at the time of product release.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.18\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 50\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ R_θ is measured at T_J of approximately 90°C .
- ⑤ When mounted on 1 inch square 2 oz copper pad on 1.5x1.5 in. board of FR-4 material.
- ⑥ Calculated continuous current based on maximum allowable junction temperature.

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IR WORLD HEADQUARTERS: 101 N. Sepulveda Blvd., El Segundo, California 90245, USA

To contact International Rectifier, please visit <http://www.irf.com/whoto-call/>