

International **IR** Rectifier

- Ultra Low On-Resistance
- P-Channel
- Surface Mount (IRFR5505)
- Straight Lead (IRFU5505)
- Advanced Process Technology
- Fast Switching
- Fully Avalanche Rated
- Lead-Free
- Halogen-Free

PD - 95077B

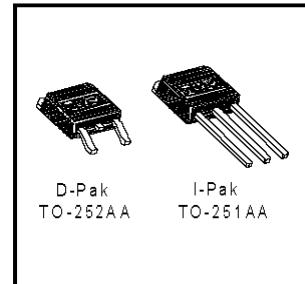
IRFR5505PbF IRFU5505PbF

	$V_{DSS} = -55V$ $R_{DS(on)} = 0.11\Omega$ $I_D = -18A$
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Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D-Pak is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.



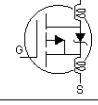
Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$	-18	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$	-11	
I_{DM}	Pulsed Drain Current ①	-64	
$P_D @ T_C = 25^\circ C$	Power Dissipation	57	W
	Linear Derating Factor	0.45	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	150	mJ
I_{AR}	Avalanche Current ①	-9.6	A
E_{AR}	Repetitive Avalanche Energy ①	5.7	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.0	V/ns
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

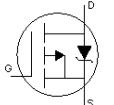
Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	2.2	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)**	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-55	---	---	V	$V_{GS} = 0V, I_D = -250\mu\text{A}$
$\Delta V_{(BR)DSS/\Delta T_J}$	Breakdown Voltage Temp. Coefficient	---	-0.049	---	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = -1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	---	---	0.11	Ω	$V_{GS} = -10V, I_D = -9.6\text{A}$ ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	---	-4.0	V	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$
g_{fs}	Forward Transconductance	4.2	---	---	S	$V_{DS} = -25V, I_D = -9.6\text{A}$
I_{DSS}	Drain-to-Source Leakage Current	---	---	-25	μA	$V_{DS} = -55V, V_{GS} = 0V$
		---	---	-250	μA	$V_{DS} = -44V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	---	---	-100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	---	---	100	nA	$V_{GS} = -20V$
Q_g	Total Gate Charge	---	---	32	nC	$I_D = -9.6\text{A}$
Q_{gs}	Gate-to-Source Charge	---	---	7.1	nC	$V_{DS} = -44V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	---	---	15	nC	$V_{GS} = -10V$, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	---	12	---	ns	$V_{DD} = -28V$
t_r	Rise Time	---	28	---		$I_D = -9.6\text{A}$
$t_{d(off)}$	Turn-Off Delay Time	---	20	---		$R_G = 2.6\Omega$
t_f	Fall Time	---	16	---		$R_D = 2.8\Omega$, See Fig. 10 ④
L_D	Internal Drain Inductance	---	4.5	---	nH	Between lead, 6mm (0.25in.) from package and center of die contact ⑤
L_S	Internal Source Inductance	---	7.5	---		
C_{iss}	Input Capacitance	---	650	---	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	---	270	---		$V_{DS} = -25V$
C_{rss}	Reverse Transfer Capacitance	---	120	---		$f = 1.0\text{MHz}$, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	---	---	-18	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	---	---	-64		
V_{SD}	Diode Forward Voltage	---	---	-1.6	V	$T_J = 25^\circ\text{C}, I_S = -9.6\text{A}, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	---	51	77	ns	$T_J = 25^\circ\text{C}, I_F = -9.6\text{A}$
Q_{rr}	Reverse Recovery Charge	---	110	160	nC	$di/dt = 100\text{A}/\mu\text{s}$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.

② Starting $T_J = 25^\circ\text{C}$, $L = 3.2\text{mH}$

⑤ This is applied for I-PAK, L_S of D-PAK is measured between lead and center of die contact

$R_G = 25\Omega, I_{AS} = -9.6\text{A}$. (See Figure 12)

③ $I_{SD} \leq -9.6\text{A}$, $di/dt \leq 290\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$

** When mounted on 1" square PCB (FR-4 or G-10 Material) .

For recommended footprint and soldering techniques refer to application note #AN-994

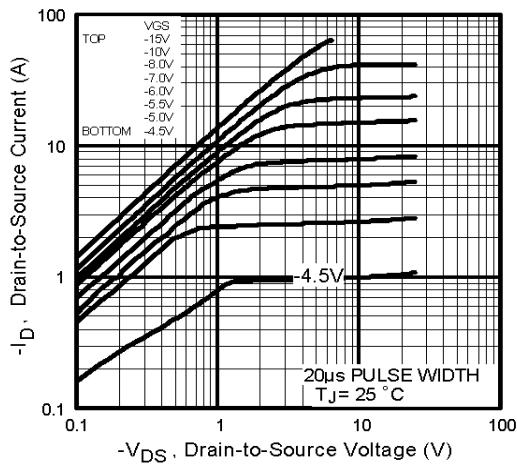


Fig 1. Typical Output Characteristics

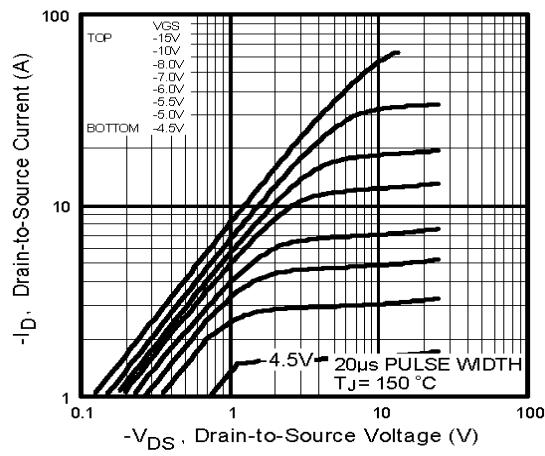


Fig 2. Typical Output Characteristics

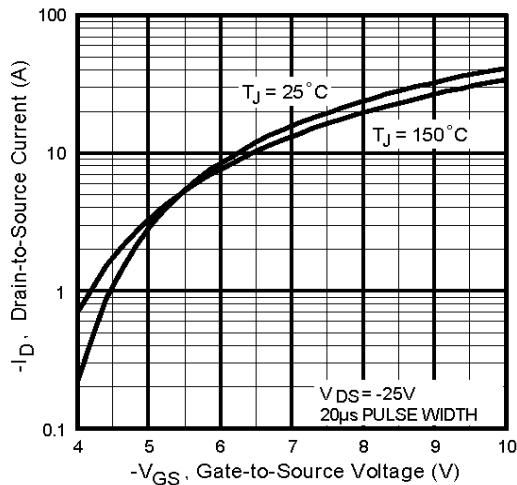


Fig 3. Typical Transfer Characteristics

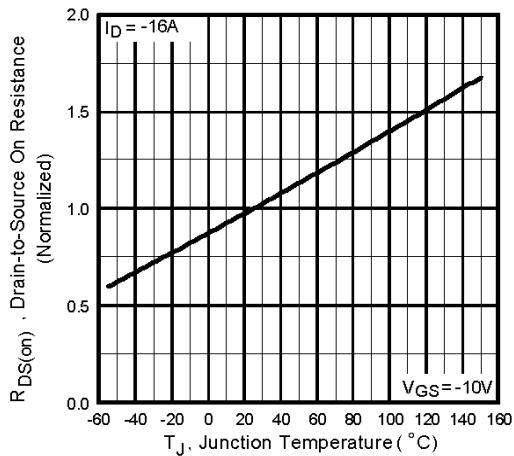


Fig 4. Normalized On-Resistance
Vs. Temperature

IRFR/U5505PbF

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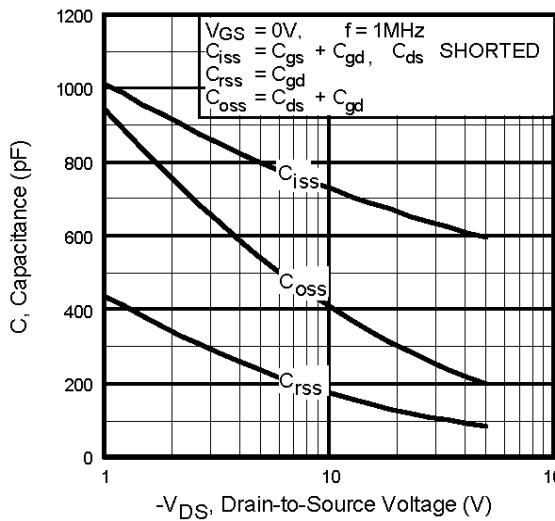


Fig 5. Typical Capacitance Vs.
Drain-to-Source Voltage

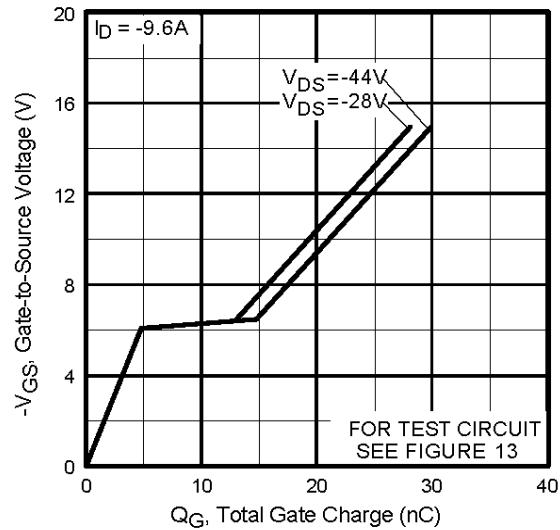


Fig 6. Typical Gate Charge Vs.
Gate-to-Source Voltage

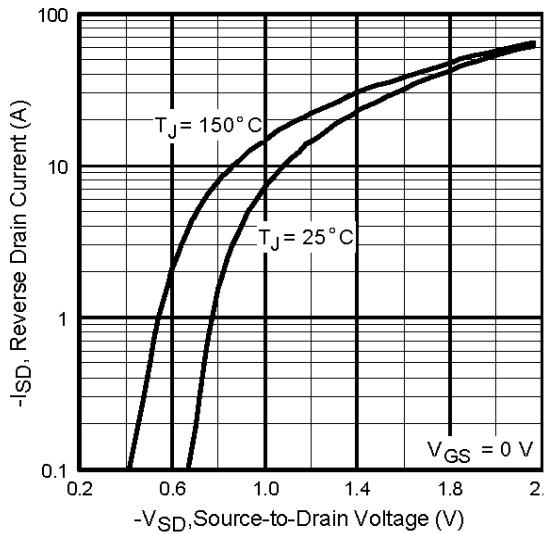


Fig 7. Typical Source-Drain Diode
Forward Voltage

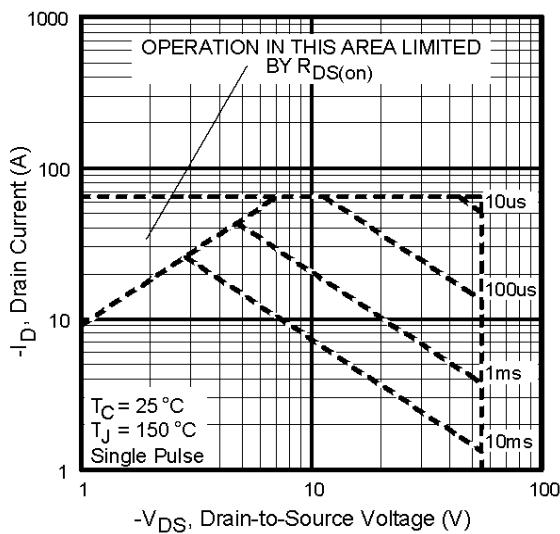


Fig 8. Maximum Safe Operating Area

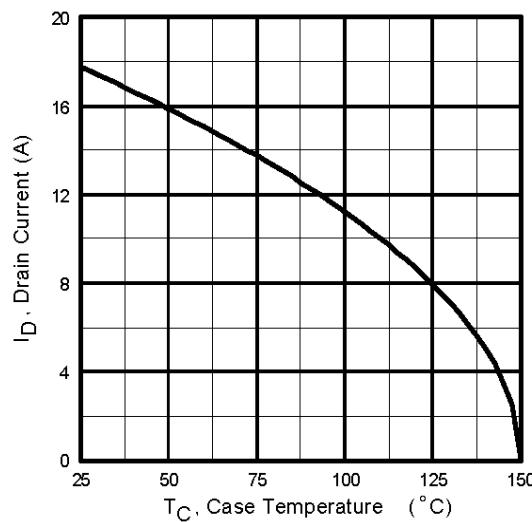


Fig 9. Maximum Drain Current Vs.
 Case Temperature

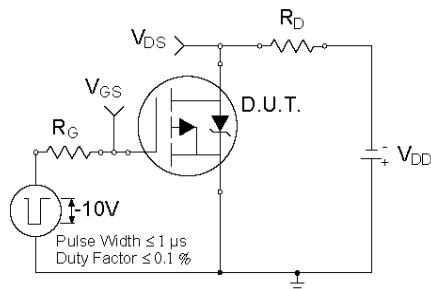


Fig 10a. Switching Time Test Circuit

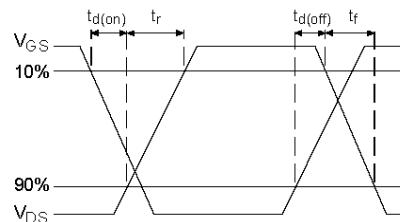


Fig 10b. Switching Time Waveforms

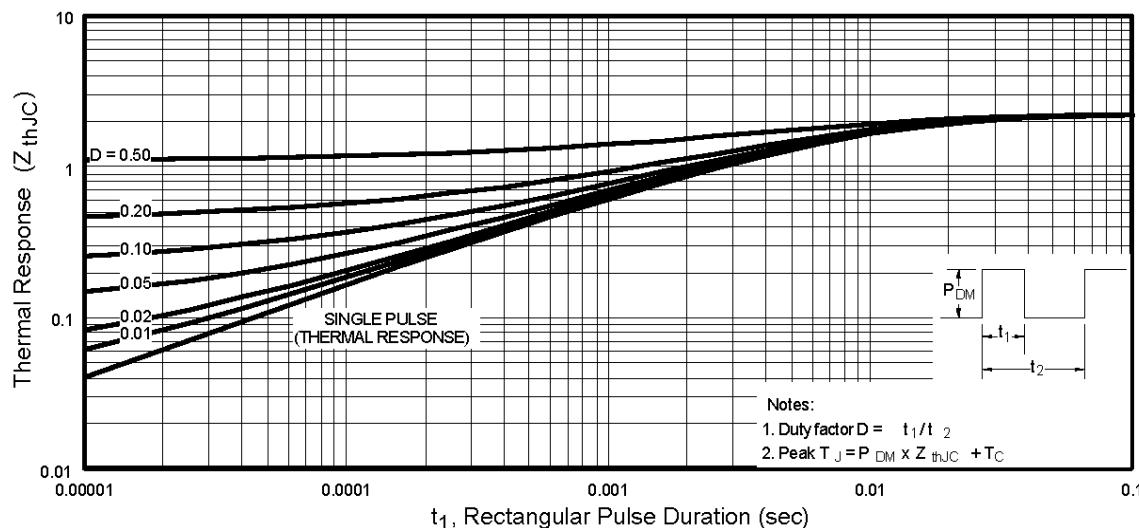


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

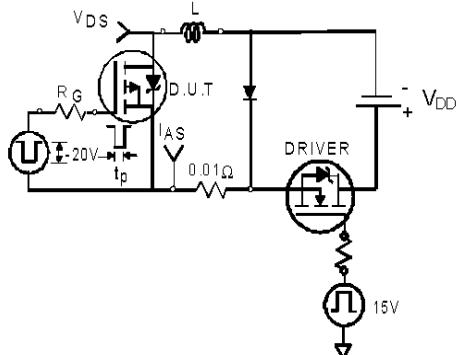


Fig 12a. Unclamped Inductive Test Circuit

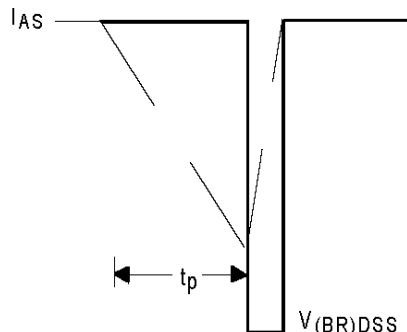


Fig 12b. Unclamped Inductive Waveforms

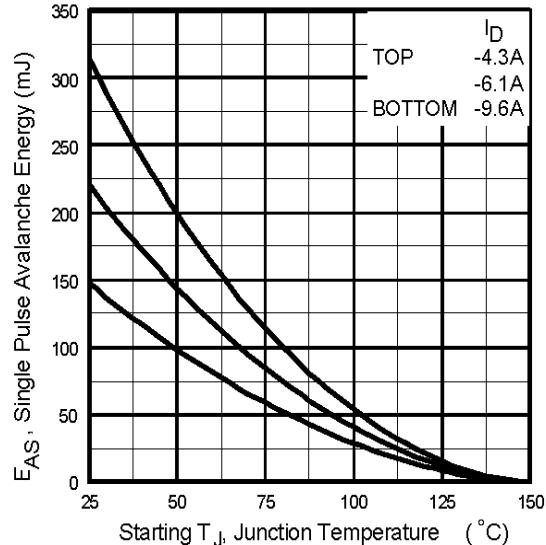


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

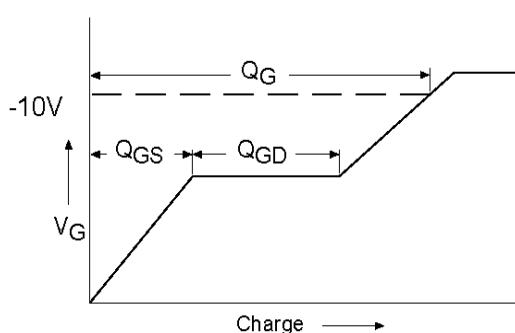


Fig 13a. Basic Gate Charge Waveform

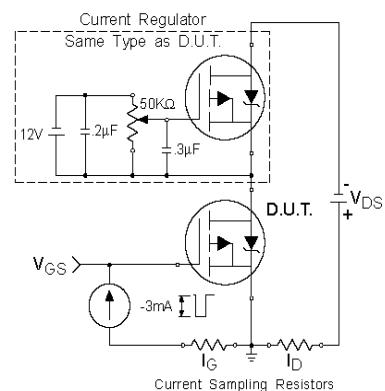
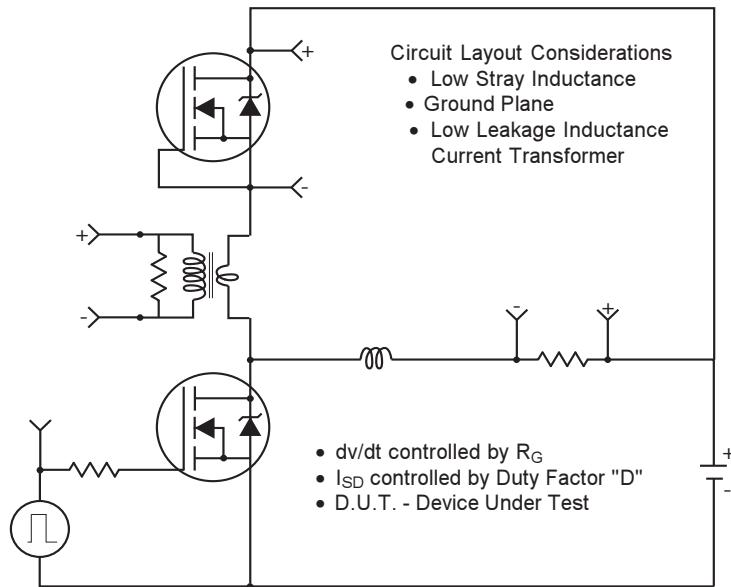


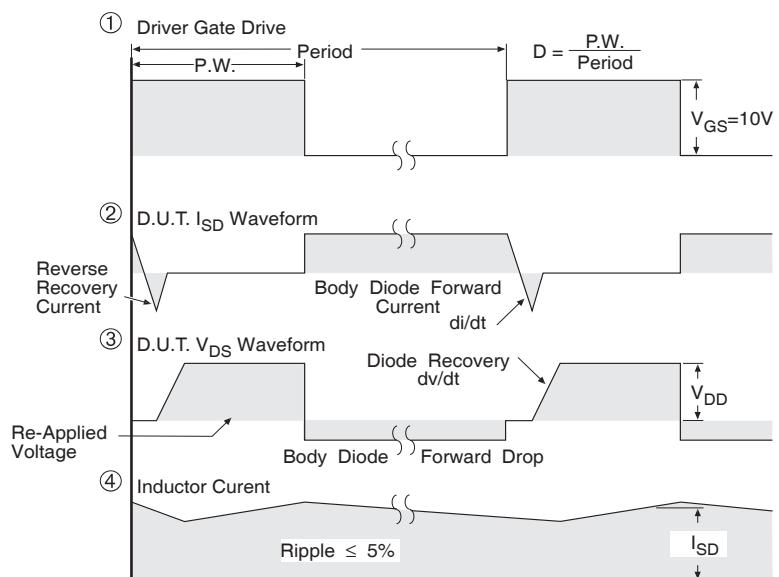
Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity for P-Channel

** Use P-Channel Driver for P-Channel Measurements



*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

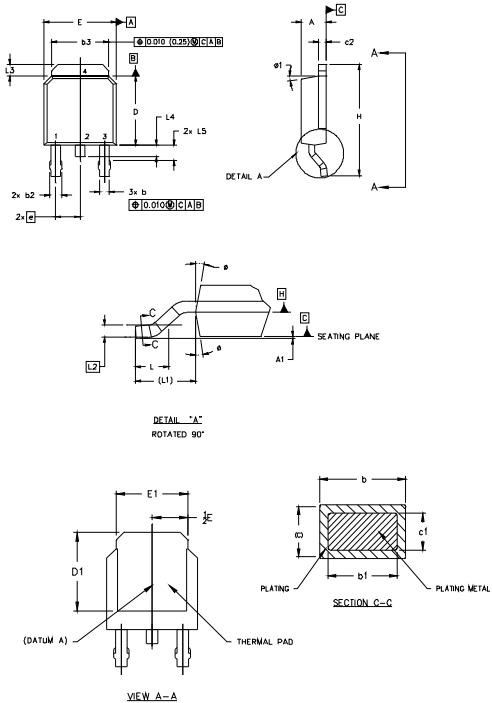
Fig 14 For P Channel HEXFETS

IRFR/U5505PbF

D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)

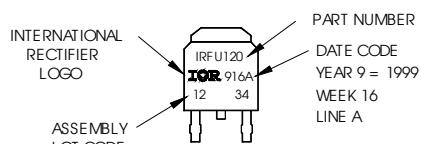
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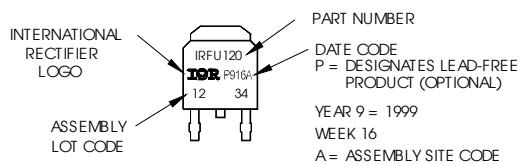
D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IFRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW 16, 1999
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position indicates "Lead-Free"



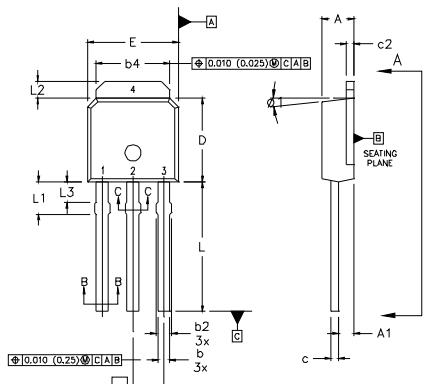
OR



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

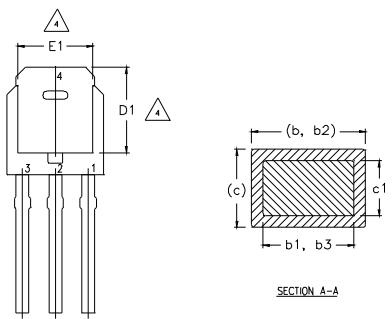
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
5. LEAD DIMENSION UNCONTROLLED IN L3.
6. DIMENSION b1, b3 APPLY TO BASE METAL ONLY.
7. OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA.
8. CONTROLLING DIMENSION : INCHES.

SYMBOL	DIMENSIONS		NOTES
	MILLIMETERS	INCHES	
	MIN.	MAX.	
A	2.18	2.39	
A1	0.89	1.14	0.086 .094
b	0.64	0.89	0.035 0.045
b1	0.64	0.79	0.025 0.035
b2	0.76	1.14	0.030 0.045
b3	0.76	1.04	0.030 0.041
b4	5.00	5.46	0.195 0.215
c	0.46	0.61	0.018 0.024
c1	0.41	0.56	0.016 0.022
c2	.046	0.86	0.018 0.035
D	5.97	6.22	0.235 0.245
D1	5.21	—	0.205 —
E	6.35	6.73	0.250 0.265
E1	4.32	—	0.170 —
e	2.29		0.090 BSC
L	8.89	9.60	0.350 0.380
L1	1.91	2.29	0.075 0.090
L2	0.89	1.27	0.035 0.050
L3	1.14	1.52	0.045 0.060
ø1	0"	15"	0" 15"

LEAD ASSIGNMENTS

HEXFET

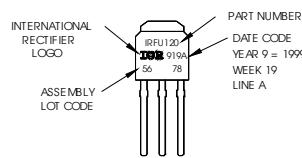
1. - GATE
2. - DRAIN
3. - SOURCE
4. - DRAIN



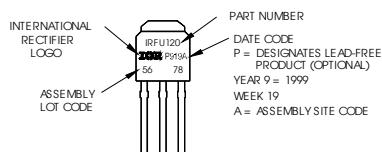
I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120
WITH ASSEMBLY
LOT CODE 5678
ASSEMBLED ON WW 19, 1999
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position indicates "Lead-Free"



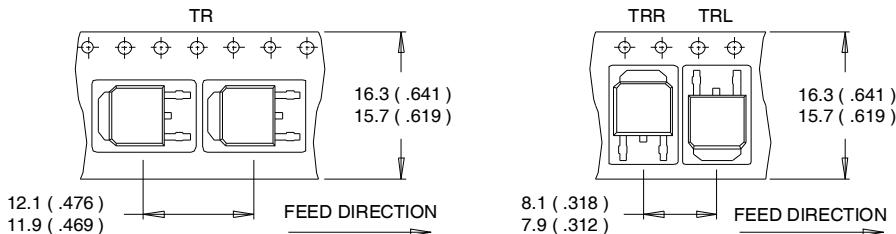
OR



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

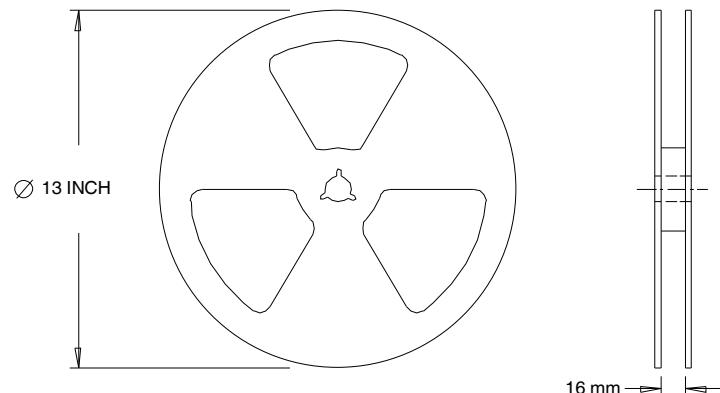
D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Revision History

Date	Comments
11/6/2012	Added Halogen -Free bullet-pg1

Data and specifications subject to change without notice.

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