

# INA2141

## Dual, Low Power, $G = 10, 100$ INSTRUMENTATION AMPLIFIER

### FEATURES

- **LOW OFFSET VOLTAGE:**  $50\mu\text{V}$  max
- **LOW DRIFT:**  $0.5\mu\text{V}/^\circ\text{C}$  max
- **EXCELLENT GAIN ACCURACY:**  
 $\pm 0.05\%$  max at  $G = 10$
- **LOW INPUT BIAS CURRENT:**  $5\text{nA}$  max
- **HIGH CMR:**  $117\text{dB}$  min ( $G = 100$ )
- **INPUTS PROTECTED TO  $\pm 40\text{V}$**
- **WIDE SUPPLY RANGE:**  $\pm 2.25\text{V}$  to  $\pm 18\text{V}$
- **LOW QUIESCENT CURRENT:**  $750\mu\text{A}/\text{IA}$
- **16-PIN PLASTIC DIP, SOL-16**

### APPLICATIONS

- **SENSOR AMPLIFIER**  
THERMOCOUPLE, RTD, BRIDGE
- **MEDICAL INSTRUMENTATION**
- **MULTIPLE CHANNEL SYSTEMS**

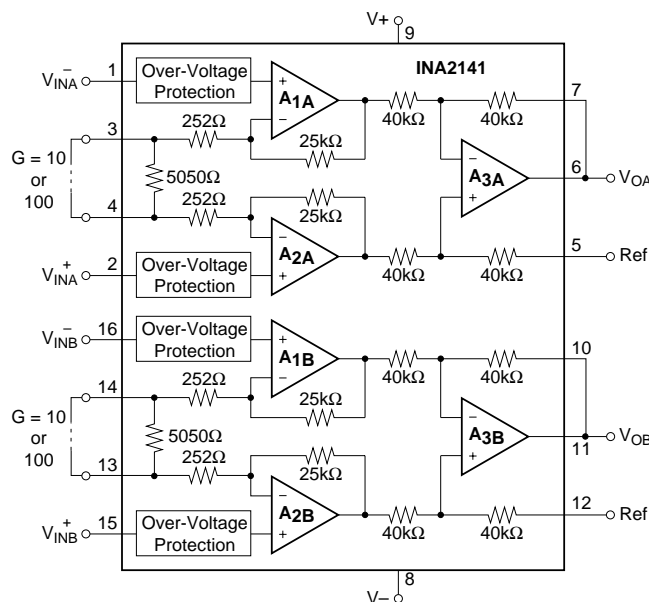
### DESCRIPTION

The INA2141 is a low power, dual instrumentation amplifier offering excellent accuracy. Its versatile 3-op amp design and small size make it ideal for a wide range of applications. Current-feedback input circuitry provides wide bandwidth even at high gain ( $200\text{kHz}$  at  $G = 100$ ).

Simple pin connections set an accurate gain of 10 or  $100\text{V/V}$  without external resistors. Internal input protection can withstand up to  $\pm 40\text{V}$  without damage.

The INA2141 is laser trimmed for very low offset voltage ( $50\mu\text{V}$ ), drift ( $0.5\mu\text{V}/^\circ\text{C}$ ) and high common-mode rejection ( $117\text{dB}$  at  $G = 100$ ). It operates with power supplies as low as  $\pm 2.25\text{V}$ , and quiescent current is only  $750\mu\text{A}$  per amplifier—ideal for battery operated systems.

Packages are 16-pin plastic DIP, and SOL-16 surface-mount, specified for the  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  temperature range.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111  
Internet: <http://www.burr-brown.com/> • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

At  $T_A = +25^{\circ}\text{C}$ ,  $V_S = \pm 15\text{V}$ , and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.

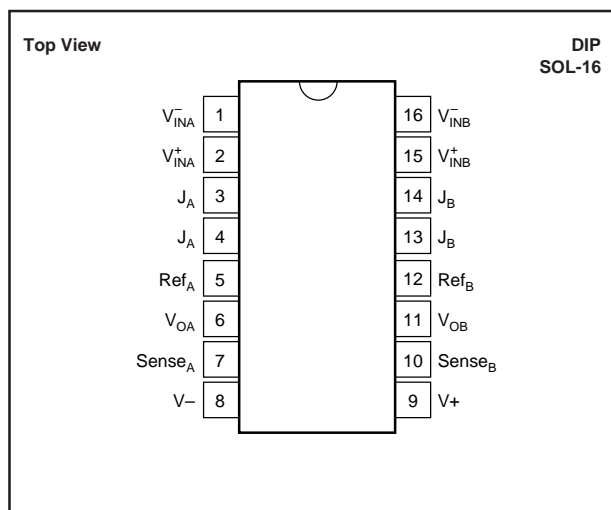
PARAMETER	CONDITIONS	INA2141P, U			INA2141PA, UA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT								
Offset Voltage, RTI	G = 100		±20	±50		*	±125	μV
	G = 10		±50	±100		*	±250	μV
vs Temperature	G = 100		±0.2	±0.5		*	±1.5	μV/°C
	G = 10 <sup>(2)</sup>		±0.5	±2		*	±5	μV/°C
vs Power Supply	V <sub>S</sub> = ±2.25 to ±18V, G = 100		±1	±2		*	±5	μV/V
	G = 10		±2	±10		*	±20	μV/V
Long-Term Stability	G = 100		0.2			*		μV/mo
	G = 10		0.5			*		μV/mo
Impedance, Differential			10 <sup>10</sup>    2			*		Ω    pF
Common-Mode			10 <sup>10</sup>    9			*		Ω    pF
Common-Mode Voltage Range <sup>(1)</sup>	V <sub>O</sub> = 0V	(V+) – 2 (V–) + 2	(V+) – 1.4 (V–) + 1.7		*	*		V
Safe Input Voltage				±40			*	V
Common-Mode Rejection	V <sub>CM</sub> = ±13V, ΔR <sub>S</sub> = 1kΩ							
	G = 100	117	125		110	120		dB
	G = 10	97	106		93	100		dB
BIAS CURRENT			±2	±5		*	±10	nA
vs Temperature			±30			*		pA/°C
Offset Current			±1	±5		*	±10	nA
vs Temperature			±30			*		pA/°C
NOISE VOLTAGE, RTI								
f = 10Hz	G = 100, R <sub>S</sub> = 0Ω		10			*		nV/√Hz
f = 100Hz			8			*		nV/√Hz
f = 1kHz			8			*		nV/√Hz
f <sub>B</sub> = 0.1Hz to 10Hz			0.2			*		μVp-p
f = 10Hz	G = 10, R <sub>S</sub> = 0Ω		22			*		nV/√Hz
f = 100Hz			13			*		nV/√Hz
f = 1kHz			12			*		nV/√Hz
f <sub>B</sub> = 0.1Hz to 10Hz			0.6			*		μVp-p
Noise Current								
f = 10Hz			0.9			*		pA/√Hz
f = 1kHz			0.3			*		pA/√Hz
f <sub>B</sub> = 0.1Hz to 10Hz			30			*		pAp-p
GAIN								
Gain Error	V <sub>O</sub> = ±13.6V, G = 100		±0.03	±0.075		*	±0.15	%
	G = 10		±0.01	±0.05		*	±0.15	%
Gain vs Temperature <sup>(2)</sup>	G = 10, 100		±2	±10		*	*	ppm/°C
Nonlinearity	G = 100		±0.0005	±0.002		*	±0.004	% of FSR
	G = 10		±0.0003	±0.001		*	±0.002	% of FSR
OUTPUT								
Voltage: Positive	R <sub>L</sub> = 10kΩ	(V+) – 1.4	(V+) – 0.9		*	*		V
Negative	R <sub>L</sub> = 10kΩ	(V–) + 1.4	(V–) + 0.9		*	*		V
Load Capacitance Stability			1000			*		pF
Short-Circuit Current			+6/–15			*		mA
FREQUENCY RESPONSE								
Bandwidth, –3dB	G = 100		200			*		kHz
	G = 10		1			*		MHz
Slew Rate	V <sub>O</sub> = ±10V, G = 10		4			*		V/μs
Settling Time, 0.01%	V <sub>O</sub> = ±5V, G = 100		9			*		μs
	G = 10		7			*		μs
Overload Recovery	50% Overdrive		4			*		μs
POWER SUPPLY								
Voltage Range		±2.25	±15	±18	*	*	*	V
Current, Total	V <sub>IN</sub> = 0V		±1.5	±1.6		*	*	mA
TEMPERATURE RANGE								
Specification		–40		85	*		*	°C
Operating		–40		125	*		*	°C
θ <sub>JA</sub>			80			*		°C/W

\* Specification same as INA2141P, U.

NOTE: (1) Input common-mode range varies with output voltage—see typical curves. (2) Guaranteed by wafer test.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## PIN CONFIGURATION



## ABSOLUTE MAXIMUM RATINGS

Supply Voltage .....	$\pm 18V$
Analog Input Voltage Range .....	$\pm 40V$
Output Short-Circuit (to ground) .....	Continuous
Operating Temperature .....	$-40^{\circ}C$ to $+125^{\circ}C$
Storage Temperature .....	$-40^{\circ}C$ to $+125^{\circ}C$
Junction Temperature .....	$+150^{\circ}C$
Lead Temperature (soldering, 10s) .....	$+300^{\circ}C$



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

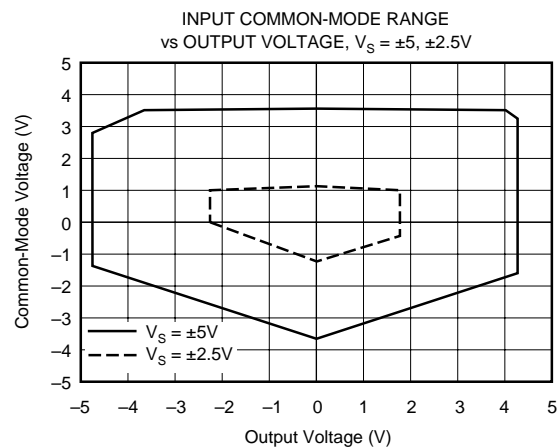
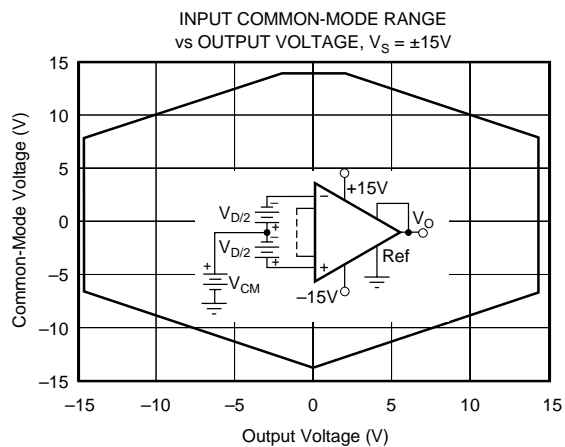
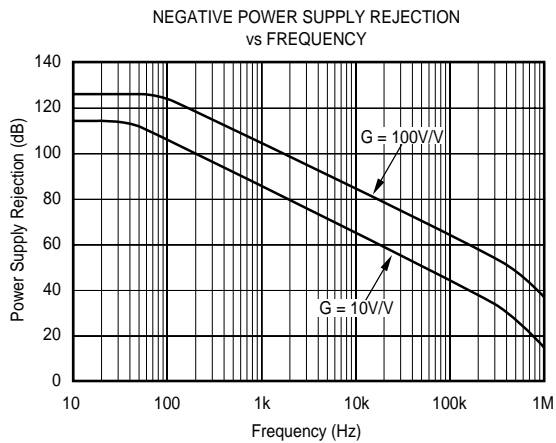
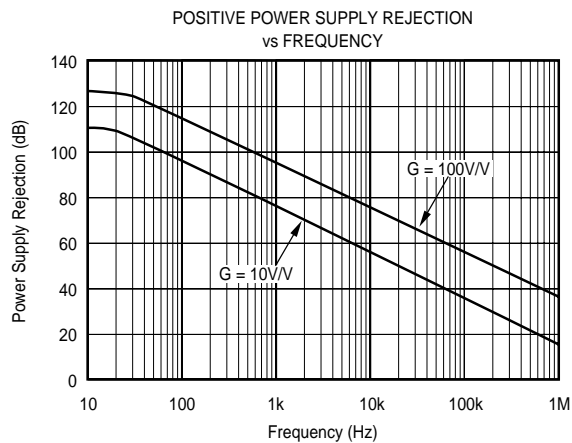
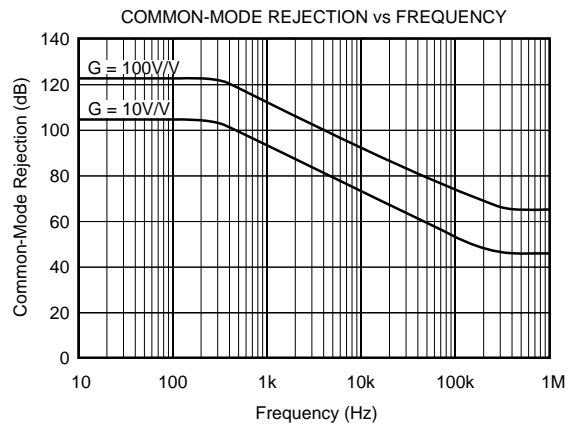
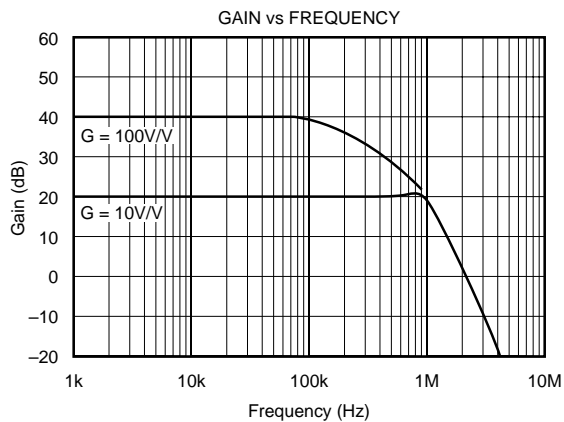
## ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER <sup>(1)</sup>	TEMPERATURE RANGE
INA2141PA	16-Pin Plastic DIP	180	$-40^{\circ}C$ to $+85^{\circ}C$
INA2141P	16-Pin Plastic DIP	180	$-40^{\circ}C$ to $+85^{\circ}C$
INA2141UA	SOL-16 Surface-Mount	211	$-40^{\circ}C$ to $+85^{\circ}C$
INA2141U	SOL-16 Surface-Mount	211	$-40^{\circ}C$ to $+85^{\circ}C$

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

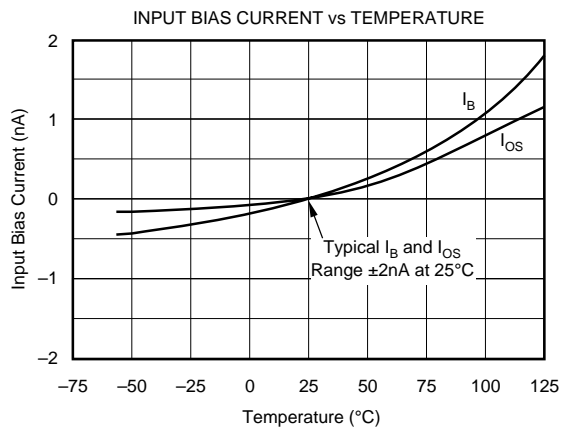
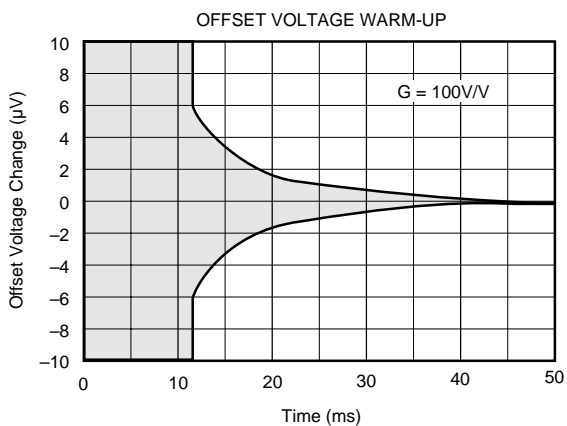
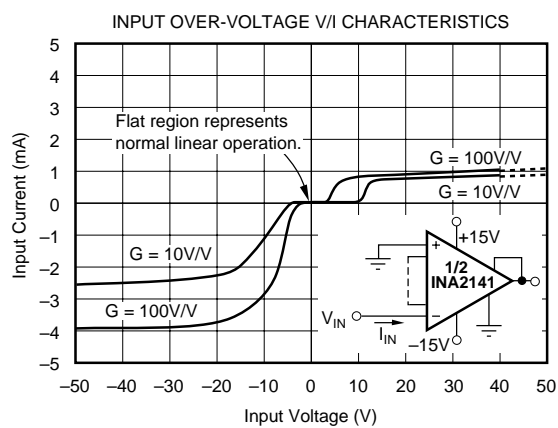
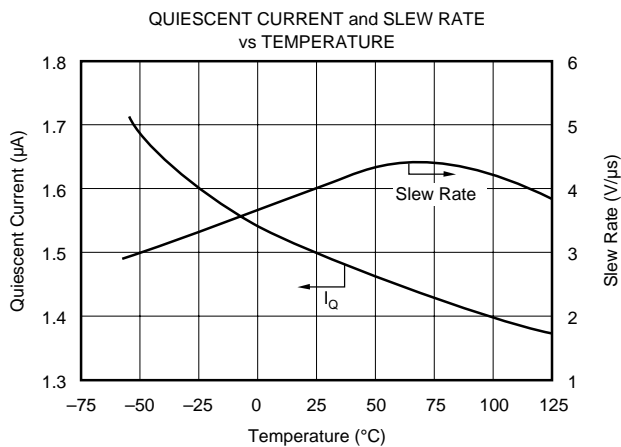
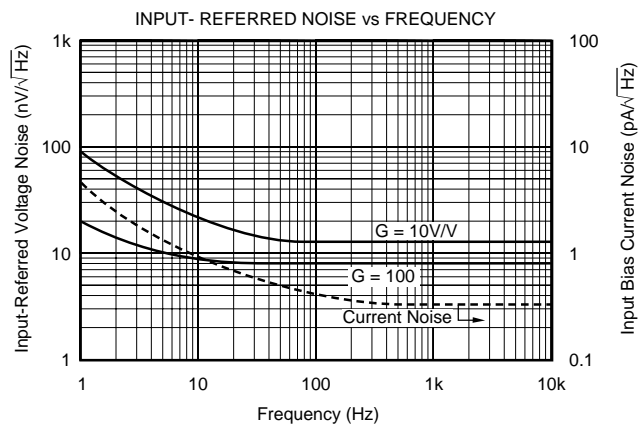
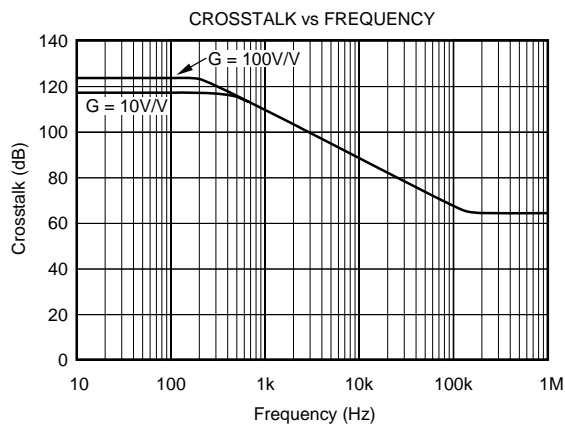
# TYPICAL PERFORMANCE CURVES

At  $T_A = +25^\circ\text{C}$ , and  $V_S = \pm 15\text{V}$ , unless otherwise noted.



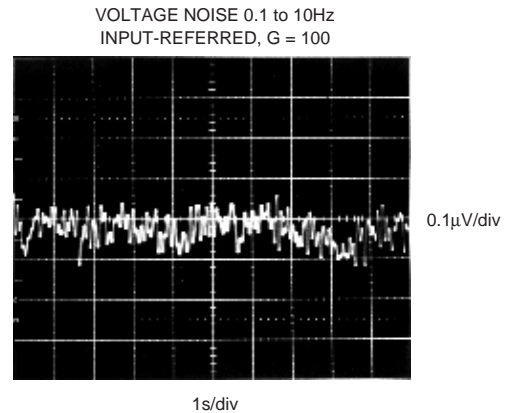
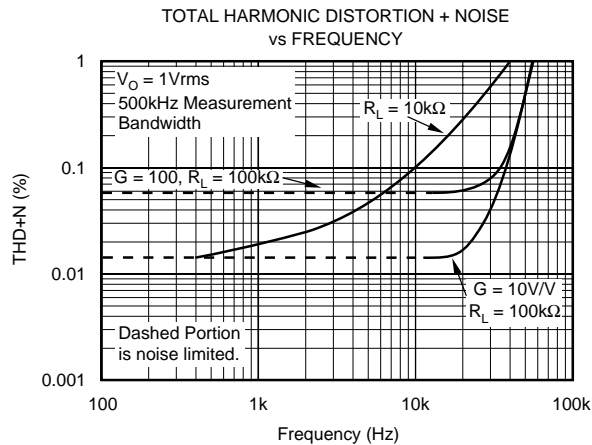
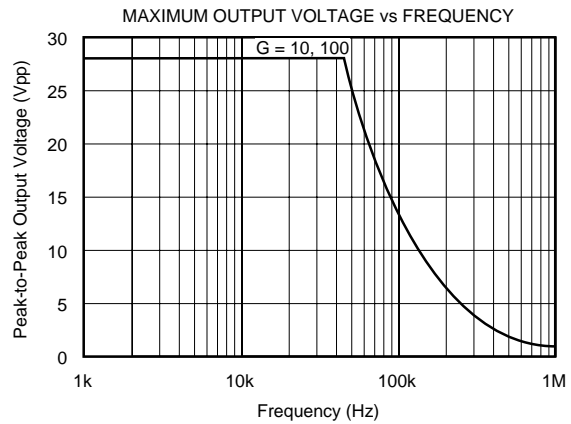
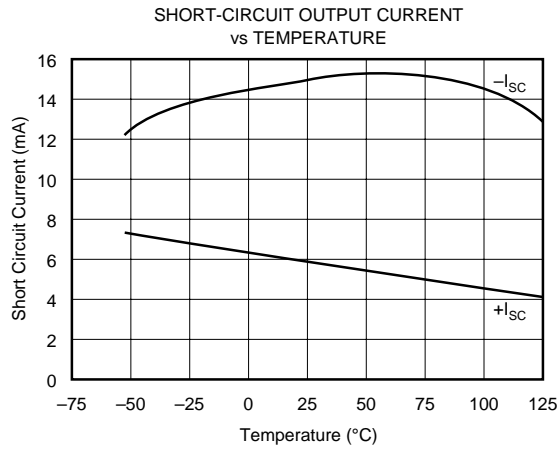
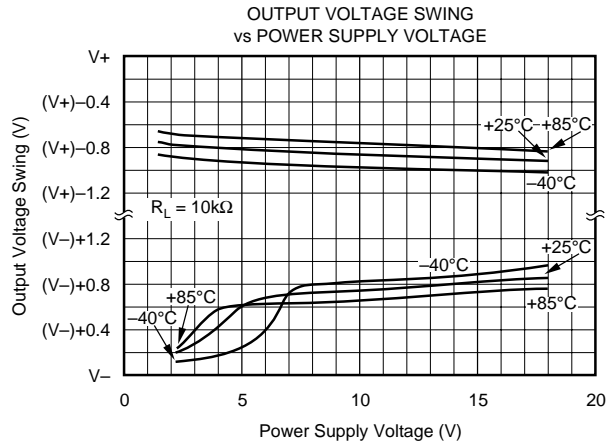
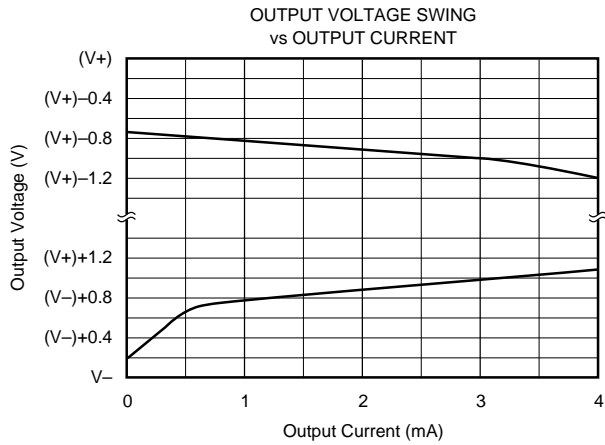
# TYPICAL PERFORMANCE CURVES (CONT)

At  $T_A = +25^\circ\text{C}$ , and  $V_S = \pm 15\text{V}$ , unless otherwise noted.



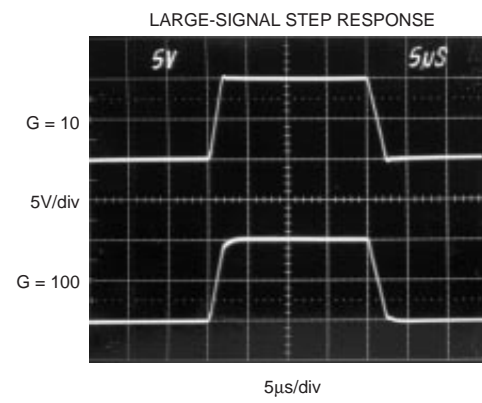
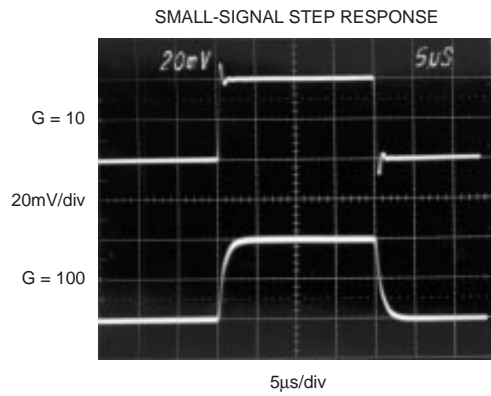
# TYPICAL PERFORMANCE CURVES (CONT)

At  $T_A = +25^\circ\text{C}$ , and  $V_S = \pm 15\text{V}$ , unless otherwise noted.



## TYPICAL PERFORMANCE CURVES (CONT)

At  $T_A = +25^\circ\text{C}$ , and  $V_S = \pm 15\text{V}$  unless otherwise noted.



## APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA2141. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminals (Ref<sub>A</sub> and Ref<sub>B</sub>) which are normally grounded. These must be low-impedance connections to assure good common-mode rejection. A resistance of 8Ω in series with a Ref pin will cause a typical device to degrade to approximately 80dB CMR (G = 1).

The INA2141 has a separate output sense feedback connections Sense<sub>A</sub> and Sense<sub>B</sub>. These must be connected to their respective output terminals for proper operation. The output sense connection can be used to sense the output voltage directly at the load for best accuracy.

### SETTING THE GAIN

Gain of each IA can be independently selected with a jumper connection as shown in Figure 1. G = 10V/V with no jumper installed. With a jumper installed G = 100V/V. To preserve good gain accuracy, this jumper must have low series resistance. A resistance of 0.5Ω in series with the jumper will decrease the gain by 0.1%.

Internal resistor ratios are laser trimmed to assure excellent gain accuracy. Actual resistor values can vary by approximately ±25% from the nominal values shown.

Gains between 10 and 100 can be achieved by connecting an external resistor to the jumper pins. This is not recommended, however, because the ±25% variation of internal resistor values makes the required external resistor value uncertain. A companion model, INA2128, features accurately trimmed internal resistors so that gains from 1 to 10,000 can be set with an external resistor.

### DYNAMIC PERFORMANCE

The typical performance curve “Gain vs Frequency” shows that despite its low quiescent current, the INA2141 achieves wide bandwidth, even at high gain. This is due to its current-feedback topology. Settling time also remains excellent at high gain.

### NOISE PERFORMANCE

The INA2141 provides very low noise in most applications. Low frequency noise is approximately 0.2μVp-p measured from 0.1 to 10Hz (G = 100). This provides dramatically improved noise when compared to state-of-the-art chopper-stabilized amplifiers.

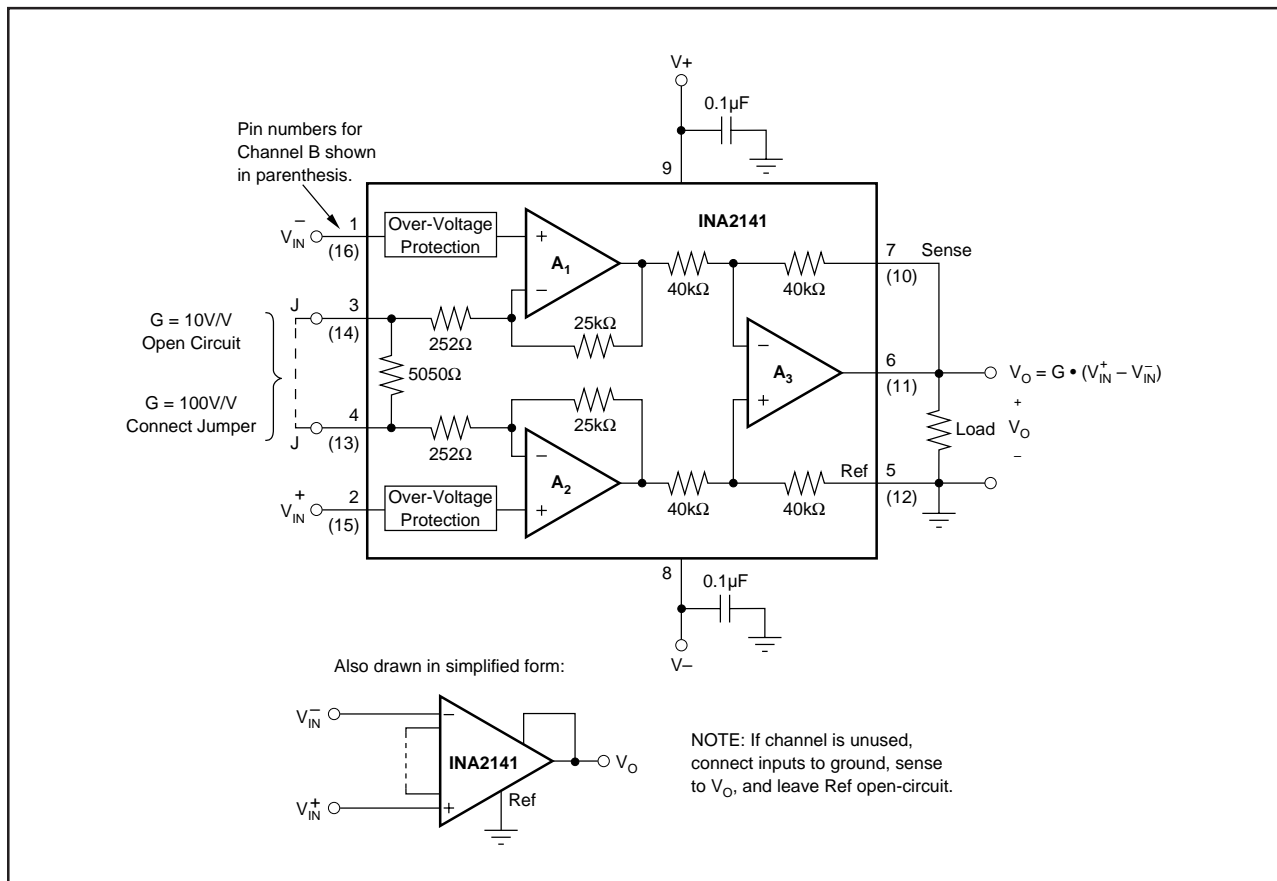


FIGURE 1. Basic Connections.



## OFFSET TRIMMING

The INA2141 is laser trimmed for low offset voltage and offset voltage drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed with the output. The op amp buffer provides low impedance at the Ref terminal to preserve good common-mode rejection.

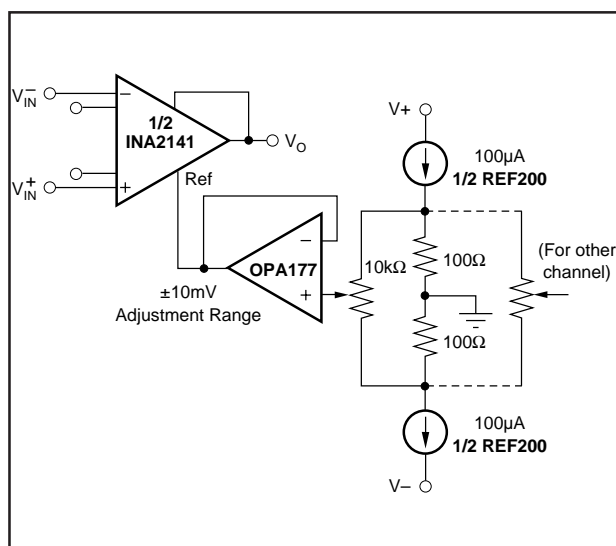


FIGURE 2. Optional Trimming of Output Offset Voltage.

## INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA2141 is extremely high—approximately  $10^{10}\Omega$ . However, a path must be provided for the input bias current of both inputs. This input bias current is approximately  $\pm 2\text{nA}$ . High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 3 shows various provisions for an input bias current path. Without a bias current path, the inputs will float to a potential which exceeds the common-mode range of the INA2141 and the input amplifiers will saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 3). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

## INPUT COMMON-MODE RANGE

The linear input voltage range of the input circuitry of the INA2141 is from approximately 1.4V below the positive supply voltage to 1.7V above the negative supply. As a differential input voltage causes the output voltage increase, however, the linear input range will be limited by the output voltage swing of amplifiers  $A_1$  and  $A_2$ . So the linear com-

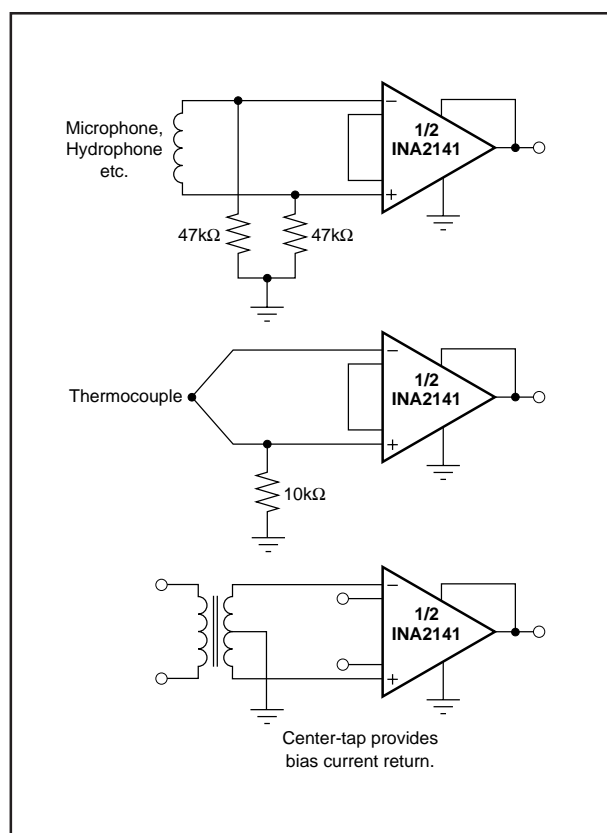


FIGURE 3. Providing an Input Common-Mode Current Path.

mon-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage—see performance curves “Input Common-Mode Range vs Output Voltage”.

Input-overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier will be near zero. The output of the INA2141 will be near 0V even though both inputs are overloaded.

## LOW VOLTAGE OPERATION

The INA2141 can be operated on power supplies as low as  $\pm 2.25\text{V}$ . Performance remains excellent with power supplies ranging from  $\pm 2.25\text{V}$  to  $\pm 18\text{V}$ . Most parameters vary only slightly throughout this supply voltage range—see typical performance curves. Operation at very low supply voltage requires careful attention to assure that the input voltages remain within their linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power supply voltage. Typical performance curves, “Input Common-Mode Range vs Output Voltage” show the range of linear operation for  $\pm 15\text{V}$ ,  $\pm 5\text{V}$ , and  $\pm 2.5\text{V}$  supplies.

## INPUT PROTECTION

The inputs of the INA2141 are individually protected for voltages up to  $\pm 40\text{V}$ . For example, a condition of  $-40\text{V}$  on one input and  $+40\text{V}$  on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value of approximately 1.5 to 5mA. The typical performance curve “Input Bias Current vs Common-Mode Input Voltage” shows this input current limit behavior. The inputs are protected even if the power supplies are disconnected or turned off.

## CHANNEL CROSSTALK

The two channels of the INA2141 are completely independent, including all bias circuitry. At DC and low frequency

there is virtually no signal coupling between channels. Crosstalk increases with frequency and is dependent on circuit gain, source impedance and signal characteristics.

As source impedance increases, careful circuit layout will help achieve lowest channel crosstalk. Most crosstalk is produced by capacitive coupling of signals from one channel to the input section of the other channel. To minimize coupling, separate the input traces as far as practical from any signals associated with the opposite channel. A grounded guard trace surrounding the inputs helps reduce stray coupling between channels. Run the differential inputs of each channel parallel to each other or directly adjacent on top and bottom side of a circuit board. Stray coupling then tends to produce a common-mode signal which is rejected by the IA's input.

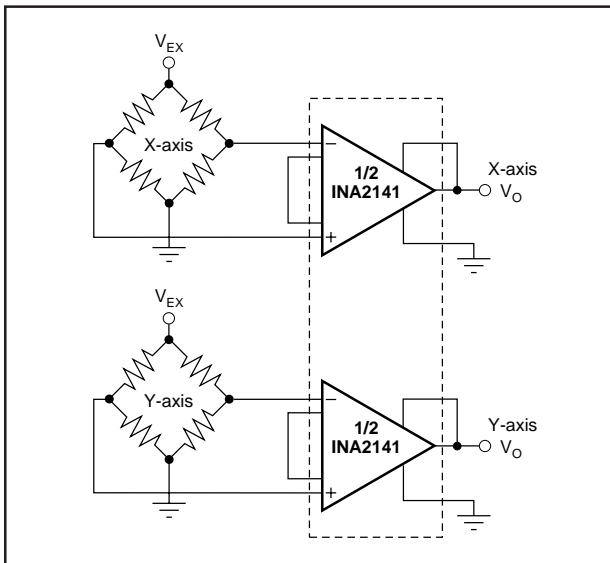


FIGURE 4. Two-Axis Bridge Amplifier.

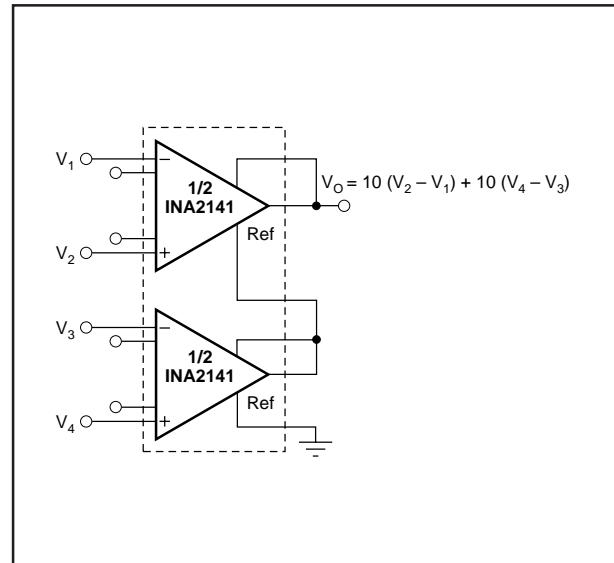


FIGURE 5. Sum of Differences Amplifier.

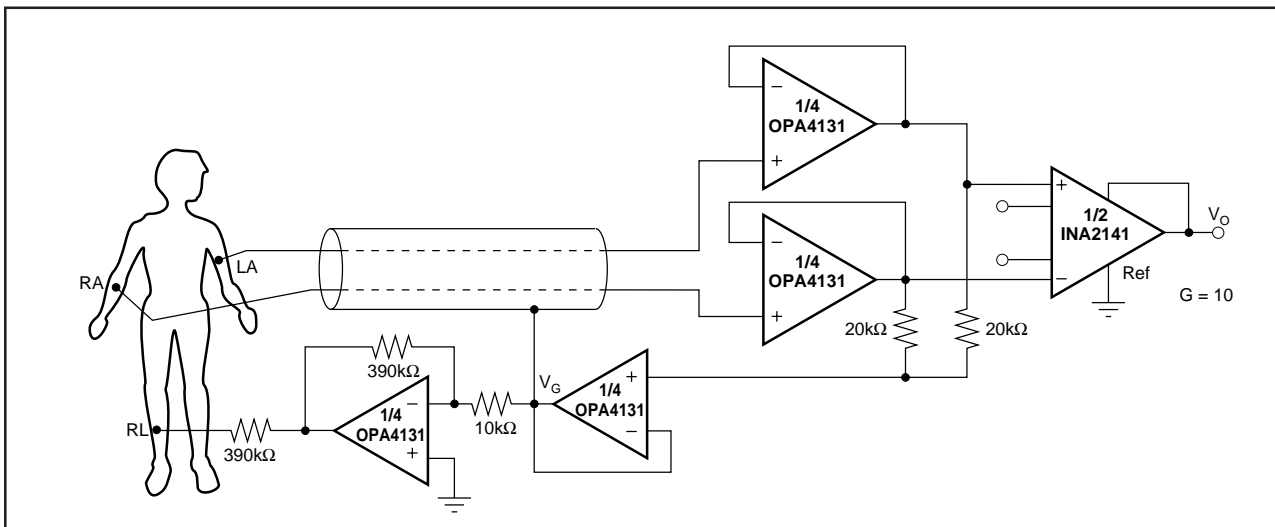


FIGURE 6. ECG Amplifier With Right-Leg Drive.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">INA2141U</a>	Active	Production	SOIC (DW)   16	40   TUBE	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	INA2141U A
INA2141U.A	Active	Production	SOIC (DW)   16	40   TUBE	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	INA2141U A
<a href="#">INA2141UA</a>	Active	Production	SOIC (DW)   16	40   TUBE	Yes	Call TI	Level-3-260C-168 HR	-	INA2141U A
INA2141UA.A	Active	Production	SOIC (DW)   16	40   TUBE	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	INA2141U A
<a href="#">INA2141UA/1K</a>	Active	Production	SOIC (DW)   16	1000   LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-	INA2141U A
INA2141UA/1K.A	Active	Production	SOIC (DW)   16	1000   LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	INA2141U A

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA2141UA/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA2141UA/1K	SOIC	DW	16	1000	353.0	353.0	32.0

## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
INA2141U	DW	SOIC	16	40	507	12.83	5080	6.6
INA2141U	DW	SOIC	16	40	507	12.83	5080	6.6
INA2141U.A	DW	SOIC	16	40	507	12.83	5080	6.6
INA2141U.A	DW	SOIC	16	40	507	12.83	5080	6.6
INA2141UA	DW	SOIC	16	40	507	12.83	5080	6.6
INA2141UA	DW	SOIC	16	40	507	12.83	5080	6.6
INA2141UA.A	DW	SOIC	16	40	507	12.83	5080	6.6
INA2141UA.A	DW	SOIC	16	40	507	12.83	5080	6.6

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2025, Texas Instruments Incorporated