



High Speed 256K×16 CMOS DRAM (Fast page mode)

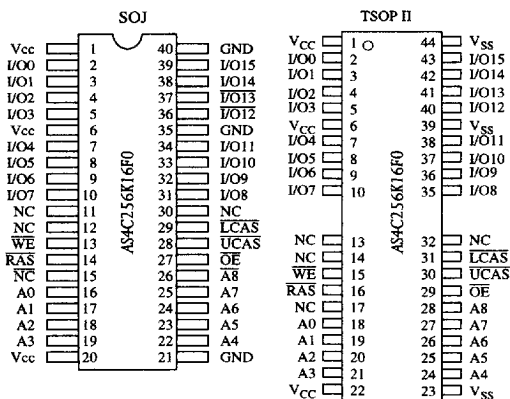
Preliminary information

Features

- Organization: 262,144 words by 16 bits
- High speed
  - 50/60 ns  $\overline{\text{RAS}}$  access time
  - 25/30 ns column address access time
  - 10/12 ns  $\overline{\text{CAS}}$  access time
- Low power consumption
  - Active: 770 mW max (4C256K16F0-50)
  - Standby: 5.5 mW max, CMOS I/O
- Fast page mode
  - 512 refresh cycles, 8 ms refresh interval
  - $\overline{\text{RAS}}$ -only or  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh

- Read-modify-write
- TTL-compatible, three-state I/O
- JEDEC standard packages
  - 400 mil, 40-pin SOJ
  - 400 mil, 40/44-pin TSOP II
- Single 5V power supply / built-in  $V_{bb}$  generator
- Latch-up current > 200 mA

Pin arrangement



Pin designation

| Pin(s)        | Description                       |
|---------------|-----------------------------------|
| A0 to A8      | Address inputs                    |
| RAS           | Row address strobe                |
| I/O0 to I/O15 | Input/output                      |
| OE            | Output enable                     |
| UCAS          | Column address strobe, upper byte |
| LCAS          | Column address strobe, lower byte |
| WE            | Read/write control                |
| $V_{CC}$      | Power (+5V $\pm$ 10%)             |
| GND           | Ground                            |

DRAM

Selection guide

|                                                              | Symbol           | 4C256K16F0-50 | 4C256K16F0-60 | Unit |
|--------------------------------------------------------------|------------------|---------------|---------------|------|
| Maximum $\overline{\text{RAS}}$ access time                  | $t_{\text{RAC}}$ | 50            | 60            | ns   |
| Maximum column address access time                           | $t_{\text{CAA}}$ | 25            | 30            | ns   |
| Maximum $\overline{\text{CAS}}$ access time                  | $t_{\text{CAC}}$ | 10            | 12            | ns   |
| Maximum output enable ( $\overline{\text{OE}}$ ) access time | $t_{\text{OEA}}$ | 8             | 10            | ns   |
| Minimum read or write cycle time                             | $t_{\text{RC}}$  | 85            | 100           | ns   |
| Minimum fast page mode cycle time                            | $t_{\text{PC}}$  | 25            | 30            | ns   |
| Maximum operating current                                    | $I_{\text{CC1}}$ | 140           | 130           | mA   |
| Maximum CMOS standby current                                 | $I_{\text{CCS}}$ | 1.0           | 1.0           | mA   |

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ALLIANCE SEMICONDUCTOR



Functional description

The AS4C256K16F0 is a high performance 4 megabit CMOS Dynamic Random Access Memory (DRAM) organized as 262,144 words by 16 bits. The AS4C256K16F0 is fabricated with advanced CMOS technology and designed with innovative design techniques resulting in high speed, extremely low power and wide operating margins at component and system levels.

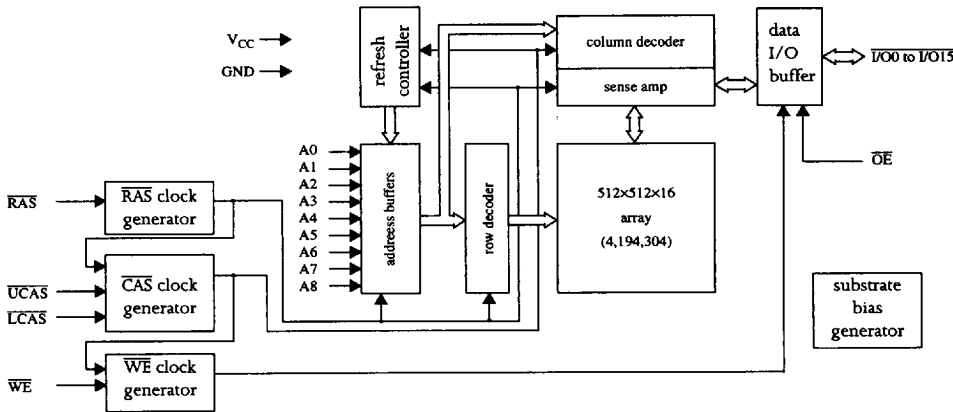
The AS4C256K16F0 features a high speed page mode operation in which high speed read, write and read-write are performed on any of the 512 × 16 bits defined by the column address. The asynchronous column address uses an extremely short row address capture time to ease the system level timing constraints associated with multiplexed addressing. Output is tri-stated by a column address strobe ( $\overline{\text{CAS}}$ ) which acts as an output enable independent of  $\overline{\text{RAS}}$ . Very fast  $\overline{\text{CAS}}$  to output access time eases system design.

Refresh on the 512 address combinations of A0 to A8 during an 8 ms period is accomplished by performing any of the following:

- $\overline{\text{RAS}}$ -only refresh cycles
- Hidden refresh cycles
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycles
- Normal read or write cycles

The AS4C256K16F0 is available in standard 40-pin plastic SOJ and 44-pin TSOP II packages compatible with widely available automated testing and insertion equipment. System level features include single power supply of 5V ± 10% tolerance and direct interface with TTL logic families.

Logic block diagram



Recommended operating conditions

| Parameter      | Symbol          | Min  | Typ | Max                 | Unit |
|----------------|-----------------|------|-----|---------------------|------|
| Supply voltage | V <sub>CC</sub> | 4.5  | 5.0 | 5.5                 | V    |
|                | GND             | 0.0  | 0.0 | 0.0                 | V    |
| Input voltage  | V <sub>IH</sub> | 2.4  | —   | V <sub>CC</sub> + 1 | V    |
|                | V <sub>IL</sub> | -1.0 | —   | 0.8                 | V    |



## Absolute maximum ratings

| Parameter                     | Symbol       | Min  | Max      | Unit     |
|-------------------------------|--------------|------|----------|----------|
| Input voltage                 | $V_{in}$     | -1.0 | +7.0     | V        |
| Output voltage                | $V_{out}$    | -1.0 | +7.0     | V        |
| Power supply voltage          | $V_{CC}$     | -1.0 | +7.0     | V        |
| Operating temperature         | $T_{OPR}$    | 0    | +70      | °C       |
| Storage temperature (plastic) | $T_{STG}$    | -55  | +150     | °C       |
| Soldering temperature × time  | $T_{SOLDER}$ | —    | 260 × 10 | °C × sec |
| Power dissipation             | $P_D$        | —    | 1        | W        |
| Short circuit output current  | $I_{out}$    | —    | 50       | mA       |
| Latch-up current              |              | 200  | —        | mA       |

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## DC electrical characteristics

( $V_{CC} = 5 \pm 10\%$ , GND = 0V,  $T_a = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ )

| Parameter                                                               | Symbol    | Test Conditions                                                                                     | -50   |       | -60   |       | Unit | Notes |
|-------------------------------------------------------------------------|-----------|-----------------------------------------------------------------------------------------------------|-------|-------|-------|-------|------|-------|
|                                                                         |           |                                                                                                     | Min   | Max   | Min   | Max   |      |       |
| Input leakage current                                                   | $I_{IL}$  | $0V \leq V_{in} \leq +5.5V$<br>pins not under test = 0V                                             | -10.0 | +10.0 | -10.0 | +10.0 | μA   |       |
| Output leakage current                                                  | $I_{OL}$  | $D_{OUT}$ disabled,<br>$0V \leq V_{out} \leq +5.5V$                                                 | -10.0 | +10.0 | -10.0 | +10.0 | μA   |       |
| Operating power supply current                                          | $I_{CC1}$ | $\overline{RAS}$ , $\overline{UCAS}$ , $\overline{LCAS}$ , address cycling; $t_{RC} = \min$         | —     | 140   | —     | 130   | mA   | 1,2   |
| TTL standby power supply current                                        | $I_{CC2}$ | $\overline{RAS} = \overline{UCAS} = \overline{LCAS} = V_{IH}$                                       | —     | 2.0   | —     | 2.0   | mA   |       |
| Average power supply current, $\overline{RAS}$ refresh mode             | $I_{CC3}$ | $\overline{RAS}$ cycling,<br>$\overline{UCAS} = \overline{LCAS} = V_{IH}$ ,<br>$t_{RC} = \min$      | —     | 140   | —     | 130   | mA   | 1     |
| Fast page mode average power supply current                             | $I_{CC4}$ | $\overline{RAS} = \overline{UCAS} = \overline{LCAS} = V_{IL}$ ,<br>address cycling; $t_{SC} = \min$ | —     | 70    | —     | 65    | mA   | 1,2   |
| CMOS standby power supply current                                       | $I_{CC5}$ | $\overline{RAS} = \overline{UCAS} = \overline{LCAS} = V_{CC} - 0.2V$                                | —     | 1.0   | —     | 1.0   | mA   |       |
| $\overline{CAS}$ -before- $\overline{RAS}$ refresh power supply current | $I_{CC6}$ | $\overline{RAS}$ , $\overline{UCAS}$ , $\overline{LCAS}$ , cycling;<br>$t_{RC} = \min$              | —     | 140   | —     | 130   | mA   | 1     |
| Output voltage                                                          | $V_{OH}$  | $I_{OUT} = -5.0 \text{ mA}$                                                                         | 2.4   | —     | 2.4   | —     | V    |       |
|                                                                         | $V_{OL}$  | $I_{OUT} = 4.2 \text{ mA}$                                                                          | —     | 0.4   | —     | 0.4   | V    |       |



## AC parameters common to all waveforms

(V<sub>CC</sub> = 5V±10%, GND = 0V, T<sub>a</sub> = 0°C to +70°C)

| Std Symbol          | Parameter                                                                 | -50 |     | -60 |     | Unit | Notes |
|---------------------|---------------------------------------------------------------------------|-----|-----|-----|-----|------|-------|
|                     |                                                                           | Min | Max | Min | Max |      |       |
| t <sub>RC</sub>     | Random read or write cycle time                                           | 85  | —   | 100 | —   | ns   |       |
| t <sub>RP</sub>     | $\overline{\text{RAS}}$ precharge time                                    | 25  | —   | 30  | —   | ns   |       |
| t <sub>RAS</sub>    | $\overline{\text{RAS}}$ pulse width                                       | 50  | 75K | 60  | 75K | ns   |       |
| t <sub>CAS</sub>    | $\overline{\text{CAS}}$ pulse width                                       | 10  | —   | 12  | —   | ns   |       |
| t <sub>RCD</sub>    | $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time             | 15  | 35  | 15  | 45  | ns   | 6     |
| t <sub>RAD</sub>    | $\overline{\text{RAS}}$ to column address delay time                      | 15  | 25  | 15  | 30  | ns   | 7     |
| t <sub>RSH(R)</sub> | $\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ hold time (read cycle) | 10  | —   | 12  | —   | ns   |       |
| t <sub>CSH</sub>    | $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ hold time              | 50  | —   | 60  | —   | ns   |       |
| t <sub>CRP</sub>    | $\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time         | 5   | —   | 5   | —   | ns   |       |
| t <sub>ASR</sub>    | Row address setup time                                                    | 0   | —   | 0   | —   | ns   |       |
| t <sub>RAH</sub>    | Row address hold time                                                     | 9   | —   | 9   | —   | ns   |       |
| t <sub>T</sub>      | Transition time (rise and fall)                                           | 3   | 50  | 3   | 50  | ns   | 4,5   |
| t <sub>REF</sub>    | Refresh period                                                            | —   | 8   | —   | 8   | ms   | 3     |
| t <sub>CLZ</sub>    | $\overline{\text{CAS}}$ to output in low Z                                | 3   | —   | 3   | —   | ns   | 8     |

## Read cycle

(V<sub>CC</sub> = 5V±10%, GND = 0V, T<sub>a</sub> = 0°C to +70°C)

| Std Symbol         | Parameter                                           | -50 |     | -60 |     | Unit | Notes |
|--------------------|-----------------------------------------------------|-----|-----|-----|-----|------|-------|
|                    |                                                     | Min | Max | Min | Max |      |       |
| t <sub>RAC</sub>   | Access time from $\overline{\text{RAS}}$            | —   | 50  | —   | 60  | ns   | 6     |
| t <sub>CAC</sub>   | Access time from $\overline{\text{CAS}}$            | —   | 10  | —   | 12  | ns   | 6,13  |
| t <sub>AA</sub>    | Access time from address                            | —   | 25  | —   | 30  | ns   | 7,13  |
| t <sub>AR(R)</sub> | Column add hold from $\overline{\text{RAS}}$        | 30  | —   | 40  | —   | ns   |       |
| t <sub>RCS</sub>   | Read command setup time                             | 0   | —   | 0   | —   | ns   |       |
| t <sub>RCH</sub>   | Read command hold time to $\overline{\text{CAS}}$   | 0   | —   | 0   | —   | ns   | 9     |
| t <sub>RRH</sub>   | Read command hold time to $\overline{\text{RAS}}$   | 0   | —   | 0   | —   | ns   | 9     |
| t <sub>RAL</sub>   | Column address to $\overline{\text{RAS}}$ lead time | 25  | —   | 30  | —   | ns   |       |
| t <sub>CPN</sub>   | $\overline{\text{CAS}}$ precharge time              | 5   | —   | 5   | —   | ns   |       |
|                    | Parameter deleted                                   |     |     |     |     |      |       |
| t <sub>OFF</sub>   | Output buffer turn-off time                         | 0   | 8   | 0   | 10  | ns   | 8,10  |



## Write cycle

(V<sub>CC</sub> = 5V±10%, GND = 0V, T<sub>a</sub> = 0°C to +70°C)

| Std Symbol       | Parameter                                           | -50 |     | -60 |     | Unit | Notes |
|------------------|-----------------------------------------------------|-----|-----|-----|-----|------|-------|
|                  |                                                     | Min | Max | Min | Max |      |       |
| t <sub>ASC</sub> | Column address setup time                           | 0   | —   | 0   | —   | ns   |       |
| t <sub>CAH</sub> | Column address hold time                            | 9   | —   | 10  | —   | ns   |       |
| t <sub>AWR</sub> | Column address hold time to $\overline{\text{RAS}}$ | 30  | —   | 40  | —   | ns   |       |
| t <sub>WCS</sub> | Write command setup time                            | 0   | —   | 0   | —   | ns   | 11    |
| t <sub>WCH</sub> | Write command hold time                             | 0   | —   | 0   | —   | ns   | 11    |
| t <sub>WCR</sub> | Write command hold time to $\overline{\text{RAS}}$  | 30  | —   | 40  | —   | ns   |       |
| t <sub>WP</sub>  | Write command pulse width                           | 9   | —   | 10  | —   | ns   |       |
| t <sub>RWL</sub> | Write command to $\overline{\text{RAS}}$ lead time  | 12  | —   | 12  | —   | ns   |       |
| t <sub>CWL</sub> | Write command to $\overline{\text{CAS}}$ lead time  | 12  | —   | 12  | —   | ns   |       |
| t <sub>DS</sub>  | Data-in setup time                                  | 0   | —   | 0   | —   | ns   | 12    |
| t <sub>DH</sub>  | Data-in hold time                                   | 9   | —   | 10  | —   | ns   | 12    |
| t <sub>DHR</sub> | Data-in hold time to $\overline{\text{RAS}}$        | 30  | —   | 45  | —   | ns   |       |

## Read-modify-write cycle

(V<sub>CC</sub> = 5V±10%, GND = 0V, T<sub>a</sub> = 0°C to +70°C)

| Std Symbol          | Parameter                                                            | -50 |     | -60 |     | Unit | Notes |
|---------------------|----------------------------------------------------------------------|-----|-----|-----|-----|------|-------|
|                     |                                                                      | Min | Max | Min | Max |      |       |
| t <sub>RWC</sub>    | Read-write cycle time                                                | 120 | —   | 130 | —   | ns   |       |
| t <sub>RWD</sub>    | $\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time         | 60  | —   | 70  | —   | ns   | 11    |
| t <sub>CWD</sub>    | $\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time         | 30  | —   | 35  | —   | ns   | 11    |
| t <sub>AWD</sub>    | Column address to $\overline{\text{WE}}$ delay time                  | 40  | —   | 50  | —   | ns   | 11    |
| t <sub>RSH(W)</sub> | $\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ hold time (write) | 12  | —   | 15  | —   | ns   |       |
| t <sub>CAS(W)</sub> | $\overline{\text{CAS}}$ pulse width (write)                          | 15  | —   | 15  | —   | ns   |       |

## Fast page mode cycle

(V<sub>CC</sub> = 5V±10%, GND = 0V, T<sub>a</sub> = 0°C to +70°C)

| Std Symbol        | Parameter                                           | -50 |     | -60 |     | Unit | Notes |
|-------------------|-----------------------------------------------------|-----|-----|-----|-----|------|-------|
|                   |                                                     | Min | Max | Min | Max |      |       |
| t <sub>PC</sub>   | Read or write cycle time (fast page)                | 25  | —   | 30  | —   | ns   | 14    |
| t <sub>CAP</sub>  | Access time from $\overline{\text{CAS}}$ precharge  | —   | 23  | —   | 28  | ns   | 13    |
| t <sub>CP</sub>   | $\overline{\text{CAS}}$ precharge time (fast page)  | 5   | —   | 5   | —   | ns   |       |
| t <sub>PCM</sub>  | Fast page mode RMW cycle                            | 60  | —   | 60  | —   | ns   |       |
| t <sub>CRW</sub>  | Page mode $\overline{\text{CAS}}$ pulse width (RMW) | 50  | —   | 50  | —   | ns   |       |
| t <sub>RASP</sub> | $\overline{\text{RAS}}$ pulse width                 | 50  | 75K | 60  | 75K | ns   |       |



## Refresh cycle

(V<sub>CC</sub> = 5V±10%, GND = 0V, T<sub>a</sub> = 0°C to +70°C)

| Std Symbol       | Parameter                                                                                                          | -50 |     | -60 |     | Unit | Notes |
|------------------|--------------------------------------------------------------------------------------------------------------------|-----|-----|-----|-----|------|-------|
|                  |                                                                                                                    | Min | Max | Min | Max |      |       |
| t <sub>CSR</sub> | $\overline{\text{CAS}}$ setup time ( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ )                    | 5   | —   | 5   | —   | ns   | 3     |
| t <sub>CHR</sub> | $\overline{\text{CAS}}$ hold time ( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ )                     | 10  | —   | 10  | —   | ns   | 3     |
| t <sub>RPC</sub> | $\overline{\text{RAS}}$ precharge to $\overline{\text{CAS}}$ hold time                                             | 0   | —   | 0   | —   | ns   |       |
| t <sub>CPT</sub> | $\overline{\text{CAS}}$ precharge time<br>( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ counter test) | 8   | —   | 8   | —   | ns   |       |

## Output enable

(V<sub>CC</sub> = 5V±10%, GND = 0V, T<sub>a</sub> = 0°C to +70°C)

| Std Symbol       | Parameter                                                              | -50 |     | -60 |     | Unit | Notes |
|------------------|------------------------------------------------------------------------|-----|-----|-----|-----|------|-------|
|                  |                                                                        | Min | Max | Min | Max |      |       |
| t <sub>ROH</sub> | $\overline{\text{RAS}}$ hold time referenced to $\overline{\text{OE}}$ | 5   | —   | 5   | —   | ns   |       |
| t <sub>OEa</sub> | $\overline{\text{OE}}$ access time                                     | —   | 10  | —   | 10  | ns   |       |
| t <sub>OED</sub> | $\overline{\text{OE}}$ to data delay                                   | 8   | —   | 10  | —   | ns   |       |
| t <sub>OEZ</sub> | Output buffer turnoff delay from $\overline{\text{OE}}$                | —   | 8   | —   | 10  | ns   | 8     |
| t <sub>OEh</sub> | $\overline{\text{OE}}$ command hold time                               | 8   | —   | 10  | —   | ns   |       |

## Self refresh cycle

(V<sub>CC</sub> = 5V±10%, GND = 0V, T<sub>a</sub> = 0°C to +70°C)

| Std Symbol        | Parameter                                                    | -50  |     | -60  |     | Unit | Notes |
|-------------------|--------------------------------------------------------------|------|-----|------|-----|------|-------|
|                   |                                                              | Min  | Max | Min  | Max |      |       |
| t <sub>ASSH</sub> | $\overline{\text{RAS}}$ pulse width (CBR self refresh)       | 100K | —   | 100K | —   | ns   |       |
| t <sub>RPS</sub>  | $\overline{\text{RAS}}$ precharge time<br>(CBR self refresh) | 85   | —   | 100  | —   | ns   |       |
| t <sub>OED</sub>  | $\overline{\text{CAS}}$ hold time (CBR self refresh)         | 30   | —   | 30   | —   | ns   |       |



## Notes

- 16  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$  and  $I_{CC6}$  depend on cycle rate.
- 17  $I_{CC1}$  and  $I_{CC4}$  depend on output loading. Specified values are obtained with the output open.
- 18 An initial pause of 200  $\mu$ s is required after power-up followed by any 8  $\overline{RAS}$  cycles before proper device operation is achieved. In the case of an internal refresh counter, a minimum of 8  $\overline{CAS}$ -before- $\overline{RAS}$  initialization cycles instead of 8  $\overline{RAS}$  cycles are required. 8 initialization cycles are required after extended periods of bias without clocks (greater than 8 ms).
- 19 AC Characteristics assume  $t_T = 5$  ns. All AC parameters are measured with a load equivalent to two TTL loads and 100 pF,  $V_{IL}(\min) \geq \text{GND}$  and  $V_{IH}(\max) \leq V_{CC}$ .
- 20  $V_{IH}(\min)$  and  $V_{IL}(\max)$  are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
- 21 Operation within the  $t_{RCD}(\max)$  limit insures that  $t_{RAC}(\max)$  can be met.  $t_{RCD}(\max)$  is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\max)$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
- 22 Operation within the  $t_{RAD}(\max)$  limit insures that  $t_{RAC}(\max)$  can be met.  $t_{RAD}(\max)$  is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\max)$  limit, then access time is controlled exclusively by  $t_{AA}$ .
- 23 Assumes three state test load (5 pF and a 380  $\Omega$  Thevenin equivalent).
- 24 Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
- 25  $t_{OFF}(\max)$  defines the time at which the output achieves the open circuit condition; it is not referenced to output voltage levels.
- 26  $t_{WCS}$ ,  $t_{WCH}$ ,  $t_{RWD}$ ,  $t_{CWD}$  and  $t_{AWD}$  are not restrictive operating parameters. They are included in the datasheet as electrical characteristics only. If  $t_{WS} \geq t_{WS}(\min)$  and  $t_{WH} \geq t_{WH}(\min)$ , the cycle is an early write cycle and data out pins will remain open circuit, high impedance, throughout the cycle. If  $t_{RWD} \geq t_{RWD}(\min)$ ,  $t_{CWD} \geq t_{CWD}(\min)$  and  $t_{AWD} \geq t_{AWD}(\min)$ , the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data out at access time is indeterminate.
- 27 These parameters are referenced to  $\overline{CAS}$  leading edge in early write cycles and to  $\overline{WE}$  leading edge in read-write cycles.
- 28 Access time is determined by the longest of  $t_{CAA}$  or  $t_{CAC}$  or  $t_{CAP}$ .
- 29  $t_{ASC} \geq t_{CP}$  to achieve  $t_{PC}(\min)$  and  $t_{CAP}(\max)$  values.
- 30 These parameters are sampled and not 100% tested.

## Key to switching waveforms



Undefined/don't care



Rising input

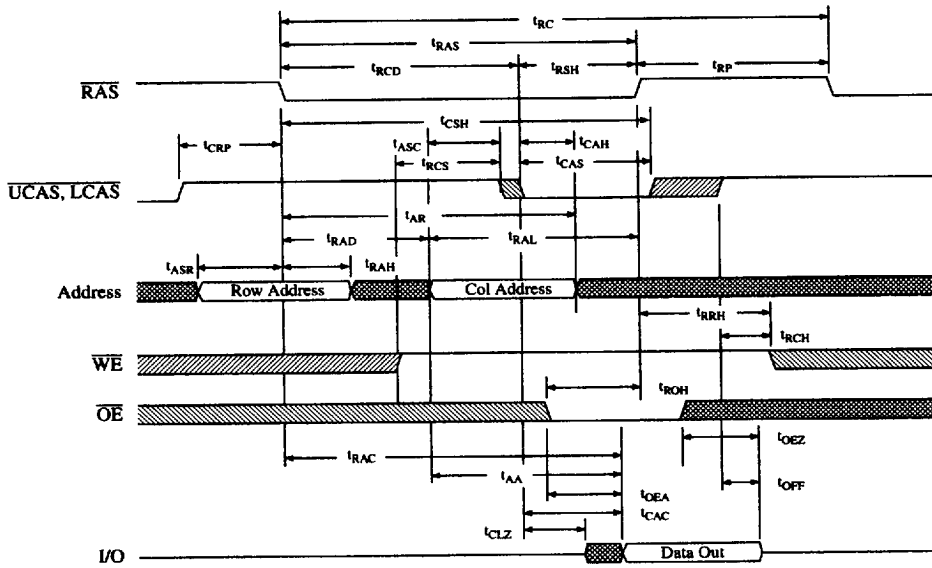


Falling input

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## Read cycle waveform

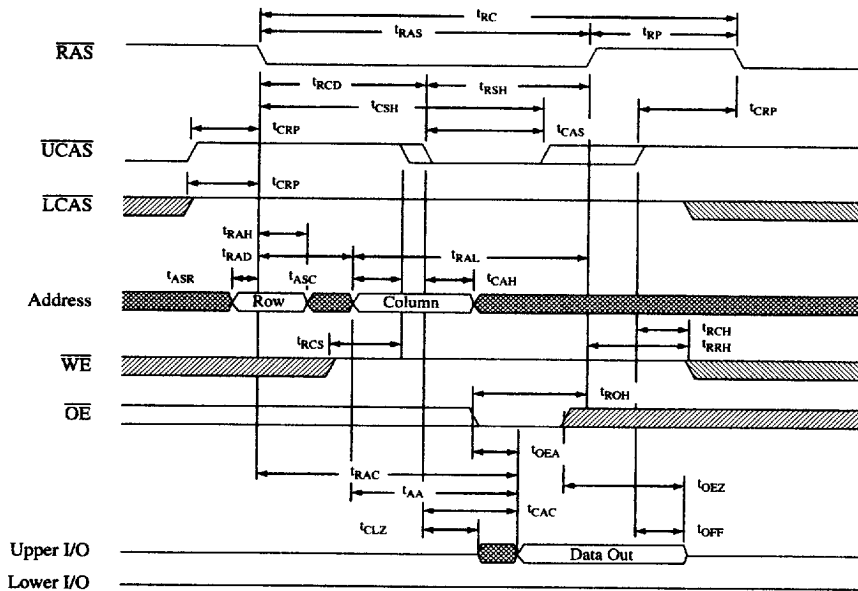


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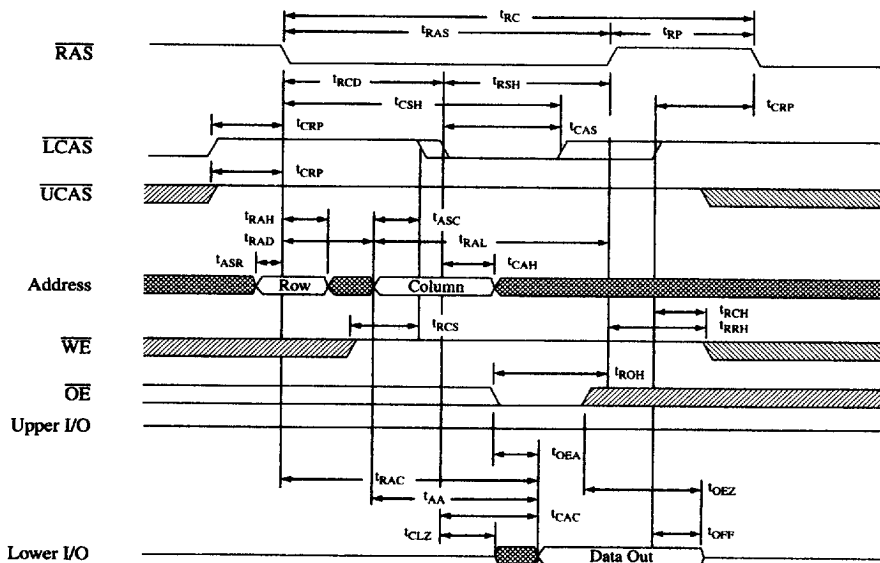




## Upper byte read waveform

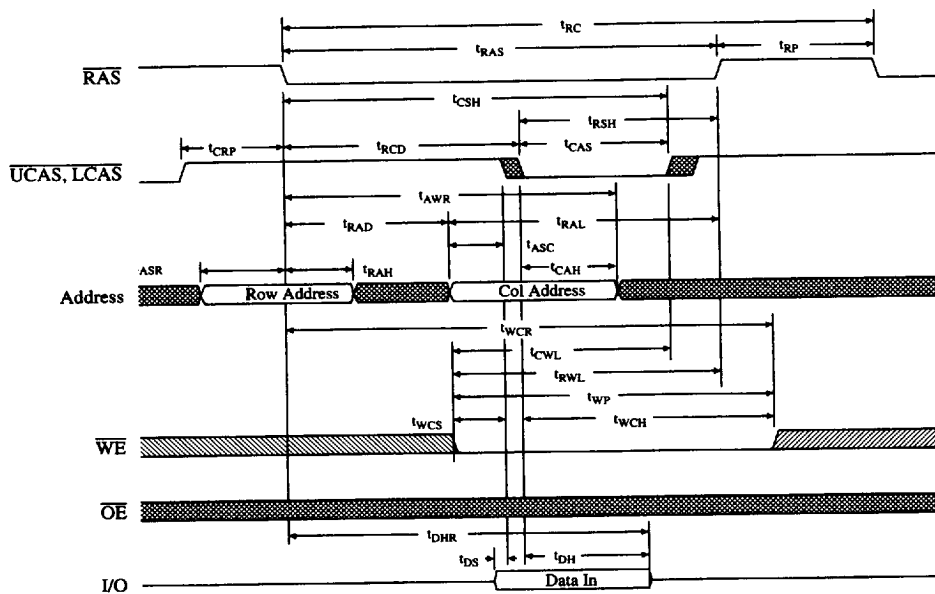


## Lower byte read waveform





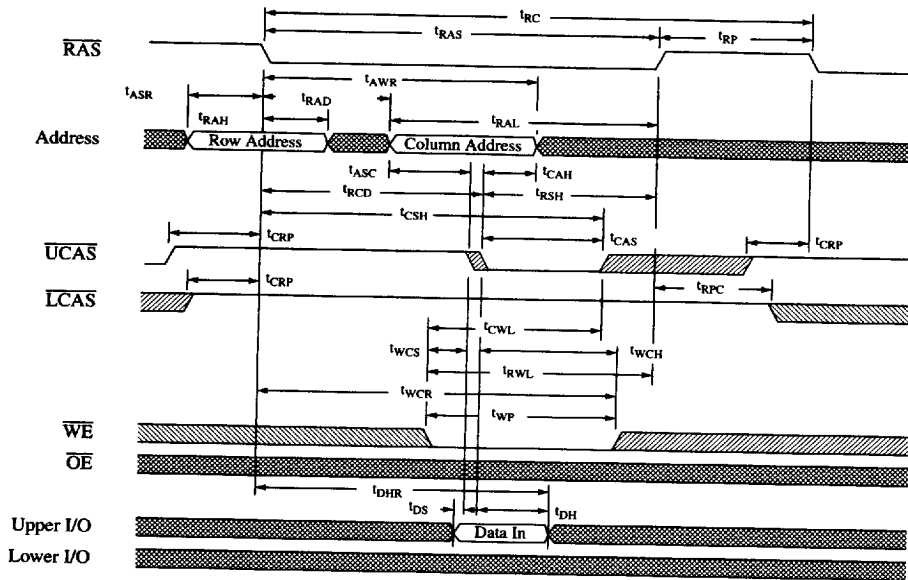
## Early write waveform



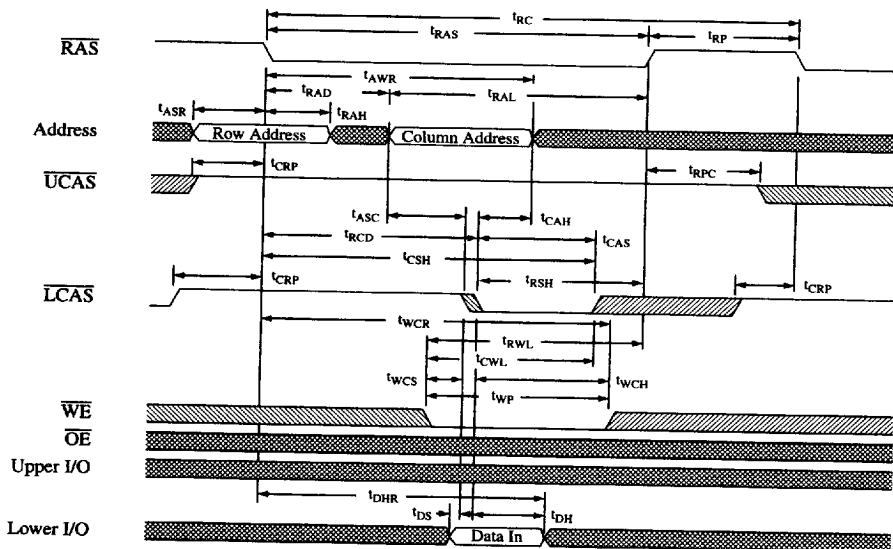
DRAM



Upper byte early write waveform



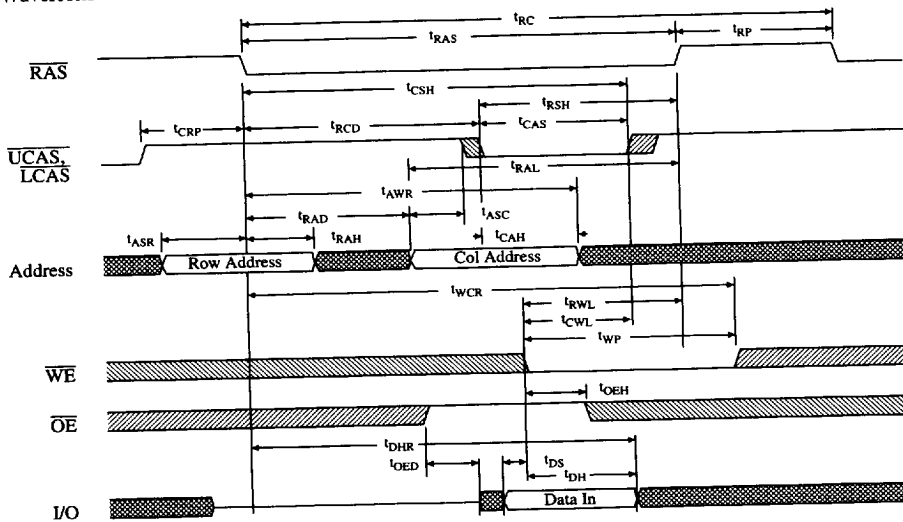
Lower byte early write waveform



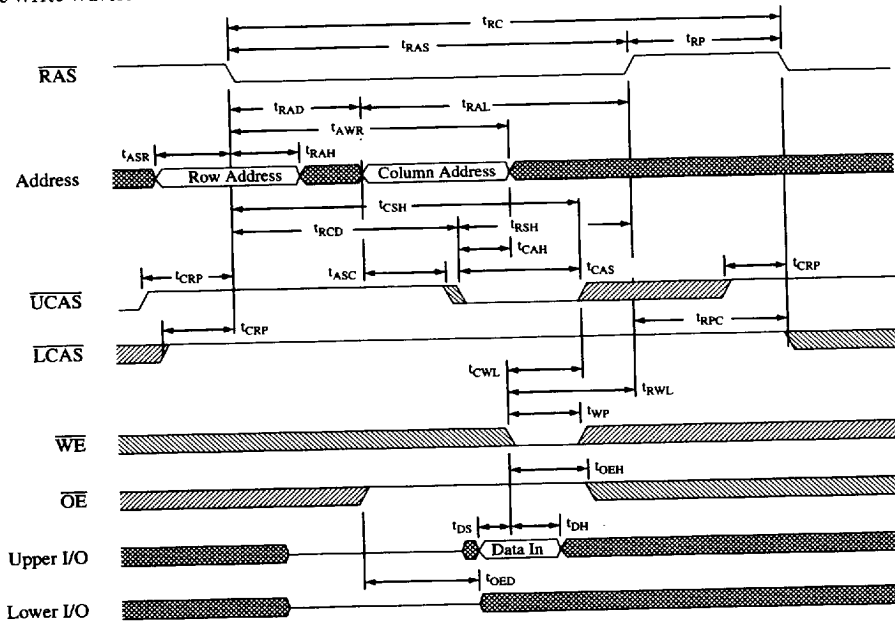
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## Write waveform

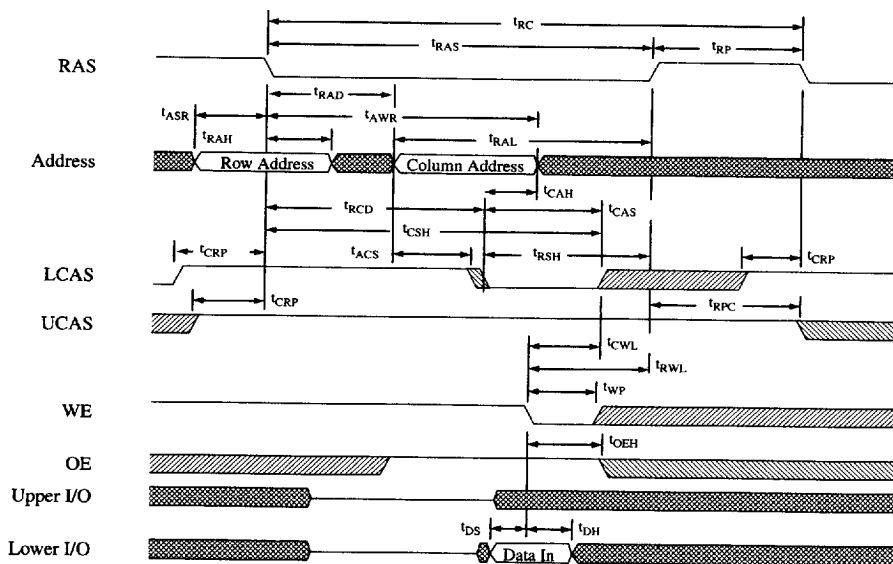


## Upper byte write waveform

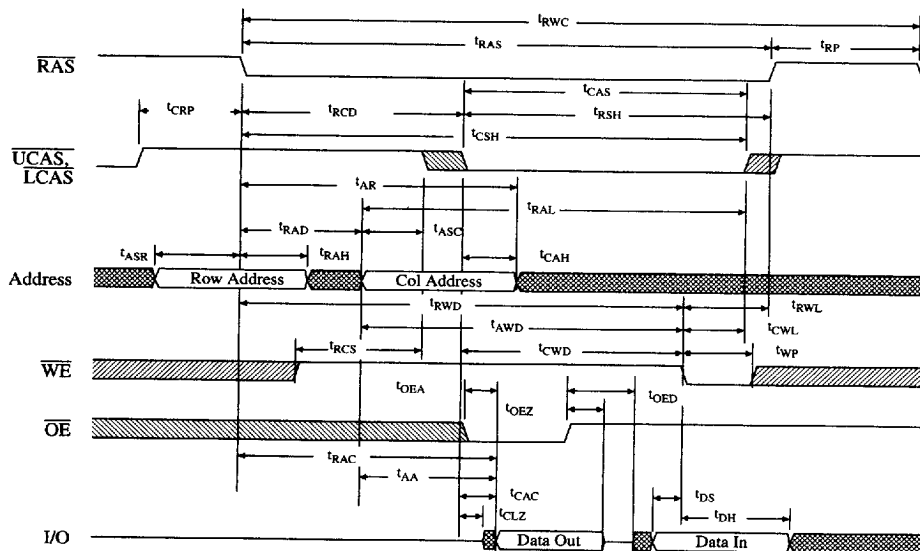




## Lower byte write waveform

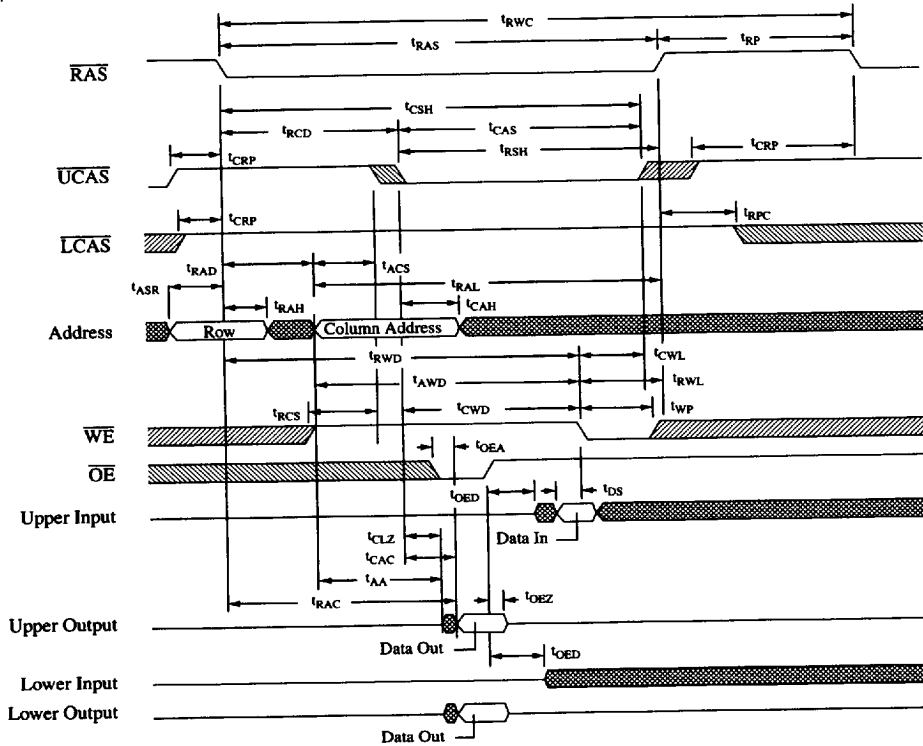


## Read-modify-write waveform





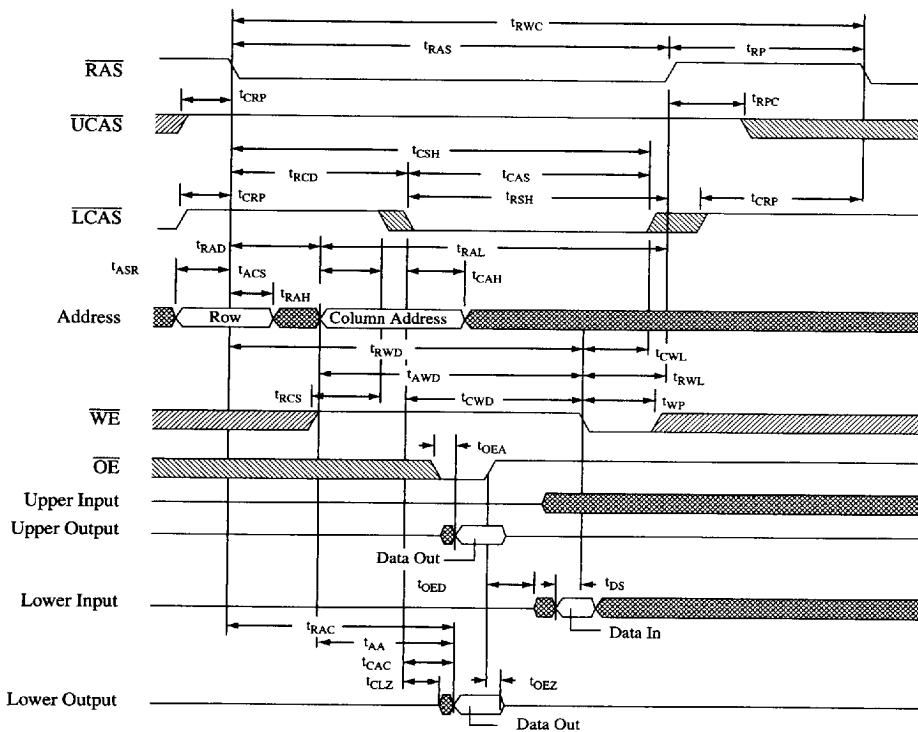
Upper byte read-modify-write waveform



DRAM



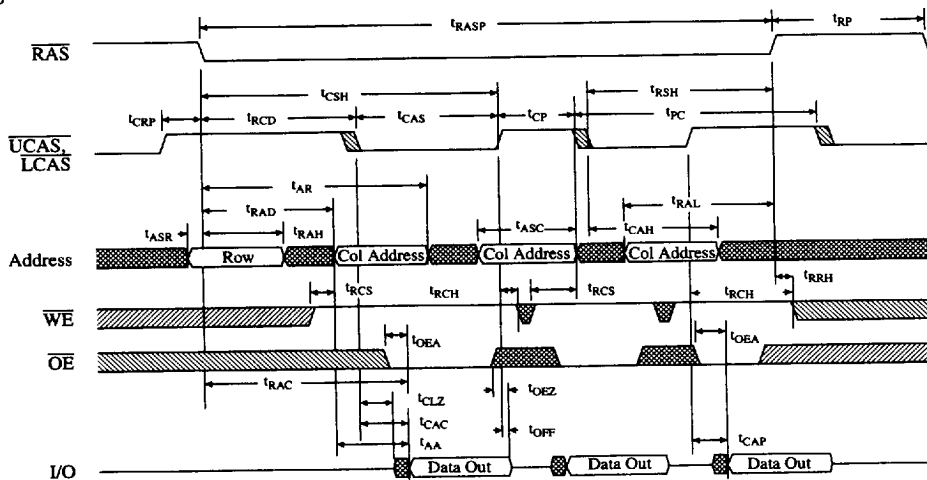
## Lower byte read-modify write waveform



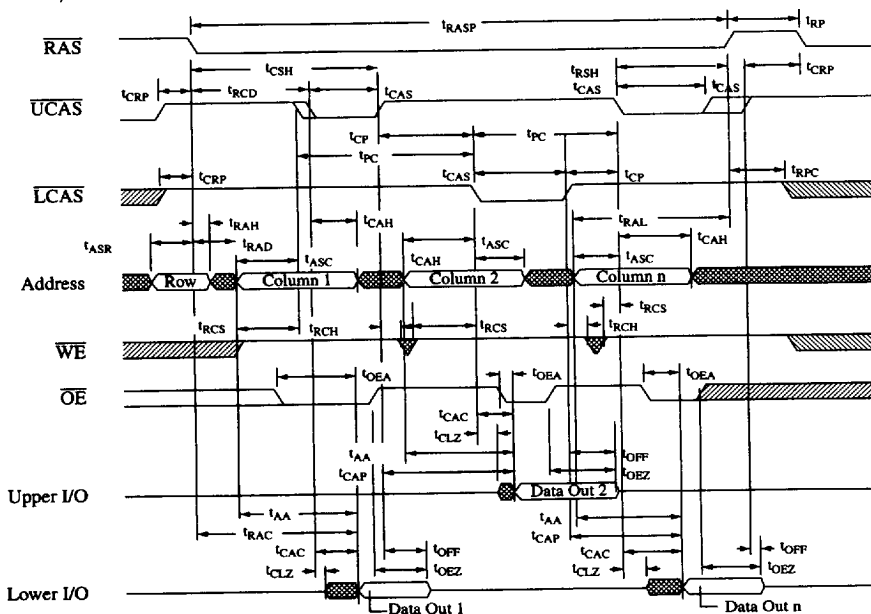
DRAM



## Fast page mode read waveform



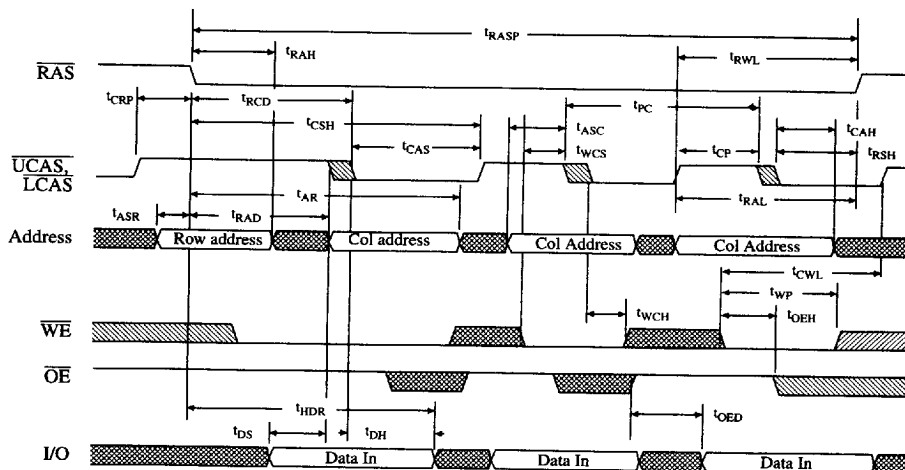
## Fast page mode byte read waveform



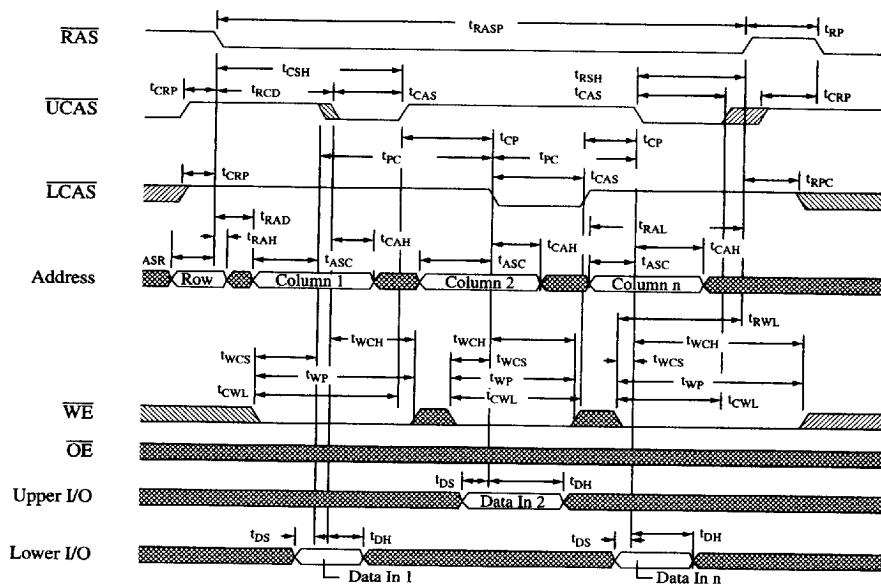




### Fast page mode early write waveform

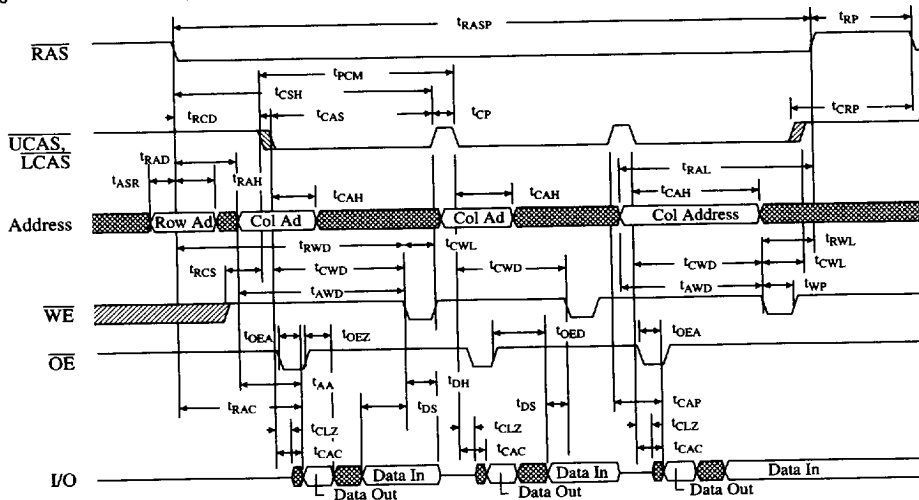


### Fast page mode byte early write waveform

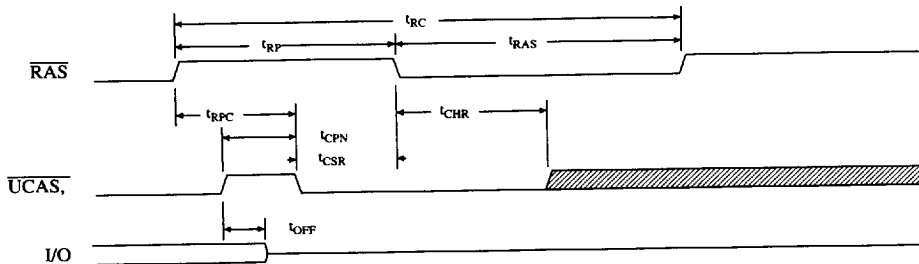




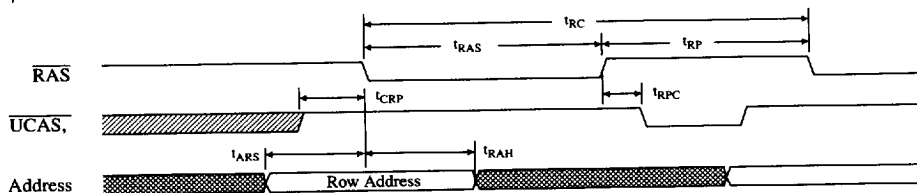
### Fast page mode read-modify-write waveform



$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh waveform

$$(\overline{\text{WE}} = \text{A9} = V_{\text{IH}} \text{ or } V_{\text{IL}})$$


RAS-only refresh waveform

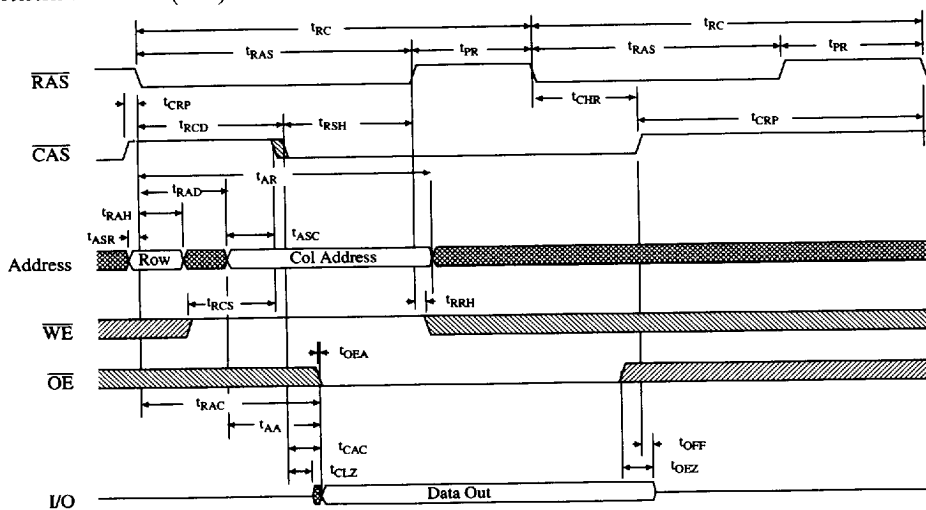
$$(\overline{WE} = \overline{OE} = V_{IH} \text{ or } V_{IL})$$


**DID 11-30002-A.**

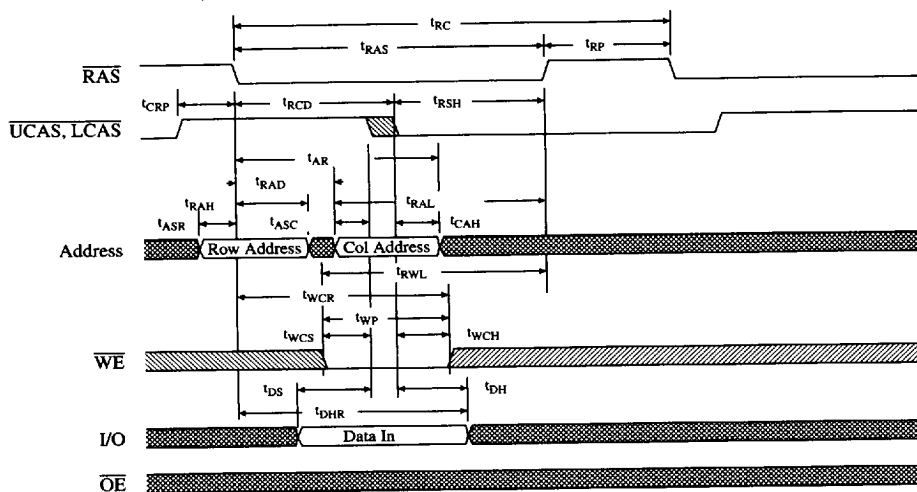


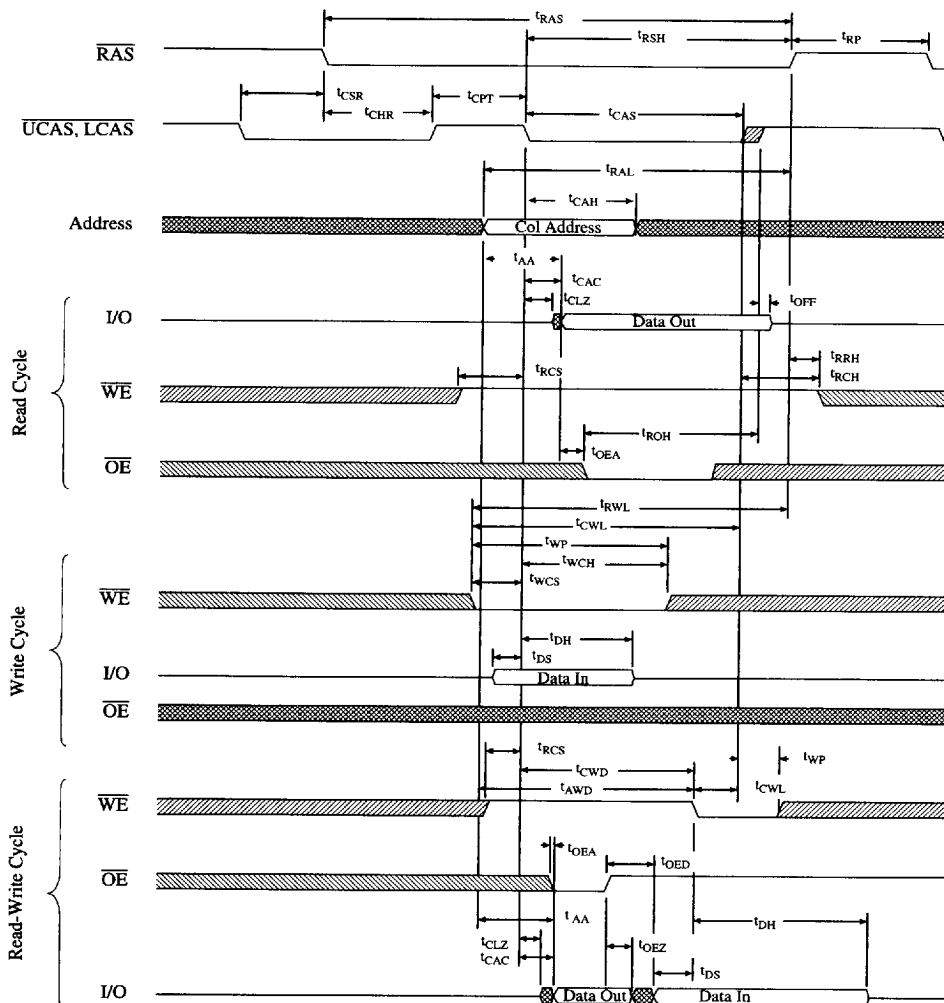


Hidden refresh waveform (read)



Hidden refresh waveform (write)

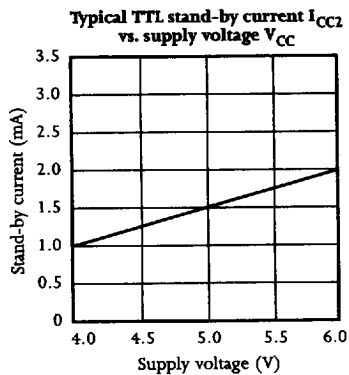
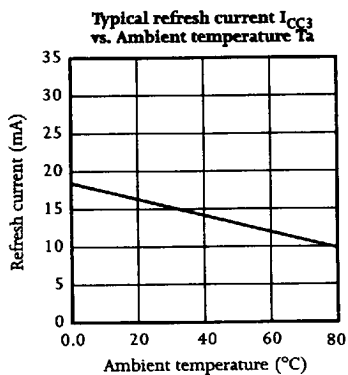
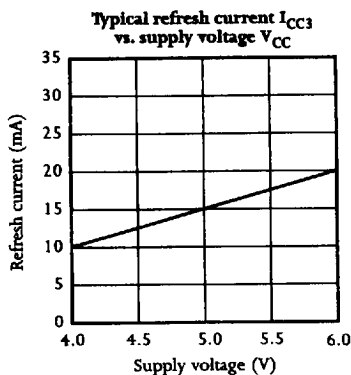
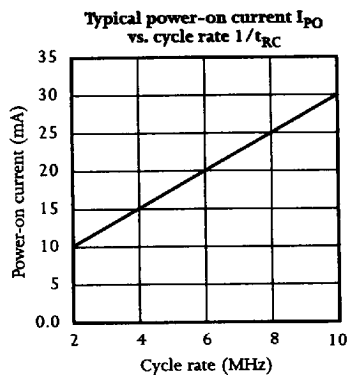
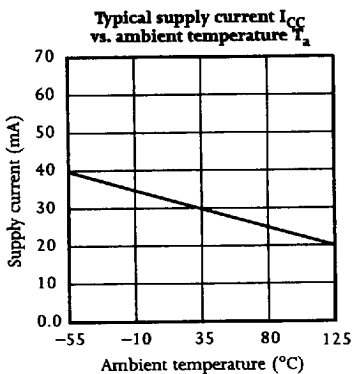
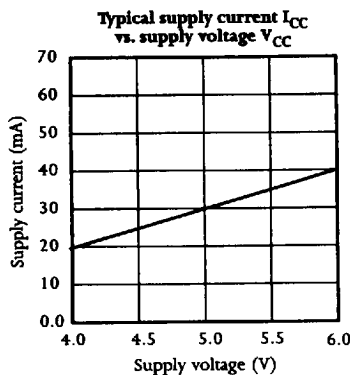
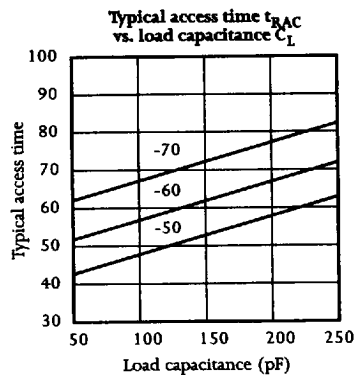
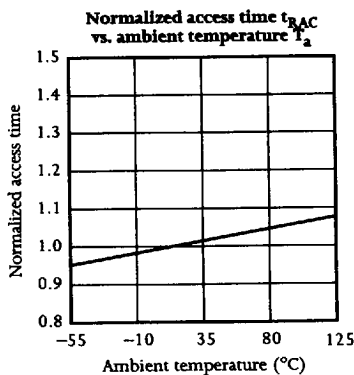
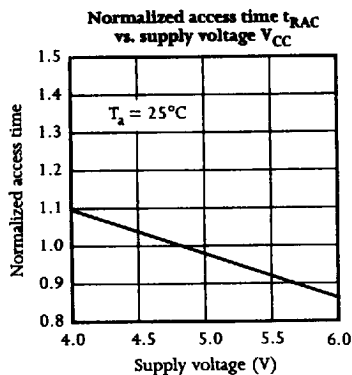


 $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh counter test waveform

DRAM

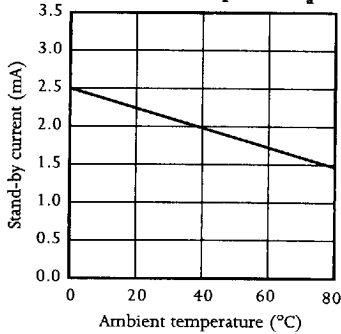


## Typical AC and DC characteristics

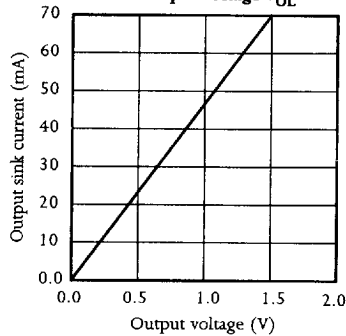




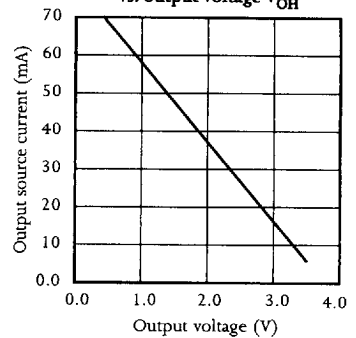
Typical TTL stand-by current  $I_{CC2}$   
vs. ambient temperature  $T_a$



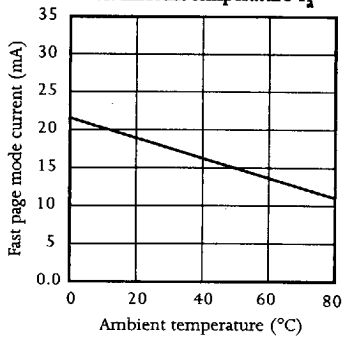
Typical output sink current  $I_{OL}$   
vs. output voltage  $V_{OL}$



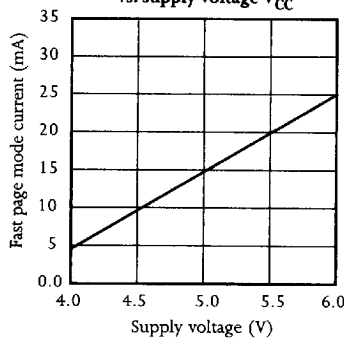
Typical output source current  $I_{OH}$   
vs. output voltage  $V_{OH}$



Typical fast page mode current  $I_{CC4}$   
vs. ambient temperature  $T_a$

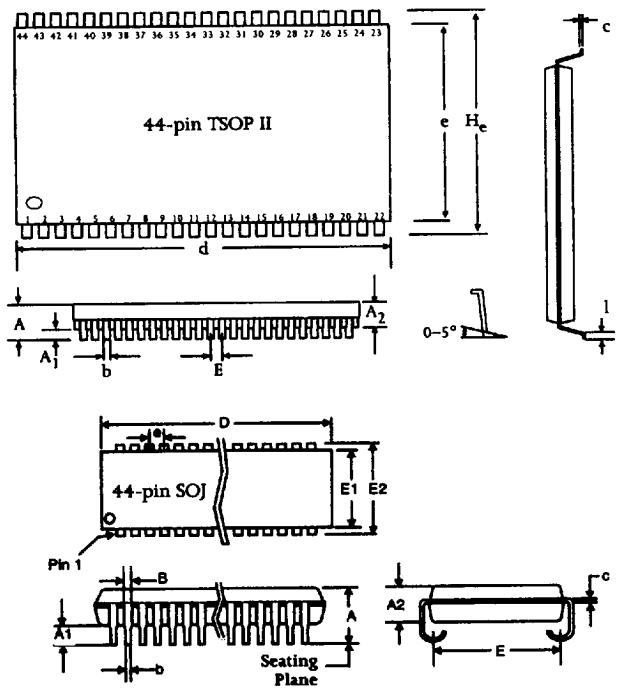


Typical fast page mode current  $I_{CC4}$   
vs. supply voltage  $V_{CC}$





Package dimensions



| 44-pin TSOP II |          |           |
|----------------|----------|-----------|
|                | Min (mm) | Max (mm)  |
| A              |          | 1.2       |
| A <sub>1</sub> | 0.05     |           |
| A <sub>2</sub> | 0.95     | 1.05      |
| b              | 0.25     | 0.45      |
| c              | 0.15     | (typical) |
| d              | 20.85    | 21.05     |
| e              | 10.06    | 10.26     |
| H <sub>c</sub> | 11.56    | 11.96     |
| E              | 0.80     | (typical) |
| l              | 0.40     | 0.60      |

| 44-pin SOJ<br>400 mil |       |           |
|-----------------------|-------|-----------|
|                       | Min   | Max       |
| A                     | 0.128 | 0.148     |
| A1                    | 0.025 | -         |
| A2                    | 1.105 | 1.115     |
| B                     | 0.026 | 0.032     |
| b                     | 0.015 | 0.020     |
| c                     | 0.007 | 0.013     |
| D                     | 1.120 | 1.130     |
| E                     | 0.370 | (typical) |
| E1                    | 0.395 | 0.405     |
| E2                    | 0.435 | 0.445     |
| e                     | 0.050 | (typical) |

DRAM

Capacitance

(f = 1 MHz, T<sub>a</sub> = Room Temperature, V<sub>CC</sub> = 5V±10%)

| Parameter         | Symbol           | Signals                 | Test conditions                         | Max | Unit |
|-------------------|------------------|-------------------------|-----------------------------------------|-----|------|
| Input capacitance | C <sub>IN1</sub> | A0 to A8                | V <sub>in</sub> = 0V                    | 5   | pF   |
|                   | C <sub>IN2</sub> | RAS, UCAS, LCAS, WE, OE | V <sub>in</sub> = 0V                    | 7   | pF   |
| I/O capacitance   | C <sub>I/O</sub> | I/O0 to I/O15           | V <sub>in</sub> = V <sub>out</sub> = 0V | 7   | pF   |

Ordering codes

|                              |                   |                   |
|------------------------------|-------------------|-------------------|
| Package \ RAS access time    | 50 ns             | 60 ns             |
| Plastic SOJ, 400 mil, 40-pin | AS4C256K16F0-50JC | AS4C256K16F0-60JC |
| TSOP II, 400 mil, 40/44-pin  | AS4C256K16F0-50TC |                   |

Part numbering system

|             |               |                 |                                 |                                            |
|-------------|---------------|-----------------|---------------------------------|--------------------------------------------|
| AS4C        | 4256          | -XX             | X                               | C                                          |
| DRAM prefix | Device number | RAS access time | Package: J = SOJ<br>T = TSOP II | Commercial temperature range, 0°C to 70 °C |

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