

ADC0801-ADC0804 **8-Bit Microprocessor** **Compatible A/D Converters**

FEATURES

- MCS-48 and MCS-80/85 bus compatible—no interfacing logic required
- Conversion time < 100 μ s
- Easy interface to all microprocessors
- Will operate "stand alone"
- Differential analog voltage inputs
- Bandgap voltage references
- TTL compatible inputs and outputs
- ON-chip clock generator
- 0V to 5V analog voltage input range (single +5V supply)
- No zero adjust required

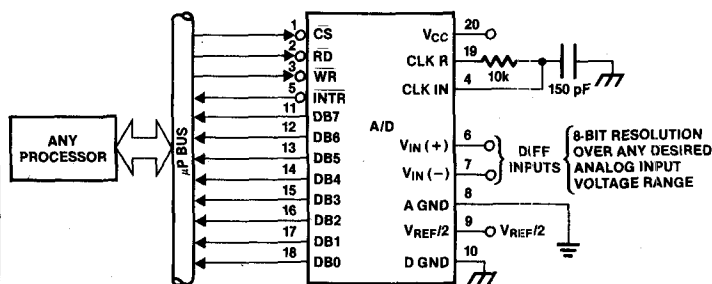
GENERAL DESCRIPTION

The ADC0801 family are CMOS 8-bit successive approximation A/D converters which use a modified potentiometric ladder, and are designed to operate with the 8080A control bus via three-state outputs. These converters appear to the processor as memory locations or I/O ports, hence no interfacing is required.

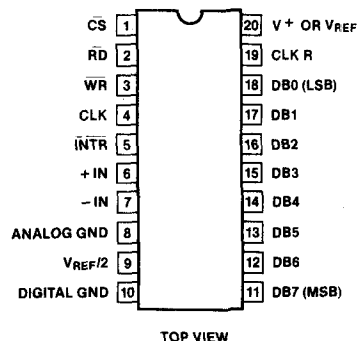
A differential analog voltage input allows increasing the common-mode-rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

The ADC0801 family is available in the industry standard 20 pin Cerdip packages.

TYPICAL APPLICATION



PIN CONFIGURATION



ORDERING INFORMATION

PART	ERROR	TEMPERATURE RANGE	PACKAGE	ORDER NUMBER
ADC0801	$\pm 1/4$ bit adjusted full scale	0°C to +70°C -40°C to +85°C -55°C to +125°C	20 pin Cerdip 20 pin Cerdip 20 pin Cerdip	ADC0801LCN ADC0801LCD ADC0801LD
ADC0802	$\pm 1/2$ bit no adjust	0°C to +70°C -40°C to +85°C -55°C to +125°C	20 pin Cerdip 20 pin Cerdip 20 pin Cerdip	ADC0802LCN ADC0802LCD ADC0802LD
ADC0803	$\pm 1/2$ bit adjusted full scale	0°C to +70°C -40°C to +85°C -55°C to +125°C	20 pin Cerdip 20 pin Cerdip 20 pin Cerdip	ADC0803LCN ADC0803LCD ADC0803LD
ADC0804	± 1 bit no adjust	0°C to +70°C -40°C to +85°C	20 pin Cerdip 20 pin Cerdip	ADC0804LCN ADC0804LCD

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 6.5V
 Voltage at Any Input $-0.3\text{V to } (V^+ + 0.3\text{V})$
 Storage Temperature Range $-65^\circ\text{C to } +150^\circ\text{C}$
 Package Dissipation at $T_A = 25^\circ\text{C}$ 875 mW
 Lead Temperature (Soldering, 10 seconds) 300°C

OPERATING RATINGS

Temperature Range
 ADC0801/02/03LD $-55^\circ\text{C to } +125^\circ\text{C}$
 ADC0801/02/03/04LCD $-40^\circ\text{C to } +85^\circ\text{C}$
 ADC0801/02/03/04LCN $0^\circ\text{C to } +70^\circ\text{C}$
 Supply Voltage Range 4.5V to 6.5V

ELECTRICAL CHARACTERISTICS

Converter Specifications: $V^+ = 5\text{V}$, $V_{\text{REF}}/2 = 2.500\text{V}$, $T_{\text{MIN}} \leq T_A \leq T_{\text{MAX}}$ and $f_c = 640\text{ kHz}$ unless otherwise stated.

PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
ADC0801: Total Adjusted Error			$\pm 1/4$	LSB	With Full Scale Adjust
ADC0802: Total Unadjusted Error			$\pm 1/2$	LSB	Completely Unadjusted
ADC0803: Total Adjusted Error			$\pm 1/2$	LSB	With Full Scale Adjust
ADC0804: Total Unadjusted Error			± 1	LSB	Completely Unadjusted
$V_{\text{REF}}/2$ Input Resistance	1.0	1.3		k Ω	Input Resistance at Pin 9
Analog Input Voltage Range	GND – 0.05		$V^+ + 0.05$	V	
DC Common-Mode Rejection		$\pm 1/16$	$\pm 1/8$	LSB	Over Analog Input Voltage Range
Power Supply Sensitivity		$\pm 1/16$	$\pm 1/8$	LSB	$V^+ = 5\text{V} \pm 10\%$ Over Allowed Input Voltage Range

Timing Specifications: $V^+ = 5\text{V}$ and $T_A = 25^\circ\text{C}$ unless otherwise stated.

PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
f_c Clock Frequency	100 100	640 640	1280 800	kHz kHz	$V^+ = 6\text{V}$, $V^+ = 5\text{V}$
t_{conv} Conversion Time	66		73	ns	
CR Conversion Rate In Free-Running Mode			8770	Conv/S	$\overline{\text{INTR}}$ tied to $\overline{\text{WR}}$ with $\overline{\text{CS}} = 0\text{V}$, $f_c = 640\text{ kHz}$ $\overline{\text{CS}} = 0\text{V}$
$t_{\text{W}}(\overline{\text{WR}})_\text{L}$ Width of $\overline{\text{WR}}$ Input (Start Pulse Width)	100			ns	$C_L = 100\text{ pF}$ (Use Bus Driver IC for Larger C_L)
t_{ACC} Access Time (Delay from Falling Edge of $\overline{\text{RD}}$ to Output Data Valid)		135	200	ns	$C_L = 10\text{ pF}$, $R_L = 10\text{ k}$
$t_{1\text{H}}, t_{0\text{H}}$ 3-State Control (Delay from Rising Edge of $\overline{\text{RD}}$ to Hi-Z State)		125	250	ns	
t_{WI} Delay from Falling Edge of $\overline{\text{WR}}$ to Reset of $\overline{\text{INTR}}$		300	450	ns	
C_{IN} Input Capacitance of Logic Control Inputs		5	7.5	pF	
C_{OUT} 3-State Output Capacitance (Data Buffers)		5	7.5	pF	