

16 V Rail-to-Rail Buffer Amplifiers

AD8568/AD8569/AD8570

FEATURES

Single-Supply Operation: 4.5 V to 16 V Input Capability Beyond the Rails

Rail-to-Rail Output Swing

Continuous Output Current: 35 mA
Peak Output Current: 250 mA
Offset Voltage: 10 mV Max
Slew Rate: 6 V/µs
Stable with 1 µF Loads

Supply Current

APPLICATIONS LCD Reference Drivers Portable Electronics

Communications Equipment

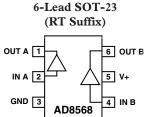
GENERAL DESCRIPTION

The AD8568, AD8569, and AD8570 are low-cost, single-supply buffer amplifiers with rail-to-rail input and output capability. They are optimized for LCD monitor applications and built on an advanced high voltage CBCMOS process. The AD8568 includes two buffers, the AD8569 includes four buffers, and the AD8570 includes eight buffers.

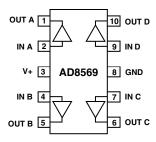
These LCD buffers have high slew rates, 35 mA continuous output drive, and high capacitive load drive capability. They have a wide supply range and offset voltages below 10 mV.

The AD8568, AD8569, and AD8570 are specified over the -40°C to +85°C temperature range. They are available on tape and reel, with the AD8568 packaged in a 6-lead SOT-23, the AD8569 in a 10-lead MSOP, and the AD8570 in a 32-lead LFCSP and 20-lead TSSOP.

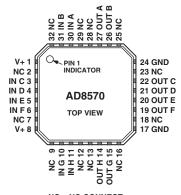
PIN CONFIGURATIONS



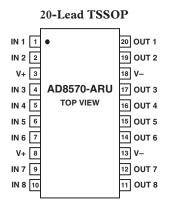
10-Lead MSOP (RM Suffix)



32-Lead LFCSP (CP Suffix)



NC = NO CONNECT



REV. C

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AD8568/AD8569/AD8570—SPECIFICATIONS

$\textbf{ELECTRICAL CHARACTERISTICS} \text{ (4.5 V} \leq \text{V}_{\text{S}} \leq \text{16 V, V}_{\text{CM}} = \text{V}_{\text{S}}/\text{2, T}_{\text{A}} = 25^{\circ}\text{C, unless otherwise noted.)}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS Offset Voltage Offset Voltage Drift Input Bias Current	$\begin{array}{c} V_{OS} \\ \Delta V_{OS}/\Delta T \\ I_{B} \end{array}$	$-40^{\circ}\text{C} \le \text{T}_{\text{A}} \le +85^{\circ}\text{C}$ $-40^{\circ}\text{C} \le \text{T}_{\text{A}} \le +85^{\circ}\text{C}$		2 5 80	10 600 800	mV μV/°C nA nA
Input Voltage Range Input Impedance Input Capacitance	$Z_{ m IN}$ $C_{ m IN}$	10 0 = 1 _R = 103 0	-0.5	400 1	$-V_{S} + 0.5$	V kΩ pF
OUTPUT CHARACTERISTICS Output Voltage High Output Voltage Low Continuous Output Current	$ m V_{OH}$ $ m V_{OL}$ $ m I_{OUT}$	$\begin{split} I_L &= 100 \; \mu\text{A} \\ V_S &= 16 \; \text{V}, \; I_L = 5 \; \text{mA} \\ -40^{\circ}\text{C} \leq T_\text{A} \leq +85^{\circ}\text{C} \\ V_S &= 4.5 \; \text{V}, \; I_L = 5 \; \text{mA} \\ -40^{\circ}\text{C} \leq T_\text{A} \leq +85^{\circ}\text{C} \\ I_L &= 100 \; \mu\text{A} \\ V_S &= 16 \; \text{V}, \; I_L = 5 \; \text{mA} \\ -40^{\circ}\text{C} \leq T_\text{A} \leq +85^{\circ}\text{C} \\ V_S &= 4.5 \; \text{V}, \; I_L = 5 \; \text{mA} \\ -40^{\circ}\text{C} \leq T_\text{A} \leq +85^{\circ}\text{C} \end{split}$	15.85 15.75 4.2 4.1	V _S - 0.005 15.95 4.38 5 42 95	150 250 300 400	V V V V V W MV mV mV mV
Peak Output Current TRANSFER CHARACTERISTICS Gain	I_{PK} A_{VCL}	$V_S = 16 \text{ V}$ $R_L = 2 \text{ k}\Omega$ $-40^{\circ}\text{C} \le T_A \le +85^{\circ}\text{C}$	0.995 0.995	0.9985 0.9980	1.005 1.005	MA V/V V/V
Gain Linearity	NL	$R_L = 2 k\Omega, V_O = 0.5 \text{ to } (V_S - 0.5 \text{ V})$	0.773	0.01	1.005	%
POWER SUPPLY Supply Voltage Power Supply Rejection Ratio Supply Current/Amplifier	V _S PSRR I _{SY}	$V_S = 4 \text{ V to } 17 \text{ V}$ $-40^{\circ}\text{C} \le T_A \le +85^{\circ}\text{C}$ $V_O = V_S/2$, No Load $-40^{\circ}\text{C} \le T_A \le +85^{\circ}\text{C}$	4.5	90 700	16 850 1	V dB μA mA
DYNAMIC PERFORMANCE Slew Rate Bandwidth Phase Margin Channel Separation	SR BW Øo	$R_{L} = 10 \text{ k}\Omega, C_{L} = 200 \text{ pF}$ -3 dB, $R_{L} = 10 \text{ k}\Omega, C_{L} = 10 \text{ pF}$ $R_{L} = 10 \text{ k}\Omega, C_{L} = 10 \text{ pF}$	4	6 6 65 75		V/µs MHz Degrees dB
NOISE PERFORMANCE Voltage Noise Density Current Noise Density	e_n e_n i_n	f = 1 kHz f = 10 kHz f = 10 kHz		26 25 0.8		$nV/\sqrt{Hz} \\ nV/\sqrt{Hz} \\ pA/\sqrt{Hz}$

Specifications subject to change without notice.

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ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V _S)
Input Voltage
Differential Input VoltageV _S
Storage Temperature Range65°C to +150°C
Operating Temperature Range40°C to +85°C
Junction Temperature Range65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)300°C

^{*}Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Type	θ_{JA}^{1}	$\theta_{ m JC}$	Ψ_{JB}^{2}	Unit
6-Lead SOT-23 (RT)	250	140		°C/W
10-Lead MSOP (RM)	200	44		°C/W
20-Lead TSSOP (RU)	72	45		°C/W
32-Lead LFCSP (CP)	35		13	°C/W

NOTES

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding Information
AD8568ART-R2	−40°C to +85°C	6-Lead SOT-23	RT-6	AWA
AD8568ART-REEL	−40°C to +85°C	6-Lead SOT-23	RT-6	AWA
AD8568ART-REEL7	−40°C to +85°C	6-Lead SOT-23	RT-6	AWA
AD8569ARM-R2	−40°C to +85°C	10-Lead MSOP	RM-10	AXA
AD8569ARM-REEL	−40°C to +85°C	10-Lead MSOP	RM-10	AXA
AD8569ARMZ-REEL*	−40°C to +85°C	10-Lead MSOP	RM-10	AXA
AD8570ACP-R2	−40°C to +85°C	32-Lead LFCSP	CP-32-2	
AD8570ACP-REEL	–40°C to +85°C	32-Lead LFCSP	CP-32-2	
AD8570ACP-REEL7	–40°C to +85°C	32-Lead LFCSP	CP-32-2	
AD8570ARU	-40°C to +85°C	20-Lead TSSOP	RU-20	
AD8570ARU-REEL	−40°C to +85°C	20-Lead TSSOP	RU-20	

^{*}Z = Pb-free part.

CAUTION -

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8568/AD8569/AD8570 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

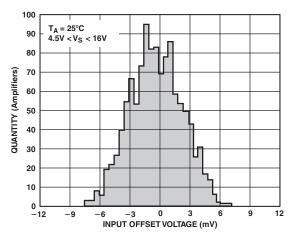


REV. C –3–

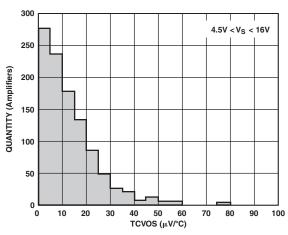
 $^{^{1}\}theta_{JA}$ is specified for worst-case conditions, i.e., θ_{JA} is specified for a device soldered onto a circuit board for surface-mount packages.

 $^{^2\}Psi_{JB}$ is applied for calculating the junction temperature by reference to the board temperature.

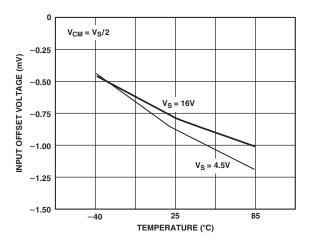
AD8568/AD8569/AD8570—Typical Performance Characteristics



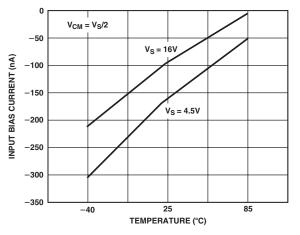
TPC 1. Input Offset Voltage Distribution



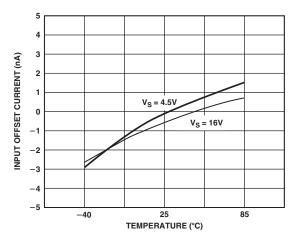
TPC 2. Input Offset Voltage Drift Distribution



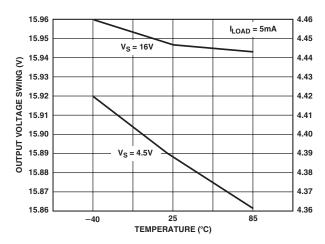
TPC 3. Input Offset Voltage vs. Temperature



TPC 4. Input Bias Current vs. Temperature

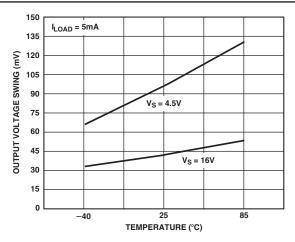


TPC 5. Input Offset Current vs. Temperature

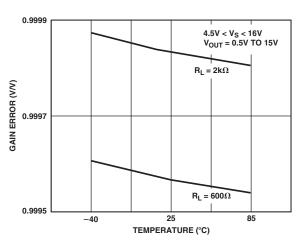


TPC 6. Output Voltage Swing vs. Temperature

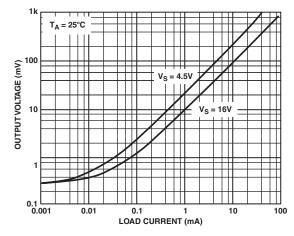
-4- REV. C



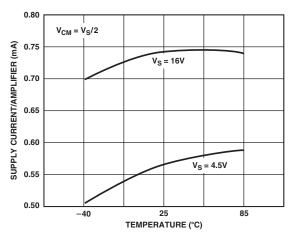
TPC 7. Output Voltage Swing vs. Temperature



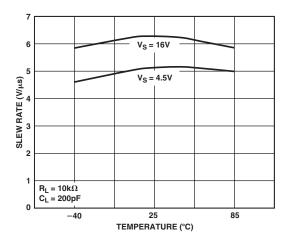
TPC 8. Voltage Gain vs. Temperature



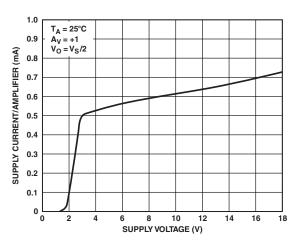
TPC 9. Output Voltage to Supply Rail vs. Load Current



TPC 10. Supply Current/Amplifier vs. Temperature

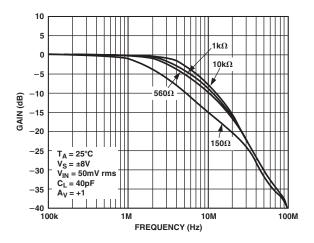


TPC 11. Slew Rate vs. Temperature

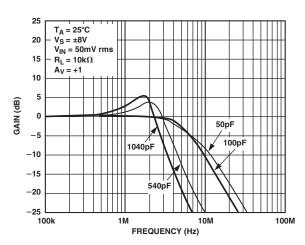


TPC 12. Supply Current/Amplifier vs. Supply Voltage

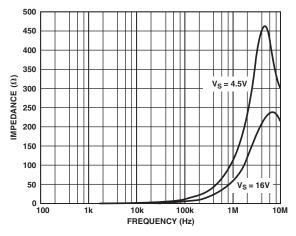
REV. C _5_



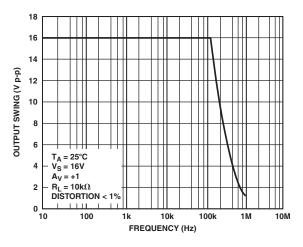
TPC 13. Frequency Response vs. Resistive Loading



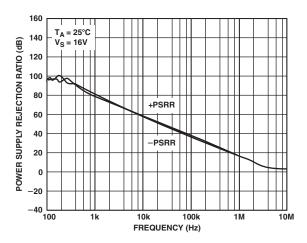
TPC 14. Frequency Response vs. Capacitive Loading



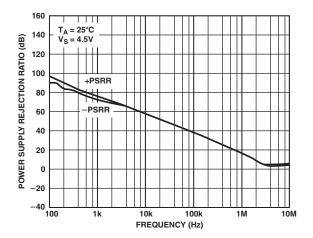
TPC 15. Closed-Loop Output Impedance vs. Frequency



TPC 16. Closed-Loop Output Swing vs. Frequency

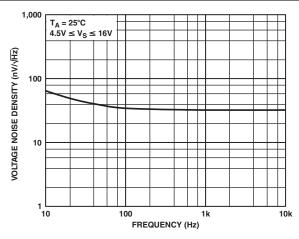


TPC 17. Power Supply Rejection Ratio vs. Frequency

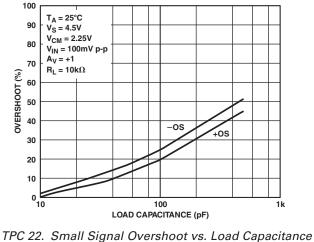


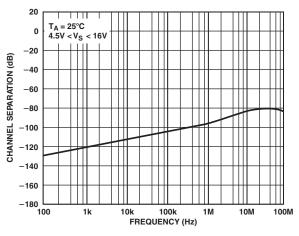
TPC 18. Power Supply Rejection Ratio vs. Frequency

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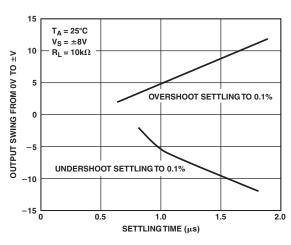


TPC 19. Voltage Noise Density vs. Frequency

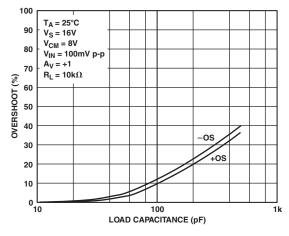




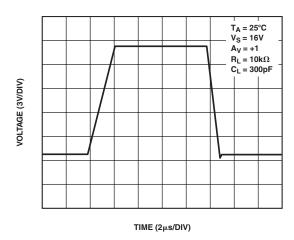
TPC 20. Channel Separation vs. Frequency



TPC 23. Settling Time vs. Step Size

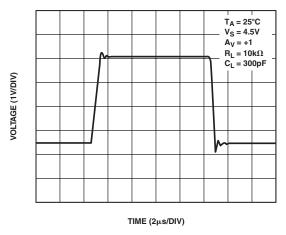


TPC 21. Small Signal Overshoot vs. Load Capacitance

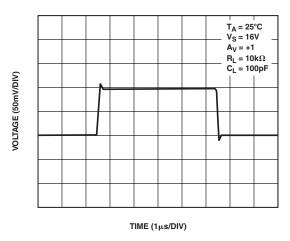


TPC 24. Large Signal Transient Response

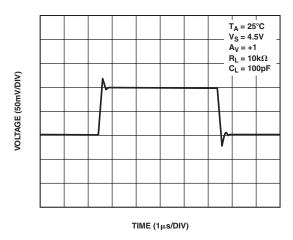
REV. C -7-



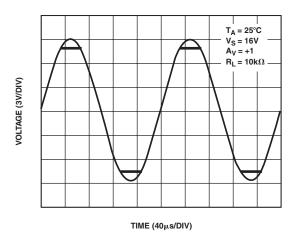
TPC 25. Large Signal Transient Response



TPC 26. Small Signal Transient Response



TPC 27. Small Signal Transient Response



TPC 28. No Phase Reversal

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APPLICATIONS

Theory of Operation

This family of buffers is designed to drive large capacitive loads in LCD applications. Each has high output current drive and rail-to-rail input/output operation and can be powered from a single 16 V supply. They are also intended for other applications where low distortion and high output current drive are needed.

Input Overvoltage Protection

As with any semiconductor device, whenever the input exceeds either supply voltage, attention needs to be paid to the input overvoltage characteristics. As an overvoltage occurs, the amplifier could be damaged, depending on the voltage level and the magnitude of the fault current. When the input voltage exceeds either supply by more than 0.6 V, the internal pn junctions will allow current to flow from the input to the supplies.

This input current is not inherently damaging to the device as long as it is limited to 5 mA or less. If a condition exists using the buffers where the input exceeds the supply by more than 0.6 V, an external series resistor should be added. The size of the resistor can be calculated by using the maximum overvoltage divided by 5 mA. This resistance should be placed in series with the input exposed to an overvoltage.

Output Phase Reversal

The buffer family is immune to phase reversal. Although the device's output will not change phase, large currents due to input overvoltage could damage the device. In applications where the possibility exists of an input voltage exceeding the supply voltage, overvoltage protection should be used as described in the previous section.

Power Dissipation

The maximum allowable internal junction temperature of 150°C limits the device's maximum power dissipation. As the ambient temperature increases, the maximum power dissipated by the device must decrease linearly to maintain the maximum junction temperature. If this maximum junction temperature is exceeded momentarily, the device will still operate properly once the junction temperature is reduced below 150°C. If the maximum junction temperature is exceeded for an extended period of time, overheating could lead to permanent damage of the device.

The maximum safe junction temperature, T_{JMAX} , is 150°C. Using the following formula, we can obtain the maximum power that the buffer family can safely dissipate as a function of temperature.

$$P_{DISS} = \left(T_{JMAX} - T_A\right) / \theta_{JA}$$

where:

 P_{DISS} = the power dissipation.

 T_{JMAX} = the maximum allowable junction temperature (150°C).

 T_A = the ambient temperature of the circuit.

 θ_{JA} = the AD856x package thermal resistance, junction-to-ambient.

The power dissipated by the device can be calculated as

$$P_{DISS} = (V_S - V_{OUT}) \times I_{LOAD}$$

where:

 V_S = the supply voltage.

 V_{OUT} = the output voltage.

 I_{LOAD} = the output load current.

Figure 1 shows the maximum power dissipation versus temperature. To achieve proper operation, use the previous equation to calculate P_{DISS} for a specific package at any given temperature, or see Figure 1.

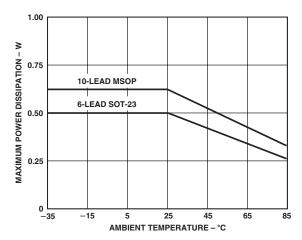


Figure 1. Maximum Power Dissipation vs. Temperature for 6- and 10-Lead Packages

Total Harmonic Distortion + Noise (THD+N)

The buffer family features low THD+N. The total harmonic distortion plus noise for the buffer over the entire supply range is below 0.08%. When the device is powered from a 16 V supply, the THD+N stays below 0.03%. Figure 2 shows the AD8568 THD+N versus frequency performance.

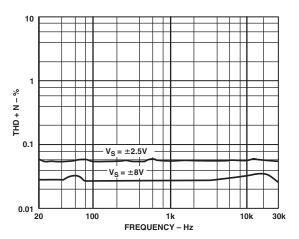


Figure 2. AD8568 THD+N vs. Frequency

Short-Circuit Output Conditions

The buffer family does not have internal short-circuit protection circuitry. As a precautionary measure, do not short the output directly to the positive power supply or to ground.

It is not recommended to operate the AD856x with more than 35 mA of continuous output current. The output current can be limited by placing a series resistor at the output of the amplifier whose value can be derived using the following equation.

$$R_X \ge \frac{V_S}{35 \, mA}$$

For a 5 V single-supply operation, R_X should have a minimum value of 143 Ω .

OUTLINE DIMENSIONS

6-Lead Small Outline Transistor Package [SOT-23] (RT-6)

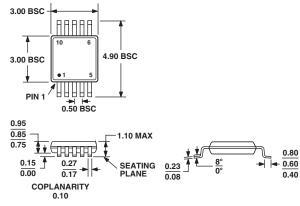
Dimensions shown in millimeters

2.90 BSC 1.60 BSC 1.90 1.90 1.45 MAX 0.50 0.15 MAX 0.50 0.15 MAX 0.50 0.15 MAX 0.50 0.15 MAX 0.22 0.08 1.45 MAX 0.22 0.08 1.45 MAX 0.22 0.08 1.45 MAX 0.22 0.08 0.45 0.30

COMPLIANT TO JEDEC STANDARDS MO-178AB

10-Lead Micro Small Outline Package [MSOP] (RM-10)

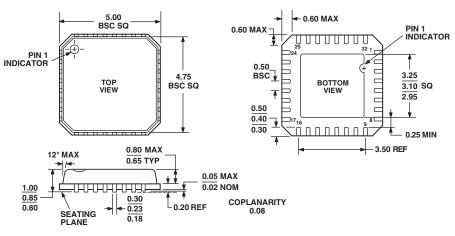
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187BA

32-Lead Lead Frame Chip Scale Package [LFCSP] 5 x 5 mm Body (CP-32-2)

Dimensions shown in millimeters



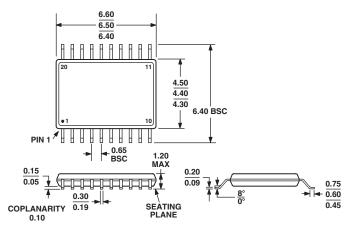
COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-2

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OUTLINE DIMENSIONS

20-Lead Thin Shrink Small Outline Package [TSSOP] (RU-20)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153AC

Revision History

Location	Page
12/03—Data Sheet changed from REV. B to REV. C.	
Updated ORDERING GUIDE	
Updated OUTLINE DIMENSIONS	
5/02—Data Sheet changed from REV. A to REV. B.	
Added 20-Lead TSSOP Package	
Added Package Type	
Updated ORDERING GUIDE	
Added TSSOP Package to OUTLINE DIMENSIONS	

REV. C -11-