

IRS210614S HIGH AND LOW SIDE DRIVER

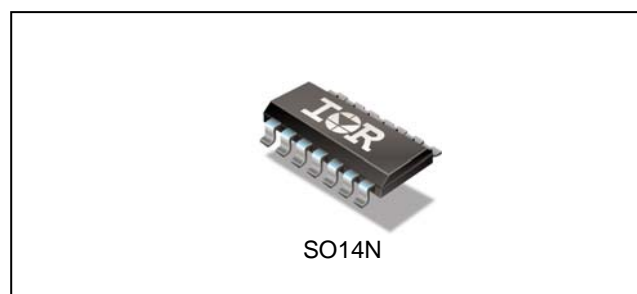
IC Features

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- 3.3 V, 5 V, and 15 V input logic compatible
- Matched propagation delay for both channels
- Logic and power ground +/- 5 V offset
- Lower di/dt gate driver for better noise immunity
- Outputs in phase with inputs
- RoHS compliant

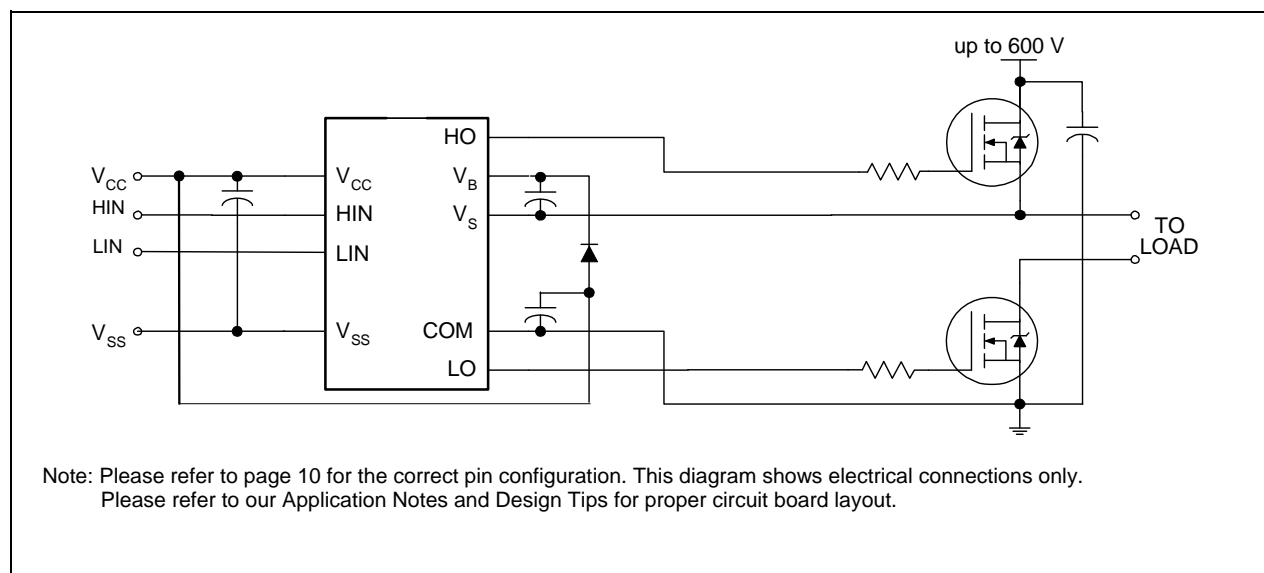
Product Summary

| | |
|--|-----------------|
| Topology | Half-Bridge |
| V_{OFFSET} | 600 V |
| V_{OUT} | 10 V-20 V |
| I_{O+} & I_{O-} (typical) | 290 mA & 600 mA |
| T_{on} & t_{off} (typical) | 165 ns & 165 ns |

Package Types



Typical Connection Diagram



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Description

The IRS21064S is a high voltage, high speed power MOSFET and IGBT driver with independent high and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 V.

Qualification Information[†]

| | | | |
|-----------------------------------|-------------------------|---|--|
| Qualification Level | | Industrial ^{††} | |
| | | Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level. | |
| Moisture Sensitivity Level | | SOIC14N | MSL2 ^{†††} (per IPC/JEDEC J-STD-020) |
| ESD | Machine Model | Class B (per JEDEC standard EIA/JESD22-A115) | |
| | Human Body Model | Class 2 (per EIA/JEDEC standard JESD22-A114) | |
| IC Latch-Up Test | | Class 1, Level A (per JESD78) | |
| RoHS Compliant | | Yes | |

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

| Symbol | Definition | Min. | Max. | Units |
|-----------|--|----------|-----------|-----------------------------|
| VB | High-side floating supply absolute voltage | -0.3 | 625 | V |
| VS | High-side floating supply offset voltage | VB - 25 | VB + 0.3 | |
| VHO | High-side floating output voltage | VS - 0.3 | VB + 0.3 | |
| VCC | Low-side output voltage | -0.3 | 25 | |
| VLO | Low-side and logic fixed supply voltage | -0.3 | VCC + 0.3 | |
| VIN | Logic input voltage | VS - 0.3 | VCC + 0.3 | |
| VSS | Logic ground | VCC - 25 | VCC + 0.3 | V/ns |
| dV_S/dt | Allowable offset supply voltage transient | --- | 50 | W |
| PD | Package power dissipation @ $T_A \leq +25\text{ }^{\circ}\text{C}$ | --- | 1.0 | |
| RthJA | Thermal resistance, junction to ambient | --- | 120 | $^{\circ}\text{C}/\text{W}$ |
| TJ | Junction temperature | --- | 150 | $^{\circ}\text{C}$ |
| TS | Storage temperature | -50 | 150 | |
| TL | Lead temperature (soldering, 10 seconds) | --- | 300 | |

Recommended Operating Conditions

The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset rating are tested with all supplies biased at a 15 V differential..

| Symbol | Definition | Min. | Max. | Units |
|--------|--|------------|------------|-------|
| VB | High-side floating supply absolute voltage | $V_S + 10$ | $V_S + 20$ | V |
| VS | High-side floating supply offset voltage | Note 1 | 600 | |
| VHO | High-side floating output voltage | V_S | VB | |
| VCC | Low-side output voltage | | 10 | |
| VLO | Low-side and logic fixed supply voltage | 0 | VCC | |
| VIN | Logic input voltage | V_{SS} | VCC | |
| VSS | Logic ground | -5 | 5 | |
| TA | Ambient temperature | -40 | 125 | °C |

† Logic operational for V_S of -5 V to +600 V. Logic state held for V_S of -5 V to -VBS.
(Please refer to the Design Tip DT97-3 for more details).

Static Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 14 V, C_T = 1 nF and T_A = 25 °C unless otherwise specified. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.
CLO1=CLO2=CHO1=CHO2=1 nF.

| Symbol | Definition | Min | Typ | Max | Units | Test Conditions |
|--|--|-----|------|-----|-------|---|
| Low Voltage Supply Characteristics | | | | | | |
| V _{IH} | Logic “1” input voltage | 2.5 | — | — | V | V _{CC} = 10 V to 20V |
| V _{IL} | Logic “0” input voltage | — | — | 0.8 | | |
| V _{OH} | High level output voltage, V _{BIAS} -V _O | — | 0.05 | 0.2 | | I _O = 2 mA |
| V _{OL} | Low level output voltage, V _O | — | 0.02 | 0.1 | | |
| I _{LK} | Offset supply leakage current | — | — | 50 | μA | V _B = V _S = 600 V |
| I _{QBS} | Quiescent VBS supply current | 20 | 75 | 130 | | V _{IN} = 0 V or 5V |
| I _{QCC} | Quiescent VCC supply current | 60 | 120 | 180 | | |
| I _{IN+} | Logic “1” input bias current V _{IN} = 5 V | — | 5 | 20 | | |
| I _{IN-} | Logic “0” input bias current V _{IN} = 0 V | — | — | 5 | | |
| V _{CCUV+} V _{BSUV} | V _{CC} and V _{BS} supply undervoltage positive going threshold | 8.0 | 8.9 | 9.8 | V | |
| V _{CCUV-} V _{BSUV-} | V _{CC} and V _{BS} supply undervoltage negative going threshold | 7.4 | 8.2 | 9.0 | | |
| V _{CCUVH} V _{BSUVH} | Hysteresis | 0.3 | 0.7 | — | | |
| I _{O+} | Output high short circuit pulsed current | 130 | 290 | — | mA | V _O = 0 V, PW ≤ 10 μs |
| I _{O-} | Output low short circuit pulsed current | 270 | 600 | — | | V _O = 15 V, PW ≤ 10 μs |

Dynamic Electrical Characteristics

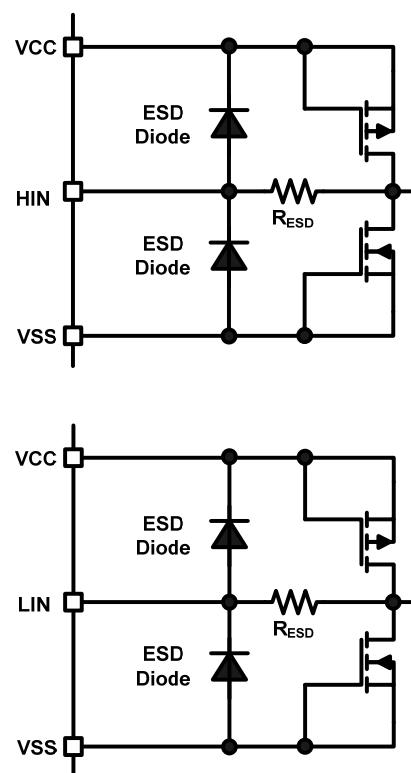
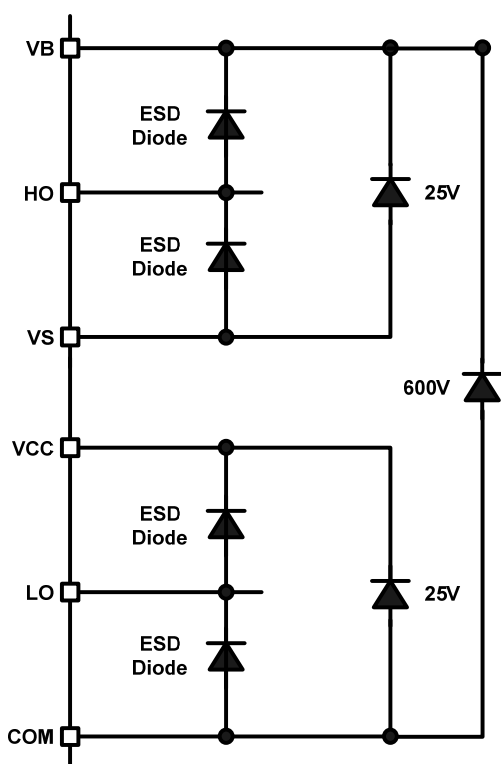
V_{BIAS} (V_{CC} , V_{BS}) = 15 V, $V_{SS} = \text{COM}$, $C_L = 1000\text{ pF}$, $T_A = 25\text{ }^\circ\text{C}$.

| Symbol | Component | Min. | Typ. | Max. | Units | Test Conditions |
|-----------|-------------------------------------|------|------|------|-------|------------------------------------|
| t_{on} | Turn-on propagation delay | --- | 165 | 230 | ns | $V_S = 0\text{ V}$ |
| t_{off} | Turn-off propagation delay | --- | 165 | 230 | | $V_S = 0\text{ V or }600\text{ V}$ |
| MT | Delay matching, HS & LS turn-on/off | --- | 0 | 30 | | |
| t_r | Turn-on rise time | --- | 100 | 220 | | $V_S = 0\text{ V}$ |
| t_f | Turn-off fall time | --- | 35 | 80 | | |

IRS210614S
PRELIMINARY

The schematic diagram illustrates the internal architecture of the IRS210614 integrated circuit. The chip is powered by VCC and VSS. The input stage features two differential inputs, HIN and LIN, each connected to a resistor and a buffer. These inputs feed into VSS/COM level shifters. The HIN path continues through a pulse generator and an HV level shifter, which is connected to a UV DETECT block and a pulse filter. The LIN path passes through a delay block and an OR gate before reaching a second UV DETECT block. The UV DETECT blocks are connected to a flip-flop (R, S, Q) and a UV DETECT block. The output stage consists of two push-pull MOSFET drivers, one for the HO (High Output) and one for the VS (VSS Output), which are connected to the Q output of the flip-flop. The HO output is also connected to a UV DETECT block. The VS output is connected to a UV DETECT block. The HO output is also connected to a UV DETECT block. The VS output is connected to a UV DETECT block. The HO output is also connected to a UV DETECT block. The VS output is connected to a UV DETECT block.

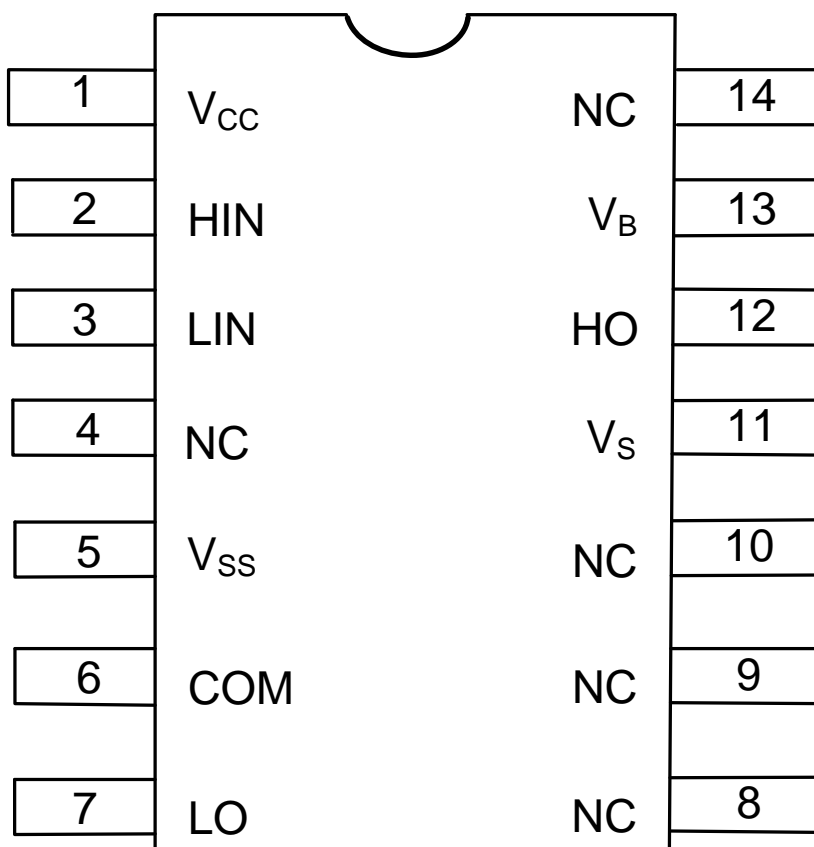
I/O Pin Equivalent Circuit Diagrams



Lead Definitions

| Pin# | Symbol | Description |
|------|----------|---|
| 1 | V_{CC} | Low-side and logic fixed supply |
| 2 | HIN | Logic input for high-side gate driver output (HO), in phase |
| 3 | LIN | Logic input for low-side gate driver output (LO), in phase |
| 4 | NC | No Connect |
| 5 | V_{SS} | Logic ground |
| 6 | COM | Low-side return |
| 7 | LO | Low-side drive output |
| 8 | NC | No Connect |
| 9 | NC | No Connect |
| 10 | NC | No Connect |
| 11 | V_S | High-side floating supply return |
| 12 | HO | High-side gate drive output |
| 13 | V_B | High-side floating supply |
| 14 | NC | No Connect |

Lead Assignments



Waveform definitions

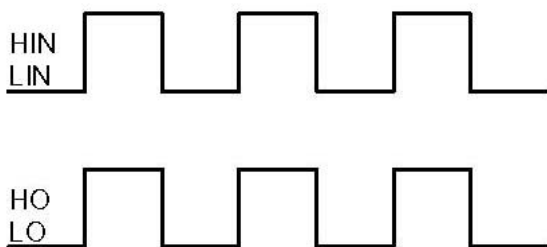


Figure 1. Input/Output Timing Diagram

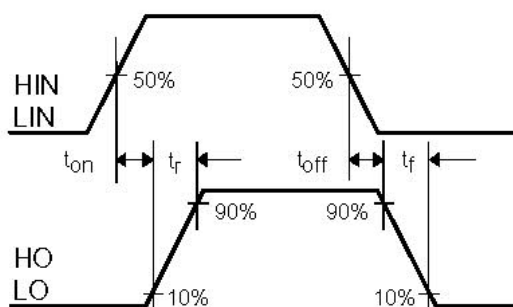


Figure 2. Switching Time Waveform Definitions

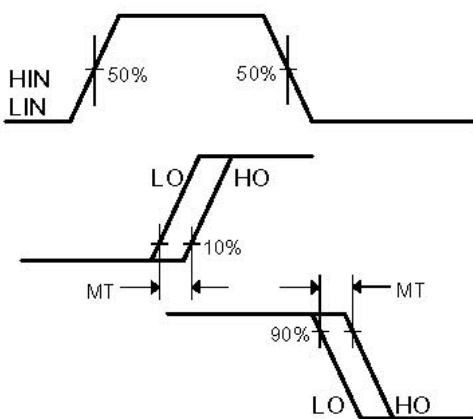
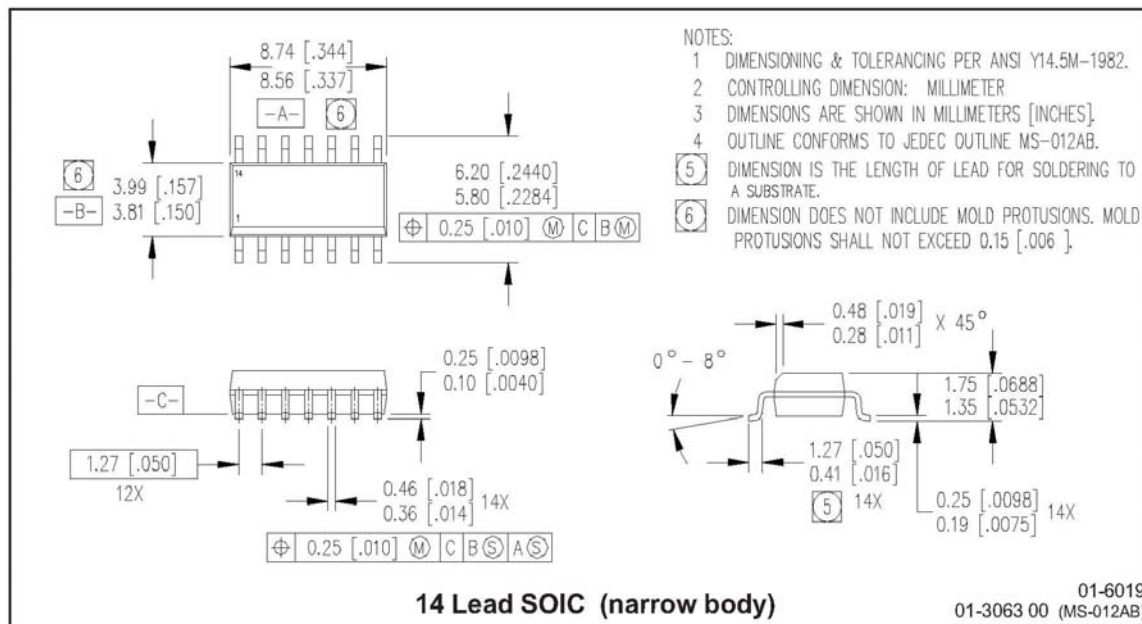
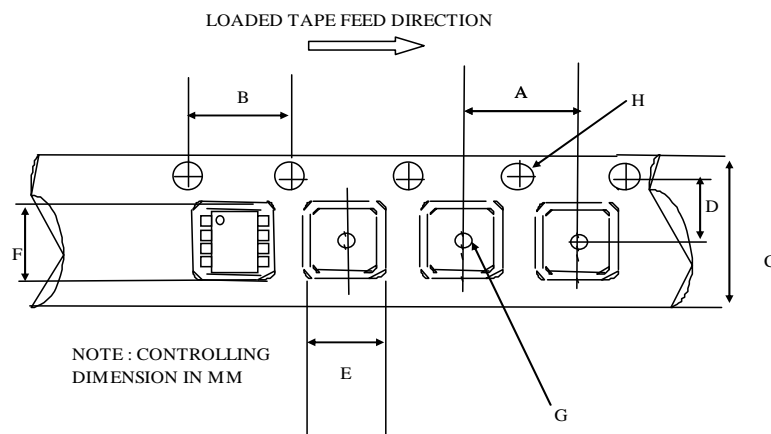


Figure 3. Delay Matching Waveform Definitions

Package Details: SO14N

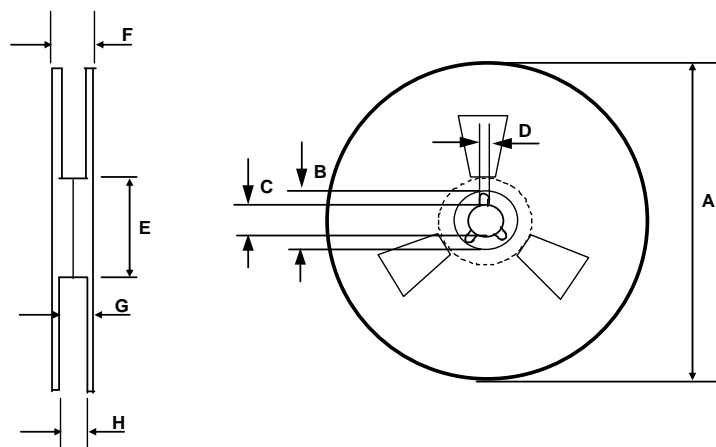


Package Details: SOIC14N, Tape and Reel



CARRIER TAPE DIMENSION FOR 14SOICN

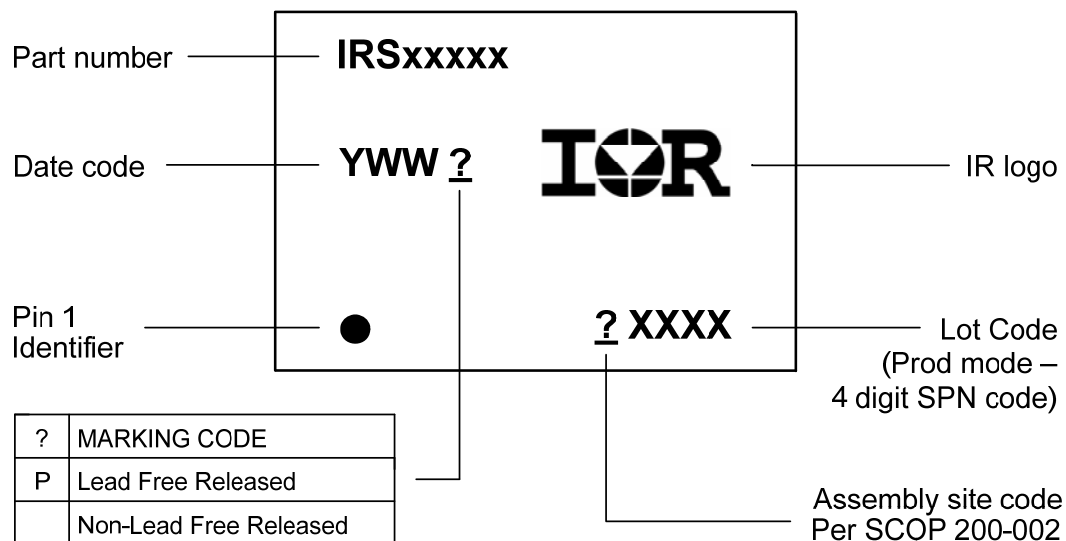
| Code | Metric | | Imperial | |
|------|--------|-------|----------|-------|
| | Min | Max | Min | Max |
| A | 7.90 | 8.10 | 0.311 | 0.318 |
| B | 3.90 | 4.10 | 0.153 | 0.161 |
| C | 15.70 | 16.30 | 0.618 | 0.641 |
| D | 7.40 | 7.60 | 0.291 | 0.299 |
| E | 6.40 | 6.60 | 0.252 | 0.260 |
| F | 9.40 | 9.60 | 0.370 | 0.378 |
| G | 1.50 | n/a | 0.059 | n/a |
| H | 1.50 | 1.60 | 0.059 | 0.062 |



REEL DIMENSIONS FOR 14SOICN

| Code | Metric | | Imperial | |
|------|--------|--------|----------|--------|
| | Min | Max | Min | Max |
| A | 329.60 | 330.25 | 12.976 | 13.001 |
| B | 20.95 | 21.45 | 0.824 | 0.844 |
| C | 12.80 | 13.20 | 0.503 | 0.519 |
| D | 1.95 | 2.45 | 0.767 | 0.096 |
| E | 98.00 | 102.00 | 3.858 | 4.015 |
| F | n/a | 22.40 | n/a | 0.881 |
| G | 18.50 | 21.10 | 0.728 | 0.830 |
| H | 16.40 | 18.40 | 0.645 | 0.724 |

Part Marking Information



Ordering Information

| Base Part Number | Package Type | Standard Pack | | Complete Part Number |
|------------------|--------------|---------------|----------|----------------------|
| | | Form | Quantity | |
| IRS210614S | SOIC14N | Tube/Bulk | 55 | IRS210614SPBF |
| | | Tape and Reel | 2500 | IRS210614STRPBF |

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