Introduction

The PD64001/H is a single-port Power over Ethernet PSE (Power Source Equipment) Manager. The PSE Manager allows for the detection of IEEE 802.3af-2003 and IEEE802.3at-draft4.2 powered devices, ensuring safe power feeding and monitoring of Ethernet ports. With a minimum of external components, the PD64001/H integrates in a one-port or two-port PoE-port switches and Midspans.

The PD64001/H has several operating modes, allowing it to be tailored to the customer's application, be it a switch or a Midspan, IEEE802.af or IEEE802.3at-draft4.2-compliant, with 1-event or 2-events classification, AC or DC disconnect and strict resistor detection or legacy detection capabilities. It operates in a total stand-alone mode, with no need for user intervention.

The PD64001/H supports 2-events classification and operates at Iport_max currents of up to 600 mA / 720 mA (in coordination with PD64001 / PD64001H) per port, making it fully compliant with the IEEE802.3at-draft4.2

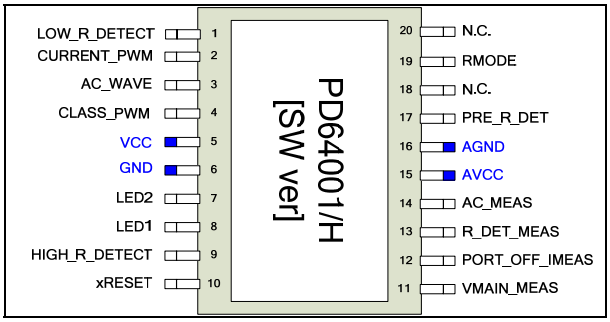
This datasheet includes a complete application note and provides detailed information and circuitry design guidelines for the implementation of a 1-port Power over Ethernet (PoE) system, based on Microsemi's™ 1-channel PoE device, the PD64001/H.

This document allows the designer to integrate PoE capabilities, as specified in the IEEE802.3af standard into an Ethernet switch, Midspan or a router.

Applicable Documents

- IEEE802.3af-2003
- IEEE802.3at-draft4.2

Pin Configuration



Features

- IEEE 802.3af-2003-compliant
- IEEE802.3at-draft4.2 compliant
- PD64001 supports Iport_max of 600 mA
- PD64001H supports Iport_max of 720 mA
- Programmable solution, can be updated as the IEEE802.3at standard evolves
- Accurate power measuring and extremely low power dissipation
- BOM and software tailored for specific application saving total solution cost
- Minimal power supply stress and EMI noises
- Legacy (pre-standard) PD's detection
- 1-port standalone PoE control
- 1-event and 2-event classification supported
- External FET and sense resistor
- AC and DC disconnect
- Detection of the disconnection method by assembled resistor
- Port On/Off Host interface
- Application uses a single operating voltage source
- Direct LED driving including IEEE802.3at indication
- SOIC-20 package
- RoHS compliant
- -40° to +85° C operating ambient temperature

Ordering Information

PART	Ilim	TEMP. RANGE	PIN PACKAGE
PD64001	600 mA	-40° to +85° C	SOIC-20
PD64001H	720 mA	-40° to +85° C	SOIC-20

Evaluation board ordering number: PD-IM-7301

Main Features Description

Feature	Description
PD64001/H features	
IEEE 802.3af-2003 Compliant	The PD64001/H meets all IEEE-802.3af-2003 standard requirements including: Multi – point resistor detection PD classification function AC disconnect and DC disconnect function Supports Back-off feature for Midspan implementation
IEEE802.3at-draft4.2 Compliant	Including support for high power and 2-events classification.
Single DC voltage Input	The PD64001/H requires a single DC voltage source: 44V to 57V. No additional voltage sources (e.g. 3.3V/5V) are required for the PoE system's operation.
Wide temperature range: -40°c to +85°c	The PD64001/H can operate over a wide temperature range: -40° C to +85° C. This temperature range enables the integration of the PD64001/H into small unventilated boxes and operates in harsh environments.
Low thermal dissipation (1Ω sense resistor)	The PD64001/H has a very low thermal dissipation. The Rsense in the PD64001/H applications is only 1Ω to keep the peripheral components in low temperatures as well.
External Power FET	External Mosfet is utilized to increase the flexibility of the solution, enabling it to be tailored to the customer power requirements.
H/W Disable Port	The PD64001/H utilizes a dedicated pin, allowing an immediate disconnection of the PoE port. This disable-port pin input can be controlled via the Host CPU.
Pre-Standard PD Detection	Enables the detection and powering of pre-standard power devices (PDs).
Detection of Cisco Devices	Enables the detection and powering of all Cisco devices including pre-standard terminals.
LED Support	Direct driving of the LED circuitry. This enables the designer to implement a simple LED circuit, indicating whether an IEEE802.3af or IEEE802.3at device is connected.

Maximum Ratings

V_{main}..... -0.3 to 60 V
xRESETN input voltage..... -0.5 to 5 V
Application circuitry DC current .....25 mA
ESD (Human Body Model)..... -2V to 2kV(1)
Lead temperature (soldering, 10 s)..... 300° C

Notes:.
(1) ESD testing is performed in accordance with the Human Body Model (CZap = 100 pF, RZap = 1500 Ω).

Stresses beyond those listed above may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Conditions

PARAMETER	MIN.	NOM.	MAX.	UNIT
Operating temperature	-40		+85	°C
Storage temperature	-65		+150	°C
Operational limitations (1)	44	50	57	V

(1) To get higher power drive at the PSE output ports, it is recommended to use an operating voltage source greater then 50 V.

Electrical Characteristics

DC Characteristics for Digital Inputs and Outputs

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	REMARKS
Pin Name	**xRESET**				
Type	Schmitt Trigger CMOS input with internal pull-up				
High level input voltage	VIH	0.9 VCC	VCC+0.5V	V	Vcc = 5V
Low level input voltage	VIL	-0.5V	0.2 VCC	V	Vcc = 5V
Input high current	IIH		+1	µA	
Input low current	IIL		+1	µA	
Reset assertion time	Trst	2.5		µS	
Internal Pull-up value	Rpu	30	60	kΩ	

Dynamic Characteristics

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Automatic recovery from overload shutdown	TOVLREC value, measured from port shutdown (can be modified through control port)		8		s
Automatic recovery from no-load shutdown	TUDLREC value, measured from port shutdown (can be modified through control port)		1		s

Thermal Data

Microsemi's PD64001/H enables building very low power dissipating PoE devices. For a single port, the system worst case power dissipation can be calculated as follows.

Application	Disconnection Method	Iport_max Current	Rsense (1Ω)	Diode	MOSFET	PoE Manager	Total
EEE802.3af	DC	350 mA	0.12 W	-	0.012 W (0.1Ω)	0.60 W	0.73 W
EEE802.3af	AC	350 mA	0.12 W	0.53 W	0.012 W (0.1Ω)	0.60 W	1.26 W
EEE802.3at	DC	600 mA	0.36 W	-	0.036 W (0.1Ω)	0.60 W	1 W
EEE802.3at	AC	600 mA	0.36 W	0.9 W	0.036 W (0.1Ω)	0.60 W	1.9 W
EEE802.3at	DC	720 mA	0.52 W	-	0.052 W (0.1Ω)	0.60 W	1.17 W
EEE802.3at	AC	720 mA	0.52 W	1.1 W	0.052 W (0.1Ω)	0.60 W	2.27 W

Pin Functionality

PIN	PIN NAME	PIN TYPE	PIN DESCRIPTION
1	LOW_R_DETECT	Digital Output	Low level resistance detection command
2	CURRENT_PWM	Digital Output	Current limit set PWM output
3	AC_WAVE	Digital Output	AC disconnect output wave
4	CLASS_PWM	Digital Output	Class voltage set PWM output
5	VCC	VCC	5V Digital VCC
6	GND	GND	Digital ground
7	LED2	Digital Output	LED2 output command
8	LED1	Digital Output	LED1 output command
9	HIGH_R_DETECT	Digital Output	High level resistance detection command
10	XRESET	Digital Input	Reset on/off command from host
11	VMAIN_MEAS	Digital Output	Vmain measurement command
12	PORT_OFF_IMEAS	Digital I/O	Port Off command/ current measurement input
13	R_DET_MEAS	Digital I/O	Port voltage measurement input
14	AC_MEAS	Digital I/O	AC disconnect measurement input
15	AVCC	VCC	5V Analog VCC
16	AGND	GND	Analog ground
17	PRE_DET	Digital Output	Pre detection command
18	RESERVED1	Digital I/O	Reserved for communication future use
19	RMODE	Digital Input	POE manager mode setup
20	RESERVED2	Digital I/O	Reserved for communication future use

R Mode Pin

This pin is connected to a resistor voltage divider. It allows the user to choose a combination of three features, as specified in the following table:

R_mode Voltage	ALT A	ALT B	CAP	AT/ 720 mA	R8 (Ω)*
0.313 –	X				1.02
0.94– 1.25		X			2.8K
1.563 –	X		X		5.23
2.19 – 2. 5		X	X		8.87
2.82– 3.1	X			X	14.7
3.44 –		X		X	25.5
4.06 –	X		X	X	54.9
4.68 – 5 V		X	X	X	No

* R8 Pull-down's value depends on the actual mode, while for all of the modes, R7 Pull-up's value is 10Kohm.

The ALT A / ALT B option selects between a PSE alternative A or PSE alternative B as specified in section 33.2 of the standard. To implement a Midspan PSE, use the ALT B option. The AT option is IEEE802.3at- Compliant in accordance with the IEEE802.3at-draft4.2. The CAP option is pre-standard Capacitor detection mode.

General Application Description

The circuit comprises the following major interfaces with the Host board:

Control

A Reset control signal driven by the switch circuitry is used to reset the PoE circuit. This signal should be optically coupled by the Host in order to maintain the requirements for the 1500 Vrms isolation.

Power Supply Mains

The PoE system operates over a range of 44V to 57V.

This power must be isolated from the switch supply and chassis by 1500 Vrms.

Grounds

There are several grounds used in the system: chassis, digital and analog. The chassis ground is connected to the switch's chassis ground.

Microsemi
Analog Mixed Signal Group
2381 Morse Avenue, Irvine, CA 92614, USA; Phone (USA): (800) 713-4113, (ROW): (949) 221-7100 Fax: (949) 756-0308

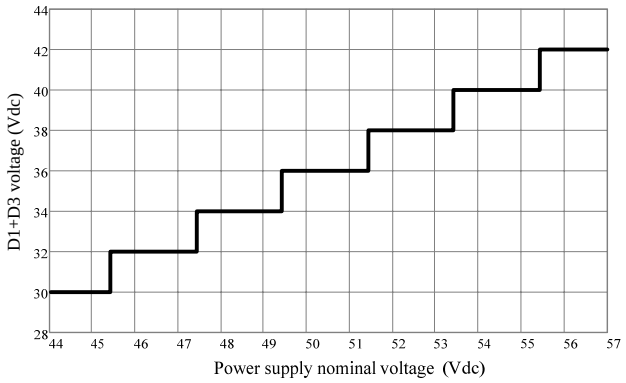
This ground plane should be 1500Vrms isolated from the PoE circuitry as well as the power supply for the PoE circuitry. The digital and analog grounds are electrically the same ground. However, in order to reduce noise coupling, the grounds are physically separated and connected only at a single point.

5V Regulator

A single port application includes a 5V regulator (Vcc) fed by the Vmain through D1 and D3 Zener diodes and provides up to 25 mA used to power the CPU and peripheral components in the PoE domain.

Using a 3% accuracy power supply for the PoE circuitry D1 and D3 should be selected according to the power supply nominal voltage set point using the following graph.

D1 voltage plus D3 voltage as seen in the below graph, should be evenly divided between the two Zener diodes.



If an adequate 5V power source is available, the 5V regulation circuitry can be removed and the Zener diodes may be replaced with lower current (5 mA) Zener diodes but with same voltage requirements.

Detailed Application Description

(See **Figure 2**)

The PD64001/H performs a multitude of internal operations and PoE functions, requiring a bare minimum of external components.

The device is based on Atmel's ATtiny461 MCU. Each PD64001/H device handles one port. **Figure 2** shows the device with its related components for a 1-port configuration.

Mode Configuration - set by the resistor divider (R7/R8) tied in to the RMODE line. The values are fixed for each mode of operation and described in the "R Mode pin" section in this document.

Line Detection Circuitry – when performing a line detection procedure, the PoE device utilizes certain voltage levels over the output port. These levels are produced by switched resistor dividers and sensed by the PD64001/H in order to confirm a valid PD connection.

Current Loop Circuitry – the current is controlled by Q4 MOSFET. The PD64001/H provides PWM signal via pin#2 with a constant duty cycle (depending on the R mode configuration). This PWM signal is filtered and utilized as the current limit circuitry voltage reference.

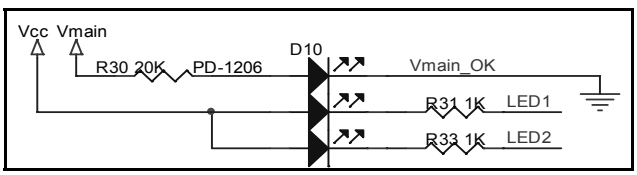
Sense Resistors – for each powered port, two 2-Ohm 2010 (1%) resistors connected in parallel (1-Ohm equivalent) are used in series with the output (R9, R11). In cases where the ambient temperature drops below 70^0C, or the product does not have to meet 802.3at power, a single 1-Ohm 2010 (1%) resistor is adequate.

Classification Circuitry – Upon port investigation completion, the PD should be classified by its classification current signature. Two voltage levels are set over the port, derived from a reference voltage filtered from PD64001/H's pin#4 (PWM signal) and sent to an operational amplifier controlling Q4.

Output port - The load resistance of the PD attached to the port is presented in parallel with R13.

The resulting voltage developed across both resistances is monitored to establish the 802.3af/at compatibility.

LED indication - The 1 port application may use the PD64001/H LED1 and LED2 pins for system status indications as shown below:



PD Operating Status	LED1	LED2
IEEE802.3af – ON	ON	OFF
IEEE802.3at – ON	ON	ON
IEEE802.3af - OVL/SC	Blink at 1Hz	OFF
IEEE802.3at - OVL/SC	Blink at 1Hz	Blink at 1Hz
Vmain out of range	Blink at 4Hz	OFF

Layout Design Guidelines

(See Figure 3 for layout example)

Isolation & Termination – as specified in the IEEE standard, certain isolation requirements need to be met in all PoE equipment. In addition, EMI limitations should be considered, according to FCC and European EN regulations.

These requirements are taken into account by PoE switch vendors, while designing the switch circuitry. However, when a PoE device is integrated into a switch, special design considerations must be taken into account, due to the unique combination of Data and Power circuitries.

The next paragraphs define these requirements and provide recommendations for their implementation, so as to assist designers in meeting those requirements and in integrating PoE Chipset.

Isolation - As specified in the IEEE standard, 1500Vac rms isolation is required between the main board circuitry of the switch, including protective and frame ground and the PoE circuitry.

Isolating the Stacked Modular Jack Assembly

The IEEE standard requires 1500 Vrms isolation between PoE voltages and frame ground (EGND). Note that RJ-45 jack assemblies may have a metal cover that reach almost to the PCB surface.

Proper traces clearance (at least 80 mils) are to be maintained between EGND traces for the RJ-45 modular jack assembly metal covering and adjacent circuit paths and components.

To prevent 1500 Vrms isolation violation, it is necessary to provide layout clearances of PoE traces, on the top layer, in the vicinity of the RJ-45 connector assemblies.

PoE Output Ports' Filtering and Terminations: A switch normally creates a noisy environment. In order to meet the EMI requirements, good filtering and line terminations may be needed when connecting the PoE circuit outputs to the switch circuitry (see Figure 1). Note that in most PoE systems, it is recommended to use 0 Ohms resistors for R100 and R101. However, certain systems may benefit from the 75Ohm value. It is recommended that filtering provisions are utilized.

A circuitry for the recommended filter includes:

- A common mode choke for conducted EMI performances
- Output differential capacitor filter for radiated EMI performances
- Y-capacitive/resistive network to chassis

Since each system is a unique EMI case, this circuit is a good starting point for EMI suppression.

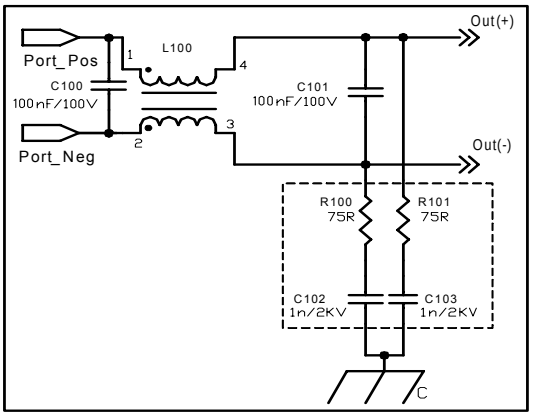


Figure 1: Recommended EMI Filter

Note For best EMI performance and to avoid additional noise accumulated on the lines between the filter and the port connectors, it is recommended to assemble this circuitry as close as possible to the port connectors.

PoE circuitry Trace Clearance - PoE technology involves voltages as high as 57VDC. Thus, plan adjacent traces for 100V operational creepage. Operational creepage should be maintained to prevent breakdown between traces carrying these potentials.

Locating PoE Circuitry in a Switch - Placement of the PoE circuitry must be as close as possible to the

switch's pulse transformers, to minimize the length of high current traces as well as RFI pick-up.

Ground & Power Planes - As the Chipset PoE solution is a mixed-signal (analog and digital) circuitry, special care must be taken when routing the ground and power signals lines. Ground planes are crucial for proper operation and should be designed in accordance with the following guidelines:

- Separate analog and digital grounds, with a gap of at least 40 mils.
- Earth ground is used to tie in the metal frame of the RJ-45 connectors. This ground is to be routed separately and connected to the switch's metal chassis/enclosure
- Only a single connection point is to be used between the digital and analog grounds, in order to prevent ground loop currents. This connection is to be accomplished near the current loop senses resistors R9, R11
- The traces from Vmain input to the port output, PoE switch (Q4) and sense resistors must be designed to carry 1A continuous current

Peripheral Components –

- To prevent hot spots on the peripheral components minimum distance of 5mm should be maintained between the powering Zener diodes D1 and D3, the linear regulator U1, sense resistors R9 and R11 (placed together) and current limit MOSFET Q4. Other methods may be used in order to dissipate the heat, such as thermal copper planes at the top and bottom layers with heat transfer vias between them
- Filtering capacitors for Vcc (U4 pins 5, 15) are to be located close to these pins
- The input and output capacitors of the linear regulator should be placed close to the regulator pins
- The trace connecting the power MOSFET and the sense resistors should be as short as possible and the current loop sampling trace should be connected as close as possible to the sense resistors

Specifying PoE Power Supply

An intelligent selection of the power supply to be used in conjunction with the 1-port system may avoid the use of additional filtering circuitry (e.g. Front End Common Mode filter) for standard regulatory approval.

Electromagnetic compatibility requirements –

Typical Power over Ethernet (PoE) technology systems are classified in most applications as Information Technology Equipment (I.T.E).

The I.T.E should comply with three tests in order to get a standard approval:

- Conducted disturbance at mains ports (AC input)
- Radiated disturbance at a measuring distance of 10m
- Conducted common mode disturbance at telecommunication ports (output port containing Ethernet+Power)
  A relatively new requirement of EN55022 that is mandatory as of August 1st, 2007

In most cases, the PSE side of a PoE system incorporates a main AC to DC Switching Mode Power Supply (SMPS) required for delivery of a DC power to the PoE ports.

This power supply is most likely to be the largest source for common mode noise injection on the output ports wires, as its noisy output voltage is super-imposed on the telecommunication wires by the PoE control circuitry. The common mode noise is generated by the high dv/dt and dI/dt switching rates in power MOSFETs and high speed rectifying diodes, common in SMPS designs.

As the system designer is usually responsible for specifying this power supply, it is important to add the standard requirements to the power supply specifications and specify a specific reference test setup to be used for the tests.

This reference test setup should be as similar as possible to the final product, which means using the same box material (plastic or metal) and the same distance and polarity between the SMPS and PoE circuitry.

When specifying and testing the power supply, it is important to assure that test requirements are met under all load conditions and line voltages.
Most switching power supplies designs will exhibit the highest conducted noise at the maximum load and the lowest line voltage.

However, other cases may also exist. As it is impractical to go through all loads span, it is recommended to test at full load, medium load and minimum load.

The cables suggested for use are Cat 5 UTP cables of at least 5m. (Both UTP and FTP cables shall be tested for compliance in the final system tests).

Note that the standard deals with shielded and un-shielded cables independently and the appropriate test procedure shall be performed.

Resistive loads are selected to remove possible noise injection from the PD side, leaving only the main power supply as the source of noise.

For radiated disturbance using a proper SMPS layout (short power patch and avoiding current loops) may contribute to disturbance reduction.
For additional reduction if needed, full or partial metal frame connected to mains earth may be used.

Immunity requirements –

An I.T.E should comply with EN55024 in order to get a standard approval:

Most power supply manufacturers are familiar with the standard requirements from the power supply and know how to design the power supply to comply with it. The requirements from the power supply's AC input power port are:

- Immunity to radio frequency continuous conducted according to IEC61000-4-6
- Voltage dips and voltage interruptions according to IEC61000-4-11
- Surges according to IEC61000-4-5
- Fast transients according to IEC61000-4-4
- **The PoE circuitry may also be exposed to immunity tests on the telecommunication ports such as:**
- Radio frequency continuous conducted according to IEC61000-4-6
- Surge line to earth according to IEC61000-4-5 (usually for port that may connect to outdoor cables)
- Fast transients according to IEC61000-4-4 and the PoE enclosure port exposed to:
- Radio frequency electromagnetic field immunity according to IEC61000-4-3
- ESD electrostatic-discharge according to IEC61000-4-2

To satisfy these tests requirements on the telecommunication lines, "Y" capacitors to the chassis (earth) will create a current path to earth.

It is a good practice to have two "Y" capacitors of 10nF/2000V each at the power supply output positive and negative nodes to earth, to create a current path for surge generated on the telecommunication lines (respect to earth).

The system may benefit from two small "Y" 1nF/2000V capacitors, on the PoE positive and negative output lines close to the output RJ45 connector, by increasing system immunity to ESD.

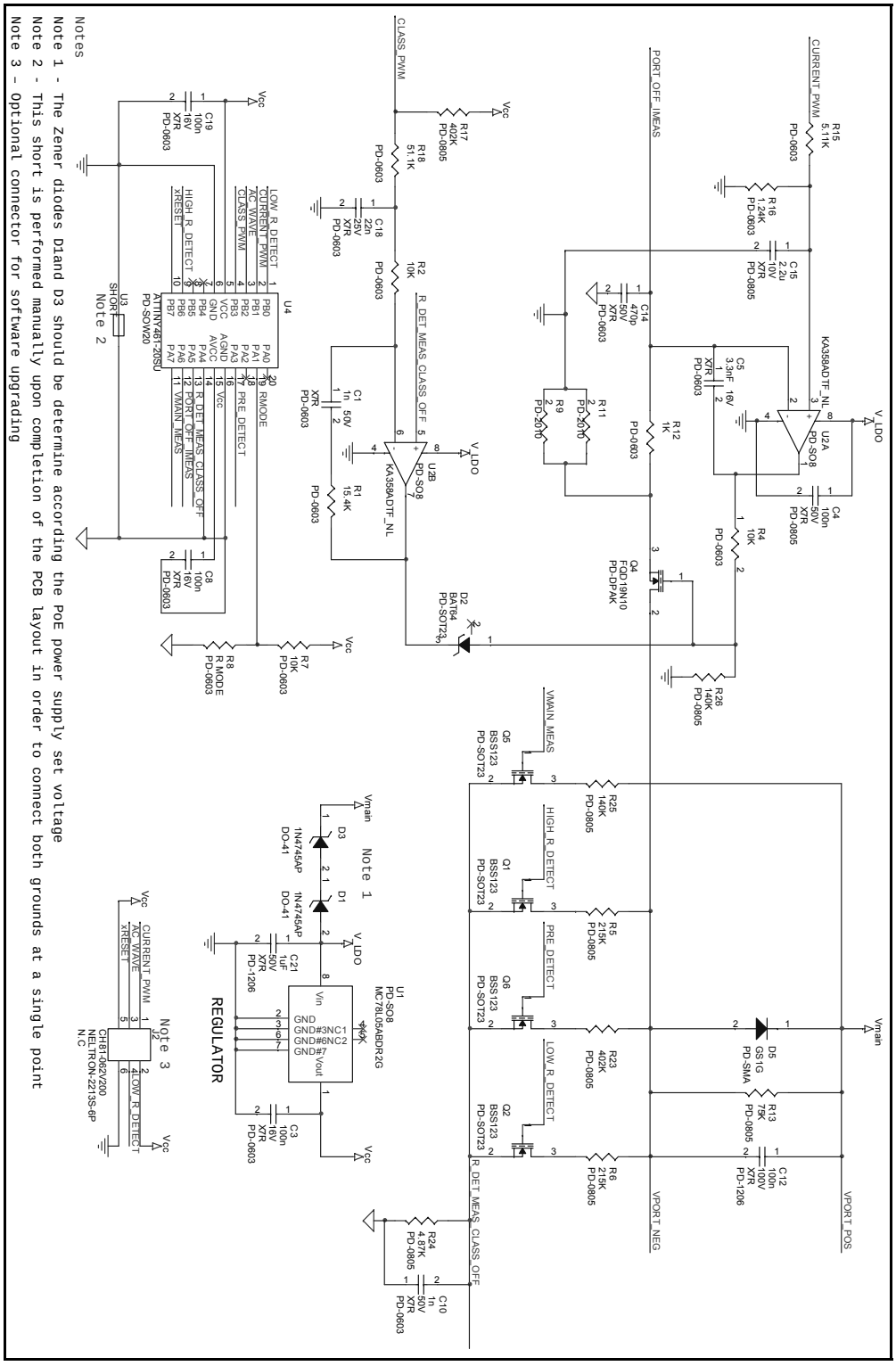


Figure 2: One Port Chipset Schematic Diagram

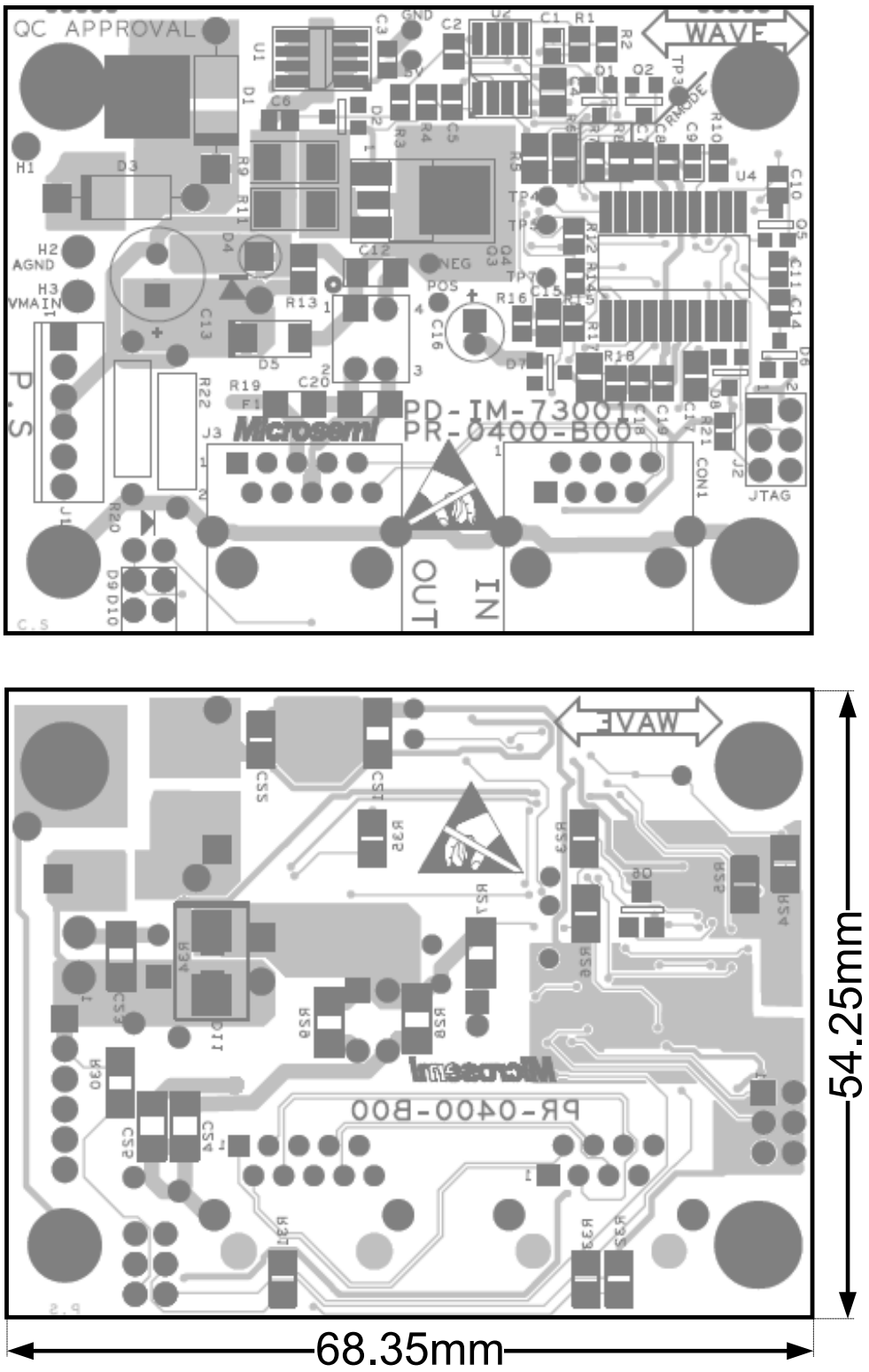


Figure 3: Layout Example of Component and Print Side

Bill of Materials for a PoE System

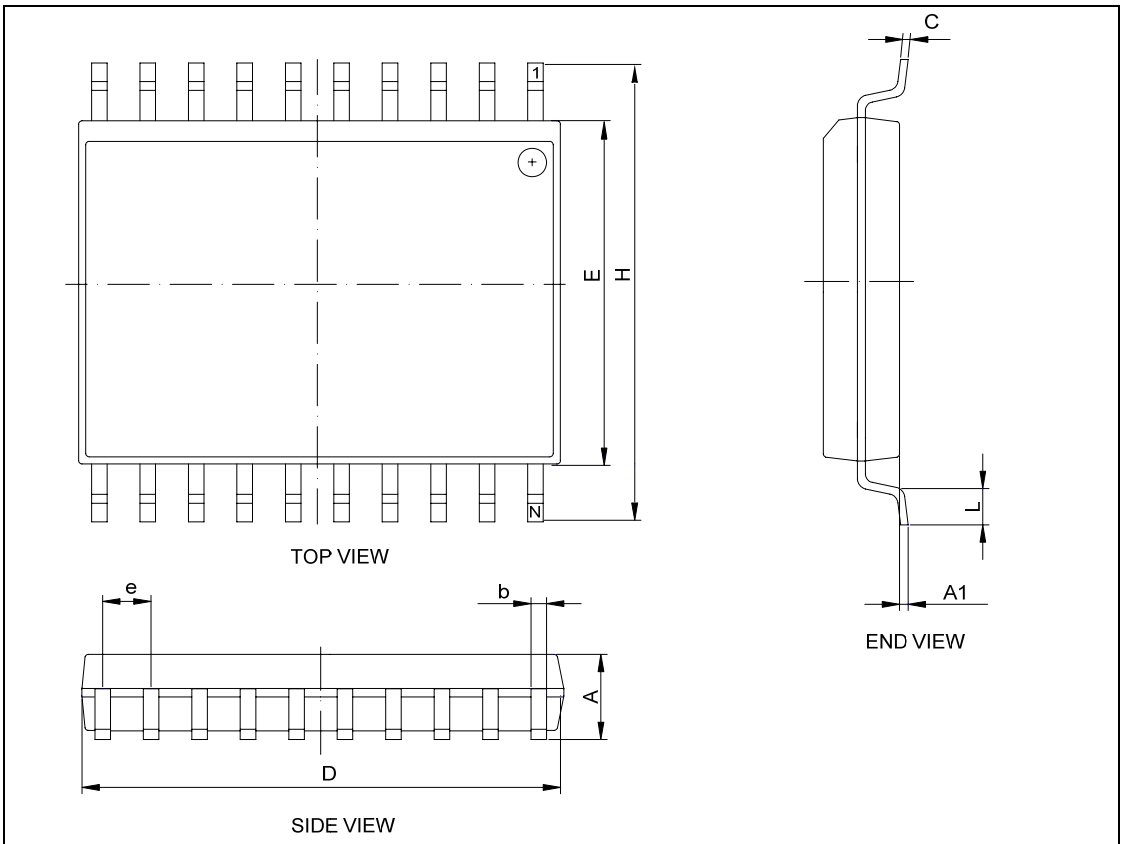
Block	QTY	Reference	Description	PCB Footprint	Manufacturer	Manufacturer's Part Number
1 port Chipset Circuitry	2	C1,C10	CAP CRM 1nF 50v 10% X7R 0603 SMT	PD-0603	EPCOS	B37931-K5102-K60
	3	C3,C8,C19	CAP CRM 100nF 16V 10% X7R 0603 SMT	PD-0603	EPCOS	B37931K9104K60
	1	C4	CAP CRM 100nF 50V 10% X7R 0805 SMT	PD-0805	Samsung	CL21B104KBAC
	1	C5	CAP CRM 3.3nF 16V 10% X7R 0603 SMT	PD-0603	TDK	C1608X7R1C332K
	1	C12	CAP CRM 100nF 100V 10% X7R 1206 SMT	PD-1206	Samsung	CL31B104KCFNNNE
	1	C14	CAP CRM 470pF 50v 10% X7R 0603 SMT	PD-0603	EPCOS	B37931-K5471-K60
	1	C15	CAP CRM 2.2uF 10V 10% X7R 0805 SMT	PD-0805	Samsung	CL21B225KPFNNNC
	1	C18	CAP CRM 22nF 25v 10% X7R 0603 SMT	PD-0603	Rohm	MCH185CN223KK
	1	C21	CAP CRM 1uF 50V 10% X7R 1206 SMT	PD-1206	TDK	C3216X7R1H105K
	2	D1,D3 (1)	DIODE 16V 1W 5% D041 Insert	DO-41	Microsemi	1N4745AP
	1	D2	DIODE SCHOT 30V 200 mA SOT23 SMT	PD-SOT23	Infineon	BAT64
	1	D5	DIODE REC 400V 1A SMA SMT	PD-SMA	Pan Jit	GS1G
	4	Q1,Q2,Q5,Q6	FET NCH 100V 0.15A 6R Logic Level SOT23	PD-SOT23	Infineon	BSS123
	1	Q4	FET NCH 100V 13A 0.12R DPAK SMT	PD-DPAK	Fairchild	FQD19N10
	1	R1	RES 15.4K 62.5 mW 1% 0603 SMT	PD-0603	Samsung	RC1608F1542CS
	3	R2,R4,R7	RES 10K 62.5 mW 1%0603 SMT	PD-0603	Rohm	MCR03EZHEFX1002
	2	R5,R6	RES 215K 0.125 W 0.5% 0805 SMT	PD-0805	Yageo	RT0805DRD07215K
	1	R8	R mode	PD-0603		
	2	R9,R11	RES 2R 0.75 W 1% 2010 SMT	PD-2010	KOA	RK73H2HTTE2R00F
	1	R12	RES 1K 62.5 mW 1%0603 SMT	PD-0603	Samsung	RC1608F1001CS
	1	R13	RES 75K 125 mW 1%0805 SMT	PD-0805	Rohm	MCR10EZHEF7502
	1	R15	RES 5.11K 62.5 mW 1%0603 SMT	PD-0603	Samsung	RC1608F5111CS
	1	R16	RES 1.24K 62.5 mW 1%0603 SMT	PD-0603	ASJ	CR16-1241FL
	2	R17,R23	RES 402K 125 mW 1%0805 SMT	PD-0805	Yageo	RC0805FRF07402K
	1	R18	RES 51.1K 62.5 mW 1%0603 SMT	PD-0603	Samsung	RC1608F5112CS
	1	R24	RES 4.87K 125 mW 1%0805 SMT	PD-0805	Samsung	RC2012F4871CS
	2	R25,R26	RES 140K 1%125 mW 0805 SMT	PD-0805	Samsung	RC2012F1403CS
	1	U1	IC VOLT REG 5V 0.1A 4% SO8 SMT	PD-SO8	ON Semi	MC78L05ABDR2G
	1	U2 (2)	IC OP AMP DUAL SO8 SMT	PD-SO8	Fairchild	KA358ADTF_NL
	1	U4	1-Port IEEE802.3at PoE PSE Manager	PD-SOW20	Microsemi	PD64001/H

1. Select these diodes as specified in "5V Regulator" section on page 4.
2. This operational amplifier should be use for applications intend for ambient temperature range of 0°C to +70°C.
   For ambient temperature range of -25°C to +85°C replace it with KA258ADTF_NL.
   For ambient temperature range of -40°C to +85°C replace it with TI's TLV342AID.

Microsemi
Analog Mixed Signal Group
2381 Morse Avenue, Irvine, CA 92614, USA; Phone (USA): (800) 713-4113, (ROW): (949) 221-7100 Fax: (949) 756-0308

Package Information

Microsemi's PD64001/H is housed in a 20-lead, 0.300" Wide, Plastic Gull Wing Small Outline Package (SOIC).



NOTES:

1. THIS DRAWING IS FOR GENERAL INFORMATION ONLY; REFER TO JEDEC DRAWING MS-013, VARIATION AC FOR ADDITIONAL INFORMATION.
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
3. DIMENSION "E" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSION. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE.
4. "L" IS THE LENGTH OF THE TERMINAL FOR SOLDERING TO A SUBSTRATE.
5. THE LEAD WIDTH "b", AS MEASURED 0.36mm OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF 0.61mm PER SIDE.

COMMON DIMENSIONS
(UNIT OF MEASURE-mm)

SIMBOL	MIN	NOM	MAX	NOTE
A	2.35		2.65	
A1	0.10		0.30	
b	0.33		0.51	4
C	0.23		0.32	
D	12.60		13.00	1
E	7.40		7.60	2
H	10.00		10.65	
L	0.40		1.27	3
e	1.27 BSC			

Microsemi
Analog Mixed Signal Group
2381 Morse Avenue, Irvine, CA 92614, USA; Phone (USA): (800) 713-4113, (ROW): (949) 221-7100 Fax: (949) 756-0308

Revision History

Revision Level / Date	Para. Affected	Description
1.0 / 26 July. 08	-	Initial Release
1.1 / 23 Feb. 09	-	Temperature range update.
1.2 / May 23. 09	-	Added PD64001H P/N
1.3 / Aug 11. 09		Formatting, Englsih

For support contact: customer.care_AMSG@microsemi.com

Visit our web site at: http://www.microsemi.com/PowerDsine/Support/

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