



PCA9522

Fast dual bidirectional bus buffer with hot insertion logic

Rev. 1 — 28 September 2011

Product data sheet

1. General description

The PCA9522 is a monolithic bipolar integrated circuit for bus buffering in applications including I²C-bus, SMBus, etc. It includes hot insertion logic for detecting stop and idle conditions, making it ideal for live insertion into backplanes. The buffer extends the bus load limit by buffering both the SCL and SDA lines. The PCA9522 is a drop-in replacement for the IES5502, with only the maximum bus voltage reduced from 15 V to 10 V.

Hot insertion logic allows the IC to be plugged into live backplanes without causing data corruption on the bus. The open-collector ready signal (RDY) indicates when the connection has been made. Precharging of the backplane ports minimizes disruptions to the bus during hot insertion.

The enable function allows sections of the bus to be isolated. Individual parts of the system can be brought on-line successively. Bus level translation between a very wide range of bus voltages, from 1.8 V to 10 V, is supported. These features provide enormous flexibility in interfacing systems of different technologies, operating speeds and loads.

The unique operation of the PCA9522 provides one of the fastest response times of such bidirectional buffers. It does this without the need for rise-time accelerators which, combined with low noise margins, may cause glitches outside of the I²C-bus specification.

2. Features and benefits

- Dual, bidirectional unity gain isolating buffer
- Hot insertion logic prevents data and clock bus corruption for live backplane applications
- Pre-charge minimizes data corruption on live insertion
- Supports I²C-bus (Standard-mode and Fast-mode), SMBus (standard and high power modes) and PMBus
- Open-collector ready output (RDY)
- Fast switching times allow operation in excess of 1 MHz
- Enable (EN) allows bus segments to be disconnected
- Low current standby mode when not enabled
- High-impedance ports when IC unpowered
- 6 mA (static) pull-down capability
- Low noise susceptibility
- Supports the connection of several buffers in series
- Level shift bus voltages from 1.8 V to 10 V



3. Applications

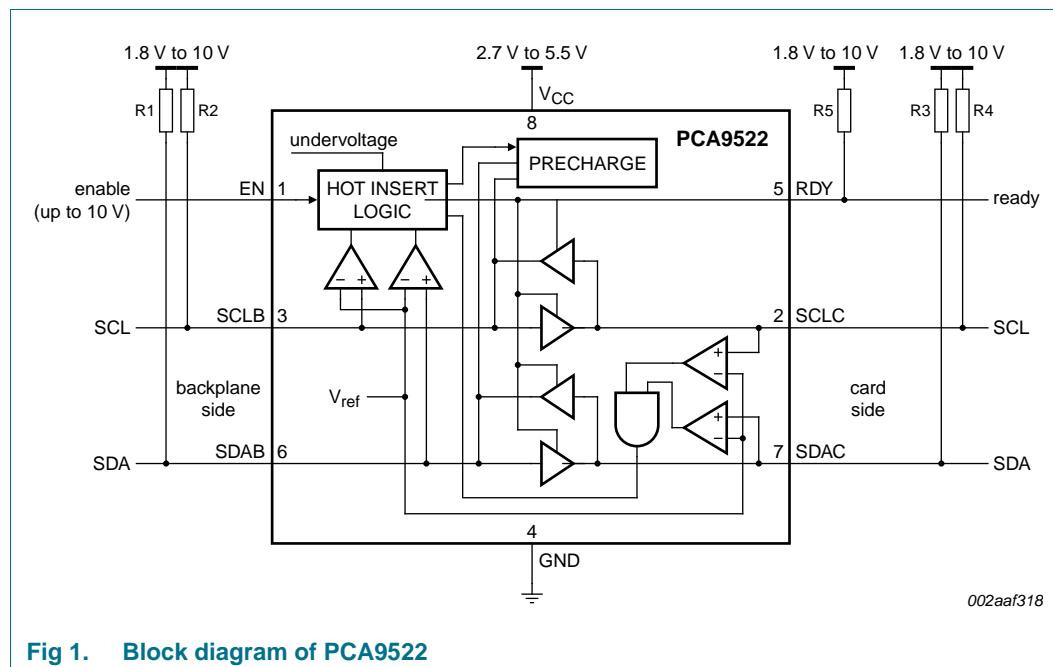
- Backplane management/interconnect
- Telecommunications systems including ATCA
- Desktop and portable computers including RAID

4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		Version
		Name	Description	
PCA9522D	PCA9522	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
PCA9522DP	9522	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1

5. Block diagram



6. Pinning information

6.1 Pinning



6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
EN	1	enable
SCLC	2	SCL buffer, card side ^[1]
SCLB	3	SCL buffer, backplane side ^[2]
GND	4	supply ground
RDY	5	ready
SDAB	6	SDA buffer, backplane side ^[2]
SDAC	7	SDA buffer, card side ^[1]
V _{CC}	8	positive supply

[1] Card side is equivalent to SCL_OUT / SDA_OUT.

[2] Backplane side is equivalent to SCL_IN / SDA_IN.

7. Functional description

Refer to [Figure 1 “Block diagram of PCA9522”](#).

7.1 V_{CC} , GND — supply pins

The PCA9522 can be driven from voltage supplies ranging from 2.7 V to 5.5 V. The threshold level below which the output will begin to match the input is 33 % of V_{CC} . Hence, the operating voltage should be chosen with the required bus voltage, switching threshold, and noise margins in mind.

7.2 SCLB, SCLC, SDAB, SDAC — buffer inputs/outputs

The two open-collector buffers (SCL and SDA) are identical and symmetrical. The buffers can be driven from either direction, with the same buffering response. However, the hot insertion logic is determined from the ‘backplane’ (SxxB) sides of the buffers. When the one side (e.g., SxxB) of the buffer is being driven LOW ($<0.3V_{CC}$) by another device on the bus, the other side (e.g., SxxC) will be driven LOW by the IC to provide the buffered output.

The ‘control’ or ‘input’ side is determined by the lowest externally driven signal. Therefore if the ‘input’ is externally pulled to $V_{SxxB} = 250$ mV, and the ‘output’ is externally pulled to $V_{SxxC} = 500$ mV, the buffer will pull the ‘output’ down further such that it becomes $V_{SxxC} = V_{SxxB} + V_{offset}$. Should the ‘output’ subsequently become lower than the ‘input’ by means of an external device pulling it LOW ($V_{SxxC} < V_{SxxB}$), control of the buffering operation will switch sides. The voltage at the ‘input’ will then become $V_{SxxB} = V_{SxxC} + V_{offset}$. Many bus buffers are prone to causing glitches during control transition, but the PCA9522 shows negligible glitching even under the worst operating conditions.

7.3 Enable (EN) — activate buffer operations

The enable input (EN) is used to disable the buffer, for the purpose of isolating sections of the bus. The IC should only be disabled when the bus is idle, to prevent truncation of commands which may confuse other devices on the bus.

Upon receiving a valid enable (EN) signal, the IC will wait to detect either a bus STOP condition, or an IDLE condition as described in the I²C-bus [[Ref. 1](#)] and SMBus [[Ref. 2](#)] specifications. This ensures that truncated transmissions are not communicated along the newly enabled bus segment.

Enable may be used to progressively activate sections of the bus during system start-up. Bus sections slow to respond on power-up can be kept isolated from the main system to avoid interference and collisions.

The EN pin may be pulled up higher than the V_{CC} of the buffer, further enhancing the capability of the PCA9522 in a level shifting role. For example, a microprocessor could drive EN, SCLB and SDAB at 5 V, while the buffer V_{CC} , SCLC and SDAC ports are at 3.3 V.

Similarly, the threshold level of the EN pin allows a 1.8 V device to enable an PCA9522 with a V_{CC} of 3.3 V.

7.4 Ready (RDY) — buffer connected indicator

The ready output (RDY) indicates that the buffer has met its enable conditions, and that communication will now occur. This is an open-collector transistor which is switched off when ready, allowing the voltage at the pin to be pulled HIGH by a pull-up resistor.

7.5 Start-up

During power-up or live insertion into backplanes, the PCA9522 will start-up in an UnderVoltage LockOut (UVLO) state where any activity on the input/output ports will be ignored. This is to ensure that the PCA9522 does not try to operate when there is not enough voltage on the supply.

During this time, the precharge circuit will charge all SCLB/SDAB backplane ports to typically 0.92 V. This will minimize any voltage difference between the ports and hence minimizes disruptions to the bus during hot insertion into backplanes.

When the supply increases above the UVLO state the PCA9522 will then monitor the bus for either stop bit or bus idle condition. When a stop bit condition is detected and SCLC/SDAC are both idle or when all SCL/SDA ports idle for a time period of typically 95 μ s, then the PCA9522 will activate the input-output connection circuitry. The precharge circuitry is switched off. The voltage at the RDY pin is pulled HIGH by an external pull-up resistor to indicate the input/output connection has been made.

8. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		[1] -0.3	+7	V
V_n	voltage on any other pin	SCLB, SCLC, SDAB, SDAC	[1] -0.3	+12	V
$V_{I(EN)}$	input voltage on pin EN		[1] -0.3	+12	V
I_{IO}	input/output current	DC; any pin	-	20	mA
P_{tot}	total power dissipation		-	300	mW
T_{stg}	storage temperature		-55	+125	°C
T_{amb}	ambient temperature	operating	-40	+85	°C

[1] Voltages are specified with respect to pin 4 (GND).

9. Characteristics

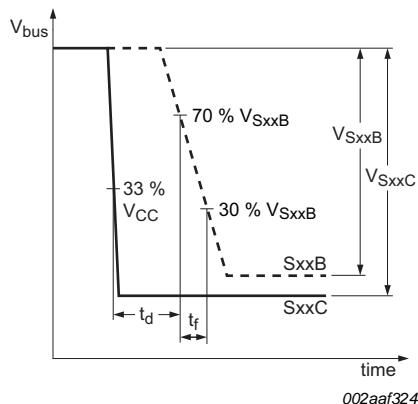
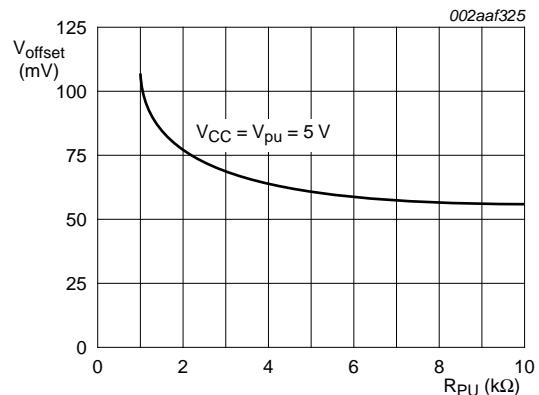
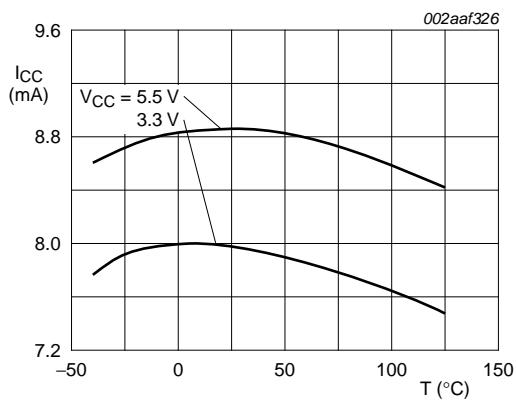
Table 4. Characteristics

$T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$; voltages are specified with respect to ground (GND).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power supply						
V_{CC}	supply voltage	operating	2.7	-	5.5	V
I_{CC}	supply current	operating; $V_{CC} = V_{I(EN)} = 5.5\text{ V}$	-	9	-	mA
Start-up circuitry						
$V_{th(UVLO)}$	undervoltage lockout threshold voltage	$V_{CC} = V_{I(EN)} = 5.5\text{ V}$	-	2.2	-	V
V_{pch}	precharge voltage	V_{SxxB} floating; $V_{CC} = 3.3\text{ V}$; $V_{i(EN)} > 1.2\text{ V}$	-	0.92	-	V
I_{pch}	precharge current	V_{SxxB} floating; $V_{CC} = 3.3\text{ V}$; $V_{i(EN)} > 1.2\text{ V}$	-	11	-	μA
V_{th}	threshold voltage	logic input	-	$0.5V_{CC}$	-	V
Buffer ports (SCLB, SCLC, SDAB, SDAC)						
V_{bus}	bus voltage		-	-	10	V
$V_{th(IL)}$	LOW-level input threshold voltage		-	-	$0.3V_{CC}$	V
$V_{th(IH)}$	HIGH-level input threshold voltage		$0.41V_{CC}$	-	-	V
I_{IL}	LOW-level input current	drive current; $V_{bus} < V_{CC}$	-	-10	-20	μA
$I_{O(sink)}$	output sink current	LOW-level; $V_{bus(out)} = 0.4\text{ V}$	6	-	-	mA
V_{offset}	offset voltage	input/output; $V_{CC} = 3.3\text{ V}$				
I_L	leakage current	$V_{bus} = V_{CC}$	-	-	5	μA
Enable (EN)						
V_{en}	enable voltage	active	1.2	-	-	V
V_{dis}	disable voltage	standby	-	-	0.7	V
I_I	input current	$V_{en} > 1.2\text{ V}$	1	-	5	μA
Ready (RDY)						
$V_{OL(RDY)}$	LOW-level output voltage on pin RDY	$I_{pu} = 3\text{ mA}$	-	-	400	mV
I_L	leakage current	$V_{OL(RDY)} = V_{CC}$	-	-	± 5	μA
Timing characteristics^[1]						
t_d	delay time	$V_{CC} = 5\text{ V}$; $V_{bus} = 5\text{ V}$; $R_{pu(bus)} = 1\text{ k}\Omega$; $C_{L(ext)} = 120\text{ pF}$; Figure 4	-	30	-	ns
t_f	fall time	$V_{CC} = 5\text{ V}$; $V_{bus} = 5\text{ V}$; $R_{pu(bus)} = 1\text{ k}\Omega$; $C_{L(ext)} = 120\text{ pF}$; Figure 4	-	15	-	ns
f_{oper}	operating frequency		0	400	-	kHz

Table 4. Characteristics ...continued $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$; voltages are specified with respect to ground (GND).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{idle}	idle time	$V_{bus} = V_{I(EN)} = V_{CC} = 3.3\text{ V}$	50	95	150	μs
		$V_{bus} = V_{I(EN)} = V_{CC} = 5.5\text{ V}$	50	75	120	μs
$t_{d(ENH-RDYoff)}$	delay time from EN HIGH to RDY off		-	95	-	μs
$t_{d(ENL-RDYon)}$	delay time from EN LOW to RDY on		-	1.1	-	μs
$t_{d(RDYH-I2Con)}$	delay time from RDY HIGH to I ² C on		-	1	-	μs
$t_{d(RDYL-I2Coff)}$	delay time from RDY LOW to I ² C off		-	-0.5	-	μs

[1] Guaranteed by design (not subject to test), except for t_{idle} at $V_{CC} = 3.3\text{ V}$.**Fig 4. Timing parameters****Fig 5. Offset voltage, $V_O - V_I$** **Fig 6. Supply current versus temperature**

10. Application information

10.1 Design considerations

[Figure 7](#) shows a typical application for the PCA9522. The IC can level shift between various bus voltages, without the need for additional external components. Higher bus voltages and currents outside the range of the standard I²C-bus specification can be catered for, providing a longer range capability and higher noise immunity.

The enable pin (EN) can be used to interface buses of different operating frequencies. When enabled, the bus frequency is limited to the maximum 100 kHz of the slave device. When disabled, the slave is isolated, and the remaining bus can be run at 400 kHz. The timing performance and current sinking capability will allow it to run well in excess of the 400 kHz maximum limit of the Fast-mode I²C-bus.

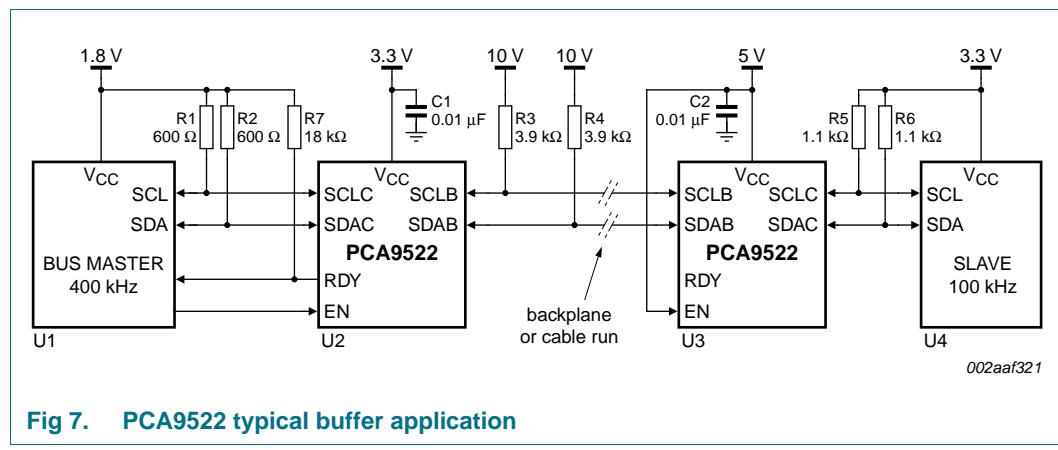


Fig 7. PCA9522 typical buffer application

[Figure 8](#) shows the PCA9522 used in a backplane application. Peripheral cards and backplanes operating at a range of voltages can be interfaced together using a minimum of components. In this example, cards are running at 1.8 V and 3.3 V, while the backplane is at 5 V. Cards operating buses between 1.8 V and 10 V can be catered for in the same system.

Each card can be safely isolated from the system by disabling the PCA9522 at the interface to the backplane. The hot insertion logic on the PCA9522 protects against corrupted or truncated data transmissions on start-up of buffer operations.

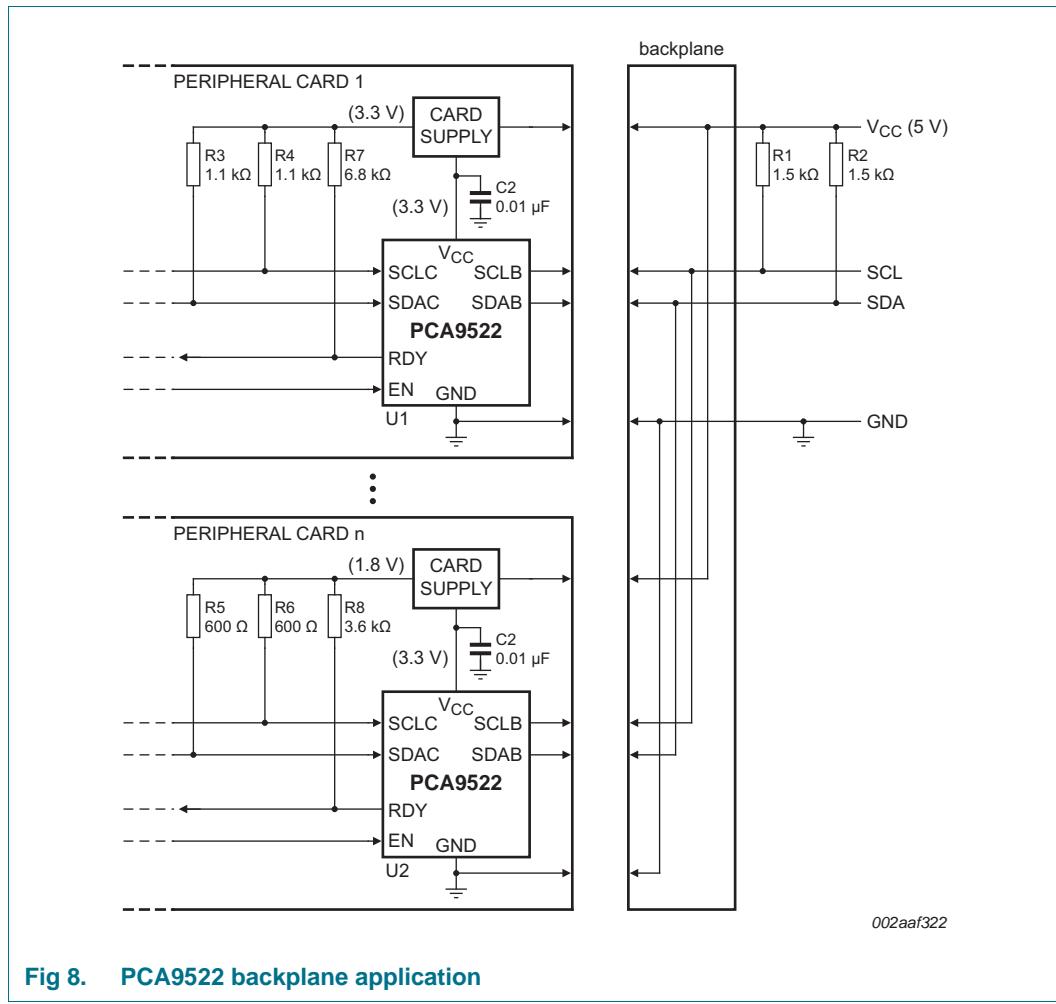
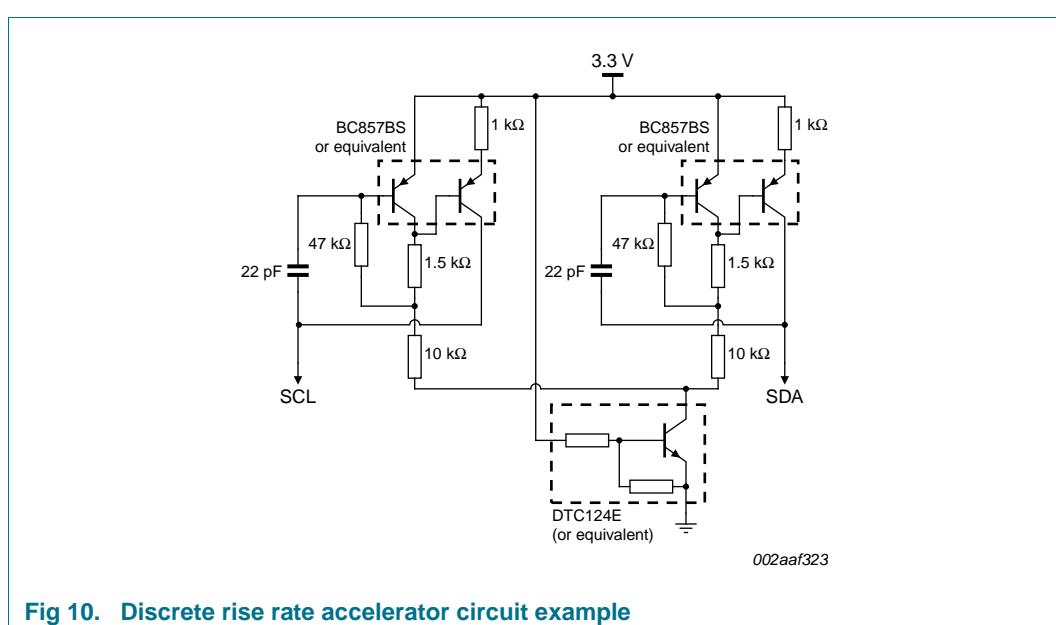
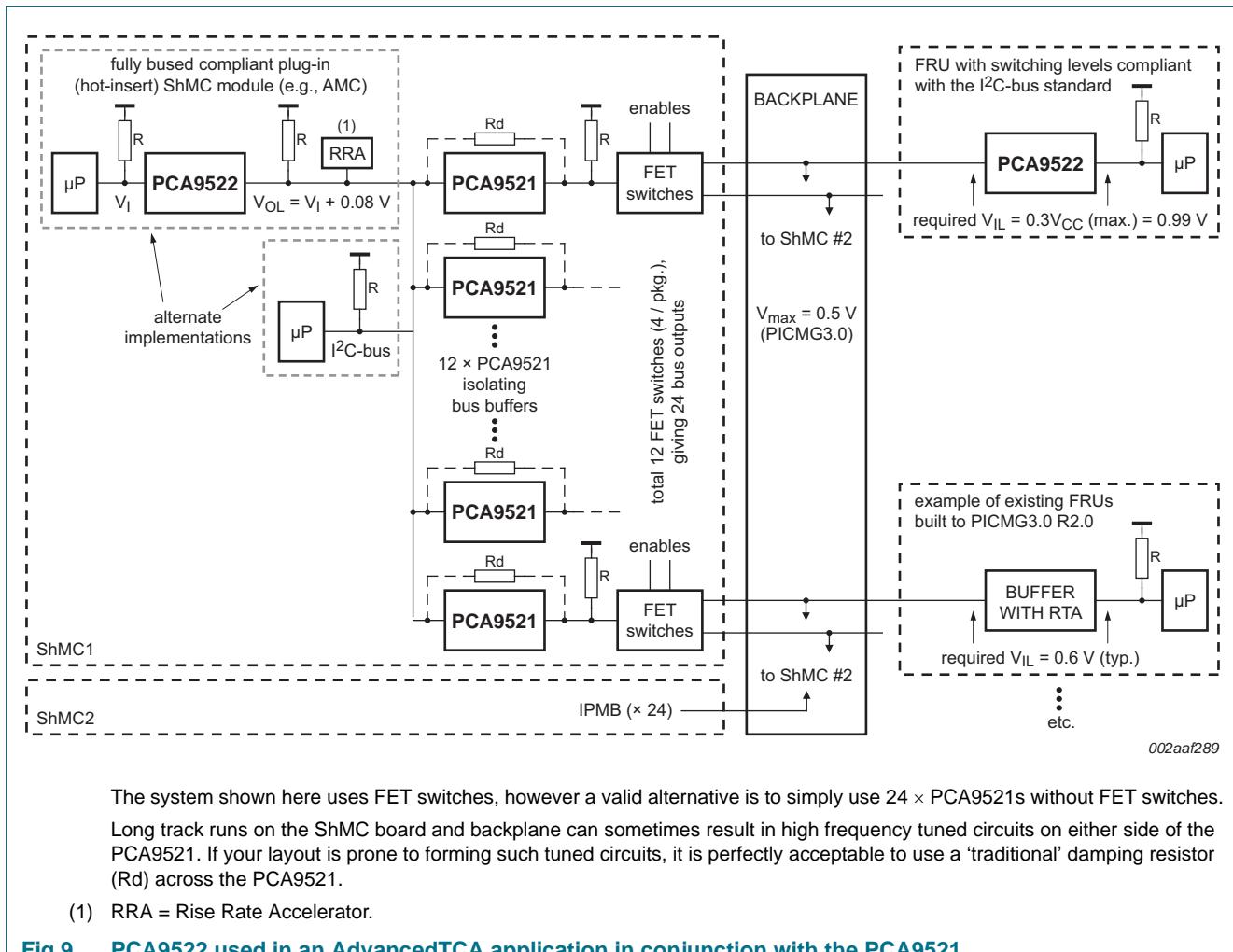


Fig 8. PCA9522 backplane application

An ideal backplane application for the PCA9522 is the Advanced Telecom Computing Architecture (AdvancedTCA) as shown in [Figure 9](#). The PCA9522 is well-suited to placement on 'Field Replaceable Units' (FRUs) used in either a conventional fully-bussed arrangement (not shown) or in the low cost, high noise margin radial architecture example as shown in [Figure 10](#). It is fully interoperable with existing systems and components. If required, [Figure 10](#) shows a simple low-cost circuit for use at the Shelf Manager for accelerating the rise in bussed systems.

In each of these examples, the buffers are intended to extend total system capacitance above 400 pF, so anticipate high capacitance on each side. When loading on one side is small, adding 47 pF is suggested to avoid any waveform ripple, should it occur.



10.2 Input to output offset voltage calculation

The offset voltage between the side acting as the output (Sxxx(out)) and the side acting as the input (Sxxx(in)) of the PCA9522 can be calculated using the relationship given in [Equation 1](#):

$$V_{offset} = V_i + 50 \text{ mV} + \left(\frac{V_{BUS}}{R} \right) \times 11 \quad (1)$$

This calculation is valid for $V_{Sxxx(in)} \geq 200 \text{ mV}$, as below this point the saturation voltage of the open-collector output drive transistor will begin to affect the characteristic. Input and output voltages are shown in millivolts, V_{BUS} (the supply voltage to the bus) is in volts, and R is in ohms.

An example calculation for $V_{BUS} = 3.3 \text{ V}$, $V_{SxxC} = 200 \text{ mV}$, the resistance R pulling up SxxB is $2 \text{ k}\Omega$, then the voltage on SxxB is typically:

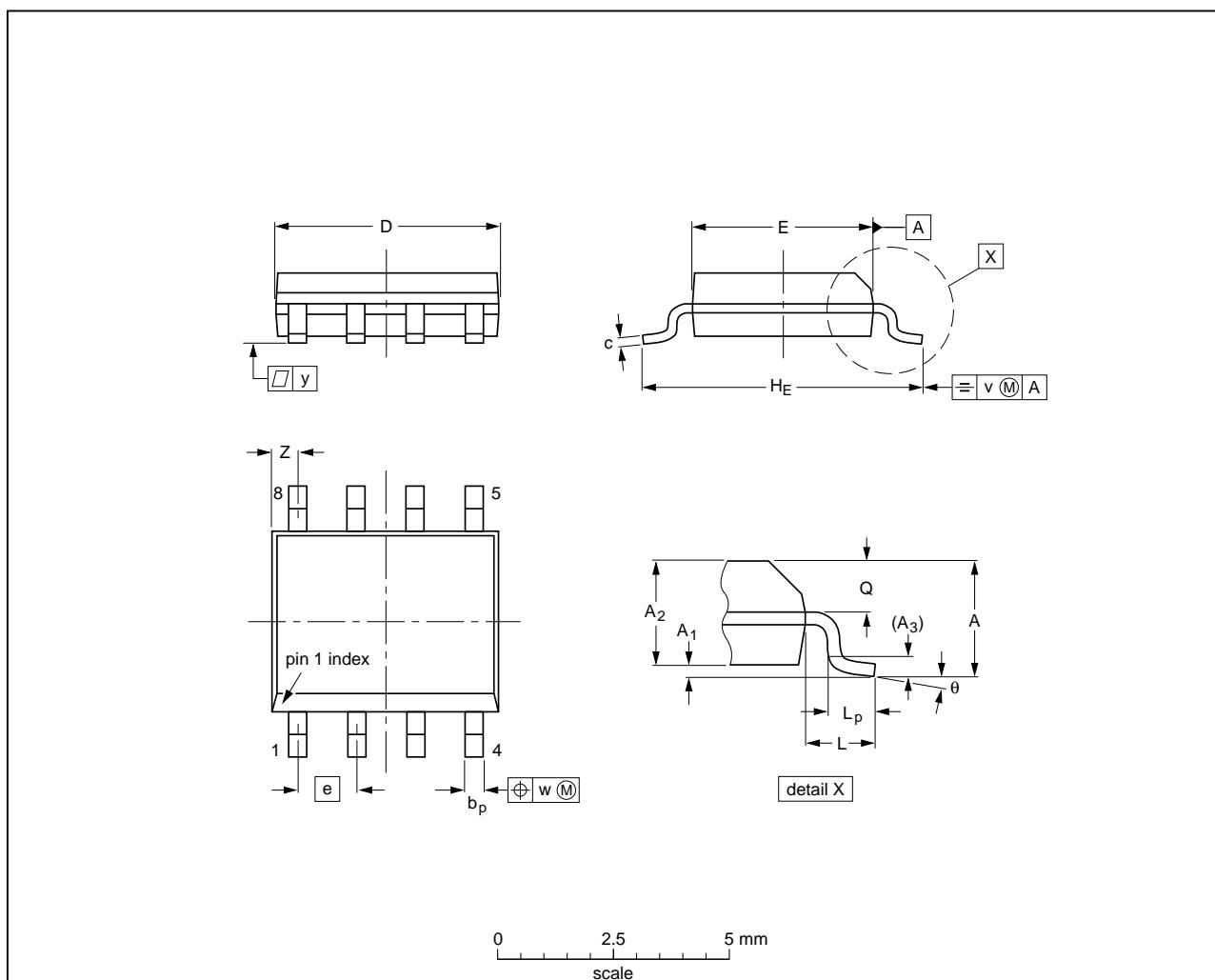
$$V_{SxxB} = 200 \text{ mV} + 50 \text{ mV} + \left(\frac{3.3}{2000} \right) \times 11 = 268 \text{ mV} \quad (2)$$

This can be compared with the offset characteristic shown in [Figure 5](#).

11. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75 0.10	0.25 1.45 0.36	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069 0.004	0.010 0.049	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

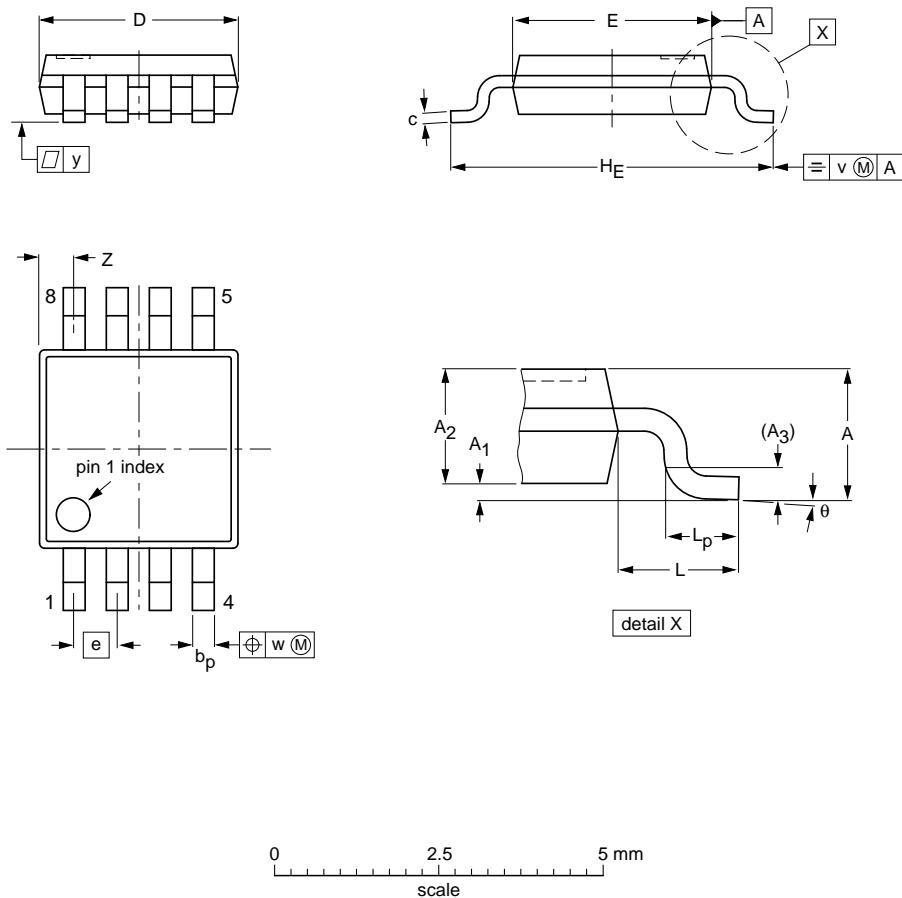
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT96-1	076E03	MS-012			99-12-27 03-02-18

Fig 11. Package outline SOT96-1 (SO8)

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm

SOT505-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	v	w	y	z ⁽¹⁾	θ
mm	1.1 0.05	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						-99-04-09- 03-02-18

Fig 12. Package outline SOT505-1 (TSSOP8)

12. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards.

13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 13](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 5](#) and [6](#)

Table 5. SnPb eutectic process (from J-STD-020C)

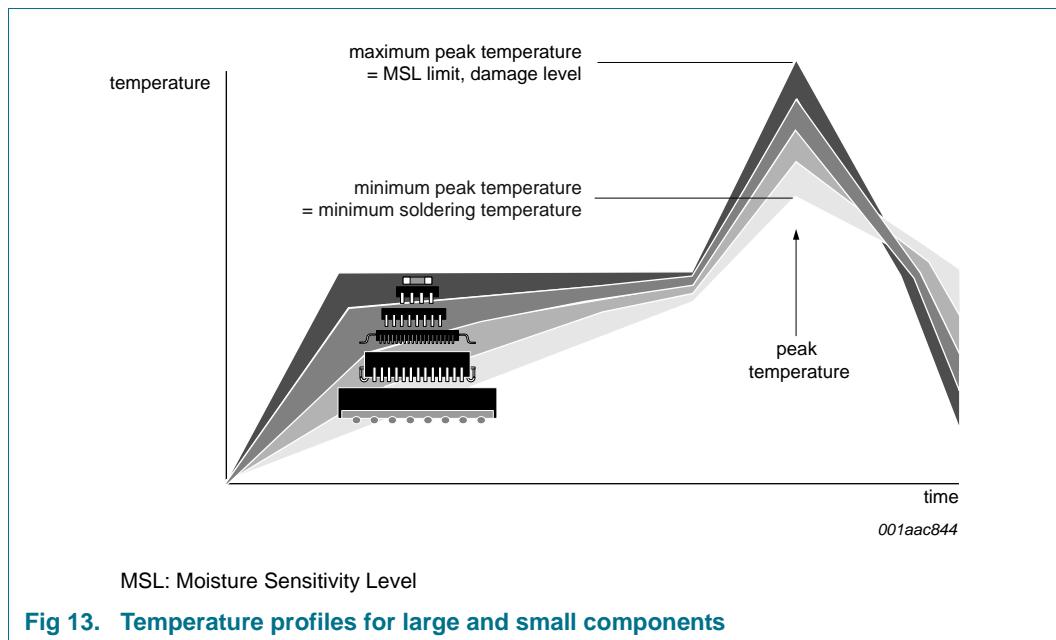
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm ³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 6. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm ³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 13](#).



For further information on temperature profiles, refer to Application Note AN10365 "Surface mount reflow soldering description".

14. Abbreviations

Table 7. Abbreviations

Acronym	Description
AMC	Advanced Mezzanine Cards
ATCA	Advanced Telecommunications Computing Architecture
ESD	ElectroStatic Discharge
FRU	Field Replaceable Unit
I ² C-bus	Inter-Integrated Circuit bus
IC	Integrated Circuit
IPMB	Intelligent Platform Management Bus
PICMG	PCI Industrial Computer Manufacturers Group
PMBus	Power Management Bus
RAID	Redundant Array of Independent Discs
RTA	Rise Time Accelerator
ShMC	Shelf Management Controller
SMBus	System Management Bus

15. References

- [1] **UM10204, I²C-bus specification and user manual** — , Rev 03, 19 June 2007; NXP B.V. www.nxp.com/documents/user_manual/UM10204.pdf
- [2] **System Management Bus (SMBus) Specification** — Version 2.0, August 3, 2000; SBS Implementers Forum.

16. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9522 v.1	20110928	Product data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

17.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

17.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's

own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

17.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I²C-bus — logo is a trademark of NXP B.V.

18. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

19. Contents

1	General description	1
2	Features and benefits	1
3	Applications	2
4	Ordering information	2
5	Block diagram	2
6	Pinning information	3
6.1	Pinning	3
6.2	Pin description	3
7	Functional description	4
7.1	V _{CC} , GND — supply pins	4
7.2	SCLB, SCLC, SDAB, SDAC — buffer inputs/outputs	4
7.3	Enable (EN) — activate buffer operations	4
7.4	Ready (RDY) — buffer connected indicator	5
7.5	Start-up	5
8	Limiting values	5
9	Characteristics	6
10	Application information	8
10.1	Design considerations	8
10.2	Input to output offset voltage calculation	11
11	Package outline	12
12	Handling information	14
13	Soldering of SMD packages	14
13.1	Introduction to soldering	14
13.2	Wave and reflow soldering	14
13.3	Wave soldering	15
13.4	Reflow soldering	15
14	Abbreviations	16
15	References	17
16	Revision history	17
17	Legal information	18
17.1	Data sheet status	18
17.2	Definitions	18
17.3	Disclaimers	18
17.4	Trademarks	19
18	Contact information	19
19	Contents	20

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[NXP:](#)

[PCA9522D,118](#)