

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74HC4049AFN TC74HC4050AFN

TC74HC4049AFN

Hex Buffer/Converter (inverting)

TC74HC4050AFN

Hex
Buffer/Converter

Note: xxxFN (JEDEC SOP) is not available in Japan.

The TC74HC4049A and TC74HC4050A are high speed CMOS HEX BUFFERS fabricated with silicon gate C²MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC4049A is an inverting buffer, while the TC74HC4050A is a non-inverting buffer. The internal circuits are composed of 3-stages (HC4049A) or 2-stages (HC4050A) of inverters, which provided high noise immunity and stable output.

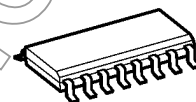
Input protection circuits are different from those of other high speed CMOS IC's. They eliminate the diodes on the VCC side thus providing of logic-level conversion from high-level volages up to 15 V to low-level volages.

They are useful for battery back up circuits, because input voltage can be applied on IC's which are not biased by VCC.

Features

- High speed: $t_{pd} = 9 \text{ ns (typ.)}$ at $V_{CC} = 5 \text{ V}$
- Low power dissipation: $I_{CC} = 1 \mu\text{A (max.)}$ at $T_a = 25^\circ\text{C}$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (min.)}$
- Output Drive Capability: 15 LSTTL loads
- Symmetrical output impedance: $|I_{OH}| = I_{OL} = 6 \text{ mA (min.)}$
- Balanced propagation delays: $t_{PLH} \approx t_{PHL}$
- Wide operating voltage range: $V_{CC \text{ (opr)}} = 2 \text{ V to } 6 \text{ V}$
- Pin and function compatible with 4049B/4050B

TC74HC4049AFN, TC74HC4050AFN

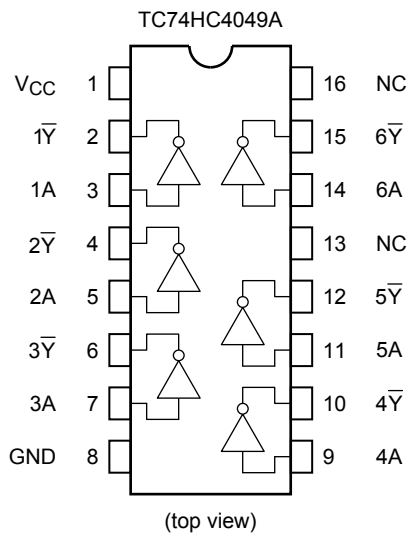


SOL16-P-150-1.27

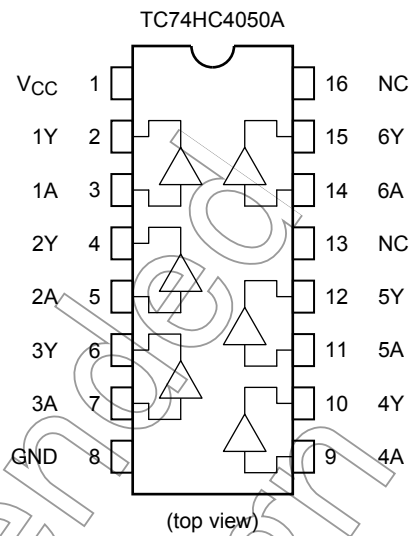
Weight

SOL16-P-150-1.27 : 0.13 g (typ.)

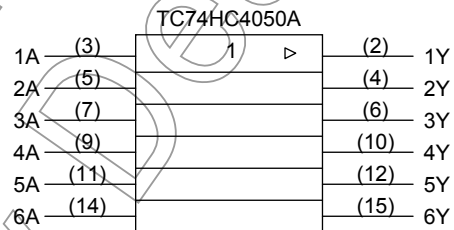
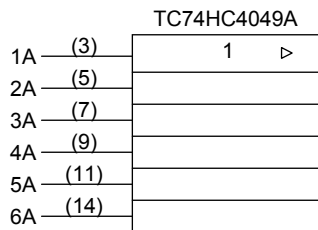
Pin Assignment



NC: No connection



IEC Logic Symbol

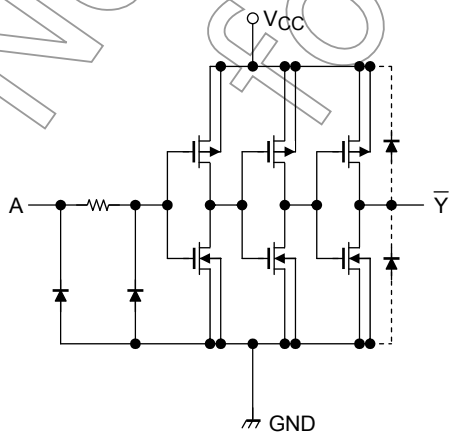


Truth Table

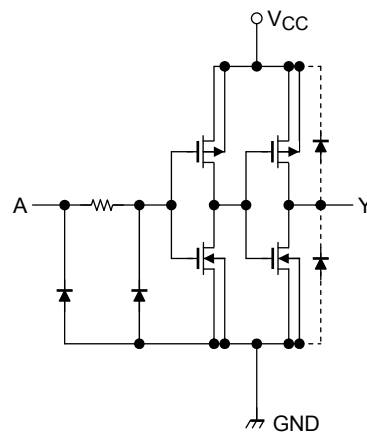
A	\bar{Y} (4049A)	Y (4050A)
L	H	L
H	L	H

Input and Output Equivalent Circuit

TC74HC4049A



TC74HC4050A



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7	V
DC input voltage	V_{IN}	-0.5 to 18 (Note 2)	V
DC output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}	-20	mA
Output diode current	I_{OK}	±20	mA
DC output current	I_{OUT}	±35	mA
DC V_{CC} /ground current	I_{CC}	±75	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 2: DC input voltage (V_{IN}) specified is measured to GND and is not related to V_{CC} .

Recommended operating range is 0 V to 15 V and it is possible to convert logic-levels from 15 V to 5 V or 5 V to 2 V.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2 to 6	V
Input voltage	V_{IN}	0 to 15	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	°C
Input rise and fall time	t_r, t_f	0 to 1000 ($V_{CC} = 2.0$ V) 0 to 500 ($V_{CC} = 4.5$ V) 0 to 400 ($V_{CC} = 6.0$ V)	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit
				V _{CC} (V)	Min	Typ.	Max	Min	Max
High-level input voltage	V _{IH}	—	—	2.0	1.50	—	—	1.50	—
				4.5	3.15	—	—	3.15	—
				6.0	4.20	—	—	4.20	—
Low-level input voltage	V _{IL}	—	—	2.0	—	—	0.50	—	0.50
				4.5	—	—	1.35	—	1.35
				6.0	—	—	1.80	—	1.80
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20 µA	2.0	1.9	2.0	—	1.9	—
				4.5	4.4	4.5	—	4.4	—
				6.0	5.9	6.0	—	5.9	—
			I _{OH} = -6 mA	4.5	4.18	4.31	—	4.13	—
			I _{OH} = -7.8 mA	6.0	5.68	5.80	—	5.63	—
			—	—	—	—	—	—	—
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20 µA	2.0	—	0.0	0.1	—	0.1
				4.5	—	0.0	0.1	—	0.1
				6.0	—	0.0	0.1	—	0.1
			I _{OL} = 6 mA	4.5	—	0.17	0.26	—	0.33
			I _{OL} = 7.8 mA	6.0	—	0.18	0.26	—	0.33
			—	—	—	—	—	—	—
Input leakage current	I _{IN}	V _{IN} = V _{CC} or GND	6.0	—	—	±0.1	—	±1.0	µA
		V _{IN} = 15 V	6.0	—	—	±0.5	—	±5.0	µA
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND	6.0	—	—	1.0	—	10.0	µA

AC Characteristics (input: t_r = t_f = 6 ns)

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = −40 to 85°C		Unit
		CL (pF)	VCC (V)	Min	Typ.	Max	Min	Max	
Output transition time	tLH	50	2.0	—	25	60	—	75	ns
	tTHL		4.5	—	6	12	—	15	
			6.0	—	5	10	—	13	
Propagation delay time	tPLH tPHL	50	2.0	—	30	75	—	95	ns
			4.5	—	9	15	—	19	
			6.0	—	8	13	—	16	
		150	2.0	—	45	100	—	145	
			4.5	—	14	20	—	29	
			6.0	—	12	17	—	25	
Input capacitance	CIN	—		—	5	10	—	10	pF
Power dissipation capacitance	CPD	(Note)		—	26	—	—	—	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

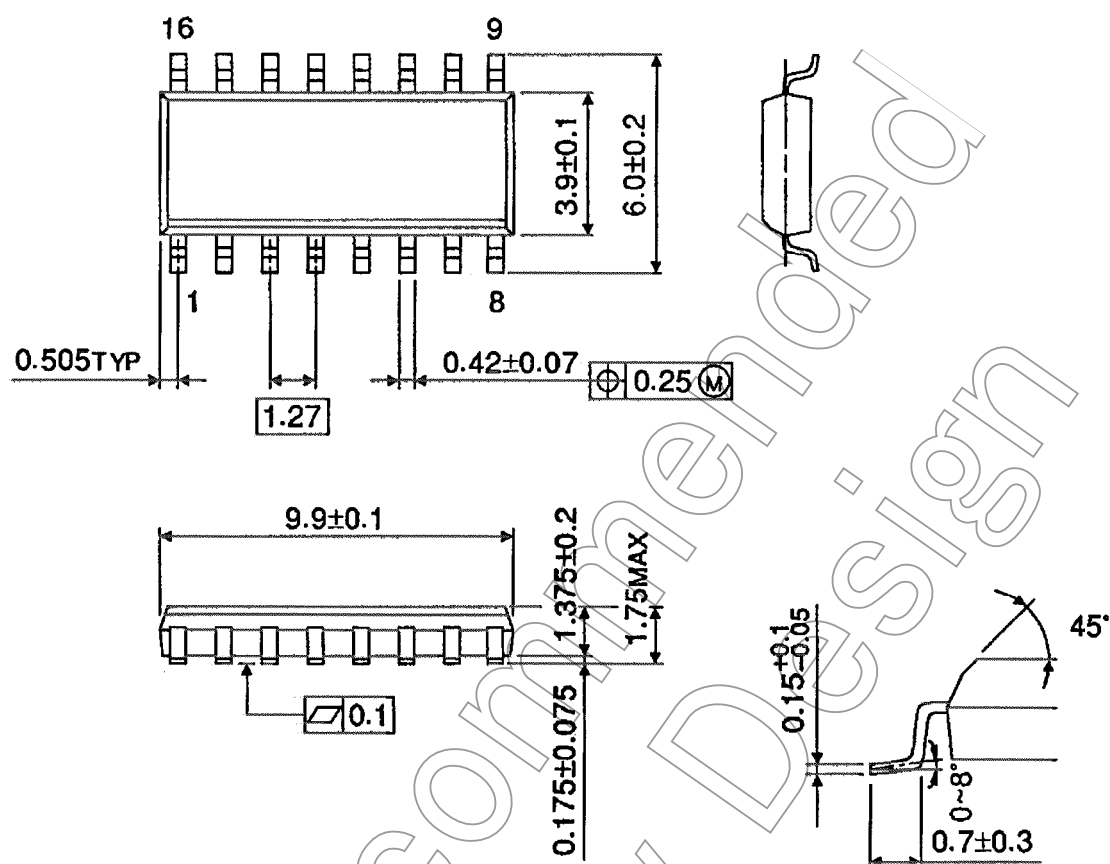
Average operating current can be obtained by the equation:

$$I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{ (per gate)}$$

Package Dimensions (Note)

SOL16-P-150-1.27

Unit : mm



Note: This package is not available in Japan.

Weight: 0.13 g (typ.)

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