DS34C87T CMOS Quad TRI-STATE Differential Line Driver

Check for Samples: DS34C87T

FEATURES

- **TTL Input Compatible**
- **Typical Propagation Delays: 6 ns**
- **Typical Output Skew: 0.5 ns**
- **Outputs Won't Load Line When V_{CC} = 0V**
- **Meets the Requirements of EIA Standard RS-422**
- **Operation from Single 5V Supply**
- **TRI-STATE Outputs for Connection to System Buses**
- **Low Quiescent Current**
- **Available in Surface Mount**

DESCRIPTION

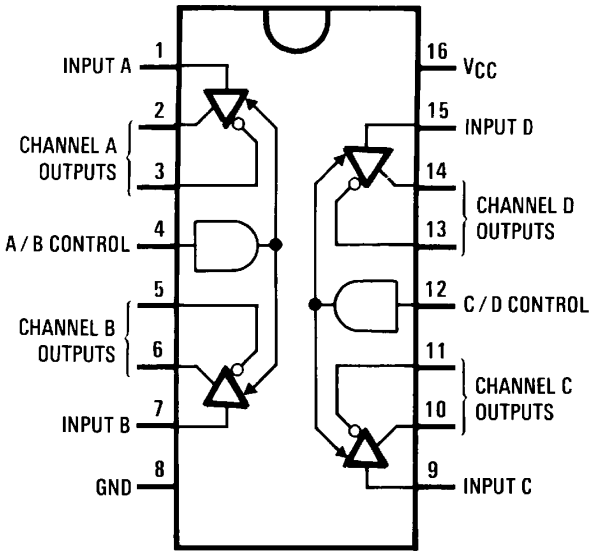
The DS34C87T is a quad differential line driver designed for digital data transmission over balanced lines. The DS34C87T meets all the requirements of EIA standard RS-422 while retaining the low power characteristics of CMOS. This enables the construction of serial and terminal interfaces while maintaining minimal power consumption.

The DS34C87T accepts TTL or CMOS input levels and translates these to RS-422 output levels. This part uses special output circuitry that enables the individual drivers to power down without loading down the bus. This device has separate enable circuitry for each pair of the four drivers. The DS34C87T is pin compatible to the DS3487T.

All inputs are protected against damage due to electrostatic discharge by diodes to V_{CC} and ground.

Connection and Logic Diagrams

Top View



See PIN DESCRIPTIONS for details.

Figure 1. PDIP Package
See Package Numbers D0016A or NFG0016E

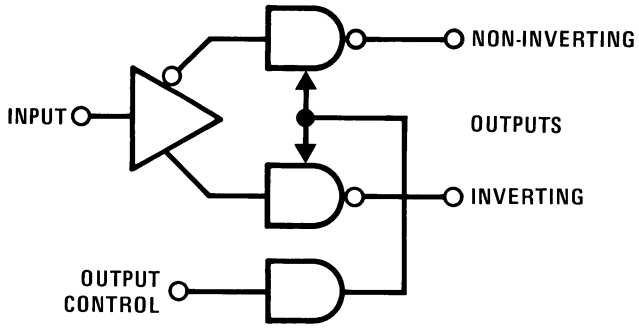


Figure 2. Logic Diagram

Truth Table(1)

Input	Control	Non-Inverting	Inverting
	Input	Output	Output
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) L = Low logic state
H = High logic state
X = Irrelevant
Z = TRI-STATE (high performance)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)(3)(4)

Supply Voltage (V_{CC})	−0.5 to 7.0V
DC Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to 7V
Clamp Diode Current (I_{IK} , I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±150 mA
DC V_{CC} or GND Current (I_{CC})	±150 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Maximum Power Dissipation (P_D) @ 25°C(5)	
PDIP Package	1736 mW
SOIC Package	1226 mW
Lead Temperature (T_L)	
(Soldering 4 sec)	260°C
This device does not meet 2000V ESD rating.(6)	

(1) Unless otherwise specified, all voltages are referenced to ground. All currents into device pins are positive; all currents out of device pins are negative.
(2) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be specified. They are not meant to imply that the device should be operated at these limits. The table of “Electrical Characteristics” provide conditions for actual device operation.
(3) ESD Rating: HBM (1.5 kΩ, 100 pF) Inputs ≥ 1500V Outputs ≥ 1000V EIAJ (0Ω, 200 pF) All Pins ≥ 350V
(4) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(5) Ratings apply to ambient temperature at 25°C. Above this temperature derate NFG0016E Package 13.89 mW/°C, and D0016A Package 9.80 mW/°C.
(6) ESD Rating: HBM (1.5 kΩ, 100 pF) Inputs ≥ 1500V Outputs ≥ 1000V EIAJ (0Ω, 200 pF) All Pins ≥ 350V

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.50	5.50	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A) DS34C87T	−40	+85	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics[1]

V_{CC} = 5V ±10% (unless otherwise specified)

Parameter		Test Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2.0			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{OH}	High Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}, $I_{OUT} = -20$ mA		2.5	3.4		V
V_{OL}	Low Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}, $I_{OUT} = 48$ mA			0.3	0.5	V
V_T	Differential Output Voltage	$R_L = 100\ \Omega$ See[2]		2.0	3.1		V
$\lvert V_T\rvert - \lvert \overline{V}_T\rvert$	Difference In Differential Output	$R_L = 100\ \Omega$ See[2]				0.4	V
V_{OS}	Common Mode Output Voltage	$R_L = 100\ \Omega$ See[2]			2.0	3.0	V
$\lvert V_{OS} - \overline{V}_{OS}\rvert$	Difference In Common Mode Output	$R_L = 100\ \Omega$ See[2]				0.4	V
I_{IN}	Input Current	$V_{IN} = V_{CC}$, GND, V_{IH}, or V_{IL}				±1.0	µA
I_{CC}	Quiescent Supply Current	$I_{OUT} = 0$ µA,					
		$V_{IN} = V_{CC}$ or GND			200	500	µA
		$V_{IN} = 2.4V$ or $0.5V$[3]			0.8	2.0	mA
I_{OZ}	TRI-STATE Output Leakage Current	$V_{OUT} = V_{CC}$ or GND Control = V_{IL}			±0.5	±5.0	µA
I_{SC}	Output Short Circuit Current	$V_{IN} = V_{CC}$ or GND See[2] and [4]		−30		−150	mA
I_{OFF}	Power Off Output Leakage Current	$V_{CC} = 0V$ See[2]	$V_{OUT} = 6V$			100	µA
			$V_{OUT} = -0.25V$			−100	µA

(1) Unless otherwise specified, min/max limits apply across the −40°C to 85°C temperature range. All typicals are given for V_{CC} = 5V and T_A = 25°C.
(2) See EIA Specification RS-422 for exact test conditions.
(3) Measured per input. All other inputs at V_{CC} or GND.
(4) This is the current sourced when a high output is shorted to ground. Only one output at a time should be shorted.

Switching Characteristics[1]

V_{CC} = 5V ±10%, t_r, t_f ≤ 6 ns (Figure 3, Figure 4, Figure 5, Figure 6)

Parameter		Test Conditions	Min	Typ	Max	Units
t_{PLH}, t_{PHL}	Propagation Delay Input to Output	S1 Open		6	11	ns
Skew	See[2]	S1 Open		0.5	3	ns
t_{TLH}, t_{THL}	Differential Output Rise And Fall Times	S1 Open		6	10	ns
t_{PZH}	Output Enable Time	S1 Closed		12	25	ns
t_{PZL}	Output Enable Time	S1 Closed		13	26	ns
t_{PHZ}	Output Disable Time[3]	S1 Closed		4	8	ns
t_{PLZ}	Output Disable Time[3]	S1 Closed		6	12	ns
C_{PD}	Power Dissipation Capacitance[4]			100		pF
C_{IN}	Input Capacitance			6		pF

(1) Unless otherwise specified, min/max limits apply across the −40°C to 85°C temperature range. All typicals are given for V_{CC} = 5V and T_A = 25°C.
(2) Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.
(3) Output disable time is the delay from the control input being switched to the output transistors turning off. The actual disable times are less than indicated due to the delay added by the RC time constant of the load.
(4) C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V^2CC f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

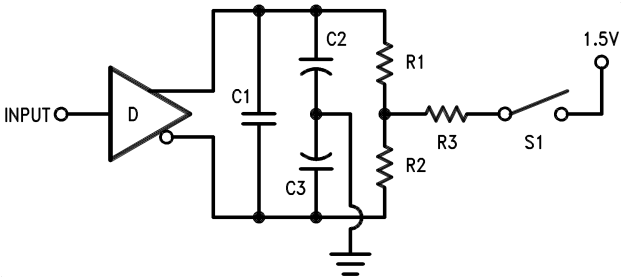
Comparison Table of Switching Characteristics into “LS-Type” Load[1]

V_{CC} = 5V, T_A = +25°C, t_r ≤ 6 ns, t_f ≤ 6 ns (Figure 6, Figure 7, Figure 8, Figure 9, Figure 10, Figure 11)

Parameter		Test Conditions	DS34C87		DS3487		Units
			Typ	Max	Typ	Max	
t_{PLH}, t_{PHL}	Propagation Delay Input to Output		6	10	10	15	ns
Skew	See[2]		1.5	2.0			ns
t_{THL}, t_{TLH}	Differential Output Rise and Fall Times		4	7	10	15	ns
t_{PHZ}	Output Disable Time See[3]	C_L = 50 pF, R_L = 200Ω, S1 Closed, S2 Closed	8	11	17	25	ns
t_{PLZ}	Output Disable Time See[3]	C_L = 50 pF, R_L = 200Ω, S1 Closed, S2 Closed	7	10	15	25	ns
t_{PZH}	Output Enable Time	C_L = 50 pF, R_L = ∞, S1 Open, S2 Closed	11	19	11	25	ns
t_{PZL}	Output Enable Time	C_L = 50 pF, R_L = 200Ω, S1 Closed, S2 Open	14	21	15	25	ns

(1) This table is provided for comparison purposes only. The values in this table for the DS34C87 reflect the performance of the device but are not tested or ensured.
(2) Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.
(3) Output disable time is the delay from the control input being switched to the output transistors turning off. The actual disable times are less than indicated due to the delay added by the RC time constant of the load.

AC TEST CIRCUIT AND SWITCHING TIME WAVEFORMS



Note: C1 = C2 = C3 = 40 pF (including Probe and Jig Capacitance), R1 = R2 = 50Ω, R3 = 500Ω

Figure 3. AC Test Circuit

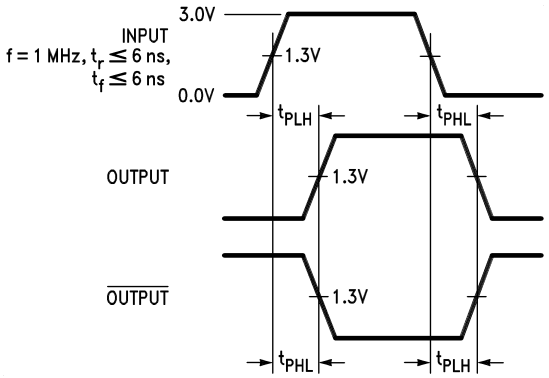
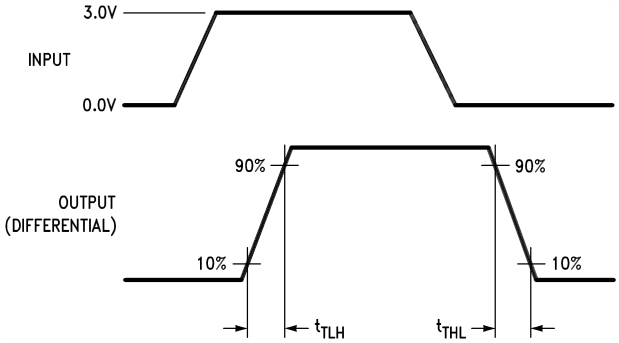


Figure 4. Propagation Delays



Input pulse; f = 1 MHz, 50%, $t_r \leq 6$ ns, $t_f \leq$ 6ns

Figure 6. Differential Rise and Fall Times

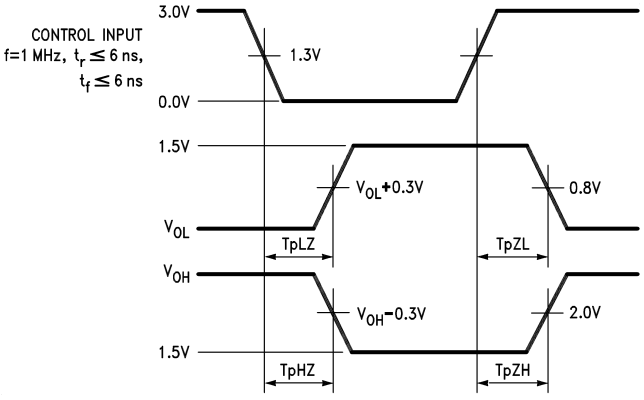


Figure 5. Enable and Disable Times

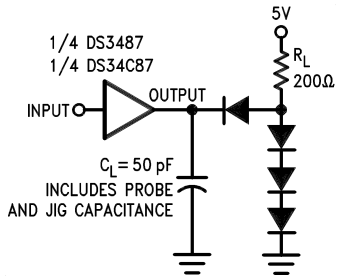


Figure 7. Propagation Delays Test Circuit for "LS-Type" Load

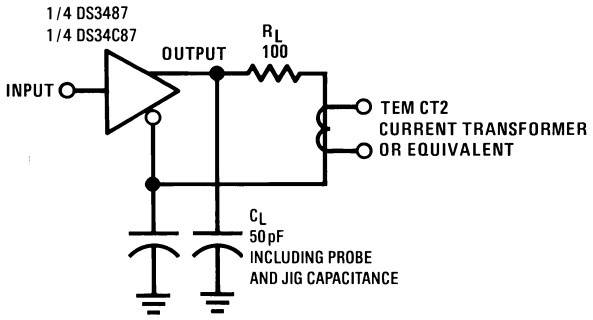


Figure 8. Differential Rise and Fall Times Test Circuit for "LS-Type" Load

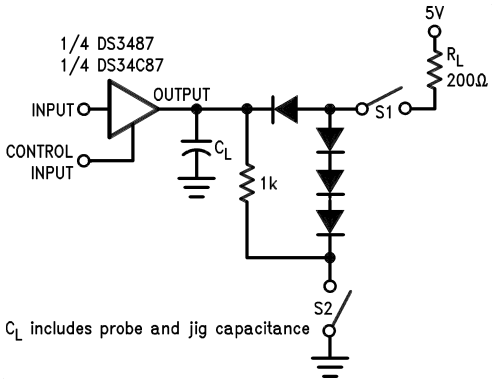


Figure 9. Load Enable and Disable Times Test Circuit for "LS-Type" Load

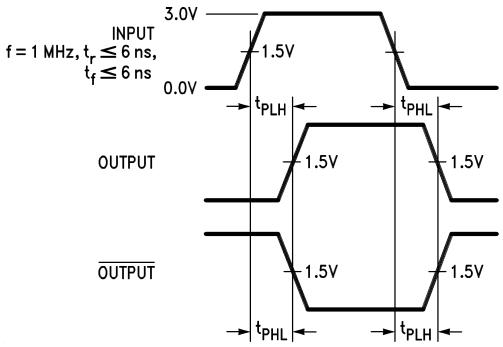


Figure 10. Load Propagation Delays for "LS-Type" Load

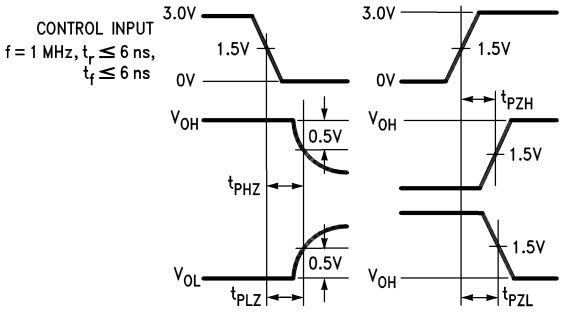
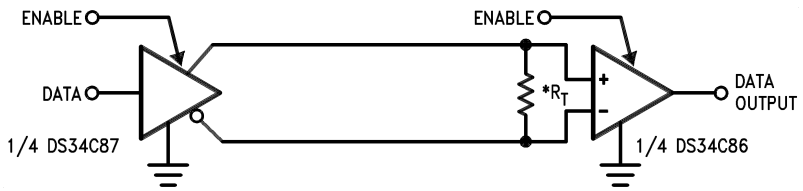


Figure 11. Load Enable and Disable Times for "LS-Type" Load

TYPICAL APPLICATIONS



*R_T is optional although highly recommended to reduce reflection.

PIN DESCRIPTIONS

Pin Number (PDIP or SOIC package)	**Pin Name**	**Function**
1	INPUT A	Channel A - TTL/CMOS input
2	OUTPUT A - True	True Output for Channel A, RS422 Levels
3	OUTPUT A - Inverting	Inverting Output for Channel A, RS422 Levels
4	A/B CONTROL	Enable Pin for Channels A and B, Active High, TTL/CMOS Levels
5	OUTPUT B - Inverting	Inverting Output for Channel B, RS422 Levels
6	OUTPUT B - True	True Output for Channel B, RS422 Levels
7	INPUT B	Channel B - TTL/CMOS input
8	GND	Ground Pin (0 V)
9	INPUT C	Channel C - TTL/CMOS input
10	OUTPUT C - True	True Output for Channel C, RS422 Levels
11	OUTPUT C - Inverting	Inverting Output for Channel C, RS422 Levels
12	C/D CONTROL	Enable Pin for Channels C and D, Active High, TTL/CMOS Levels
13	OUTPUT D - Inverting	Inverting Output for Channel D, RS422 Levels
14	OUTPUT D - True	True Output for Channel D, RS422 Levels
15	INPUT D	Channel D - TTL/CMOS input
16	V_{CC}	Power Supply Pin, 5.0V typical

REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS34C87TM	NRND	SOIC	D	16	48	TBD	Call TI	Call TI	-40 to 85	DS34C87TM	
DS34C87TM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS34C87TM	Samples
DS34C87TMX	NRND	SOIC	D	16	2500	TBD	Call TI	Call TI	-40 to 85	DS34C87TM	
DS34C87TMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS34C87TM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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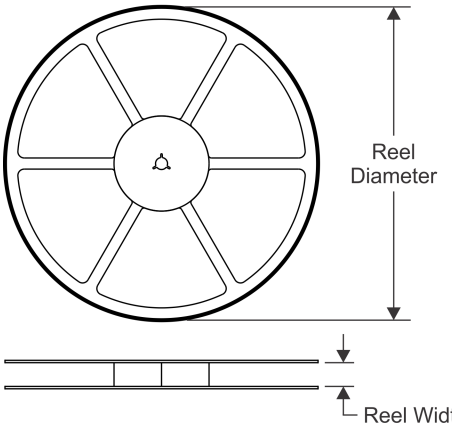
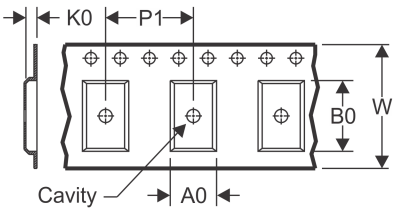
TAPE AND REEL INFORMATION

REEL DIMENSIONS

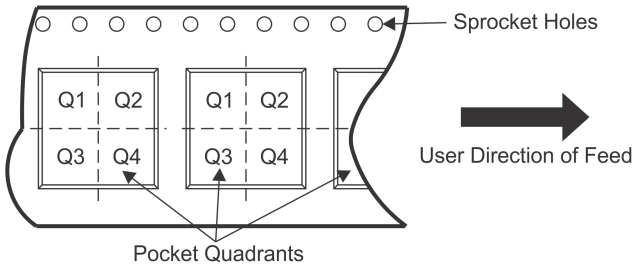


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

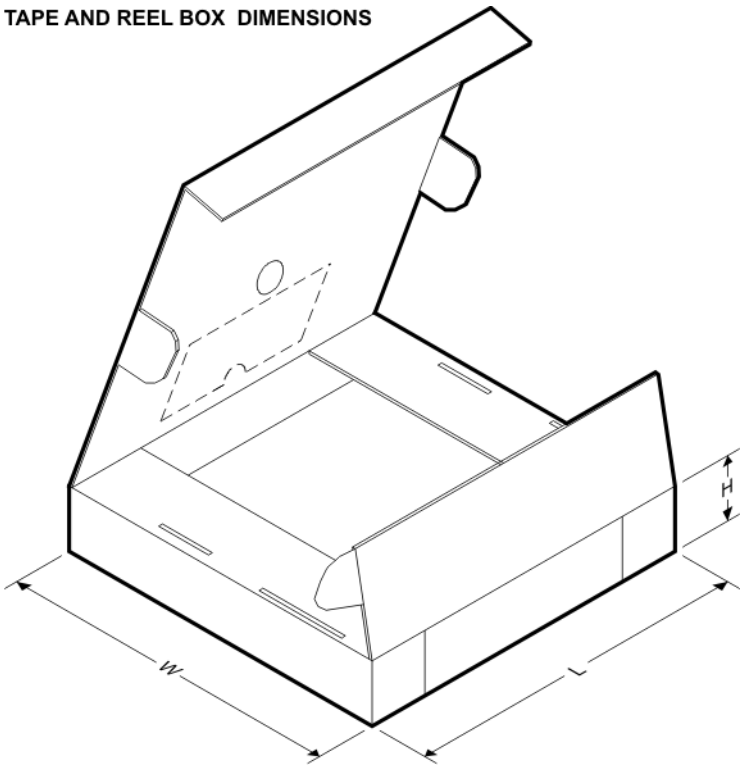
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS34C87TMX	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
DS34C87TMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

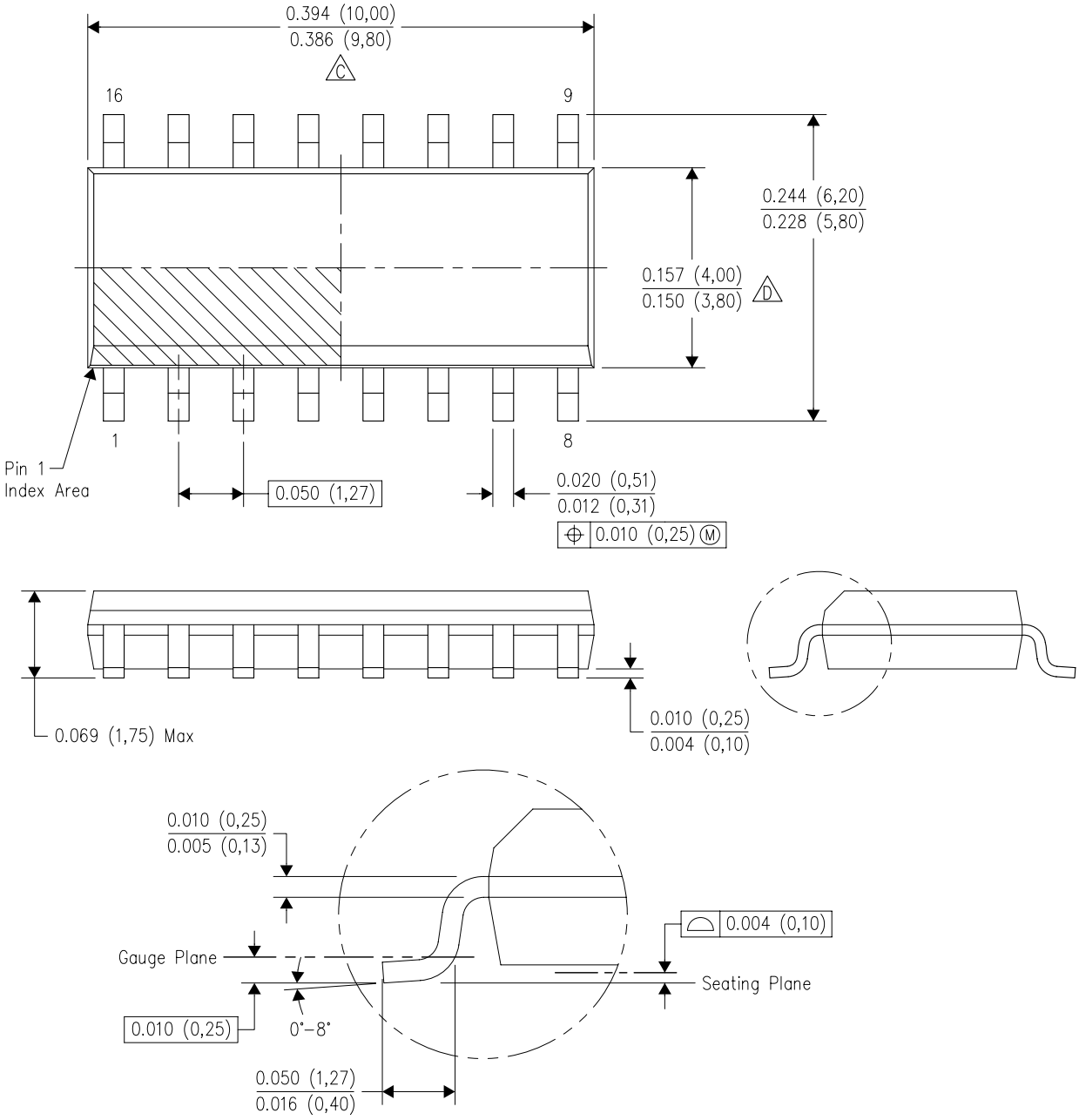
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS34C87TMX	SOIC	D	16	2500	367.0	367.0	35.0
DS34C87TMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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