

*Totally Logical*

## Z8E000

FEATURE-RICH Z8<sup>PLUS</sup> ONE-TIME-PROGRAMMABLE MICROCONTROLLER

### FEATURES

| Part Number | ROM (Bytes) | RAM* (Bytes) | Speed (MHz) |
|-------------|-------------|--------------|-------------|
| Z8E000      | 512         | 32           | 10          |

\* General-Purpose

#### Microcontroller Core Features

- All Instructions Execute in 1  $\mu$ s Instruction Cycle @ 10 MHz
- 512 x 8 On-Chip OTP EPROM Memory
- 32 x 8 General-Purpose Registers (SRAM)
- Four Vectored Hardware Interrupts with Fixed Priority
- Two Additional Software Interrupts
- Operating Speed: DC–10 MHz
- Six Addressing Modes: R, IR, X, D, RA, & IM

#### Peripheral Features

- One 16-Bit Standard Timer
- 16-Bit Programmable Watch-Dog Timer (WDT)
- 13 Total Input/Output Pins
- One 8-Bit I/O Port (Port A)
  - I/O Bit Programmable

- Each Bit Programmable as Push-Pull or Open-Drain
- One 5-Bit I/O Port (Port B)
  - I/O Bit Programmable
  - Includes Special Functionality: Stop-Mode Recovery Input, Selectable Edge Interrupts

#### Additional Features

- On-Chip Oscillator that Accepts XTAL, Ceramic Resonator, LC, or External Clock
- Programmable Options:
  - EPROM Protect
- Power Reduction Modes:
  - HALT Mode with Peripheral Units Active
  - STOP Mode with all Functionality Shut Down

#### CMOS/Technology Features

- Low-Power Consumption
- 3.5V to 5.5V Operating Range @ 0°C to +70°C  
4.5V to 5.5V Operating Range @ –40°C to +105°C
- 18-Pin DIP, SOIC, and 20-Pin SSOP Packages.

### GENERAL DESCRIPTION

ZiLOG's Z8E000 Microcontroller (MCU) is a One-Time Programmable (OTP) member of ZiLOG's single-chip Z8<sup>PLUS</sup> MCU family. The Z8E000 allows easy software development, debug, and prototyping.

For applications demanding powerful I/O capabilities, the Z8E000's dedicated input and output lines are grouped into two ports, and are configurable under software control.

One 16-bit on-chip standard timer, offloads the system of administering real-time tasks such as counting/timing and I/O data communications.

GENERAL DESCRIPTION (Continued)

**Note:** All signals with an overline, “ $\overline{\phantom{x}}$ ”, are active Low. For example,  $\overline{B/W}$  (WORD is active Low, only);  $\overline{B/W}$  (BYTE is active Low, only).

Power connections follow conventional descriptions below:

| Connection | Circuit  | Device   |
|------------|----------|----------|
| Power      | $V_{CC}$ | $V_{DD}$ |
| Ground     | GND      | $V_{SS}$ |

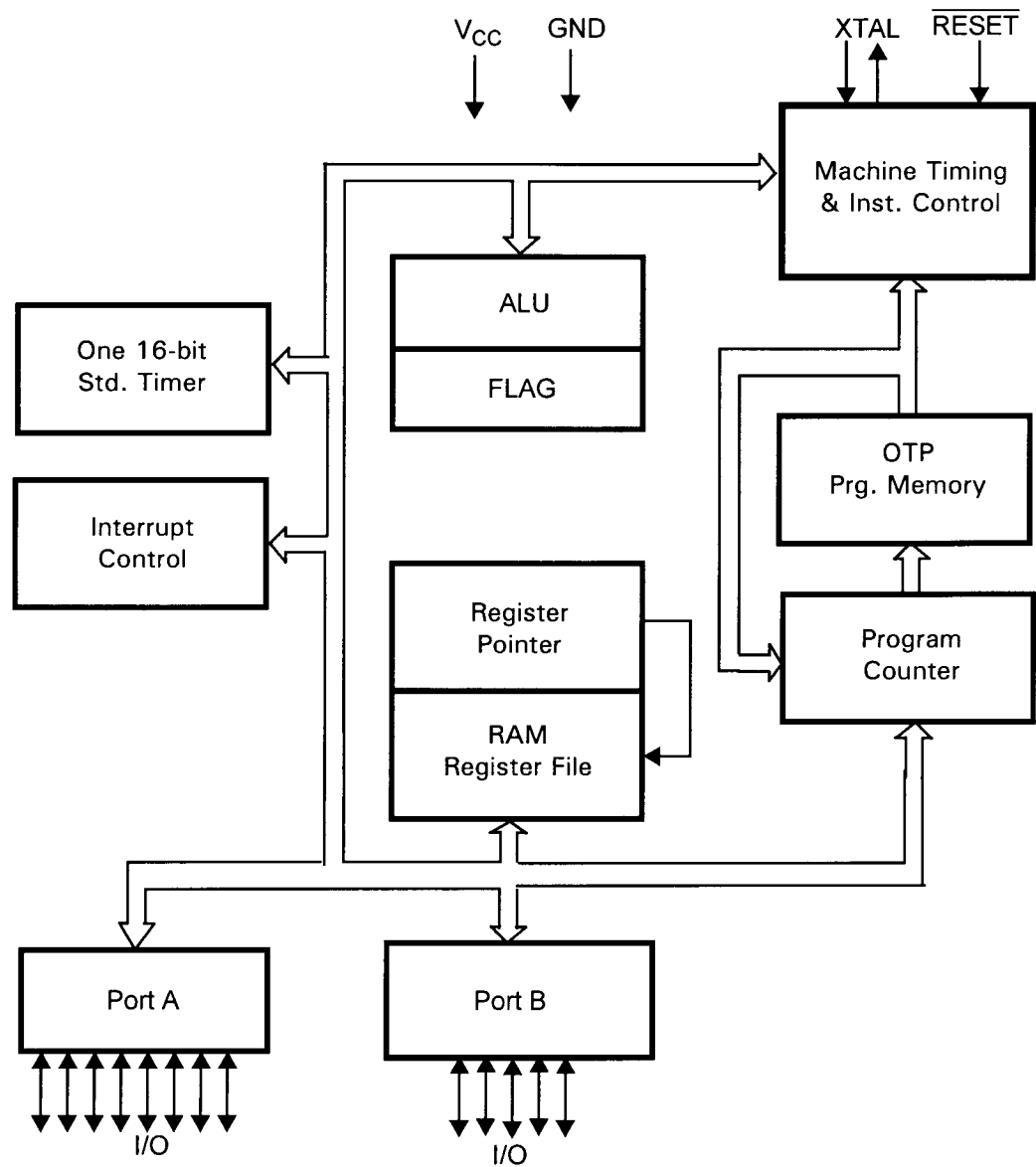


Figure 1. Functional Block Diagram

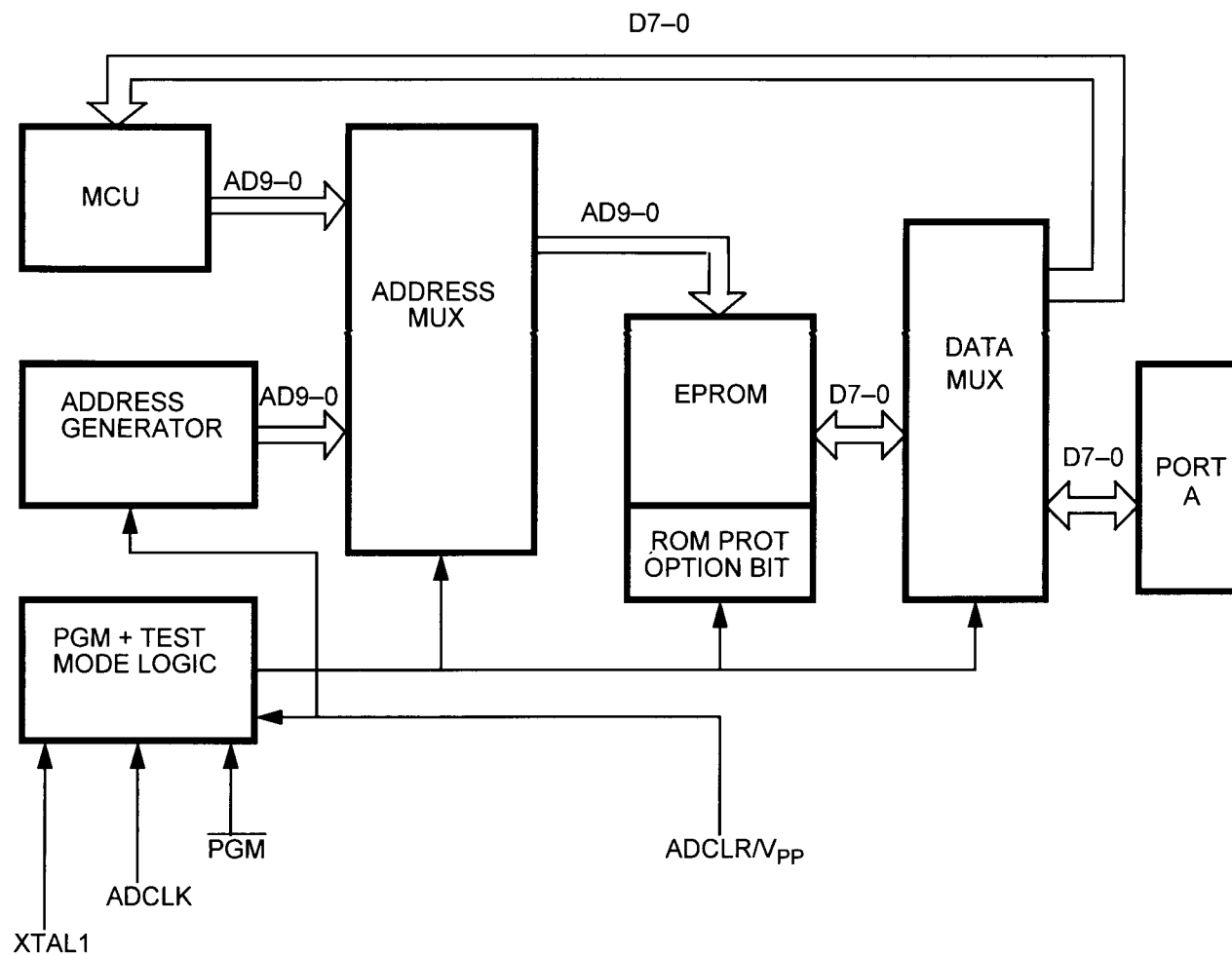


Figure 2. EPROM Programming Mode Block Diagram

PIN DESCRIPTION

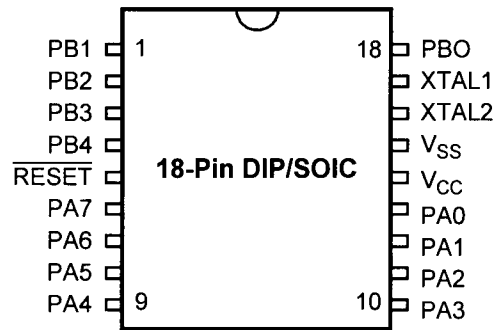
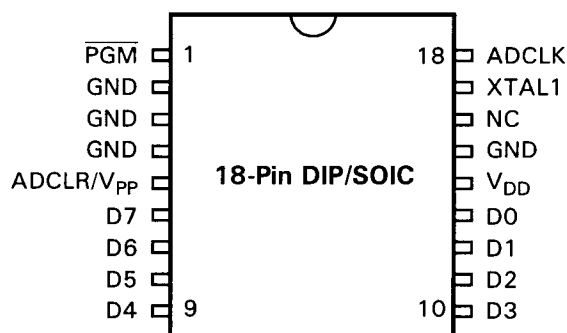


Figure 3. 18-Pin DIP/SOIC Pin Identification

Table 1. 18-Pin DIP/SOIC Pin Assignments

| Standard Mode |                 |                          |           |
|---------------|-----------------|--------------------------|-----------|
| Pin #         | Symbol          | Function                 | Direction |
| 1–4           | PB1–PB4         | Port B, Pins 1,2,3,4     | In/Output |
| 5             | RESET           | Reset                    | Input     |
| 6–9           | PA7–PA4         | Port A, Pins 7,6,5,4     | In/Output |
| 10–13         | PA3–PA0         | Port A, Pins 3,2,1,0     | In/Output |
| 14            | V <sub>CC</sub> | Power Supply             |           |
| 15            | V <sub>SS</sub> | Ground                   |           |
| 16            | XTAL2           | Crystal Oscillator Clock | Output    |
| 17            | XTAL1           | Crystal Oscillator Clock | Input     |
| 18            | PB0             | Port B, Pin 0            | In/Output |



**Figure 4. 18-Pin DIP/SOIC Pin Identification;  
EPROM Programming Mode**

**Table 2. 18-Pin DIP/SOIC Pin Assignments; EPROM Programmable Mode**

| EPROM Programming Mode |                       |                             |           |
|------------------------|-----------------------|-----------------------------|-----------|
| Pin #                  | Symbol                | Function                    | Direction |
| 1                      | PGM                   | Program Mode                | Input     |
| 2–4                    | GND                   | Ground                      |           |
| 5                      | ADCLR/V <sub>pp</sub> | Clear Clock/Program Voltage | Input     |
| 6–9                    | D7–D4                 | Data 7,6,5,4                | In/Output |
| 10–13                  | D3–D0                 | Data 3,2,1,0                | In/Output |
| 14                     | V <sub>DD</sub>       | Power Supply                |           |
| 15                     | GND                   | Ground                      |           |
| 16                     | NC                    | No Connection               |           |
| 17                     | XTAL1                 | 1 MHz Clock                 | Input     |
| 18                     | ADCLK                 | Address Clock               | Input     |

## PIN DESCRIPTION (Continued)

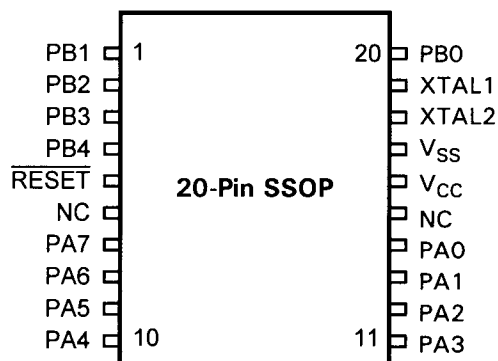


Figure 5. 20-Pin SSOP Pin Identification

Table 3. 20-Pin SSOP Pin Assignments

| Standard Mode |                 |                          |           |
|---------------|-----------------|--------------------------|-----------|
| Pin #         | Symbol          | Function                 | Direction |
| 1–4           | PB1–PB4         | Port B, Pins 1,2,3,4     | In/Output |
| 5             | RESET           | Reset                    | Input     |
| 6             | NC              | No Connection            |           |
| 7–10          | PA7–PA4         | Port A, Pins 7,6,5,4     | In/Output |
| 11–14         | PA3–PA0         | Port A, Pins 3,2,1,0     | In/Output |
| 15            | NC              | No Connection            |           |
| 16            | V <sub>CC</sub> | Power Supply             |           |
| 17            | V <sub>SS</sub> | Ground                   |           |
| 18            | XTAL2           | Crystal Oscillator Clock | Output    |
| 19            | XTAL1           | Crystal Oscillator Clock | Input     |
| 20            | PB0             | Port B, Pin 0            | In/Output |

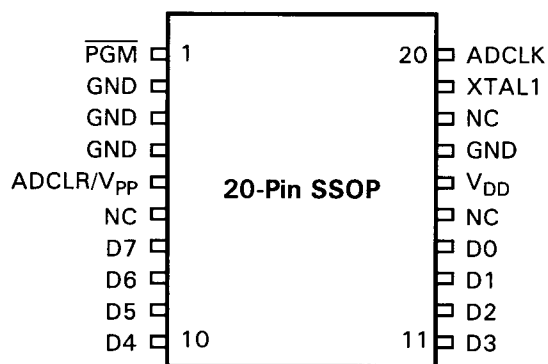


Figure 6. 20-Pin SSOP Pin Identification; EPROM Programming Mode

Table 4. 20-Pin SSOP Pin Assignments; EPROM Programming Mode

| EPROM Programming Mode |                       |                             |           |
|------------------------|-----------------------|-----------------------------|-----------|
| Pin #                  | Symbol                | Function                    | Direction |
| 1                      | PGM                   | Program Mode                | Input     |
| 2–4                    | GND                   | Ground                      |           |
| 5                      | ADCLR/V <sub>pp</sub> | Clear Clock/Program Voltage | Input     |
| 6                      | NC                    | No Connection               |           |
| 7–10                   | D7–D4                 | Data 7,6,5,4                | In/Output |
| 11–14                  | D3–D0                 | Data 3,2,1,0                | In/Output |
| 15                     | NC                    | No Connection               |           |
| 16                     | V <sub>DD</sub>       | Power Supply                |           |
| 17                     | GND                   | Ground                      |           |
| 18                     | NC                    | No Connection               |           |
| 19                     | XTAL1                 | 1 MHz Clock                 | Input     |
| 20                     | ADCLK                 | Address Clock               | Input     |

## ABSOLUTE MAXIMUM RATINGS

| Parameter                                                  | Min  | Max        | Units | Note |
|------------------------------------------------------------|------|------------|-------|------|
| Ambient Temperature under Bias                             | -40  | +105       | C     |      |
| Storage Temperature                                        | -65  | +150       | C     |      |
| Voltage on any Pin with Respect to $V_{SS}$                | -0.6 | +7         | V     | 1    |
| Voltage on $V_{DD}$ Pin with Respect to $V_{SS}$           | -0.3 | +7         | V     |      |
| Voltage on $\overline{RESET}$ Pin with Respect to $V_{SS}$ | -0.6 | $V_{DD}+1$ | V     | 2    |
| Total Power Dissipation                                    |      | 880        | mW    |      |
| Maximum Allowable Current out of $V_{SS}$                  |      | 80         | mA    |      |
| Maximum Allowable Current into $V_{DD}$                    |      | 80         | mA    |      |
| Maximum Allowable Current into an Input Pin                | -600 | +600       | mA    | 3    |
| Maximum Allowable Current into an Open-Drain Pin           | -600 | +600       | mA    | 4    |
| Maximum Allowable Output Current Sunk by Any I/O Pin       |      | 25         | mA    |      |
| Maximum Allowable Output Current Sourced by Any I/O Pin    |      | 25         | mA    |      |
| Maximum Allowable Output Current Sunk by Port A            |      | 40         | mA    |      |
| Maximum Allowable Output Current Sourced by Port A         |      | 40         | mA    |      |
| Maximum Allowable Output Current Sunk by Port B            |      | 40         | mA    |      |
| Maximum Allowable Output Current Sourced by Port B         |      | 40         | mA    |      |

### Notes:

1. Applies to all pins except the  $\overline{RESET}$  pin and where otherwise noted.
2. There is no input protection diode from pin to  $V_{DD}$ .
3. Excludes XTAL pins.
4. Device pin is not at an output Low state.

Stresses greater than those listed under Absolute Maximum Ratings can cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period can affect device reliability. Total power dissipation should

not exceed 880 mW for the package. Power dissipation is calculated as follows:

$$\begin{aligned} \text{Total Power Dissipation} &= V_{DD} \times [I_{DD} - (\text{sum of } I_{OH})] \\ &+ \text{sum of } [(V_{DD} - V_{OH}) \times I_{OH}] \\ &+ \text{sum of } (V_{OL} \times I_{OL}) \end{aligned}$$



## STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 7).

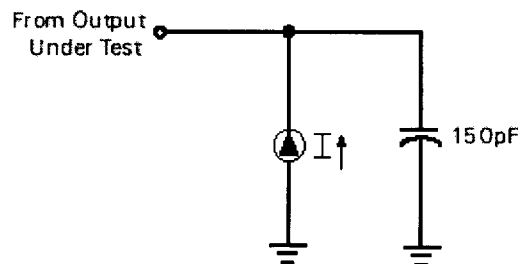


Figure 7. Test Load Diagram

## CAPACITANCE

$T_A = 25^\circ\text{C}$ ,  $V_{CC} = \text{GND} = 0\text{V}$ ,  $f = 1.0\text{ MHz}$ , unmeasured pins returned to GND.

| Parameter          | Min | Max   |
|--------------------|-----|-------|
| Input capacitance  | 0   | 12 pF |
| Output capacitance | 0   | 12 pF |
| I/O capacitance    | 0   | 12 pF |

## DC ELECTRICAL CHARACTERISTICS

| $T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ |                          |            |              |              |                                |               |                                                           |       |
|---------------------------------------------------|--------------------------|------------|--------------|--------------|--------------------------------|---------------|-----------------------------------------------------------|-------|
| Sym                                               | Parameter                | $V_{CC}^1$ | Min          | Max          | Typical<br>@ 25°C <sup>2</sup> | Units         | Conditions                                                | Notes |
| $V_{CH}$                                          | Clock Input High Voltage | 3.5V       | $0.7V_{CC}$  | $V_{CC}+0.3$ | 1.3                            | V             | Driven by External Clock Generator                        |       |
|                                                   |                          | 5.5V       | $0.7V_{CC}$  | $V_{CC}+0.3$ | 2.5                            | V             | Driven by External Clock Generator                        |       |
| $V_{CL}$                                          | Clock Input Low Voltage  | 3.5V       | $V_{SS}-0.3$ | $0.2V_{CC}$  | 0.7                            | V             | Driven by External Clock Generator                        |       |
|                                                   |                          | 5.5V       | $V_{SS}-0.3$ | $0.2V_{CC}$  | 1.5                            | V             | Driven by External Clock Generator                        |       |
| $V_{IH}$                                          | Input High Voltage       | 3.5V       | $0.7V_{CC}$  | $V_{CC}+0.3$ | 1.3                            | V             |                                                           |       |
|                                                   |                          | 5.5V       | $0.7V_{CC}$  | $V_{CC}+0.3$ | 2.5                            | V             |                                                           |       |
| $V_{IL}$                                          | Input Low Voltage        | 3.5V       | $V_{SS}-0.3$ | $0.2V_{CC}$  | 0.7                            | V             |                                                           |       |
|                                                   |                          | 5.5V       | $V_{SS}-0.3$ | $0.2V_{CC}$  | 1.5                            | V             |                                                           |       |
| $V_{OH}$                                          | Output High Voltage      | 3.5V       | $V_{CC}-0.4$ |              | 3.1                            | V             | $I_{OH} = -2.0 \text{ mA}$                                |       |
|                                                   |                          | 5.5V       | $V_{CC}-0.4$ |              | 4.8                            | V             | $I_{OH} = -2.0 \text{ mA}$                                |       |
| $V_{OL1}$                                         | Output Low Voltage       | 3.5V       |              | 0.6          | 0.2                            | V             | $I_{OL} = +4.0 \text{ mA}$                                |       |
|                                                   |                          | 5.5V       |              | 0.4          | 0.1                            | V             | $I_{OL} = +4.0 \text{ mA}$                                |       |
| $V_{OL2}$                                         | Output Low Voltage       | 3.5V       |              | 1.2          | 0.5                            | V             | $I_{OL} = +6 \text{ mA}$                                  |       |
|                                                   |                          | 5.5V       |              | 1.2          | 0.5                            | V             | $I_{OL} = +12 \text{ mA}$                                 |       |
| $V_{RH}$                                          | Reset Input High Voltage | 3.5V       | $0.5V_{CC}$  | $V_{CC}$     | 1.1                            | V             |                                                           |       |
|                                                   |                          | 5.5V       | $0.5V_{CC}$  | $V_{CC}$     | 2.2                            | V             |                                                           |       |
| $V_{RL}$                                          | Reset Input Low Voltage  | 3.5V       | $V_{SS}-0.3$ | $0.2V_{CC}$  | 0.9                            | V             |                                                           |       |
|                                                   |                          | 5.5V       | $V_{SS}-0.3$ | $0.2V_{CC}$  | 1.4                            | V             |                                                           |       |
| $I_{IL}$                                          | Input Leakage            | 3.5V       | -1.0         | 2.0          | 0.064                          | $\mu\text{A}$ | $V_{IN} = 0\text{V}, V_{CC}$                              |       |
|                                                   |                          | 5.5V       | -1.0         | 2.0          | 0.064                          | $\mu\text{A}$ | $V_{IN} = 0\text{V}, V_{CC}$                              |       |
| $I_{OL}$                                          | Output Leakage           | 3.5V       | -1.0         | 2.0          | 0.114                          | $\mu\text{A}$ | $V_{IN} = 0\text{V}, V_{CC}$                              |       |
|                                                   |                          | 5.5V       | -1.0         | 2.0          | 0.114                          | $\mu\text{A}$ | $V_{IN} = 0\text{V}, V_{CC}$                              |       |
| $I_{IR}$                                          | Reset Input Current      | 3.5V       | -10          | -60          | -30                            | $\mu\text{A}$ |                                                           |       |
|                                                   |                          | 5.5V       | -20          | -180         | -100                           | $\mu\text{A}$ |                                                           |       |
| $I_{CC}$                                          | Supply Current           | 3.5V       |              | 2.5          | 2.0                            | mA            | @ 10 MHz                                                  | 3,4   |
|                                                   |                          | 5.5V       |              | 6.0          | 4.0                            | mA            | @ 10 MHz                                                  | 3,4   |
| $I_{CC1}$                                         | Standby Current          | 3.5V       |              | 2.0          | 1.0                            | mA            | Halt Mode $V_{IN} = 0\text{V}$<br>$V_{CC}@10 \text{ MHz}$ | 3,4   |
|                                                   |                          | 5.5V       |              | 6.0          | 4.0                            | mA            | Halt Mode $V_{IN} = 0\text{V}$<br>$V_{CC}@10 \text{ MHz}$ | 3,4   |

| $T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ |                 |            |     |     |                                |       |                                       |       |
|---------------------------------------------------|-----------------|------------|-----|-----|--------------------------------|-------|---------------------------------------|-------|
| Sym                                               | Parameter       | $V_{CC}^1$ | Min | Max | Typical<br>@ 25°C <sup>2</sup> | Units | Conditions                            | Notes |
| $I_{CC2}$                                         | Standby Current | 3.5V       |     | 500 | 150                            | nA    | Stop Mode $V_{IN} = 0V$ ,<br>$V_{CC}$ | 5     |
|                                                   |                 | 5.5V       |     | 500 | 250                            | nA    | Stop Mode $V_{IN} = 0V$ ,<br>$V_{CC}$ | 5     |

**Notes:**

1. The  $V_{CC}$  voltage specification of 3.5 V guarantees 3.5 V and the  $V_{CC}$  voltage specification of 5.5 V guarantees 5.0 V  $\pm 0.5$  V.
2. Typical values are measured at  $V_{CC} = 3.3V$  and  $V_{CC} = 5.0V$ .
3. All outputs unloaded, I/O pins floating, and all inputs are at  $V_{CC}$  or  $V_{SS}$  level.
4. CL1 = CL2 = 22 pF.
5. Same as note 3 except inputs at  $V_{CC}$ .

# DC ELECTRICAL CHARACTERISTICS (Continued)

| T <sub>A</sub> = −40°C to +105°C |                          |                              |                      |                      |                                |       |                                                             |       |
|----------------------------------|--------------------------|------------------------------|----------------------|----------------------|--------------------------------|-------|-------------------------------------------------------------|-------|
| Sym                              | Parameter                | V <sub>CC</sub> <sup>1</sup> | Min                  | Max                  | Typical<br>@ 25°C <sup>2</sup> | Units | Conditions                                                  | Notes |
| V <sub>CH</sub>                  | Clock Input High Voltage | 4.5V                         | 0.7 V <sub>CC</sub>  | V <sub>CC</sub> +0.3 | 2.5                            | V     | Driven by External Clock Generator                          |       |
|                                  |                          | 5.5V                         | 0.7 V <sub>CC</sub>  | V <sub>CC</sub> +0.3 | 2.5                            | V     | Driven by External Clock Generator                          |       |
| V <sub>CL</sub>                  | Clock Input Low Voltage  | 4.5V                         | V <sub>SS</sub> −0.3 | 0.2 V <sub>CC</sub>  | 1.5                            | V     | Driven by External Clock Generator                          |       |
|                                  |                          | 5.5V                         | V <sub>SS</sub> −0.3 | 0.2 V <sub>CC</sub>  | 1.5                            | V     | Driven by External Clock Generator                          |       |
| V <sub>IH</sub>                  | Input High Voltage       | 4.5V                         | 0.7 V <sub>CC</sub>  | V <sub>CC</sub> +0.3 | 2.5                            | V     |                                                             |       |
|                                  |                          | 5.5V                         | 0.7 V <sub>CC</sub>  | V <sub>CC</sub> +0.3 | 2.5                            | V     |                                                             |       |
| V <sub>IL</sub>                  | Input Low Voltage        | 4.5V                         | V <sub>SS</sub> −0.3 | 0.2 V <sub>CC</sub>  | 1.5                            | V     |                                                             |       |
|                                  |                          | 5.5V                         | V <sub>SS</sub> −0.3 | 0.2 V <sub>CC</sub>  | 1.5                            | V     |                                                             |       |
| V <sub>OH</sub>                  | Output High Voltage      | 4.5V                         | V <sub>CC</sub> −0.4 |                      | 4.8                            | V     | I <sub>OH</sub> = −2.0 mA                                   |       |
|                                  |                          | 5.5V                         | V <sub>CC</sub> −0.4 |                      | 4.8                            | V     | I <sub>OH</sub> = −2.0 mA                                   |       |
| V <sub>OL1</sub>                 | Output Low Voltage       | 4.5V                         |                      | 0.4                  | 0.1                            | V     | I <sub>OL</sub> = +4.0 mA                                   |       |
|                                  |                          | 5.5V                         |                      | 0.4                  | 0.1                            | V     | I <sub>OL</sub> = +4.0 mA                                   |       |
| V <sub>OL2</sub>                 | Output Low Voltage       | 4.5V                         |                      | 1.2                  | 0.5                            | V     | I <sub>OL</sub> = +12 mA,                                   |       |
|                                  |                          | 5.5V                         |                      | 1.2                  | 0.5                            | V     | I <sub>OL</sub> = +12 mA,                                   |       |
| V <sub>RH</sub>                  | Reset Input High Voltage | 4.5V                         | 0.5V <sub>CC</sub>   | V <sub>CC</sub>      | 1.1                            | V     |                                                             |       |
|                                  |                          | 5.5V                         | 0.5V <sub>CC</sub>   | V <sub>CC</sub>      | 2.2                            | V     |                                                             |       |
| I <sub>IL</sub>                  | Input Leakage            | 4.5V                         | −1.0                 | 2.0                  | <1.0                           | μA    | V <sub>IN</sub> = 0V, V <sub>CC</sub>                       |       |
|                                  |                          | 5.5V                         | −1.0                 | 2.0                  | <1.0                           | μA    | V <sub>IN</sub> = 0V, V <sub>CC</sub>                       |       |
| I <sub>OL</sub>                  | Output Leakage           | 4.5V                         | −1.0                 | 2.0                  | <1.0                           | μA    | V <sub>IN</sub> = 0V, V <sub>CC</sub>                       |       |
|                                  |                          | 5.5V                         | −1.0                 | 2.0                  | <1.0                           | μA    | V <sub>IN</sub> = 0V, V <sub>CC</sub>                       |       |
| I <sub>IR</sub>                  | Reset Input Current      | 4.5V                         | −18                  | −180                 | −112                           | mA    |                                                             |       |
|                                  |                          | 5.5V                         | −18                  | −180                 | −112                           | mA    |                                                             |       |
| I <sub>CC</sub>                  | Supply Current           | 4.5V                         |                      | 7.0                  | 4.0                            | mA    | @ 10 MHz                                                    | 3,4   |
|                                  |                          | 5.5V                         |                      | 7.0                  | 4.0                            | mA    | @ 10 MHz                                                    | 3,4   |
| I <sub>CC1</sub>                 | Standby Current          | 4.5V                         |                      | 2.0                  | 1.0                            | mA    | HALT Mode V <sub>IN</sub> = 0V,<br>V <sub>CC</sub> @ 10 MHz | 3,4   |
|                                  |                          | 5.5V                         |                      | 2.0                  | 1.0                            | mA    | HALT Mode V <sub>IN</sub> = 0V,<br>V <sub>CC</sub> @ 10 MHz | 3,4   |

| T <sub>A</sub> = −40°C to +105°C |                 |                              |     |     |                                |       |                                                 |       |
|----------------------------------|-----------------|------------------------------|-----|-----|--------------------------------|-------|-------------------------------------------------|-------|
| Sym                              | Parameter       | V <sub>CC</sub> <sup>1</sup> | Min | Max | Typical<br>@ 25°C <sup>2</sup> | Units | Conditions                                      | Notes |
| I <sub>CC2</sub>                 | Standby Current | 4.5V                         |     | 700 | 250                            | nA    | STOP Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> | 5     |
|                                  |                 | 5.5V                         |     | 700 | 250                            | nA    | STOP Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> | 5     |

**Notes:**

1. The  $V_{CC}$  voltage specification of 4.5 V and 5.5 V guarantees  $5.0\text{ V} \pm 0.5\text{ V}$ .
2. Typical values are measured at  $V_{CC} = 3.3V$  and  $V_{CC} = 5.0V$ .
3. All outputs unloaded, I/O pins floating, and all inputs are at  $V_{CC}$  or  $V_{SS}$  level.
4.  $CL1 = CL2 = 22\text{ pF}$ .
5. Same as note 3 except inputs at  $V_{CC}$ .

## AC ELECTRICAL CHARACTERISTICS

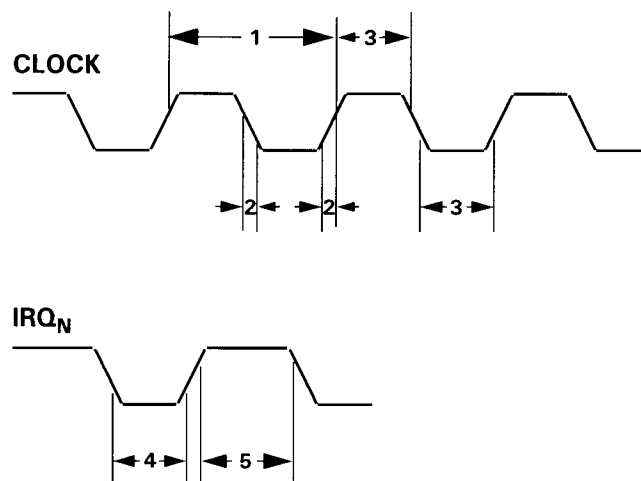


Figure 8. AC Electrical Timing Diagram

Table 5. Additional Timings

$T_A = -40^{\circ}\text{C to } +105^{\circ}\text{C}$   
@ 10 MHz

| No | Symbol   | Parameter                       | $V_{CC}^1$ | Min  | Max  | Units | Notes |
|----|----------|---------------------------------|------------|------|------|-------|-------|
| 1  | TpC      | Input Clock Period              | 3.5V       | 100  | DC   | ns    | 2     |
|    |          |                                 | 5.5V       | 100  | DC   | ns    | 2     |
| 2  | TrC, TfC | Clock Input Rise and Fall Times | 3.5V       |      | 15   | ns    | 2     |
|    |          |                                 | 5.5V       |      | 15   | ns    | 2     |
| 3  | TwC      | Input Clock Width               | 3.5V       | 50   |      | ns    | 2     |
|    |          |                                 | 5.5V       | 50   |      | ns    | 2     |
| 4  | TwIL     | Int. Request Input Low Time     | 3.5V       | 70   |      | ns    | 2     |
|    |          |                                 | 5.5V       | 70   |      | ns    | 2     |
| 5  | TwIH     | Int. Request Input High Time    | 3.5V       | 5TpC |      |       | 2     |
|    |          |                                 | 5.5V       | 5TpC |      |       | 2     |
| 6  | Twsm     | STOP Mode Recovery Width Spec.  | 3.5V       | 12   |      | ns    |       |
|    |          |                                 | 5.5V       | 12   |      | ns    |       |
| 7  | Tost     | Oscillator Start-Up Time        | 3.5V       |      | 5TpC |       |       |
|    |          |                                 | 5.5V       |      | 5TpC |       |       |

**Notes:**

1. The  $V_{DD}$  voltage specification of 3.5V guarantees 3.5V. The  $V_{DD}$  voltage specification of 5.5V guarantees  $5.0V \pm 0.5V$ .
2. Timing Reference uses  $0.7 V_{CC}$  for a logic 1 and  $0.2 V_{CC}$  for a logic 0.

## Z8<sup>PLUS</sup> CORE

The Z8E000 is based on the ZiLOG Z8<sup>Plus</sup> Core Architecture. This core is capable of addressing up to 64KBytes of program memory and 4KBytes of RAM. Register RAM is accessed as either 8- or 16-bit registers, using a combination of 4-, 8-, and 12-bit addressing modes. The architecture sup-

ports up to 15 vectored interrupts from external and internal sources. The processor decodes 44 CISC instructions, using six addressing modes. See the Z8<sup>Plus</sup> User's Manual for more information.

## RESET

This section describes the Z8E000 reset conditions, reset timing, and register initialization procedures. Reset is generated by the Reset Pin, Watch-Dog Timer (WDT), and Stop-Mode Recovery (SMR).

A system reset overrides all other operating conditions and puts the Z8E000 into a known state. To initialize the chip's internal logic, the  $\overline{\text{RESET}}$  input must be held Low for at least 30 XTAL clock cycles. The control registers and ports are

reset to their default conditions after a reset from the  $\overline{\text{RESET}}$  pin. The control registers and ports are not reset to their default conditions after wakeup from Stop Mode or WDT timeout.

During  $\overline{\text{RESET}}$ , the program counter is loaded with 0020H. I/O ports and control registers are configured to their default reset state. Resetting the Z8E000 does not affect the contents of the general-purpose registers.

## RESET PIN OPERATION

The Z8E000 hardware  $\overline{\text{RESET}}$  pin initializes the control and peripheral registers, as indicated in Table 6. Specific reset values are indicated by 1 or 0, while bits whose states are unchanged are indicated by the letter U.

$\overline{\text{RESET}}$  must first be held Low until the oscillator stabilizes. From that point, the pin then must be held for an additional 30 XTAL clock cycles to be sure that the internal reset is complete. The  $\overline{\text{RESET}}$  pin has a Schmitt-Trigger input with a trip point. There is no High side protection diode. The user should place an external diode from  $\overline{\text{RESET}}$  to  $V_{CC}$ . The

internal pull-up resistor on the  $\overline{\text{RESET}}$  pin is approximately 500 K $\Omega$ , typical.

Program execution starts 10 XTAL clock cycles after  $\overline{\text{RESET}}$  has returned High. The initial instruction fetch is from location 0020H. Figure 9 indicates reset timing.

After a reset, the first routine executed must be one that initializes the TCTLHI control register to the required system configuration. This routine is then followed by initialization of the remaining control registers.

**Table 6. Control and Peripheral Register Reset Values**

| Register |                           | Bits |   |   |   |   |   |   |   | Comments                                                               |
|----------|---------------------------|------|---|---|---|---|---|---|---|------------------------------------------------------------------------|
| (HEX)    | Register Name             | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                        |
| FF       | Stack Pointer             | 0    | 0 | U | U | U | U | U | U | Stack pointer is not affected by $\overline{\text{RESET}}$             |
| FE       | Reserved                  |      |   |   |   |   |   |   |   |                                                                        |
| FD       | Register Pointer          | U    | U | U | U | 0 | 0 | 0 | 0 | Register pointer is not affected by $\overline{\text{RESET}}$          |
| FC       | Flags                     | U    | U | U | U | U | U | * | * | Only WDT & SMR flags are affected by $\overline{\text{RESET}}$         |
| FB       | Interrupt Mask            | 0    | 0 | 0 | 0 | 0 | 0 | 0 | 0 | All interrupts masked by $\overline{\text{RESET}}$                     |
| FA       | Interrupt Request         | 0    | 0 | 0 | 0 | 0 | 0 | 0 | 0 | All interrupt requests cleared by $\overline{\text{RESET}}$            |
| F9–F0    | Reserved                  |      |   |   |   |   |   |   |   |                                                                        |
| EF–E0    | Virtual Copy              |      |   |   |   |   |   |   |   | Virtual Copy of the Current Working Register Set                       |
| DF–D8    | Reserved                  |      |   |   |   |   |   |   |   |                                                                        |
| D7       | PortB Spec. Func.         | 0    | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Deactivates all port special functions after $\overline{\text{RESET}}$ |
| D6       | PortB Directional Control | 0    | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Defines all bits as inputs in PortB after $\overline{\text{RESET}}$    |
| D5       | PortB Output              | U    | U | U | U | U | U | U | U | Output register not affected by $\overline{\text{RESET}}$              |

## RESET PIN OPERATION (Continued)

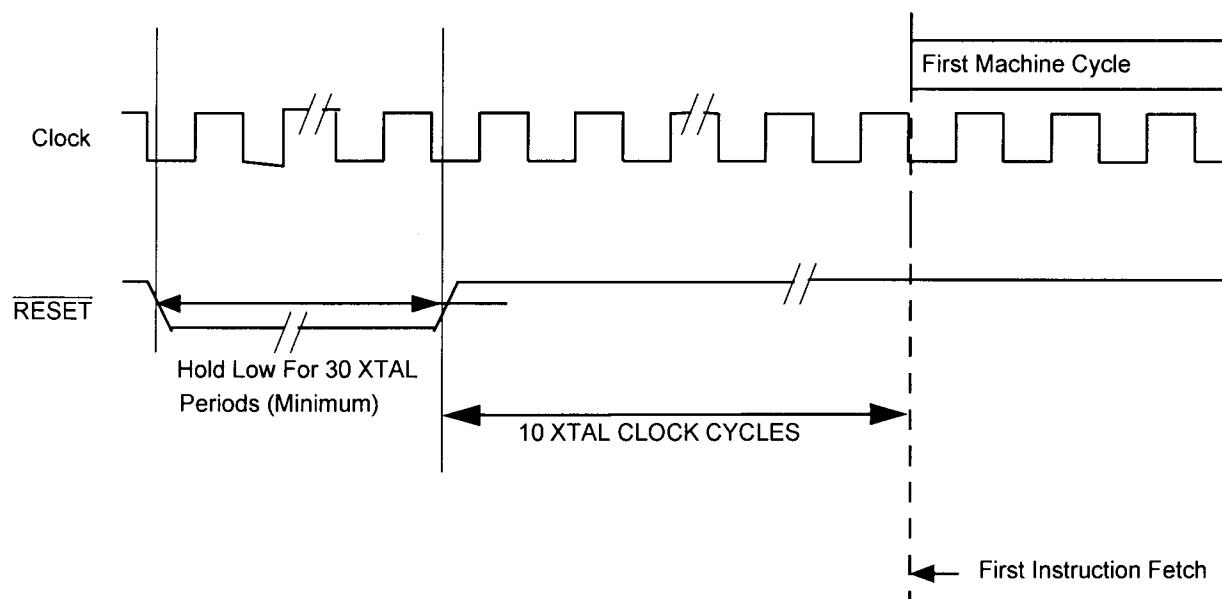
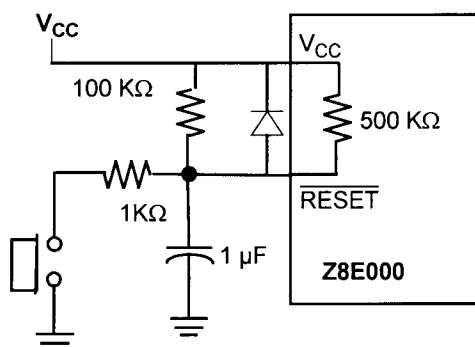
Table 6. Control and Peripheral Register Reset Values

| Register |                           | Bits |   |   |   |   |   |   |   | Comments                                                                   |
|----------|---------------------------|------|---|---|---|---|---|---|---|----------------------------------------------------------------------------|
| (HEX)    | Register Name             | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                            |
| D4       | PortB Input               | U    | U | U | U | U | U | U | U | Current sample of the input pin following $\overline{\text{RESET}}$        |
| D3       | PortA Spec. Func.         | 0    | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Deactivates all port special functions after $\overline{\text{RESET}}$     |
| D2       | PortA Directional Control | 0    | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Defines all bits as inputs in PortA after $\overline{\text{RESET}}$        |
| D1       | PortA Output              | U    | U | U | U | U | U | U | U | Output register not affected by $\overline{\text{RESET}}$                  |
| D0       | PortA Input               | U    | U | U | U | U | U | U | U | Current sample of the input pin following $\overline{\text{RESET}}$        |
| CF       | Reserved                  |      |   |   |   |   |   |   |   |                                                                            |
| CE       | Reserved                  |      |   |   |   |   |   |   |   |                                                                            |
| CD       | Reserved                  |      |   |   |   |   |   |   |   |                                                                            |
| CC       | Reserved                  |      |   |   |   |   |   |   |   |                                                                            |
| CB       | T3VAL                     | U    | U | U | U | U | U | U | U |                                                                            |
| CA       | T2VAL                     | U    | U | U | U | U | U | U | U |                                                                            |
| C9       | T3AR                      | U    | U | U | U | U | U | U | U |                                                                            |
| C8       | T2AR                      | U    | U | U | U | U | U | U | U |                                                                            |
| C7       | Reserved                  |      |   |   |   |   |   |   |   |                                                                            |
| C6       | Reserved                  |      |   |   |   |   |   |   |   |                                                                            |
| C5       | Reserved                  |      |   |   |   |   |   |   |   |                                                                            |
| C4       | Reserved                  |      |   |   |   |   |   |   |   |                                                                            |
| C3       | WDTHI                     | 1    | 1 | 1 | 1 | 1 | 1 | 1 | 1 |                                                                            |
| C2       | WDTLO                     | 1    | 1 | 1 | 1 | 1 | 1 | 1 | 1 |                                                                            |
| C1       | TCTLHI                    | 1    | 1 | 1 | 1 | 1 | 0 | 0 | 0 | WDT Enabled in HALT Mode, WDT timeout at maximum value, STOP Mode disabled |
| C0       | TCTLLO                    | 0    | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Standard timer is disabled                                                 |

**Note:** \*The SMR and WDT flags are set indicating the source of the RESET, as shown below:

| D1 | D0 | Reset Source                  |
|----|----|-------------------------------|
| 0  | 0  | $\overline{\text{RESET}}$ Pin |
| 0  | 1  | SMR Recovery                  |
| 1  | 0  | WDT Reset                     |
| 1  | 1  | Reserved                      |



**Figure 9. Reset Timing****Figure 10. Example of External Power-On Reset Circuit**

## RESET PIN OPERATION (Continued)

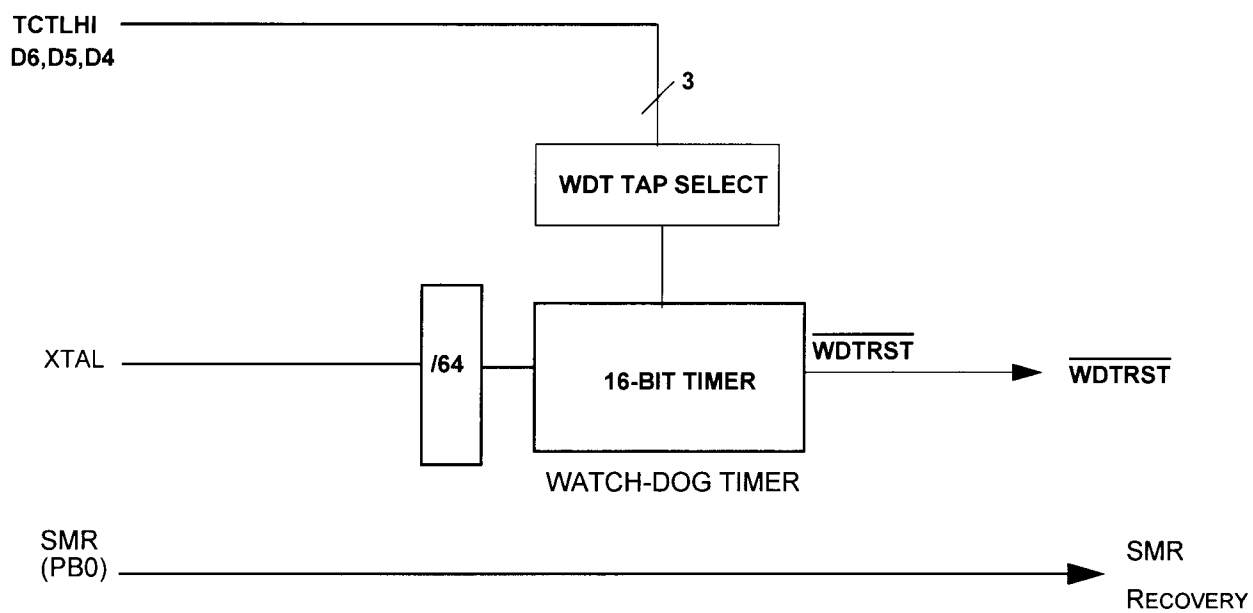


Figure 11. Z8E000 Reset Circuitry with WDT and SMR

## Z8E000 WATCH-DOG TIMER (WDT)

The Watch-Dog Timer is a retriggerable one-shot 16-bit timer that resets the Z8E000 if it reaches its terminal count. The WDT is driven by the XTAL2 clock pin. To provide the longer timeout periods required in applications, the WDT is only updated every 64th clock cycle. When operating in the RUN or HALT Modes, a WDT timeout reset is functionally equivalent to an interrupt vectoring the PC to 0020H and setting the WDT flag to a one state. Coming out of  $\overline{\text{RESET}}$ , the WDT will be fully enabled with its timeout value set at the maximum value, unless otherwise programmed during the first instruction. Subsequent executions of the WDT instruction reinitialize the watch-dog timer registers (C2H and C3H) to their initial values as defined by bits D6, D5, and D4 of the TCTLHI register (Figure 12). The WDT cannot be disabled except on the first cycle after  $\overline{\text{RESET}}$ , and if the device enters Stop mode.

The WDT instruction should be executed often enough to provide some margin before allowing the WDT registers to get near 0. Because the WDT timeout periods are relatively long, a WDT reset *will* occur in the unlikely event that the WDT times out on exactly the same cycle that the WDT instruction is executed.

The WDT and SMR flags are the only flags that are affected by the external  $\overline{\text{RESET}}$  pin.  $\overline{\text{RESET}}$  clears both the WDT and SMR flags. A WDT timeout sets the WDT flag. The STOP instruction sets the SMR flag. This behavior enables software to determine whether a pin  $\overline{\text{RESET}}$  occurred, whether a WDT timeout occurred, or whether a return from STOP Mode occurred. Reading the WDT flag does not reset it to zero. The user must clear the WDT flag via software. Failure to clear the WDT flag can result in undefined behavior.

## Z8E000 WATCH-DOG TIMER (WDT) (Continued)

OC1

TCTLHI

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
|----|----|----|----|----|----|----|----|

RESERVED (MUST BE 0)

0 = STOP MODE ENABLED  
1 = STOP MODE DISABLED\*

D6 D5 D4 WDT TIMEOUT VALUE

|   |   |   |                |
|---|---|---|----------------|
| 0 | 0 | 0 | DISABLED       |
| 0 | 0 | 1 | 65,536 TpC     |
| 0 | 1 | 0 | 131,072 TpC    |
| 0 | 1 | 1 | 262,144 TpC    |
| 1 | 0 | 0 | 524,288 TpC    |
| 1 | 0 | 1 | 1,048,576 TpC  |
| 1 | 1 | 0 | 2,097,152 TpC  |
| 1 | 1 | 1 | 4,194,304 TpC* |

(XTAL CLOCKS TO TIMEOUT)

1 = WDT ENABLED IN HALT MODE\*  
0 = WDT DISABLED IN HALT MODE

\* Designates Default Value after RESET

Figure 12. Z8E000 TCTLHI Register for Control of WDT

**Note:** The WDT can only be disabled via software if the first instruction out of RESET performs this function. Logic within the Z8E000 will detect that it is in the process of executing the first instruction after the part leaves RESET. During the execution of this instruction, the upper five bits of the TCTLHI register can be written. After this first instruction, hardware will not allow the upper five bits of this register to be written.

The TCTLHI bits for control of the WDT are described below:

**WDT Time Select (D6, D5, D4).** Bits 6, 5, and 4 determine the time-out period. Table 7 indicates the range of time-out values that can be obtained. The default values of D6, D5, and D4 are all 1, thus setting the WDT to its maximum timeout period when coming out of RESET.

Table 7. Time-Out Period of the WDT

| D6 | D5 | D4 | Crystal Clocks to Timeout | Time-Out Using a10 MHz Crystal |
|----|----|----|---------------------------|--------------------------------|
| 0  | 0  | 0  | Disabled                  | Disabled                       |
| 0  | 0  | 1  | 65,536 TpC                | 6.55 ms                        |
| 0  | 1  | 0  | 131,072 TpC               | 13.11 ms                       |
| 0  | 1  | 1  | 262,144 TpC               | 26.21 ms                       |
| 1  | 0  | 0  | 524,288 TpC               | 52.43 ms                       |
| 1  | 0  | 1  | 1,048,576 TpC             | 104.86 ms                      |
| 1  | 1  | 0  | 2,097,152 TpC             | 209.72 ms                      |
| 1  | 1  | 1  | 4,194,304 TpC             | 419.43 ms                      |

**Notes:**

TpC = XTAL clock cycle.

The default on reset is D6 = D5 = D4 = 1.

**WDT During HALT (D7).** This bit determines whether or not the WDT is active during HALT Mode. A “1” indicates active during HALT. A “0” prevents the WDT from resetting the part while halted. Coming out of reset, the WDT will be enabled during HALT Mode.

**STOP MODE (D3).** Coming out of  $\overline{\text{RESET}}$ , the Z8E000 will have the STOP Mode disabled. If an application re-

quires use of STOP Mode, bit D3 must be cleared immediately upon leaving  $\overline{\text{RESET}}$ . If bit D3 is set, the STOP instruction will execute as a NOP. If bit D3 is cleared, the STOP instruction will enter Stop Mode. Whenever the Z8E000 wakes up after having been in STOP Mode, the STOP Mode will be disabled once again.

**Bits 2, 1 and 0.** These bits are reserved and must be 0.

---

## POWER-DOWN MODES

In addition to the standard RUN mode, the Z8E000 MCU supports two Power-Down modes to minimize device cur-

rent consumption. The two modes supported are HALT and STOP.

---

## HALT MODE OPERATION

The HALT Mode suspends instruction execution and turns off the internal CPU clock. The on-chip oscillator circuit remains active, so the internal clock continues to run and is applied to the timers and interrupt logic.

To enter the HALT Mode, the Z8E000 only requires a HALT instruction. It is NOT necessary to execute a NOP instruction immediately before the HALT instruction.

The HALT Mode can be exited by servicing an interrupt (either externally or internally). Upon completion of the interrupt service routine, the user program continues from the instruction after HALT.

The HALT Mode can also be exited via a  $\overline{\text{RESET}}$  activation or a Watch-Dog Timer (WDT) timeout. In these cases, program execution will restart at the reset address 0020H.

7F    HALT    ; enter HALT Mode

## STOP MODE OPERATION

The STOP Mode provides the lowest possible device standby current. This instruction turns off the on-chip oscillator and internal system clock.

To enter the STOP Mode, the Z8E000 only requires a STOP instruction. It is NOT necessary to execute a NOP instruction immediately before the STOP instruction.

6F STOP ;enter STOP Mode

The STOP Mode is exited by any one of the following resets: RESET pin or a STOP-Mode Recovery source. Upon reset generation, the processor will always restart the application program at address 0020H, thereby setting the STOP Mode Flag. Reading the STOP-Mode flag does not clear it. The user must clear the STOP-Mode flag with software.

**Note:** Failure to clear the STOP-Mode flag can result in undefined behavior.

The Z8E000 provides a dedicated STOP Mode Recovery (SMR) circuit. In this case, a low level applied to input pin PB0 will trigger a SMR. To use this mode, pin PB0 (I/O Port B, bit 0) must be configured as an input before the STOP Mode is entered. The low level on PB0 must be held for a minimum pulse width  $T_{WSM}$ , in addition to any oscillator startup time. Program execution starts at address 0020H after PBO is raised back to a high level.

**Notes:** Use of the PB0 input for the STOP mode recovery does not initialize the control registers.

The STOP Mode current ( $I_{CC2}$ ) will be minimized when:

- $V_{CC}$  is at the low end of the device's operating range.
- Output current sourcing is minimized.
- All inputs (digital and analog) are at the Low or High rail voltages.

## CLOCK

The Z8E000 MCU derives its timing from on-board clock circuitry connected to pins XTAL1 and XTAL2. The clock circuitry consists of an oscillator, a glitch filter, a divide-by-two shaping circuit, a divide-by-four shaping circuit, and a divide-by-eight shaping circuit. Figure 13 illustrates the clock circuitry. The oscillator's input is XTAL1 and its output is XTAL2. The clock can be driven by a crystal, a ceramic resonator, LC clock, or an external clock source.

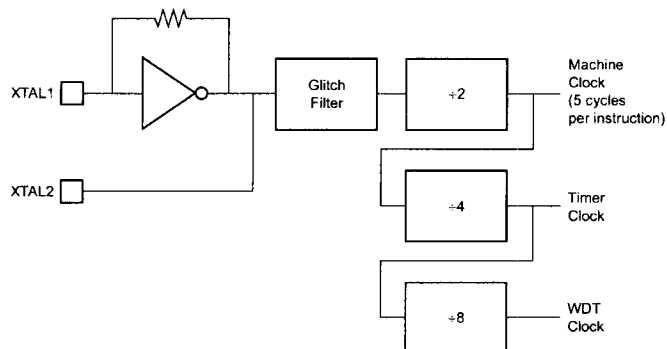


Figure 13. Z8E000 Clock Circuit

## OSCILLATOR OPERATION

The Z8E000 MCU uses a Pierce oscillator with an internal feedback circuit (Figure 14). The advantages of this circuit are low cost, large output signal, low power level in the crystal, stability with respect to  $V_{CC}$  and temperature, and low impedances (not disturbed by stray effects).

One draw back to the oscillator is the requirement for high gain in the amplifier to compensate for feedback path losses. The oscillator amplifies its own noise at start-up until it settles at the frequency that satisfies the gain/phase requirements ( $A \times B = 1$ , where  $A = V_o/V_i$  is the gain of the amplifier and  $B = V_i/V_o$  is the gain of the feedback element). The total phase shift around the loop is forced to zero (360 degrees).  $V_{IN}$  must be in phase with itself. The amplifier/inverter thereby provides a 180-degree phase shift, forcing the feedback element to provide the other 180 degrees of phase shift.

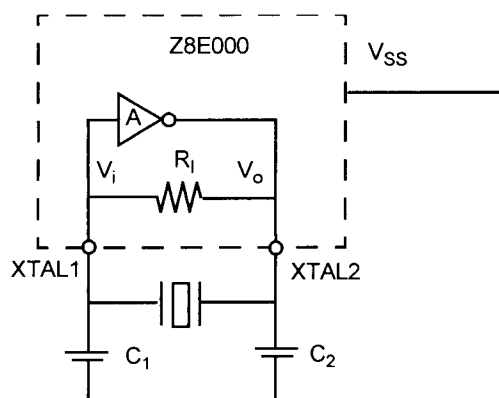
$R_1$  is a resistive component placed from output to input of the amplifier. The purpose of this feedback is to bias the amplifier in its linear region and to provide the start-up transition.

Capacitor  $C_2$ , combined with the amplifier output resistance, provides a small phase shift. It will also provide some attenuation of overtones.

Capacitor  $C_1$ , combined with the crystal resistance, provides additional phase shift.

$C_1$  and  $C_2$  can affect the start-up time if they increase dramatically in size. As  $C_1$  and  $C_2$  increase, the start-up time increases until the oscillator reaches a point where it does not start up any more.

It is recommended for fast and reliable oscillator start-up (over the manufacturing process range) that the load capacitors be sized as low as possible without resulting in overtone operation.



**Figure 14. Pierce Oscillator with Internal Feedback Circuit**

## Layout

Traces connecting crystal, caps, and the Z8E000 oscillator pins should be as short and wide as possible, to reduce parasitic inductance and resistance. The components (caps, crystal, resistors) should be placed as close as possible to the oscillator pins of the Z8E000.

The traces from the oscillator pins of the IC and the ground side of the lead caps should be guarded from all other traces (clock,  $V_{CC}$ , address/data lines, system ground) to reduce cross talk and noise injection. Guarding is usually accomplished by keeping other traces and system ground trace planes away from the oscillator circuit, and by placing a Z8E000 device  $V_{SS}$  ground ring around the traces/components. The ground side of the oscillator lead caps should be connected to a single trace of the Z8E000  $V_{SS}$  (GND) pin. The ground side of these caps should not be shared with any other system ground trace or components except at the Z8E000 device  $V_{SS}$  pin. The objective is to prevent differential system ground noise injection into the oscillator (Figure 15).

## Indications of an Unreliable Design

There are two major indicators that are used in working designs to determine their reliability over full lot and temperature variations. They are:

**Start-up Time.** If start-up time is excessive, or varies widely from unit to unit, there is probably a gain problem.  $C_1$  and  $C_2$  require reduction if the amplifier gain is not adequate at frequency, or crystal  $R$ 's are too large.

**Output Level.** The signal at the amplifier output should swing from ground to  $V_{CC}$  to indicate adequate gain in the amplifier. As the oscillator starts up, the signal amplitude grows until clipping occurs. At this point, the loop gain is effectively reduced to unity, and constant oscillation is achieved. A signal of less than 2.5 volts peak-to-peak is an indication that low gain can be a problem. Either  $C_1$  or  $C_2$  should be made smaller or a low-resistance crystal should be used.

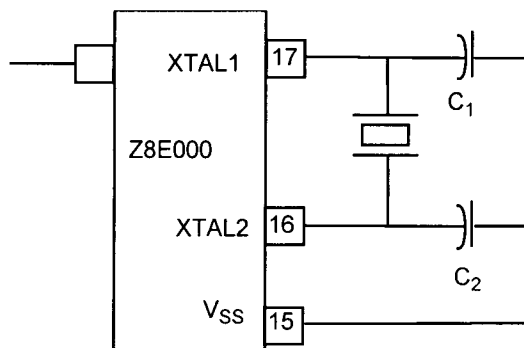
## Circuit Board Design Rules

The following circuit board design rules are suggested:

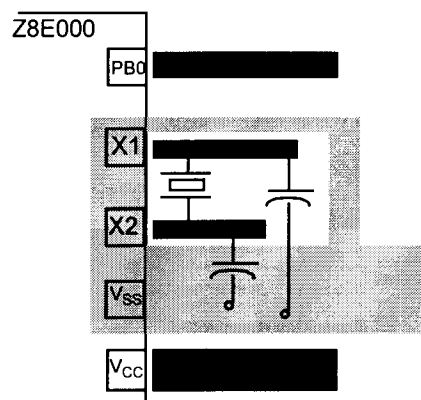
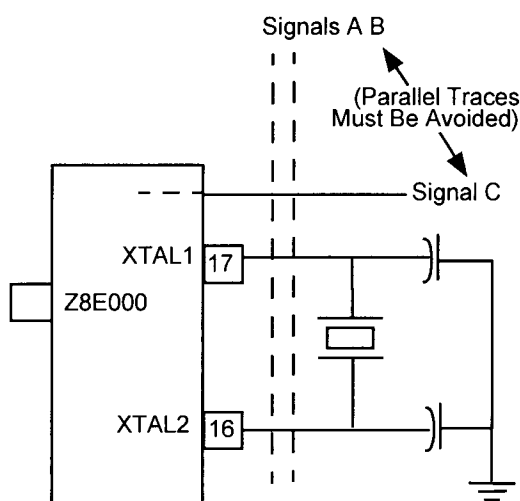
- To prevent induced noise, the crystal and load capacitors should be physically located as close to the Z8E000 as possible.
- Signal lines should not run parallel to the clock oscillator inputs. In particular, the crystal input circuitry and the internal system clock output should be separated as much as possible.

## OSCILLATOR OPERATION (Continued)

- $V_{CC}$  power lines should be separated from the clock oscillator input circuitry.
- Resistance between XTAL1 or XTAL2 and the other pins should be greater than  $10\text{ M}\Omega$ .



Clock Generator Circuit



Board Design Example  
(Top View)

Figure 15. Circuit Board Design Rules

## Crystals and Resonators

Crystals and ceramic resonators (Figure 16) should have the following characteristics to ensure proper oscillator operation:

|                     |                                                     |
|---------------------|-----------------------------------------------------|
| Crystal Cut         | AT (crystal only)                                   |
| Mode                | Parallel, Fundamental Mode                          |
| Crystal Capacitance | $<7\text{ pF}$                                      |
| Load Capacitance    | $10\text{ pF} < CL < 220\text{ pF}$ ,<br>15 typical |
| Resistance          | 100 ohms max                                        |

Depending on operation frequency, the oscillator can require the addition of capacitors  $C_1$  and  $C_2$  (shown in Figure 17 and Figure 18). The capacitance values are dependent on the manufacturer's crystal specifications.



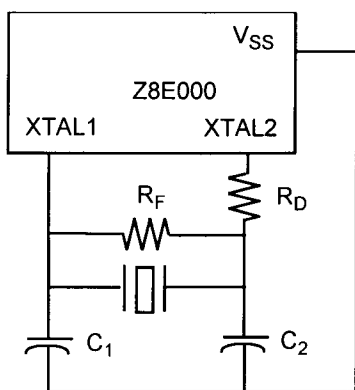


Figure 16. Crystal/Ceramic Resonator Oscillator

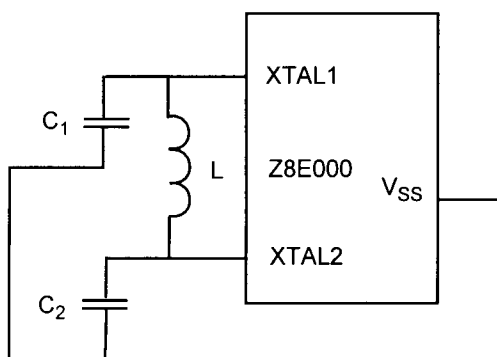


Figure 17. LC Clock

In most cases, the  $R_D$  is zero ohms ( $0\Omega$ ), and  $R_F$  is infinite. The set value is determined and specified by the crystal/ceramic resonator manufacturer.  $R_D$  can be increased to de-

crease the amount of drive from the oscillator output to the crystal.  $R_D$  can also be used as an adjustment to avoid clipping of the oscillator signal to reduce noise.  $R_F$  can be used to improve the start-up of the crystal/ceramic resonator. The Z8E000 oscillator already has an internal shunt resistor in parallel to the crystal/ceramic resonator.

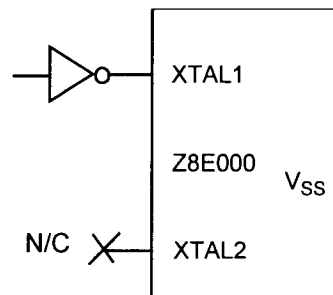


Figure 18. External Clock

Figure 16, Figure 17, and Figure 18 recommend that the load capacitor ground trace connect directly to the  $V_{SS}$  (GND) pin of the Z8E000, thereby ensuring that no system noise is injected into the Z8E000 clock. This trace should not be shared with any other components except at the  $V_{SS}$  pin of the Z8E000.

**Note:** A parallel resonant crystal or resonator data sheet will specify a load capacitor value that is the series combination of  $C_1$  and  $C_2$ , including all parasitics (PCB and holder).

## LC OSCILLATOR

The Z8E000 oscillator can use a LC network to generate a XTAL clock (Figure 18).

The frequency stays stable over  $V_{CC}$  and temperature. The oscillation frequency is determined by the equation:

$$\text{Frequency} = \frac{1}{2\pi (LC_T)^{1/2}}$$

where L is the total inductance including parasitics and  $C_T$  is the total series capacitance including the parasitics.

Simple series capacitance is calculated using the following equation:

$$\begin{aligned} \frac{1}{C_T} &= \frac{1}{C_1} + \frac{1}{C_2} \\ \text{If } C_1 &= C_2 \\ \frac{1}{C_T} &= \frac{2}{C_1} \\ C_1 &= 2 C_T \end{aligned}$$

A sample calculation of capacitance  $C_1$  and  $C_2$  for 5.83-MHz frequency and inductance value of 27  $\mu\text{H}$  is illustrated as follows:

$$5.83 (10^6) = \frac{1}{2\pi [2.7 (10^{-6}) C_T]^{1/2}}$$

$$C_T = 27.6 \text{ pf}$$

Thus  $C_1 = 55.2 \text{ pf}$  and  $C_2 = 55.2 \text{ pf}$ .

## TIMERS

Two 8-bit timers (T2 and T3), are provided but can only operate in cascade to function as a 16-bit standard timer (Figure 19).

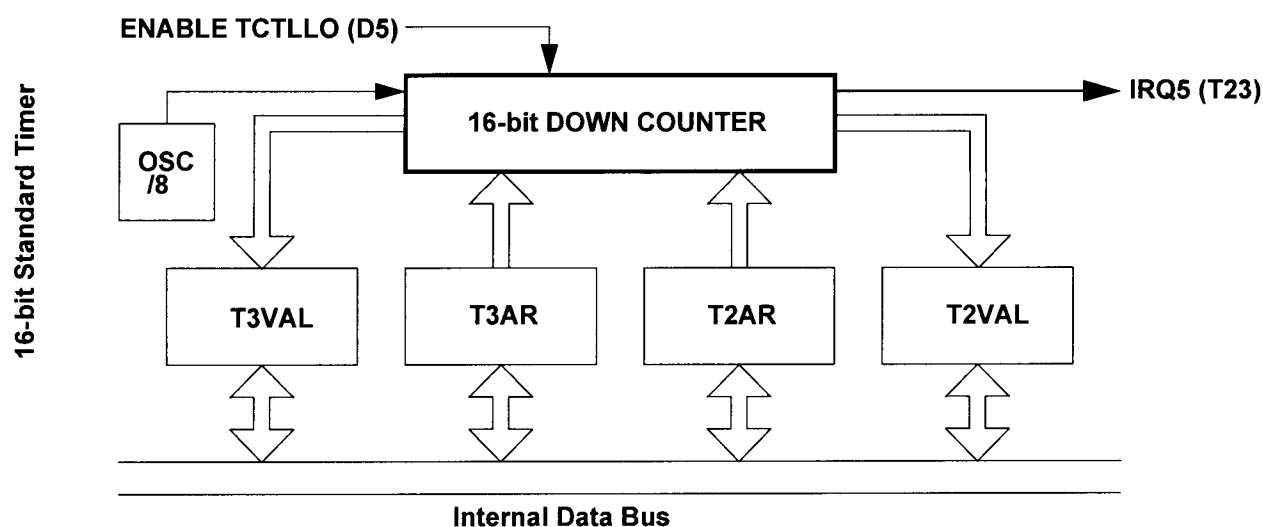
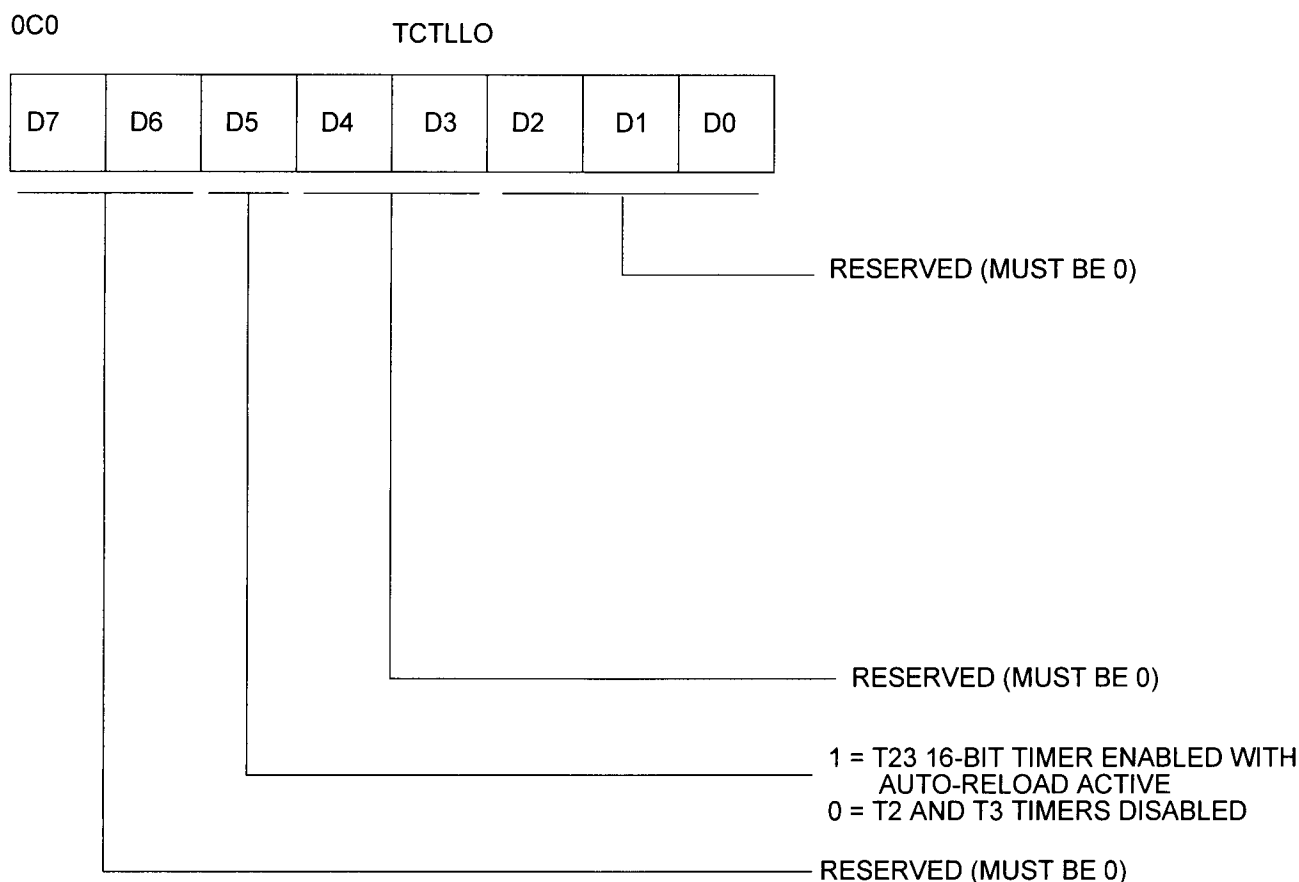


Figure 19. Timer Block Diagram



**Note:** Timer T23 is a standard 16-bit timer formed by cascading 8-bit timers t3(msb) and t2(lsb).

**Figure 20. TCTLLO Register**

Each 8-bit timer is equipped with a pair of readable and writable registers, which are both readable and writable. One of the registers is defined to contain the auto-initialization value for the timer, while the second register contains the current value for the timer. When a timer is enabled, the timer will decrement whatever value is currently held in its count register. From that point, the timer continues decrementing until it reaches 0, at which time an interrupt will be generated and the contents of the auto-initialization register are optionally copied into the count value register. If auto-initialization is not enabled, the timer will stop counting upon reaching 0, and control logic will clear the appropriate control register bit to disable the timer. This operation is referred to as a “single-shot”. If auto-initialization is enabled, the timer will continue counting from the initialization value. Software should not attempt to use registers that are defined as having timer functionality for any other purpose.

Software is allowed to write to any register at any time, but care should be taken if timer registers are updated while the timer is enabled. If software updates the count value while the timer is in operation, the timer will continue counting based upon the software-updated value. Strange behavior can result if the software update occurred at exactly the point that the timer was reaching 0 to trigger an interrupt and/or reload.

Similarly, if software updates the initialization value register while the timer is active, the next time that the timer reaches 0, it will be initialized using the updated value. Again, strange behavior could result if the initialization value register is being written while the timer is in the process of being initialized. Whether initialization is done with the new or old value is a function of the exact timing of the write operation. In all cases, the Z8E000 will prioritize the software write above that of a decremter writeback. However,

## TIMERS (Continued)

er, when hardware clears a control register bit for a timer that is configured for single-shot operation, the clearing of the control bit will override a software write. Reading either register can be done at any time, and will have no effect on the functionality of the timer.

When defined to operate as a single 16-bit entity, the entire 16-bit value must reach 0 before an interrupt is generated. In this case, a single interrupt will be generated, and the interrupt will correspond to the even 8-bit timer. For example, timers T2 and T3 are cascaded to form a single 16-bit timer, so the interrupt for the combined timer will be defined to be that of timer T2 rather than T3 (Figure 20). When a timer pair is specified to act as a single 16-bit timer, the even timer registers in the pair (timer T2) will be defined to hold the timer's least significant byte. Conversely, the odd timer in the pair (timer T3) will hold the timer's most significant byte.

In parallel with the posting of the interrupt request, the interrupting timer's count value will be initialized by copying

the contents of the auto-initialization value register to the count value register.

---

**Note:** Any time that a timer pair is defined to act as a single 16-bit timer, the auto-reload function will be performed automatically. All 16-bit timers will continue counting while their interrupt requests are active, and will operate in a free-running manner.

---

If interrupts are disabled for a long period of time, it is possible for the timer to decrement to 0 again before its initial interrupt has been responded to. This condition is termed a degenerate case, and hardware is not required to detect it.

When the timer control register is written, all timers that are enabled by the write will begin counting using the value that is held in their count register. In this case, an auto-initialization is not performed. All timers can receive an internal clock source only. Each timer that is enabled will be updated every 8th XTAL clock cycle.

## RESET CONDITIONS

After a hardware  $\overline{\text{RESET}}$ , the timers are disabled. See Table 5 for timer control, value, and auto-initialization register status after  $\overline{\text{RESET}}$ .

## I/O PORTS

The Z8E000 has 13 lines dedicated to input and output. These lines are grouped into two ports known as Port A and Port B. Port A is an 8-bit port that is bit-programmable as either inputs or outputs. Port B can be programmed to provide standard input/output or the following special functions: SMR input and external interrupt inputs.

All ports have push-pull CMOS outputs. In addition, the outputs of Port A, on a bit-wise basis, can be configured for open-drain operation. As such, the register values for “/” at a given bit position only affect the bit in question.

Each port is defined by a set of four control registers. See Figure 21.

### Directional Control and Special Function Registers

Each port on the Z8E000 has an associated and dedicated Directional Control Register that determines on a bit-wise basis whether a given port bit will operate as an input or as an output.

Each port on the Z8E000 has a Special Function Register that, in conjunction with the directional control register, implements on a bit-wise basis, and supports special functionality that can be defined for each particular port bit.

### Input and Output Value Registers

Each port has an Output Value Register and an Input Value Register. For port bits configured as an input by means of the Directional Control Register, the Input Value Register

for that bit position will contain the current synchronized input value.

| REGISTER                   | ADDRESS | IDENTIFIER |
|----------------------------|---------|------------|
| Port B SPECIAL FUNCTION    | 0D7H    | PTBSFR     |
| Port B DIRECTIONAL CONTROL | 0D6H    | PTBDIR     |
| Port B OUTPUT VALUE        | 0D5H    | PTBOUT     |
| Port B INPUT VALUE         | 0D4H    | PTBIN      |
| Port A SPECIAL FUNCTION    | 0D3H    | PTASFR     |
| Port A DIRECTIONAL CONTROL | 0D2H    | PTADIR     |
| Port A OUTPUT VALUE        | 0D1H    | PTAOUT     |
| Port A INPUT VALUE         | 0D0H    | PTAIN      |

**Figure 21. Z8E000 I/O Ports Registers**

For port bits configured as an output by means of the Directional Control Register, the value held in the corresponding bit of the Output Value Register is driven directly onto the output pin. The opposite register bit for a given pin (the output register bit for an input pin and the input register bit for an output pin) will hold their previous value. They will not be changed by hardware nor will they have any effect on the hardware.

## READ/WRITE OPERATIONS

The control for each port is done on a bit-wise basis. All bits are capable of operating as inputs or outputs, depending upon the setting of the port's directional control register. If configured as an input, each bit is provided a Schmitt-trigger. The output of the Schmitt-trigger is latched twice to perform a synchronization function, while the output of the synchronizer is fed to the port input register, which can be read by software.

A write to a port input register has the effect of updating the contents of the input register, but subsequent reads will not necessarily return the same value that was written. If the bit in question is defined as an input, the input register for that bit position will contain the current synchronized input value. Thus, writes to that bit position will be overwritten on the next clock cycle with the newly sampled input data. However, if the particular port bit is programmed as an output, the input register for that bit will retain the software-updated value. The port bits that are programmed as outputs do not sample the value being driven out.

Any bit in either port can be defined as an output by setting the appropriate bit in the directional control register. If such is the case, the value held in the appropriate bit of the port output register is driven directly onto the output pin.

---

**Note:** The above result does not necessarily reflect the actual output value. If an external error is holding an output pin

either High or Low against the output driver, the software read will return the *required* value, not the actual state caused by the contention. When a bit is defined as an output, the Schmitt-trigger on the input will be disabled to save power.

---

Updates to the output register will take effect based upon the timing of the internal instruction pipeline; however, this timing is referenced to the rising edge of the clock. The output register can be read at any time, and will return the current output value that is held. No restrictions are placed on the timing of reads and/or writes to any of the port registers with respect to the others, but care should be taken when updating the directional control and special function registers.

When updating a directional control register, the special function register should first be disabled. If this precaution is not taken, spurious events could take place as a result of the change in port I/O status. This precaution is especially important when defining changes in Port B, as the spurious event referred to above could be one or more interrupts. Clearing of the SFR register should be the first step in configuring the port, and setting the SFR register should be the final step in the port configuration process. To ensure deterministic behavior, the SFR register should not be written until the pins are being driven appropriately and all initialization has been completed.

## PORT A

Port A is a general-purpose port (Figure 23). Each of its lines can be independently programmed as input or output via the Port A Directional Control Register (PTADIR at 0D2H) as seen in Figure 22. A bit set to a “1” in PTADIR configures the corresponding bit in Port A as an output, while a bit cleared to “0” configures the corresponding bit in Port A as an input.

The input buffers are Schmitt-triggered. Bits programmed as outputs can be individually programmed as either push-pull or open drain by setting the corresponding bit in the Special Function Register (PTASFR, Figure 27.)

Register 0D2H  
PTADIR Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
|----|----|----|----|----|----|----|----|

1 = Output  
0 = Input

Figure 22. Port A Directional Control Register

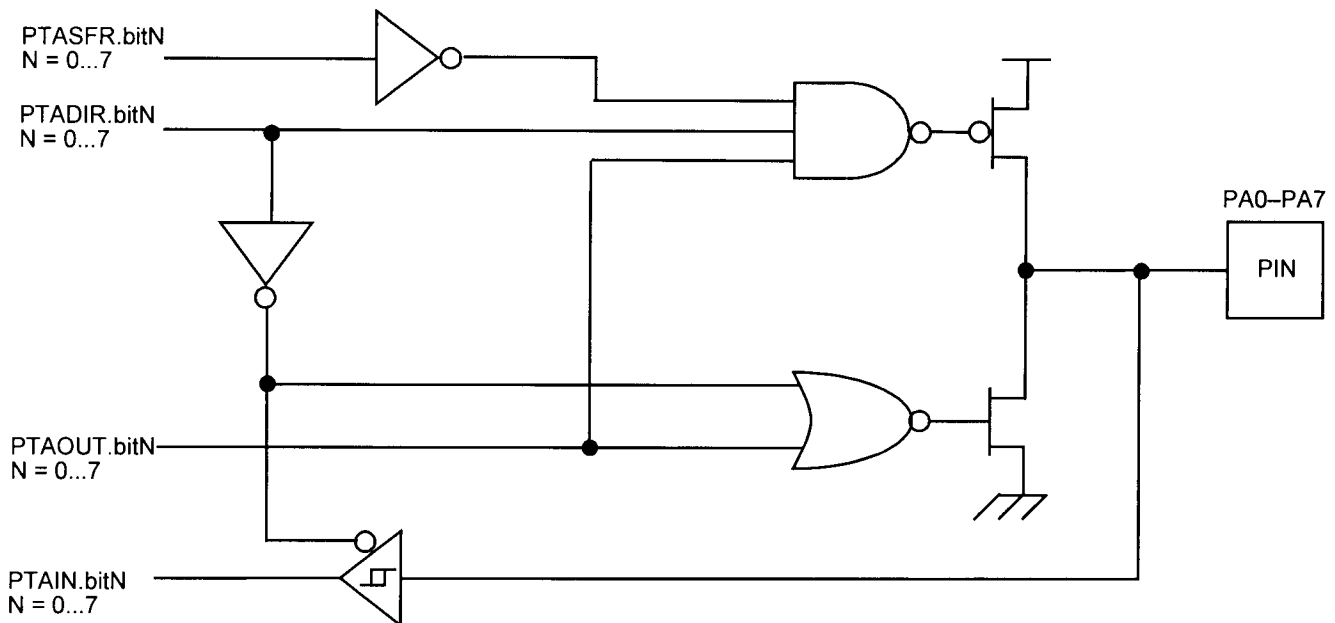


Figure 23. Port A Configuration with Open-Drain Capability and Schmitt-Trigger

PORT A REGISTER DEFINITIONS

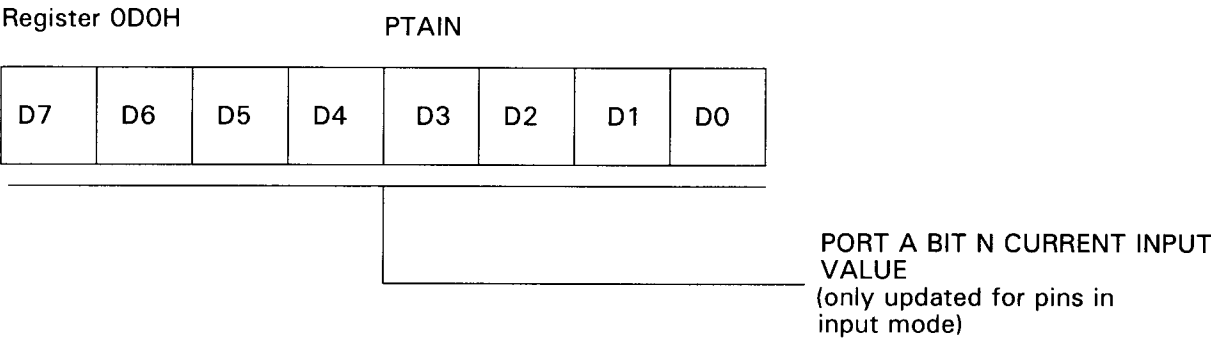


Figure 24. Port A Input Value Register

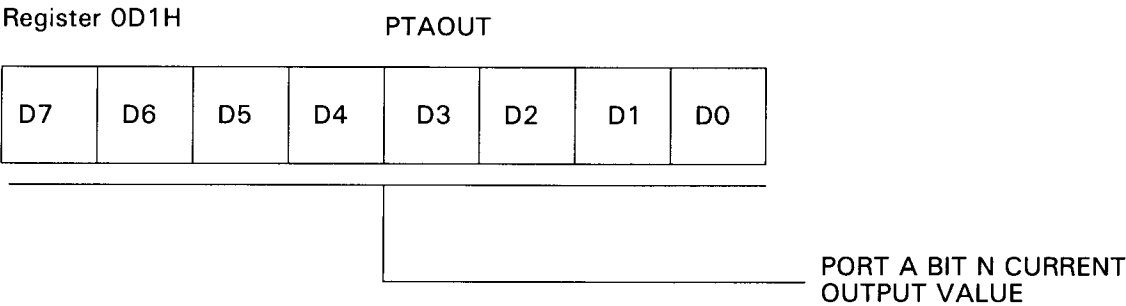


Figure 25. Port A Output Value Register



Register 0D2H

PTADIR

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
|----|----|----|----|----|----|----|----|

1 = BIT N SET AS AN OUTPUT

0 = BIT N SET AS AN INPUT

**Figure 26. Port A Directional Control Register**

Register 0D3H

PTASFR

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
|----|----|----|----|----|----|----|----|

1 = BIT N IN OPEN-DRAIN MODE

0 = BIT N IN PUSH-PULL MODE

**Figure 27. Port A Special Function Register**

## PORT B

### Port B Description

Port B is a 5-bit, bidirectional, CMOS-compatible I/O port. These five I/O lines can be configured under software control to be an input or output, independently. Input buffers are Schmitt-triggered. See Figure 29 through Figure 33 for diagrams of all five Port B pins.

In addition to standard input/output capability on all five pins of Port B, each pin provides special functionality as indicated in Table 8:

Table 8. Port B Special Functions

| Port Pin | Input Special Function   | Output Special Function |
|----------|--------------------------|-------------------------|
| PB0      | Stop Mode Recovery Input | None                    |
| PB1      | None                     | None                    |
| PB2      | IRQ3                     | None                    |
| PB3      | None                     | None                    |
| PB4      | IRQ1/IRQ4                | None                    |

Special functionality is invoked via the Port B Special Function Register. See Figure 28 for the arrangement and control conventions for this register.

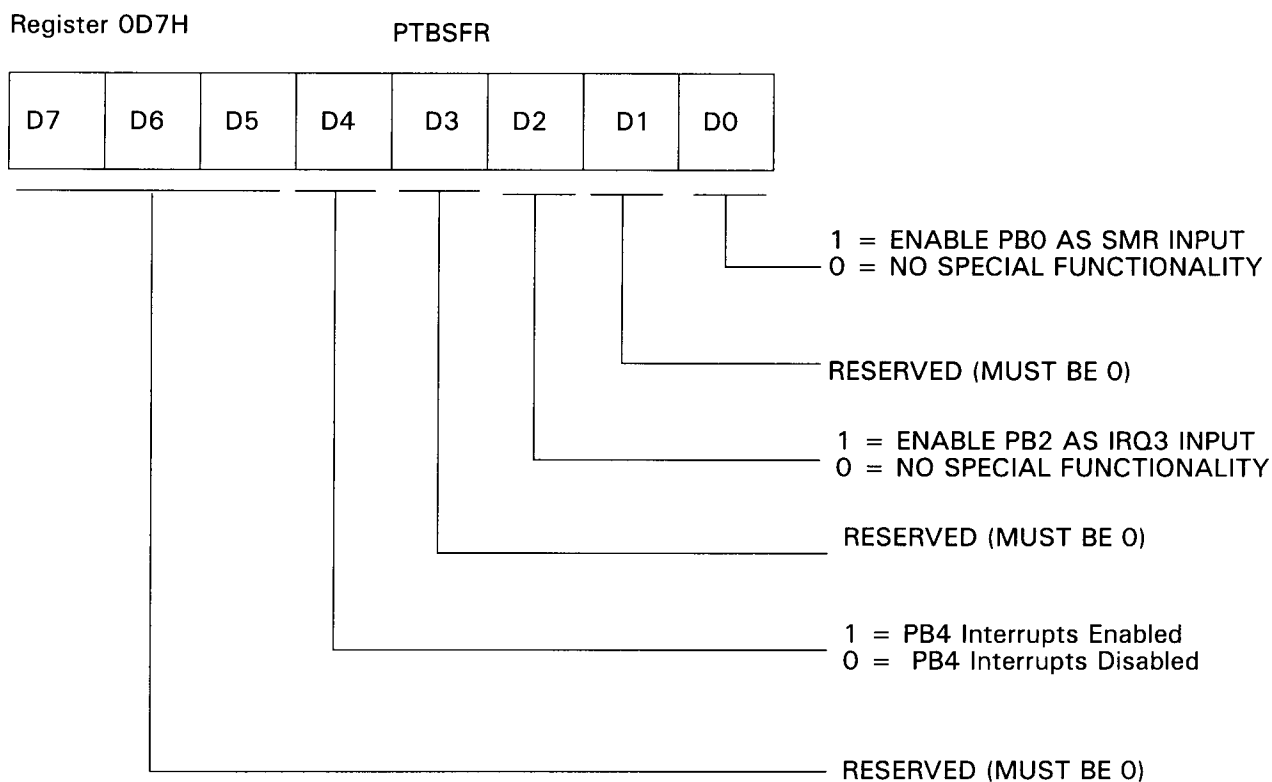


Figure 28. Port B Special Function Register

## PORT B—PIN 0 CONFIGURATION

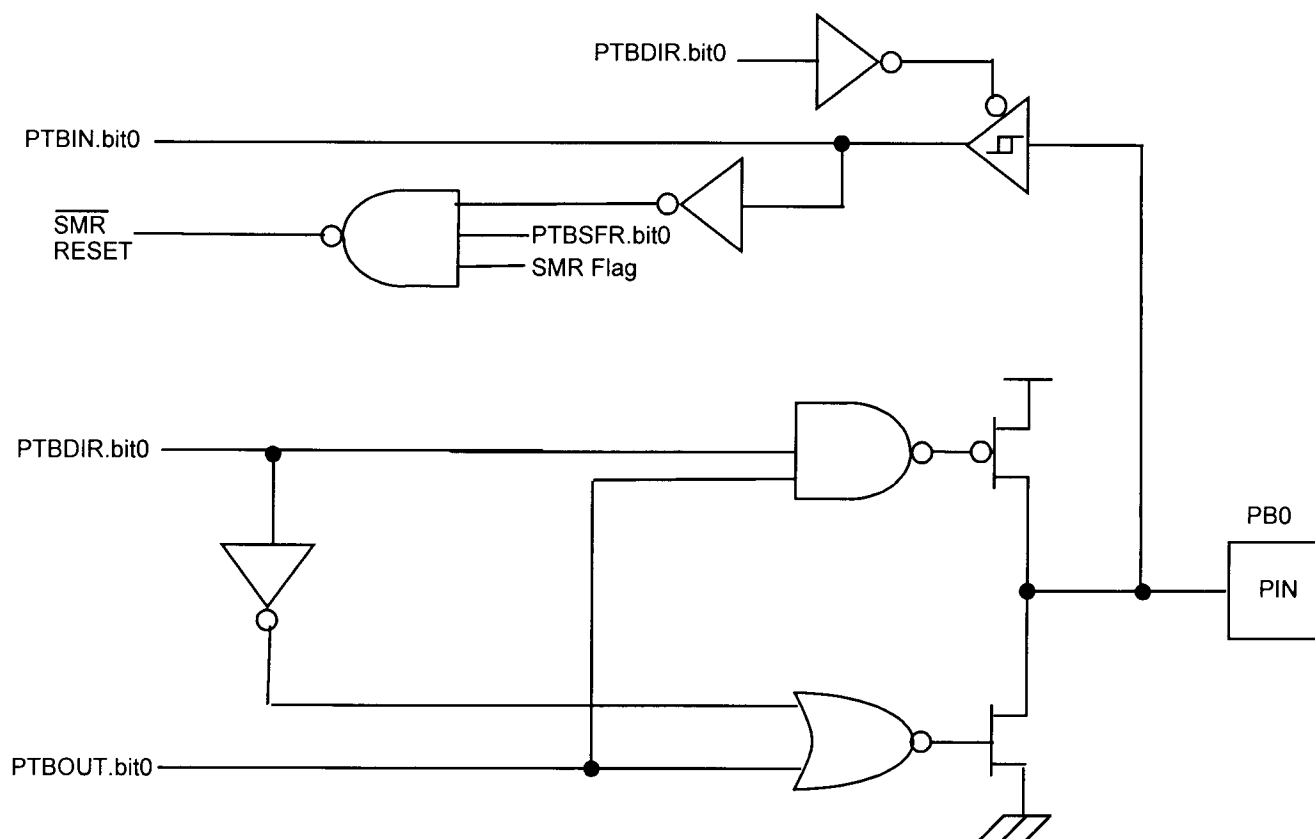


Figure 29. Port B Pin 0 Diagram

PORT B—PIN 1 CONFIGURATION

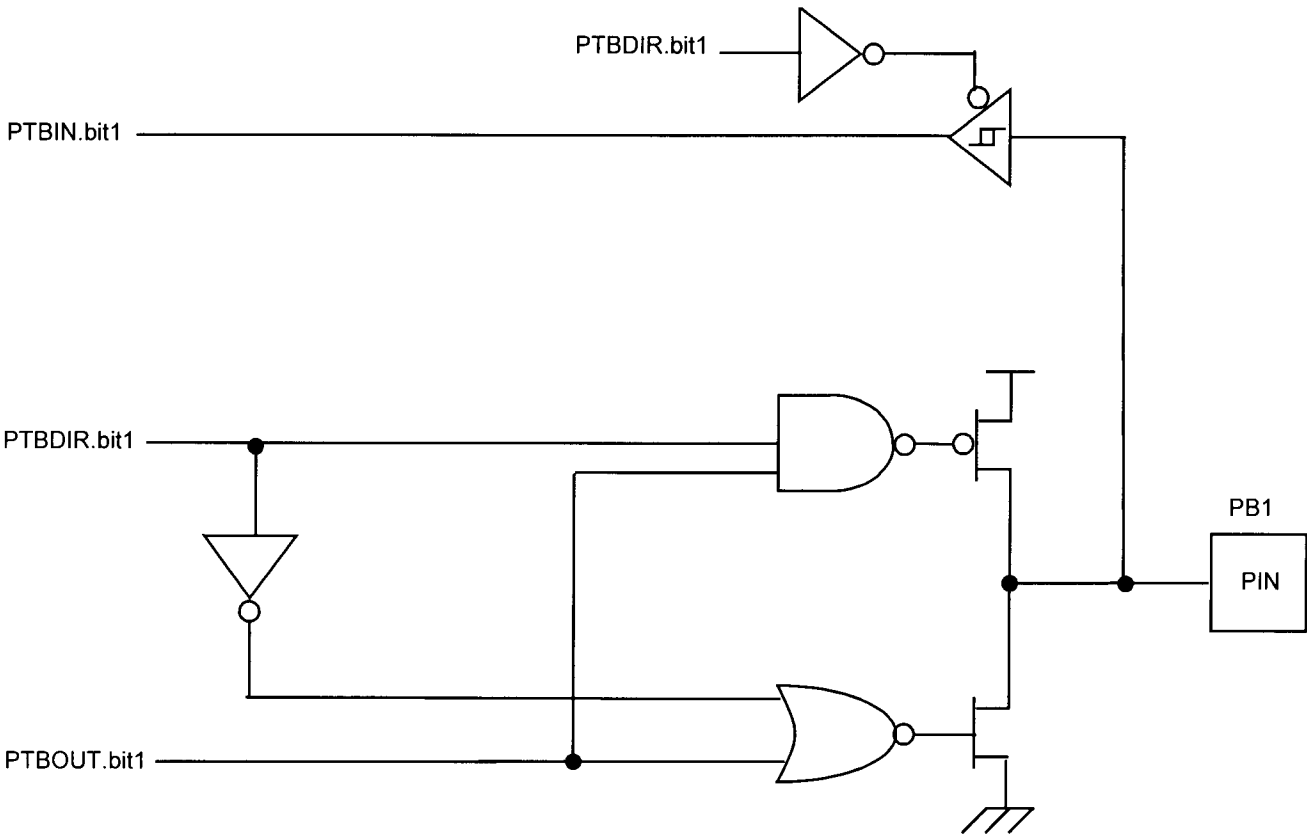


Figure 30. Port B Pin 1 Diagram

## PORT B—PIN 2 CONFIGURATION

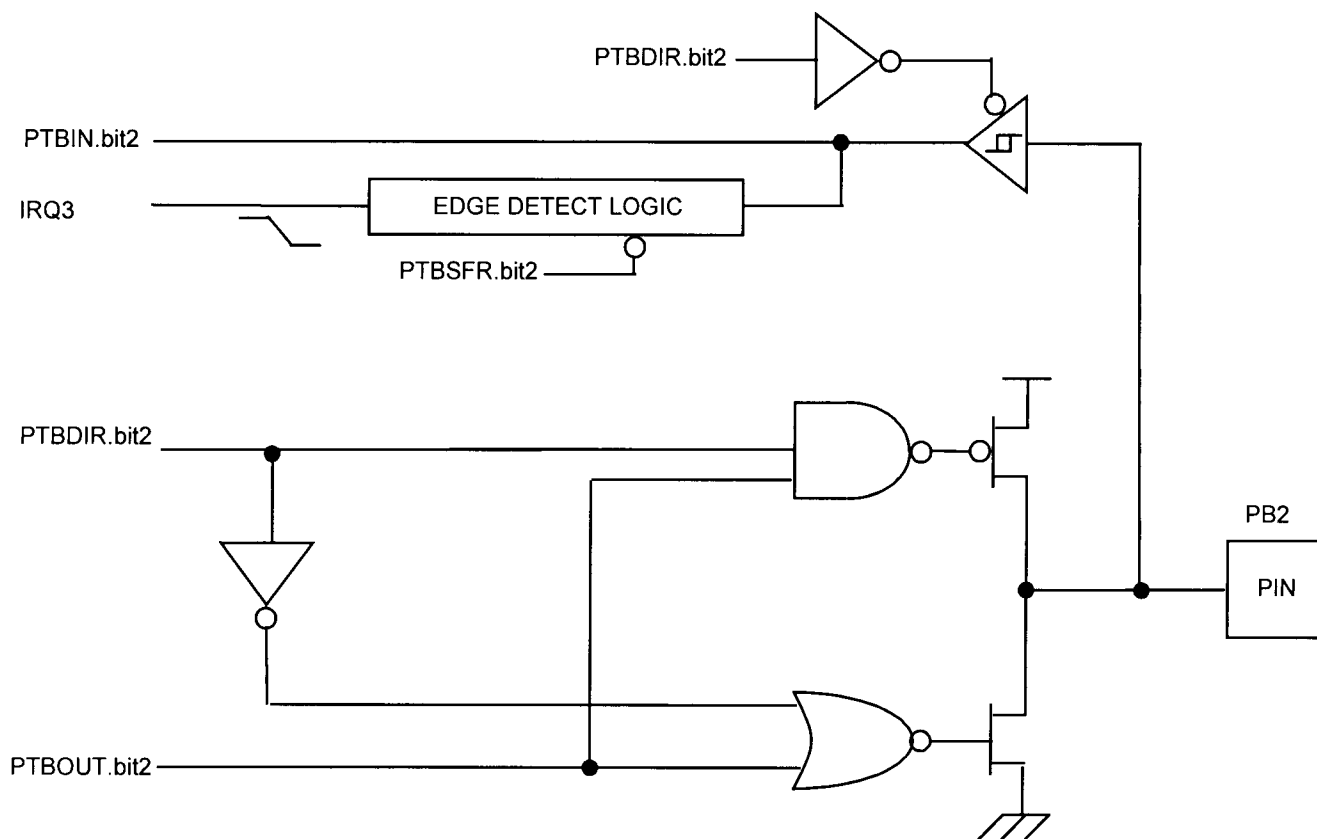


Figure 31. Port B Pin 2 Diagram

## PORT B—PINS 3 AND 4 CONFIGURATION

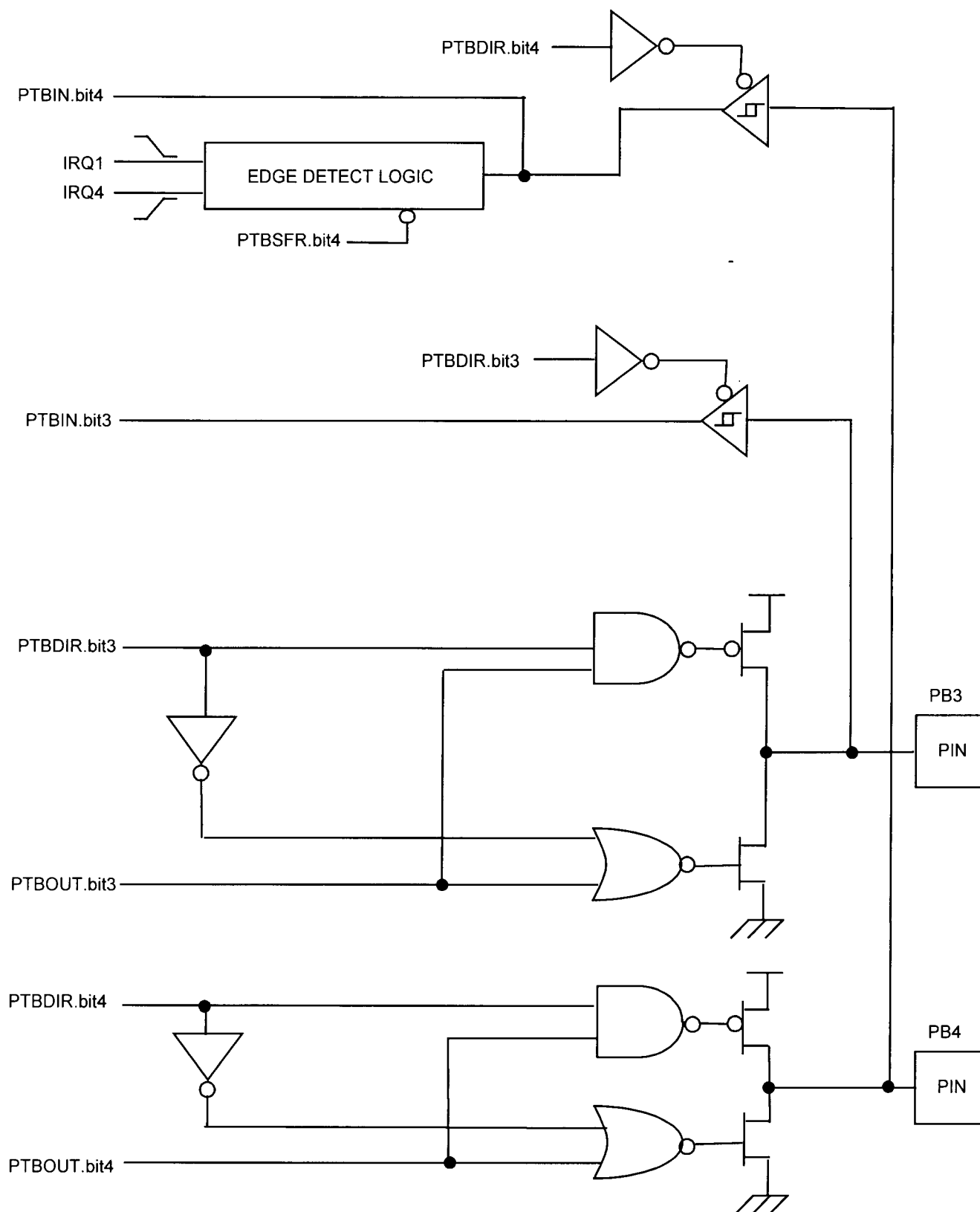


Figure 32. Port B Pins 3 and 4 Diagram

## PORT B CONTROL REGISTER DEFINITIONS

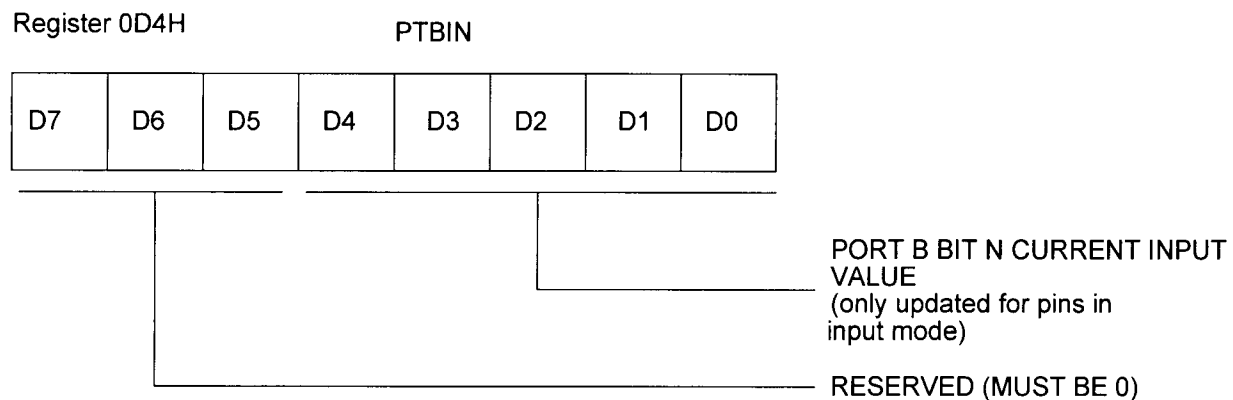


Figure 33. Port B Input Value Register

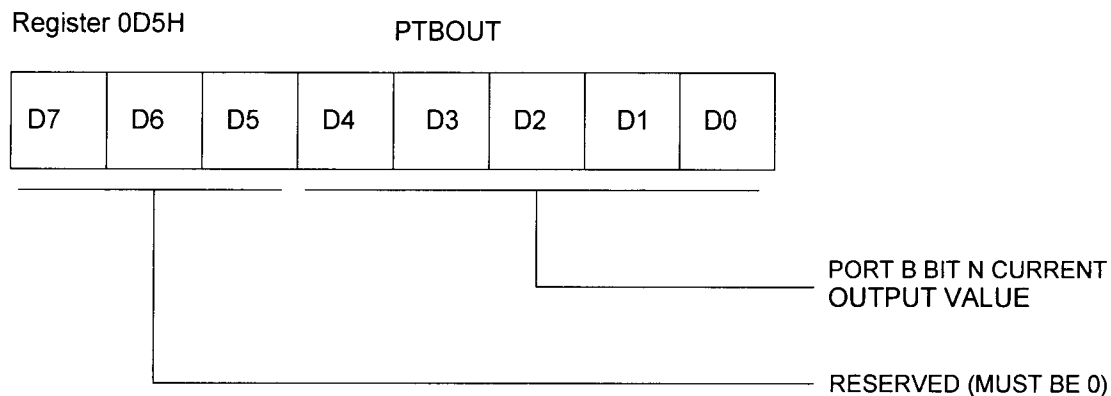


Figure 34. Port B Output Value Register

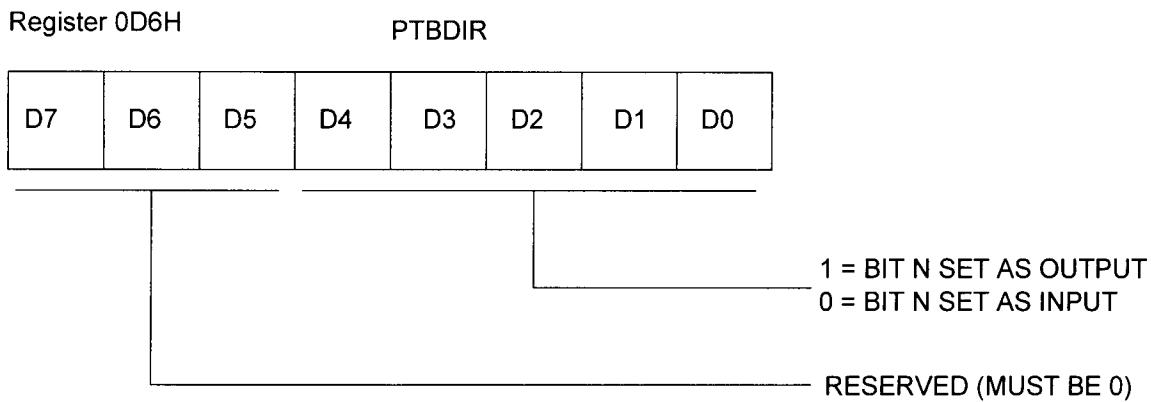


Figure 35. Port B Directional Control Register

PORT B CONTROL REGISTER DEFINITIONS (Continued)

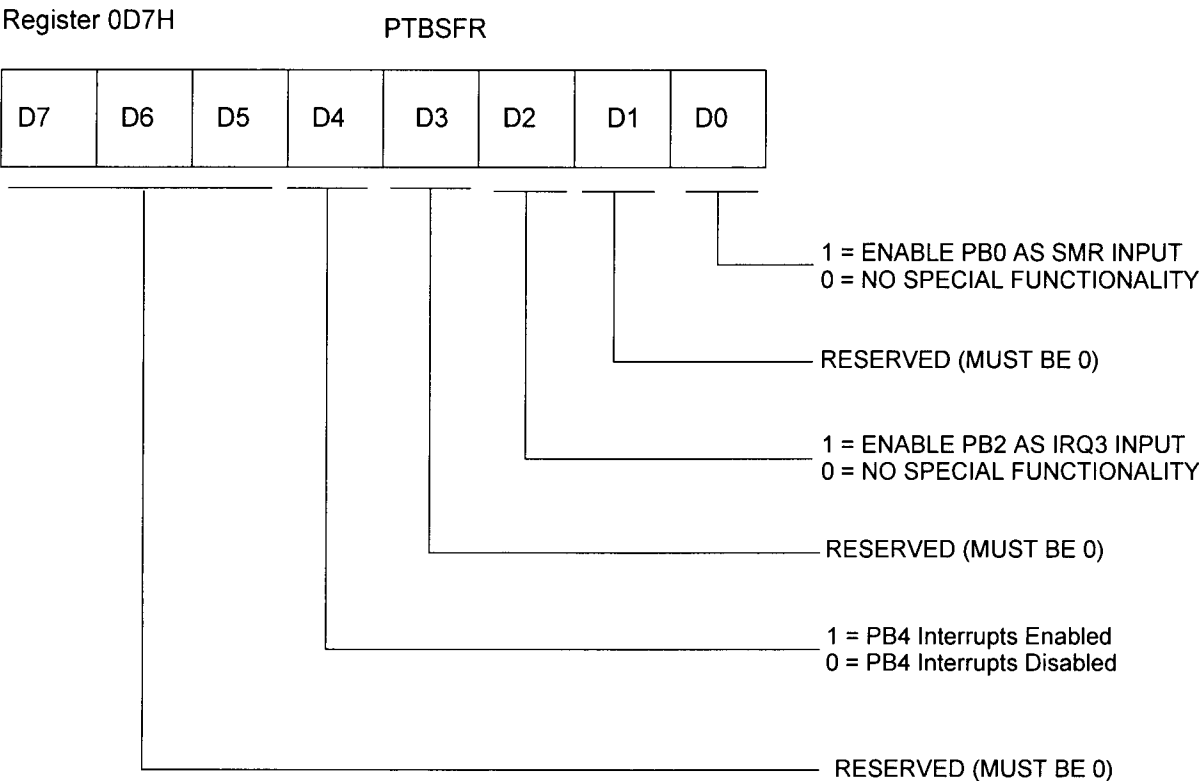


Figure 36. Port B Special Function Register



## I/O PORT RESET CONDITIONS

### Full Reset

Port A and Port B output value registers are not affected by  $\overline{\text{RESET}}$ .

On  $\overline{\text{RESET}}$ , the Port A and Port B directional control registers will be cleared to all zeros, which will define all pins in both ports as inputs.

On  $\overline{\text{RESET}}$ , the directional control registers redefine all pins as inputs, and the Port A and Port B input value registers

will overwrite the previously held data with the current sample of the input pins.

On  $\overline{\text{RESET}}$ , the Port A and Port B special function registers will be cleared to all zeros, which will deactivate all port special functions.

---

**Note:** The SMR and WDT timeout events are NOT full device resets. None of the port control registers is affected by either of these events.

---

## INPUT PROTECTION

All I/O pins on the Z8E000 have diode input protection. There is a diode from the I/O pad to  $V_{CC}$  and to  $V_{SS}$ . See Figure 37.

However, on the Z8E000, the  $\overline{\text{RESET}}$  pin has only the input protection diode from the pad to  $V_{SS}$ . See Figure 38.

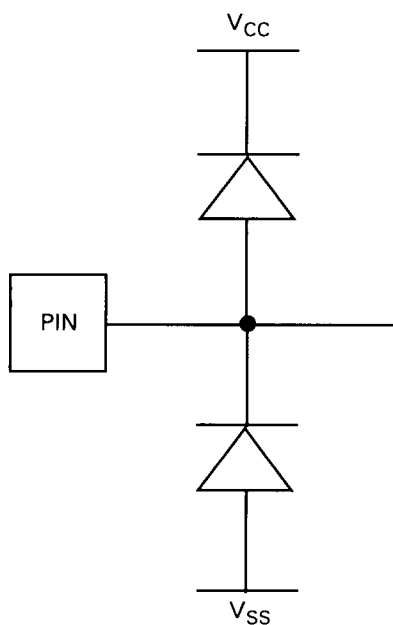


Figure 37. I/O Pin Diode Input Protection

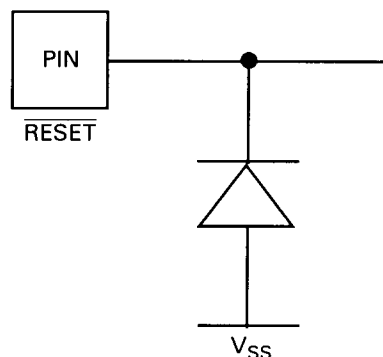
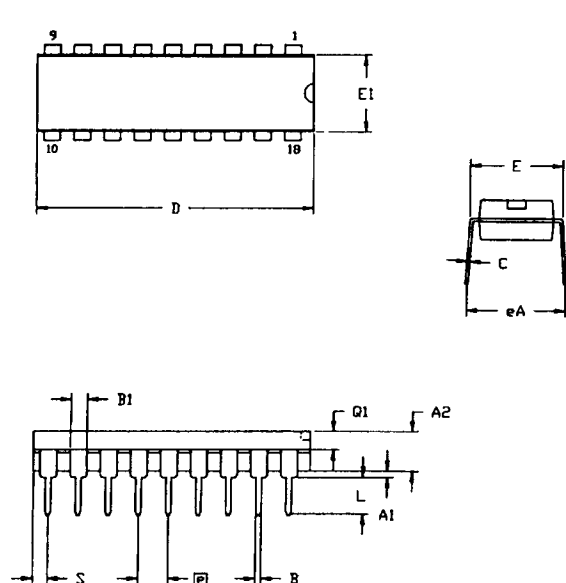


Figure 38.  $\overline{\text{RESET}}$  Pin Input Protection

The High-side input protection diode was removed on this pin to allow the application of high voltage during the OTP programming mode.

For better noise immunity in applications that are exposed to system EMI, a clamping diode to  $V_{CC}$  from this pin is required to prevent entering the OTP programming mode, or to prevent high voltage from damaging this pin.

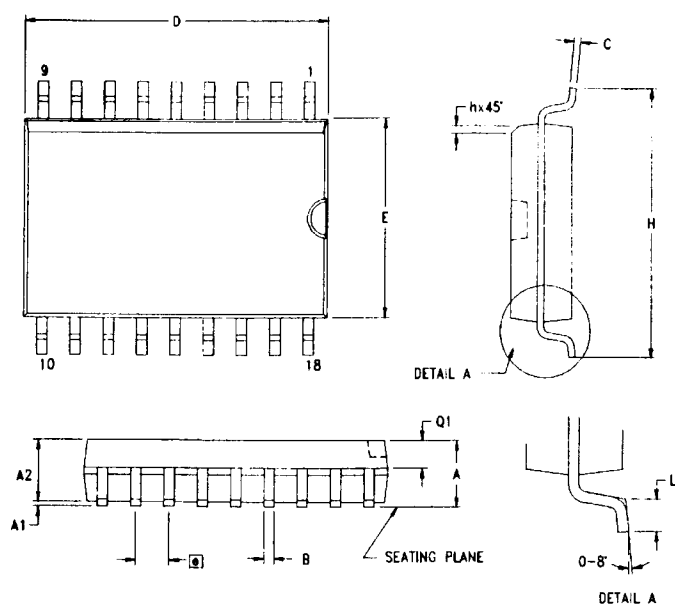
## PACKAGE INFORMATION



| SYMBOL | MILLIMETER |       | INCH     |      |
|--------|------------|-------|----------|------|
|        | MIN        | MAX   | MIN      | MAX  |
| A1     | 0.51       | 0.81  | .020     | .032 |
| A2     | 3.25       | 3.43  | .128     | .135 |
| B      | 0.38       | 0.53  | .015     | .021 |
| B1     | 1.14       | 1.65  | .045     | .065 |
| C      | 0.23       | 0.38  | .009     | .015 |
| D      | 22.35      | 23.37 | .880     | .920 |
| E      | 7.62       | 8.13  | .300     | .320 |
| E1     | 6.22       | 6.48  | .245     | .255 |
| ⌀      | 2.54 TYP   |       | .100 TYP |      |
| eA     | 7.87       | 8.89  | .310     | .350 |
| L      | 3.18       | 3.81  | .125     | .150 |
| Q1     | 1.52       | 1.65  | .060     | .065 |
| S      | 0.89       | 1.65  | .035     | .065 |

CONTROLLING DIMENSIONS : INCH

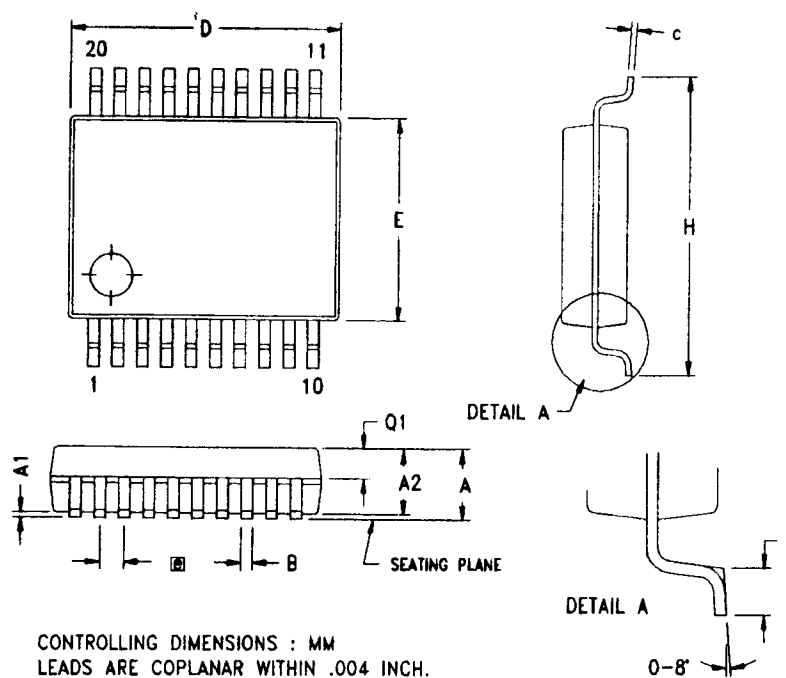
Figure 39. 18-Pin DIP Package Diagram



| SYMBOL | MILLIMETER |       | INCH      |       |
|--------|------------|-------|-----------|-------|
|        | MIN        | MAX   | MIN       | MAX   |
| A      | 2.40       | 2.65  | 0.094     | 0.104 |
| A1     | 0.10       | 0.30  | 0.004     | 0.012 |
| A2     | 2.24       | 2.44  | 0.088     | 0.096 |
| B      | 0.36       | 0.46  | 0.014     | 0.018 |
| C      | 0.23       | 0.30  | 0.009     | 0.012 |
| D      | 11.40      | 11.75 | 0.449     | 0.463 |
| E      | 7.40       | 7.60  | 0.291     | 0.299 |
| ⌀      | 1.27 TYP   |       | 0.050 TYP |       |
| H      | 10.00      | 10.65 | 0.394     | 0.419 |
| h      | 0.30       | 0.50  | 0.012     | 0.020 |
| L      | 0.60       | 1.00  | 0.024     | 0.039 |
| Q1     | 0.97       | 1.07  | 0.038     | 0.042 |

CONTROLLING DIMENSIONS : MM  
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 40. 18-Pin SOIC Package Diagram



| SYMBOL | MILLIMETER |      |      | INCH       |       |       |
|--------|------------|------|------|------------|-------|-------|
|        | MIN        | NOM  | MAX  | MIN        | NOM   | MAX   |
| A      | 1.73       | 1.85 | 1.98 | 0.068      | 0.073 | 0.078 |
| A1     | 0.05       | 0.13 | 0.21 | 0.002      | 0.005 | 0.008 |
| A2     | 1.68       | 1.73 | 1.83 | 0.066      | 0.068 | 0.072 |
| B      | 0.25       | 0.30 | 0.38 | 0.010      | 0.012 | 0.015 |
| C      | 0.13       | 0.15 | 0.22 | 0.005      | 0.006 | 0.009 |
| D      | 7.07       | 7.20 | 7.33 | 0.278      | 0.283 | 0.289 |
| E      | 5.20       | 5.30 | 5.38 | 0.205      | 0.209 | 0.212 |
| ⓐ      | 0.65 TYP   |      |      | 0.0256 TYP |       |       |
| H      | 7.65       | 7.80 | 7.90 | 0.301      | 0.307 | 0.311 |
| L      | 0.56       | 0.75 | 0.94 | 0.022      | 0.030 | 0.037 |
| Q1     | 0.74       | 0.78 | 0.82 | 0.029      | 0.031 | 0.032 |

Figure 41. 20-Pin SSOP Package Diagram

## ORDERING INFORMATION

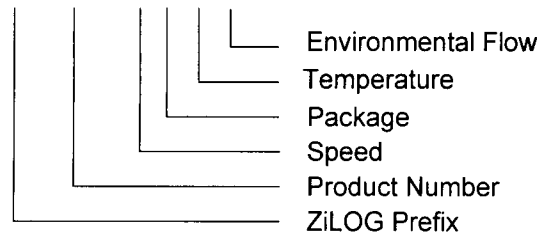
| Standard Temperature |             |             |
|----------------------|-------------|-------------|
| 18-Pin DIP           | 18-Pin SOIC | 20-Pin SSOP |
| Z8E00010PSC          | Z8E00010SSC | Z8E00010HSC |
| Extended Temperature |             |             |
| 18-Pin DIP           | 18-Pin SOIC | 20-Pin SSOP |
| Z8E00010PEC          | Z8E00010SEC | Z8E00010HEC |

For fast results, contact your local ZiLOG sales office for assistance in ordering the part(s) required.

| Codes                 |                                         |
|-----------------------|-----------------------------------------|
| Preferred Package     | P = Plastic DIP                         |
| Longer Lead Time      | S = SOIC<br>H = SSOP                    |
| Preferred Temperature | S = 0°C to +70°C<br>E = -40°C to +105°C |
| Speed                 | 10 = 10 MHz                             |
| Environmental         | C = Plastic Standard                    |

Example:

Z 8E000 10 P S C is a Z86E000, 10 MHz, DIP, 0° to +70°C, Plastic Standard Flow



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The product represented by this data sheet is newly introduced and ZiLOG has not completed the full characterization of the product. The data sheet states what ZiLOG knows about this product at this time, but additional features or nonconformance with some aspects

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