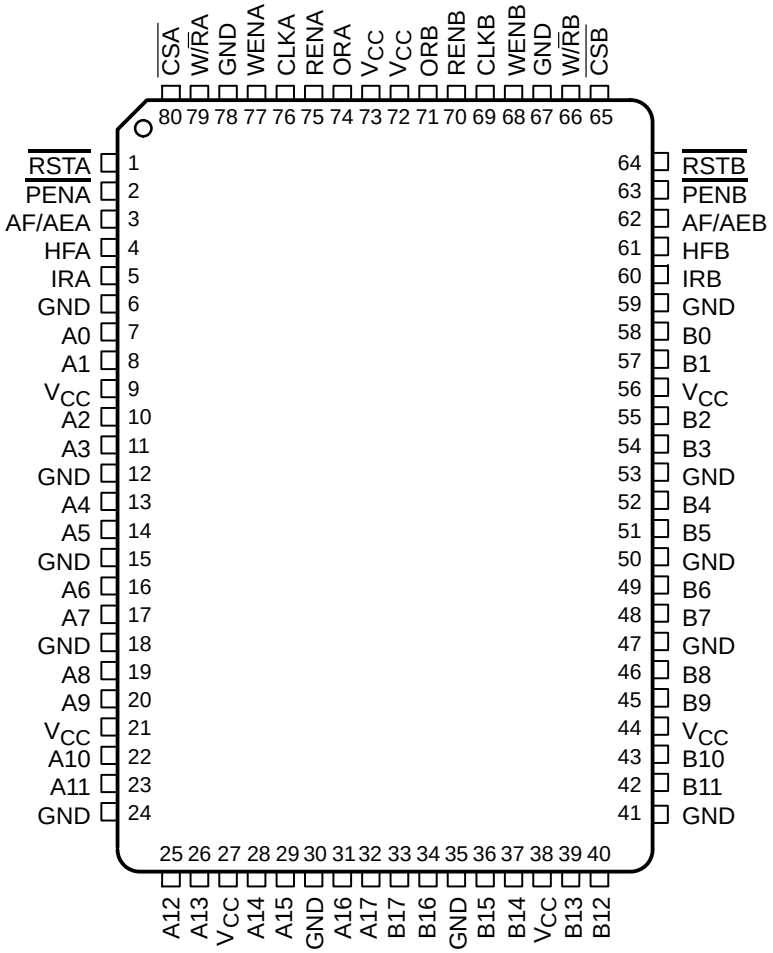
- **Member of the Texas Instruments Widebus™ Family**
- **Free-Running CLKA and CLKB Can Be Asynchronous or Coincident**
- **Read and Write Operations Synchronized to Independent System Clocks**
- **Two Separate 512 × 18 Clocked FIFOs Buffering Data in Opposite Directions**
- **IRA and ORA Synchronized to CLKA**
- **IRB and ORB Synchronized to CLKB**
- **Microprocessor Interface Control Logic**
- **Programmable Almost-Full/Almost-Empty Flag**
- **Fast Access Times of 9 ns With a 50-pF Load and Simultaneous Switching Data Outputs**
- **Data Rates up to 100 MHz**
- **Advanced BiCMOS Technology**
- **Package Options Include 80-Pin Plastic Quad Flatpack (PH) and 80-Pin Thin Plastic Quad Flatpack (PN)**

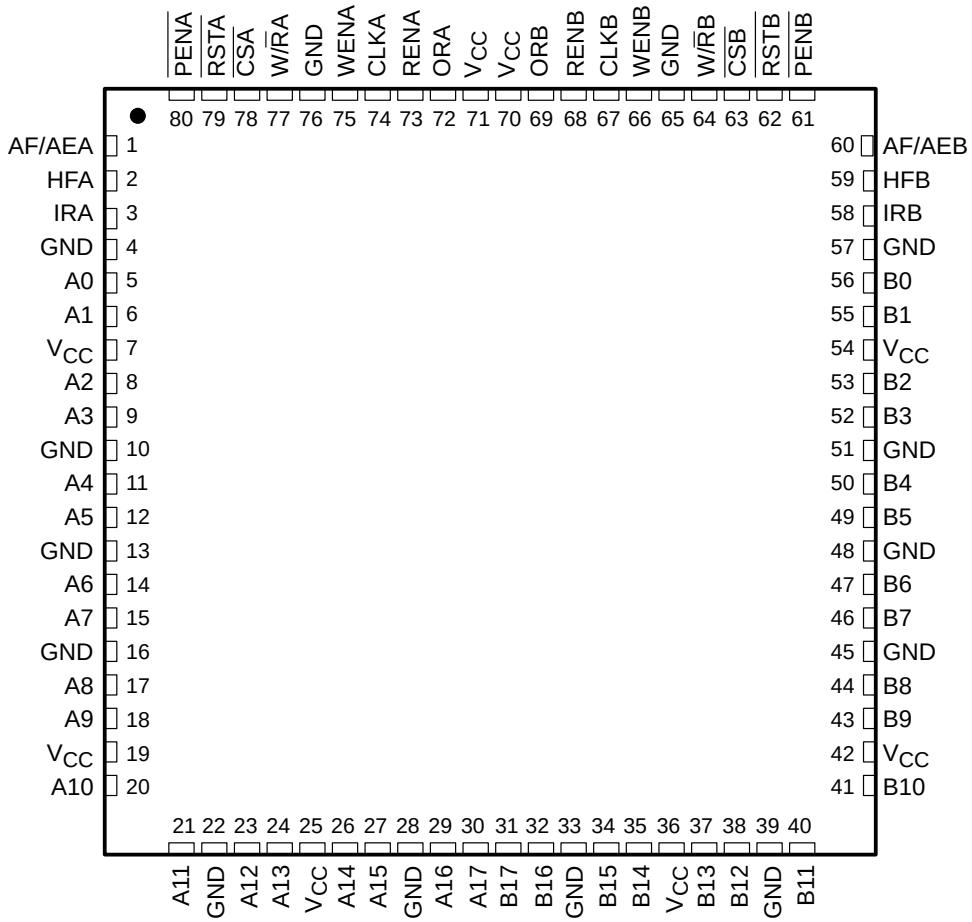
PH PACKAGE
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

PN PACKAGE
(TOP VIEW)



description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ABT7819A is a high-speed, low-power, BiCMOS, bidirectional, clocked FIFO memory. Two independent 512 × 18 dual-port SRAM FIFOs (FIFOA, FIFOB) on the chip buffer data in opposite directions. Each FIFO has flags to indicate empty and full conditions, a half-full flag, and a programmable almost-full/almost-empty flag.

The SN74ABT7819A is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the low-to-high transition of a continuous (free-running) port clock by enable signals. The continuous clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses with synchronous control.

The state of the A0–A17 outputs is controlled by the port-A chip select ($\overline{CSA}$) and the port-A write/read select (W/$\overline{R}$A). When both $\overline{CSA}$ and W/$\overline{R}$A are low, the outputs are active. The A0–A17 outputs are in the high-impedance state when either $\overline{CSA}$ or W/$\overline{R}$A is high. Data is written to FIFOA–B from port A on the low-to-high transition of the port-A clock (CLKA) input when $\overline{CSA}$ is low, W/$\overline{R}$A is high, the port-A write enable (WENA) is high, and the port-A input-ready ($\overline{IRA}$) flag is high. Data is read from FIFOB–A to the A0–A17 outputs on the low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{R}$A is low, the port-A read enable (RENA) is high, and the port-A output-ready (ORA) flag is high.

description (continued)

The state of the B0–B17 outputs is controlled by the port-B chip select ($\overline{CSB}$) and the port-B write/read select (W/$\overline{R}$B). When both $\overline{CSB}$ and W/$\overline{R}$B are low, the outputs are active. The B0–B17 outputs are in the high-impedance state when either $\overline{CSB}$ or W/$\overline{R}$B is high. Data is written to FIFOB–A from port B on the low-to-high transition of the port-B clock (CLKB) when $\overline{CSB}$ is low, W/$\overline{R}$B is high, the port-B write enable (WENB) is high, and the port-B input-ready (IRB) flag is high. Data is read from FIFOA–B to the B0–B17 outputs on the low-to-high transition of CLKB when $\overline{CSB}$ is low, W/$\overline{R}$B is low, the port-B read enable (RENB) is high, and the port-B output-ready (ORB) flag is high.

The setup- and hold-time constraints for the chip selects ($\overline{CSA}$, $\overline{CSB}$) and write/read selects (W/$\overline{R}$A, W/$\overline{R}$B) enable write and read operations on memory and are not related to the high-impedance control of the data outputs. If a port read enable (RENA or RENB) and write enable (WENA or WENB) are set low during a clock cycle, the chip select and write/read select can switch at any time during the cycle to change the state of the data outputs.

The input-ready (IR) and output-ready (OR) flags of a FIFO are two-stage synchronized to the port clocks for use as reliable control signals. CLKA synchronizes the status of the input-ready flag of FIFOA–B (IRA) and the output-ready flag of FIFOB–A (ORA). CLKB synchronizes the status of the input-ready flag of FIFOB–A (IRB) and the output-ready flag of FIFOA–B (ORB). When the IR flag of a port is low, the FIFO receiving input from the port is full and writes are disabled to its array. When the OR flag of a port is low, the FIFO that outputs data to the port is empty and reads from its memory are disabled. The first word loaded to an empty memory is sent to the FIFO output register at the same time its OR flag is asserted (high). When the memory is read empty and the OR flag is forced low, the last valid data remains on the FIFO outputs until the OR flag is asserted (high) again. In this way, a high on the OR flag indicates new data is present on the FIFO outputs.

The SN74ABT7819A is characterized for operation from 0°C to 70°C.

Function Tables

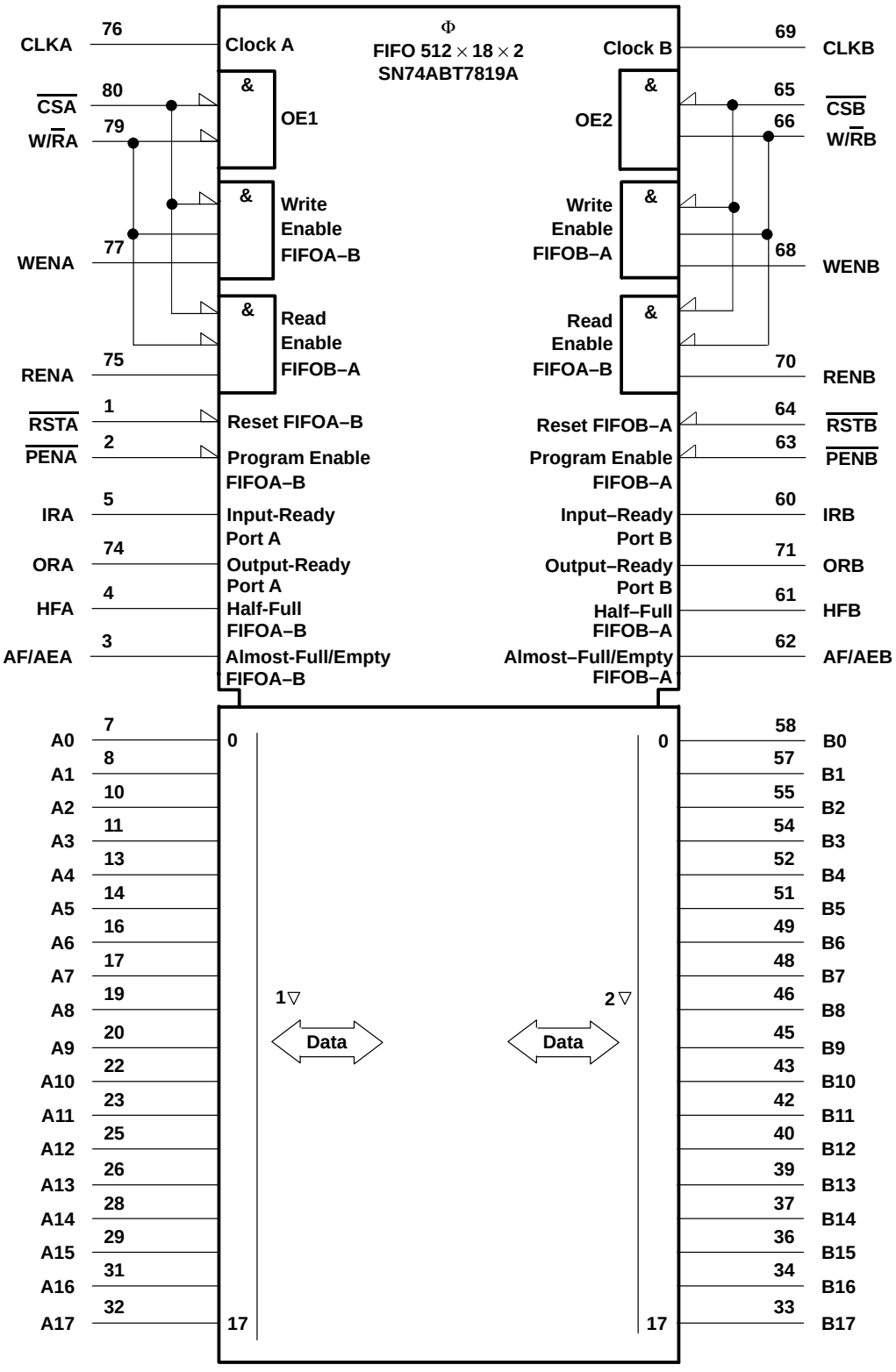
PORT A

SELECT INPUTS					A0–A17	PORT-A OPERATION
CLKA	$\overline{CSA}$	W/$\overline{R}$A	WENA	RENA		
X	H	X	X	X	High Z	None
↑	L	H	H	X	High Z	Write A0–A17 to FIFOA–B
↑	L	L	X	H	Active	Read FIFOB–A to A0–A17

PORT B

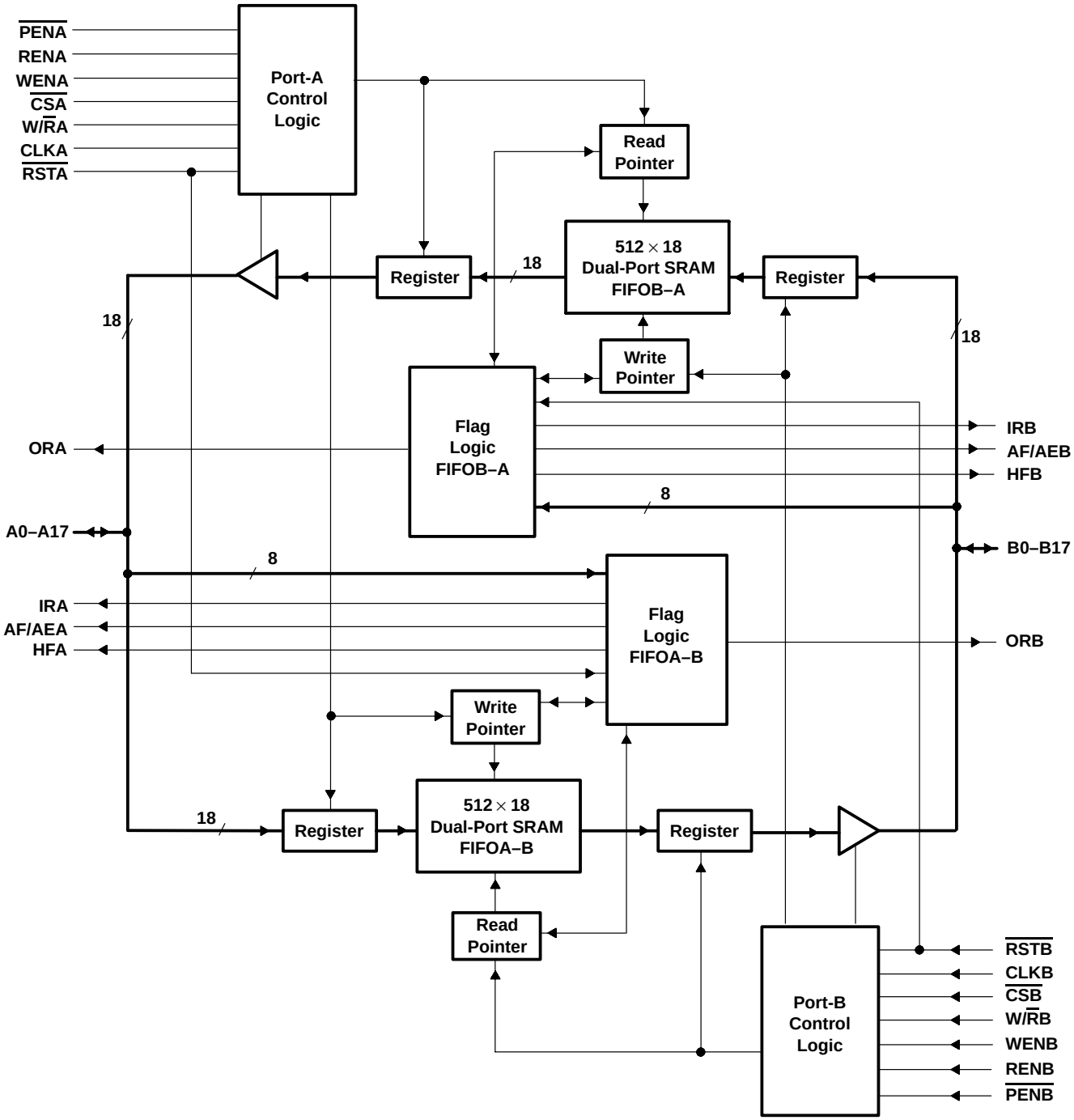
SELECT INPUTS					B0–B17	PORT-B OPERATION
CLKB	$\overline{CSB}$	W/$\overline{R}$B	WENB	RENB		
X	H	X	X	X	High Z	None
↑	L	H	H	X	High Z	Write B0–B17 to FIFOB–A
↑	L	L	X	H	Active	Read FIFOA–B to B0–B17

logic symbol†

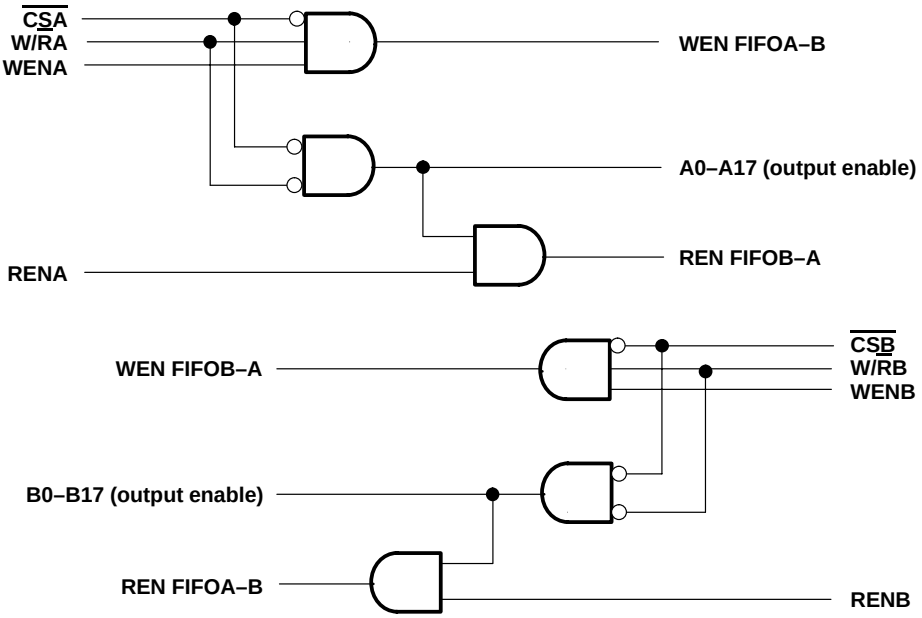


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Terminal numbers are for the PH package.

functional block diagram



enable logic diagram (positive logic)



Terminal Functions

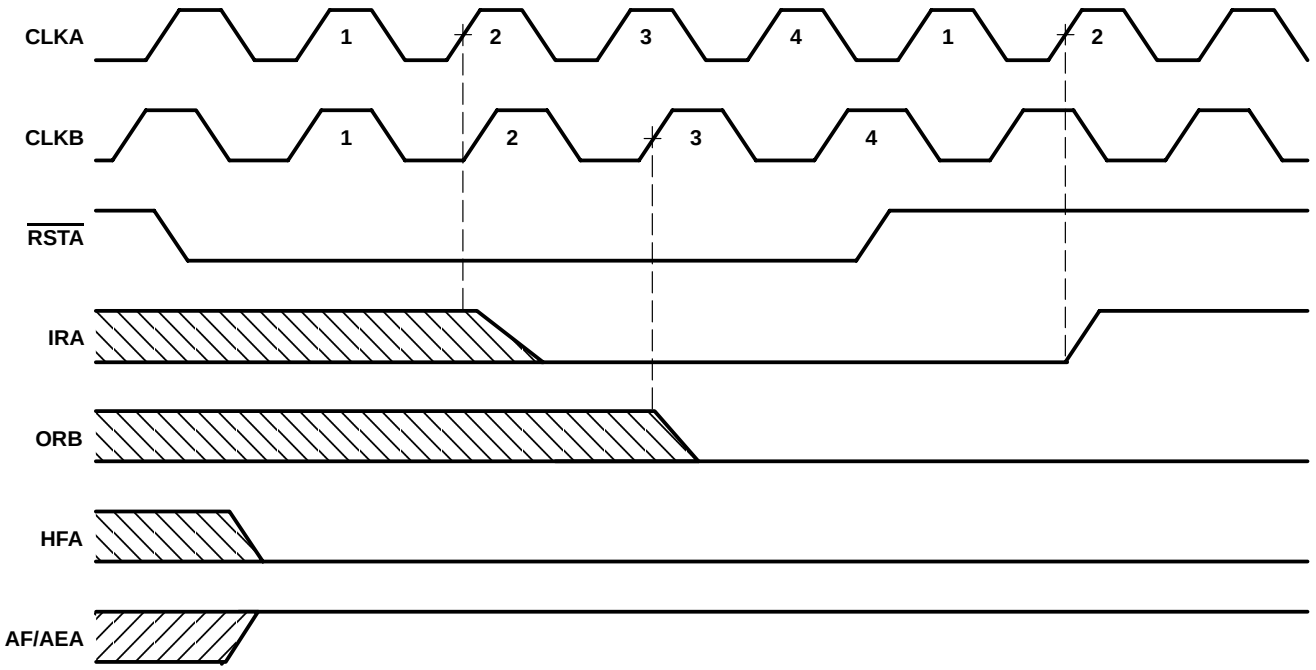
TERMINAL† NAME	TERMINAL† NO.	I/O	DESCRIPTION
A0–A17	7, 8, 10, 11, 13, 14, 16, 17, 19, 20, 22, 23, 25, 26, 28, 29, 31, 32	I/O	Port-A data. The 18-bit bidirectional data port for side A.
AF/AEA	3	O	FIFOA–B almost-full/almost-empty flag. Depth offsets can be programmed for AF/AEA or the default value of 128 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AEA is high when X or fewer words or (512 – Y) or more words are stored in FIFOA–B. AF/AEA is forced high when FIFOA–B is reset.
AF/AEB	62	O	FIFOB–A almost-full/almost-empty flag. Depth offsets can be programmed for AF/AEB or the default value of 128 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AEB is high when X or fewer words or (512 – Y) or more words are stored in FIFOB–A. AF/AEB is forced high when FIFOB–A is reset.
B0–B17	58, 57, 55, 54, 52, 51, 49, 48, 46, 45, 43, 42, 40, 39, 37, 36, 34, 33	I/O	Port-B data. The 18-bit bidirectional data port for side B.
CLKA	76	I	Port-A clock. CLKA is a continuous clock that synchronizes all data transfers through port A to its low-to-high transition and can be asynchronous or coincident to CLKB.
CLKB	69	I	Port-B clock. CLKB is a continuous clock that synchronizes all data transfers through port B to its low-to-high transition and can be asynchronous or coincident to CLKA.
$\overline{CSA}$	80	I	Port-A chip select. $\overline{CSA}$ must be low to enable a low-to-high transition of CLKA to either write data from A0–A17 to FIFOA–B or read data from FIFOB–A to A0–A17. The A0–A17 outputs are in the high-impedance state when $\overline{CSA}$ is high.
$\overline{CSB}$	65	I	Port-B chip select. $\overline{CSB}$ must be low to enable a low-to-high transition of CLKB to either write data from B0–B17 to FIFOB–A or read data from FIFOA–B to B0–B17. The B0–B17 outputs are in the high-impedance state when $\overline{CSB}$ is high.

† Terminal numbers are for the PH package.

Terminal Functions (Continued)

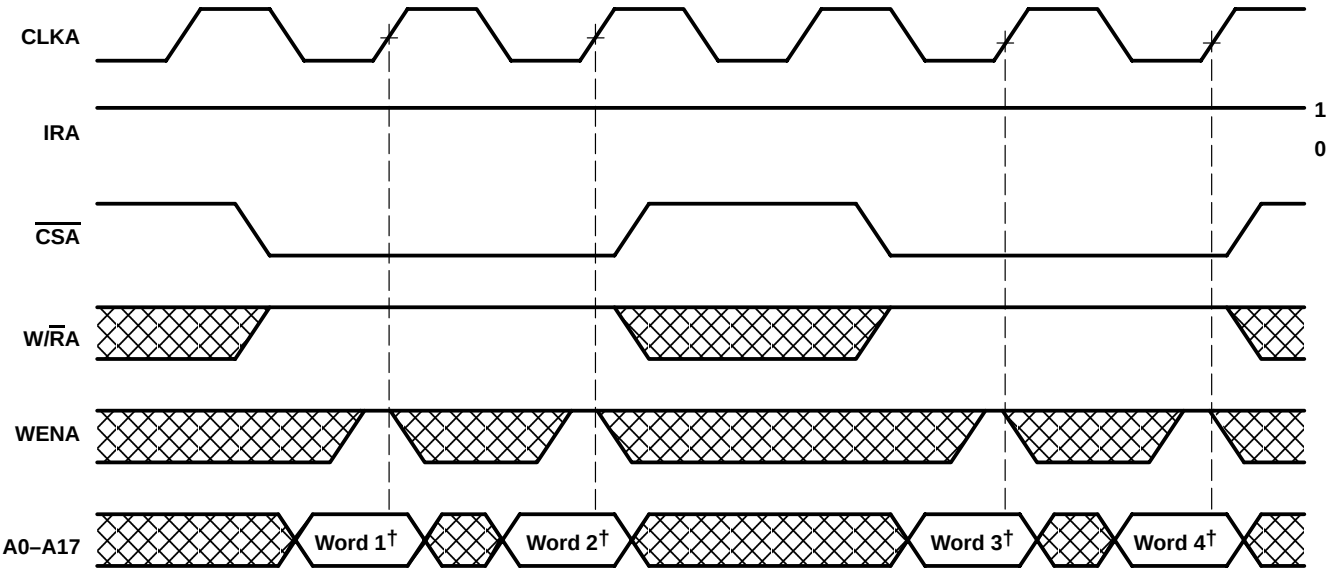
TERMINAL† NAME	TERMINAL† NO.	I/O	DESCRIPTION
HFA	4	O	FIFOA–B half-full flag. HFA is high when FIFOA–B contains 256 or more words and is low when FIFOA–B contains 255 or fewer words. HFA is set low after FIFOA–B is reset.
HFB	61	O	FIFOB–A half-full flag. HFB is high when FIFOB–A contains 256 or more words and is low when FIFOB–A contains 255 or fewer words. HFB is set low after FIFOB–A is reset.
IRA	5	O	Port-A input-ready flag. IRA is synchronized to the low-to-high transition of CLKA. When IRA is low, FIFOA–B is full and writes to its array are disabled. IRA is set low during a FIFOA–B reset and is set high on the second low-to-high transition of CLKA after reset.
IRB	60	O	Port-B input-ready flag. IRB is synchronized to the low-to-high transition of CLKB. When IRB is low, FIFOB–A is full and writes to its array are disabled. IRB is set low during a FIFOB–A reset and is set high on the second low-to-high transition of CLKB after reset.
ORA	74	O	Port-A output-ready flag. ORA is synchronized to the low-to-high transition of CLKA. When ORA is low, FIFOB–A is empty and reads from its array are disabled. The last valid word remains on the FIFOB–A outputs when ORA is low. Ready data is present for the A0–A17 outputs when ORA is high. ORA is set low during a FIFOB–A reset and goes high on the third low-to-high transition of CLKA after the first word is loaded to an empty FIFOB–A.
ORB	71	O	Port-B output-ready flag. ORB is synchronized to the low-to-high transition of CLKB. When ORB is low, FIFOA–B is empty and reads from its array are disabled. The last valid word remains on the FIFOA–B outputs when ORB is low. Ready data is present for the B0–B17 outputs when ORB is high. ORB is set low during a FIFOA–B reset and goes high on the third low-to-high transition of CLKB after the first word is loaded to an empty FIFOA–B.
$\overline{\text{PENA}}$	2	I	AF/AEA program enable. After FIFOA–B is reset and before a word is written to its array, the binary value on A0–A7 is latched as an AF/AEA offset when $\overline{\text{PENA}}$ is low and CLKA is high.
$\overline{\text{PENB}}$	63	I	AF/AEB program enable. After FIFOB–A is reset and before a word is written to its array, the binary value on B0–B7 is latched as an AF/AEB offset when $\overline{\text{PENB}}$ is low and CLKB is high.
RENA	75	I	Port-A read enable. A high level on RENA enables data to be read from FIFOB–A on the low-to-high transition of CLKA when $\overline{\text{CSA}}$ is low, W/$\overline{\text{R}}$A is low, and ORA is high.
RENB	70	I	Port-B read enable. A high level on RENB enables data to be read from FIFOA–B on the low-to-high transition of CLKB when $\overline{\text{CSB}}$ is low, W/$\overline{\text{R}}$B is low, and ORB is high.
$\overline{\text{RSTA}}$	1	I	FIFOA–B reset. To reset FIFOA–B, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{\text{RSTA}}$ is low. This sets HFA low, IRA low, ORB low, and AF/AEA high.
$\overline{\text{RSTB}}$	64	I	FIFOB–A reset. To reset FIFOB–A, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{\text{RSTB}}$ is low. This sets HFB low, IRB low, ORA low, and AF/AEB high.
WENA	77	I	Port-A write enable. A high level on WENA enables data on A0–A17 to be written into FIFOA–B on the low-to-high transition of CLKA when W/$\overline{\text{R}}$A is high, $\overline{\text{CSA}}$ is low, and IRA is high.
WENB	68	I	Port-B write enable. A high level on WENB enables data on B0–B17 to be written into FIFOB–A on the low-to-high transition of CLKB when W/$\overline{\text{R}}$B is high, $\overline{\text{CSB}}$ is low, and IRB is high.
W/$\overline{\text{R}}$A	79	I	Port-A write/$\overline{\text{read}}$ select. A high on W/$\overline{\text{R}}$A enables A0–A17 data to be written to FIFOA–B on a low-to-high transition of CLKA when WENA is high, $\overline{\text{CSA}}$ is low, and IRA is high. A low on W/$\overline{\text{R}}$A enables data to be read from FIFOB–A on a low-to-high transition of CLKA when RENA is high, $\overline{\text{CSA}}$ is low, and ORA is high. The A0–A17 outputs are in the high-impedance state when W/$\overline{\text{R}}$A is high.
W/$\overline{\text{R}}$B	66	I	Port-B write/read select. A high on W/$\overline{\text{R}}$B enables B0–B17 data to be written to FIFOB–A on a low-to-high transition of CLKB when WENB is high, $\overline{\text{CSB}}$ is low, and IRB is high. A low on W/$\overline{\text{R}}$B enables data to be read from FIFOA–B on a low-to-high transition of CLKB when RENB is high, $\overline{\text{CSB}}$ is low, and ORB is high. The B0–B17 outputs are in the high-impedance state when W/$\overline{\text{R}}$B is high.

† Terminal numbers are for the PH package.



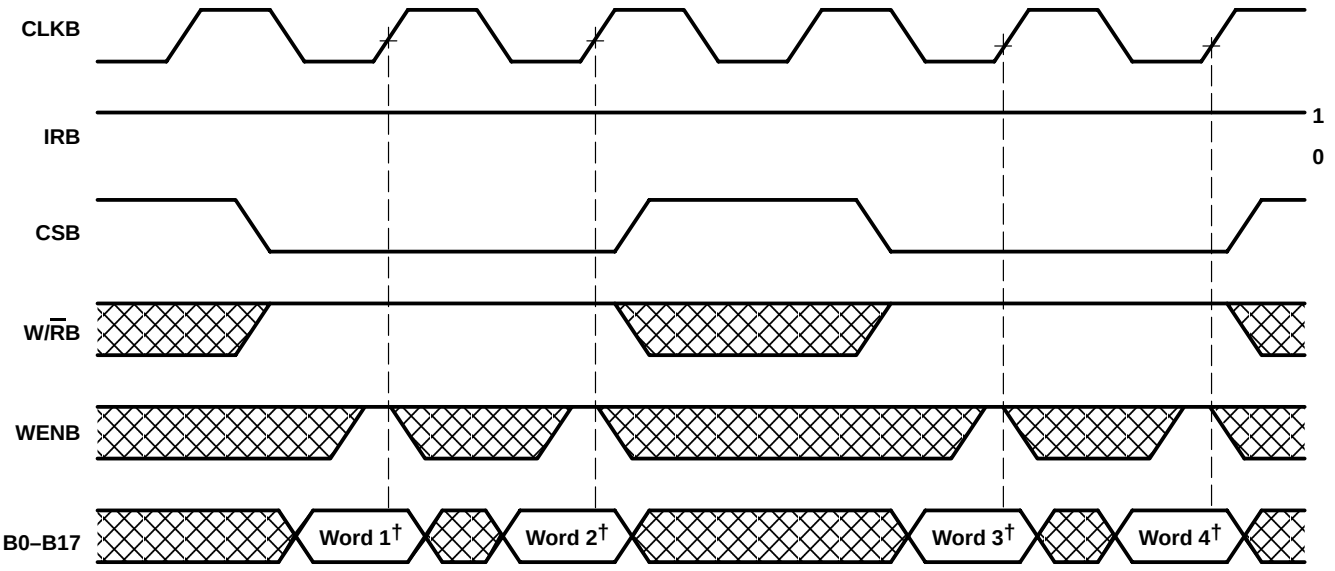
NOTE: FIFOB–A is reset in the same manner.

Figure 1. Reset Cycle for FIFOA–B



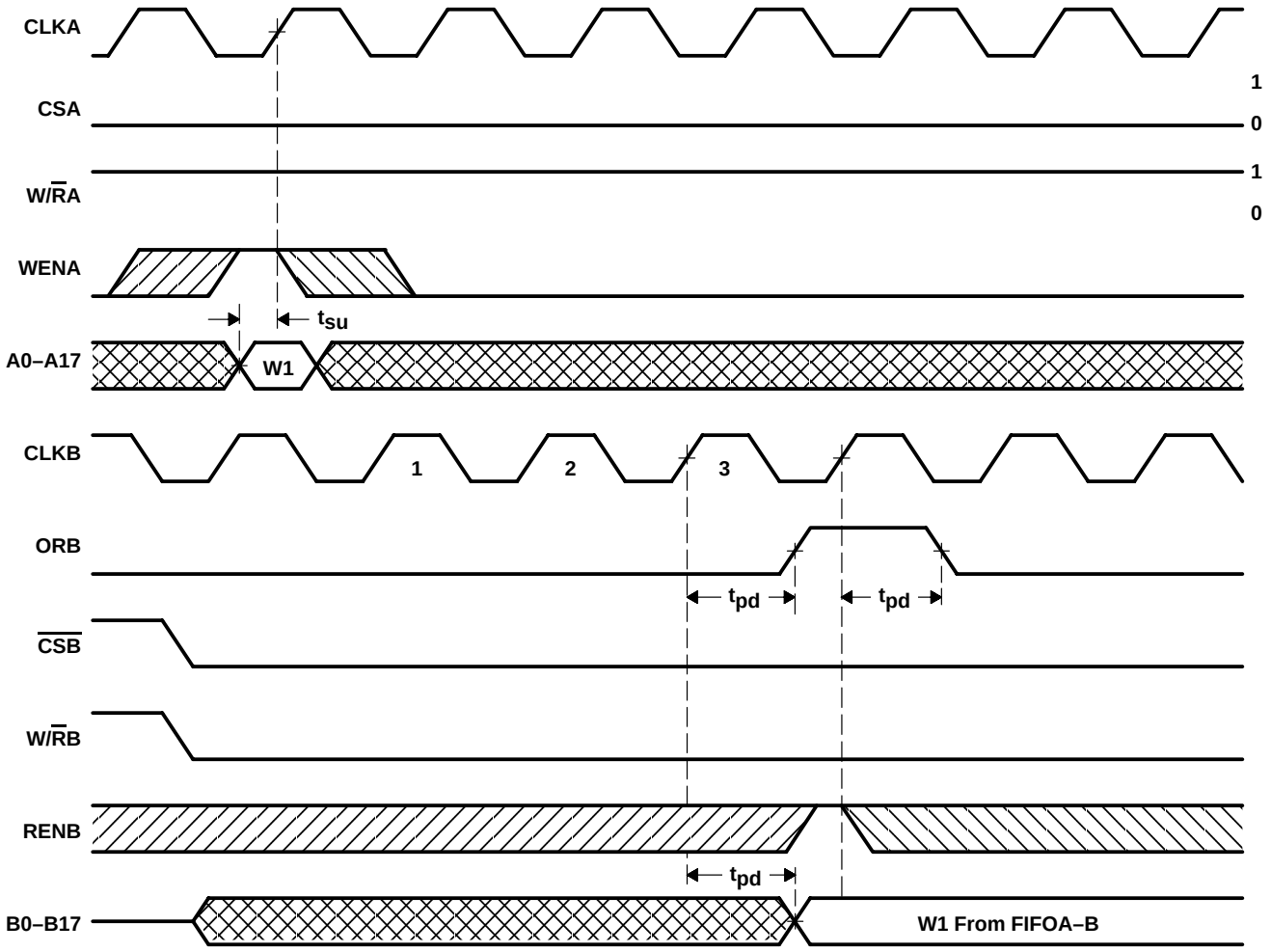
† Written to FIFOA–B

Figure 2. Write Timing – Port A



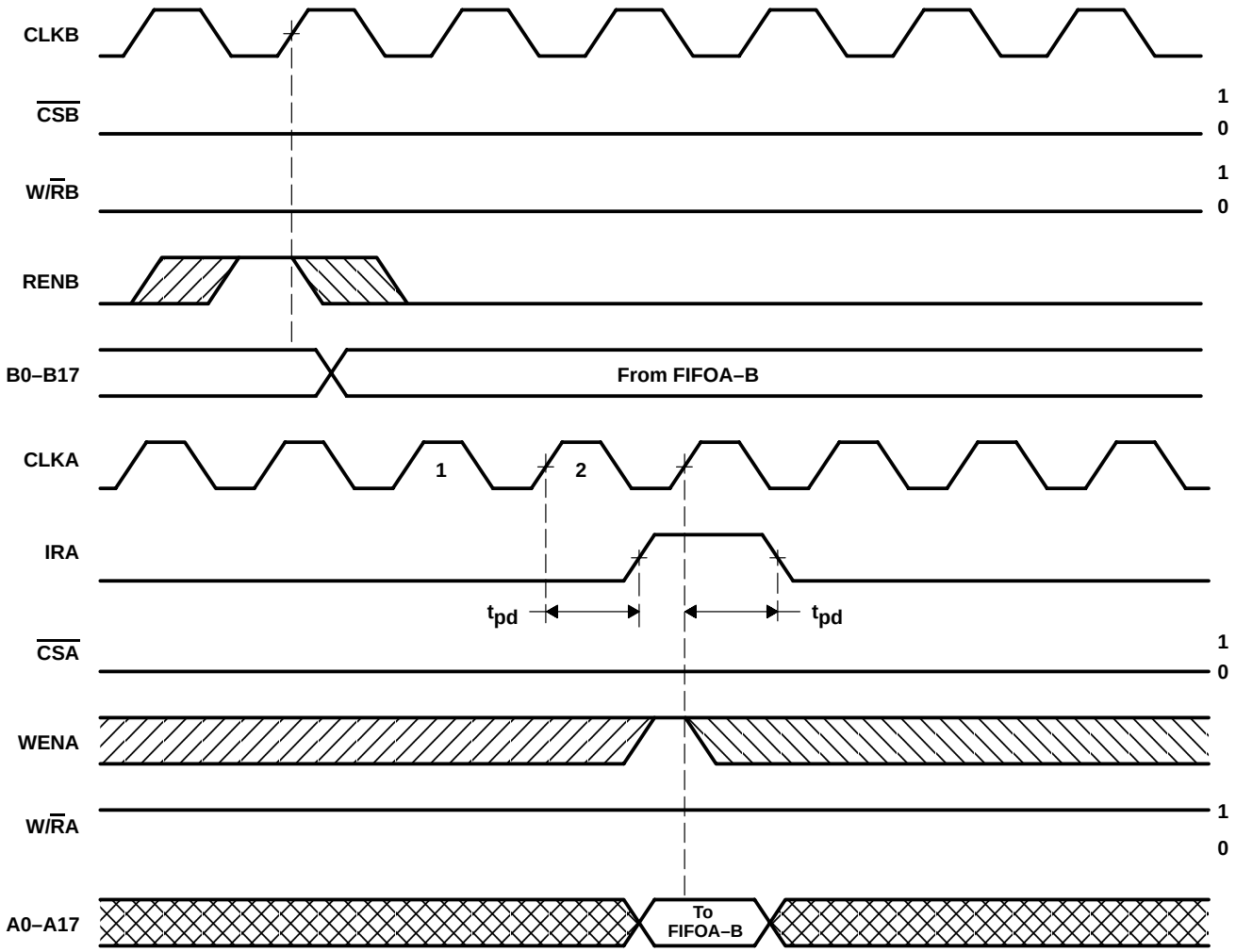
† Written to FIFOB–A

Figure 3. Write Timing – Port B



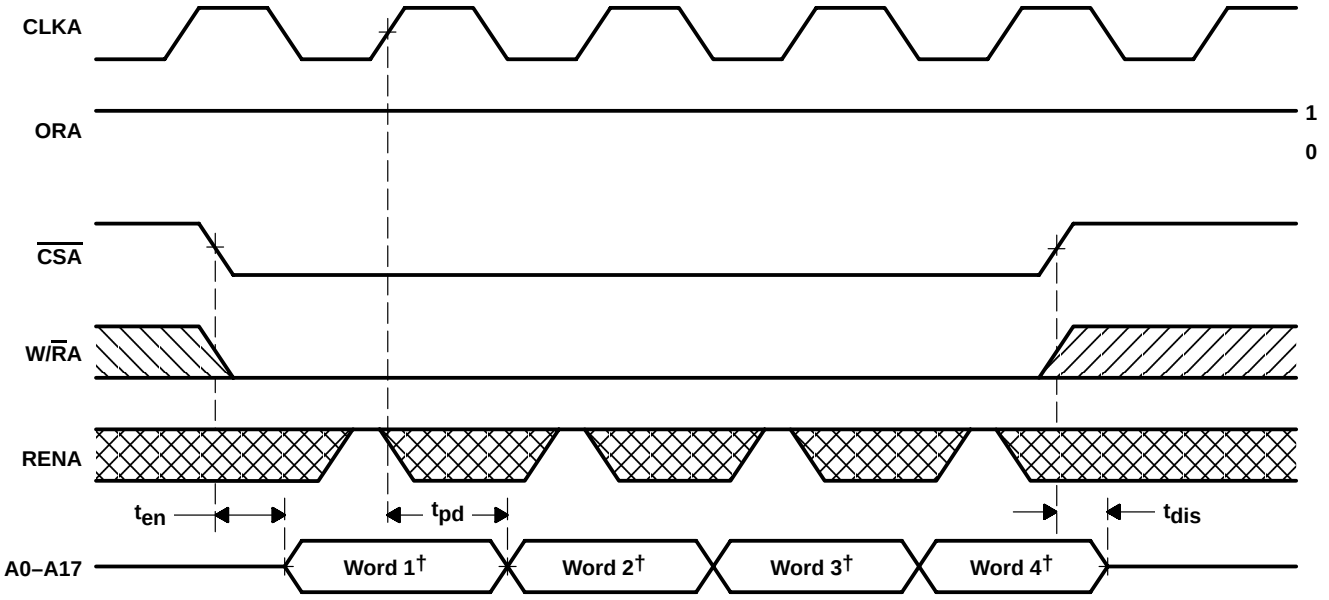
NOTE: Operation of FIFOB–A is identical to that of FIFOA–B.

Figure 4. ORB-Flag Timing and First Data-Word Fall Through When FIFOA–B Is Empty



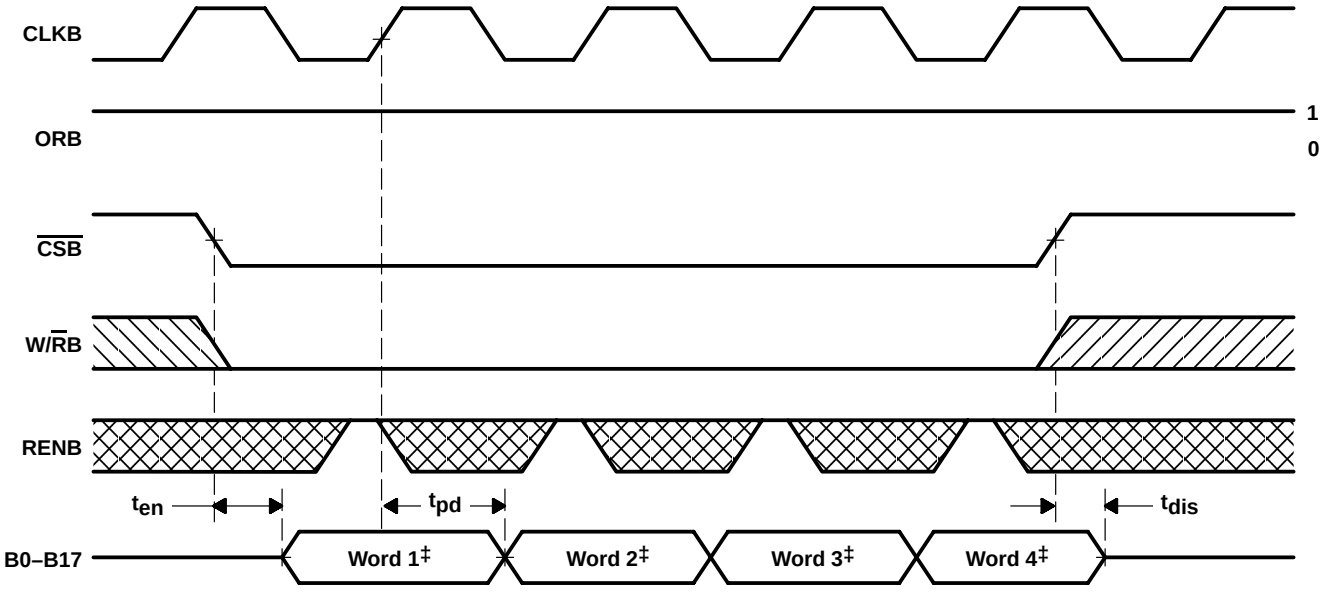
NOTE: Operation of FIFOB–A is identical to that of FIFOA–B.

Figure 5. Write-Cycle and IRA-Flag Timing When FIFOA–B Is Full



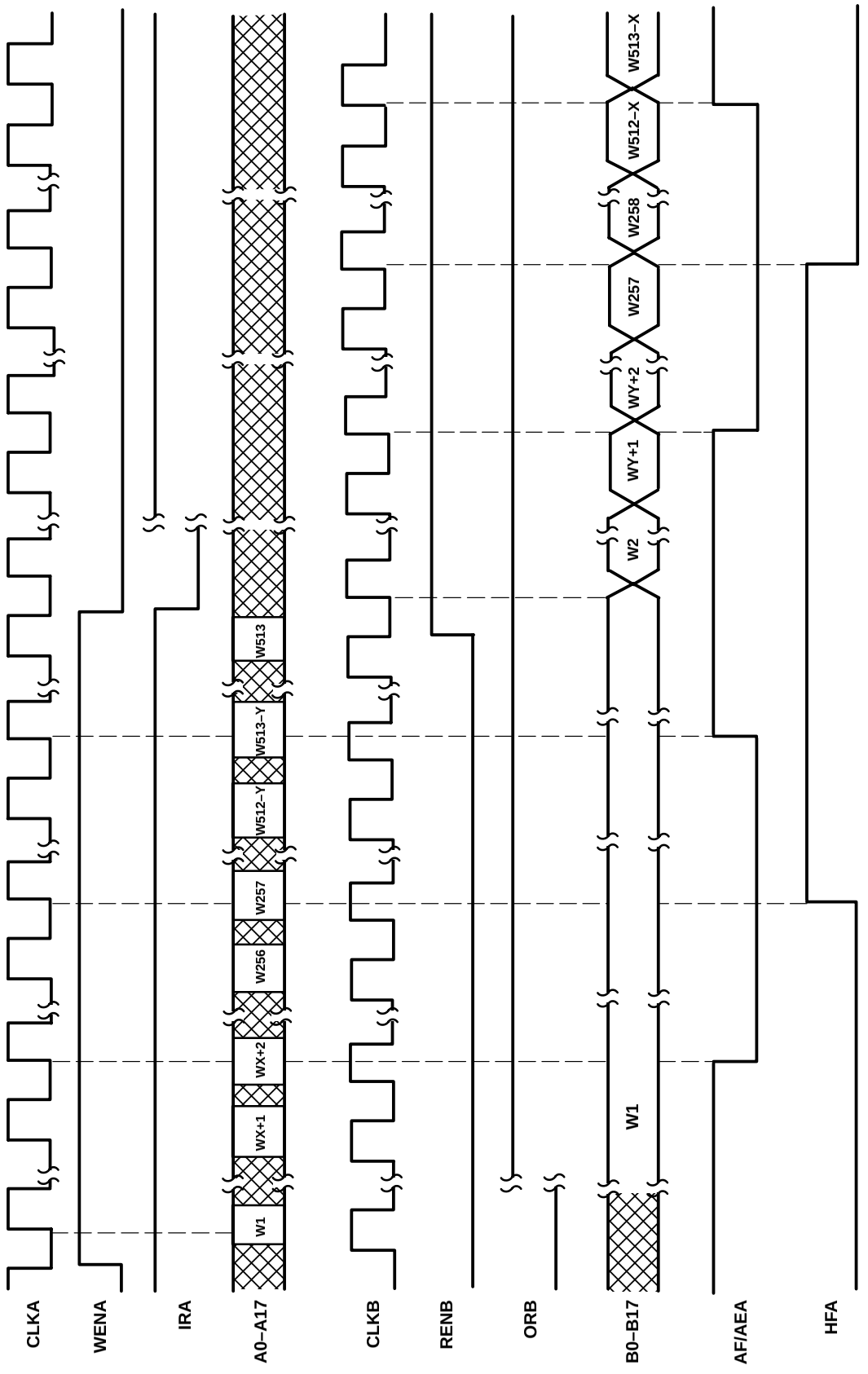
† Read from FIFOB–A

Figure 6. Read Timing – Port A



‡ Read from FIFOA–B

Figure 7. Read Timing – Port B



NOTES: A. $\overline{CSA}$, $\overline{CSB}$ = 0, W/$\overline{RA}$ = 1, W/$\overline{RB}$ = 0
B. X is the almost-empty offset and Y is the almost-full offset for AF/AEA.
C. HFB and AF/AEB function in the same manner for FIFOB–A.

Figure 8. FIFOA–B (HFA, AF/AEA) Asynchronous Flag Timing

offset values for AF/AE

The AF/AE flag of each FIFO has two programmable limits: the almost-empty offset value (X) and the almost-full offset value (Y). They can be programmed from the input of the FIFO after it is reset and before a word is written to its memory. An AF/AE flag is high when its FIFO contains X or fewer words or (512 – Y) or more words.

To program the offset values for AF/AEA, $\overline{\text{PENA}}$ is brought low after FIFOA–B is reset and only when CLKA is low. On the following low-to-high transition of CLKA, the binary value on A0–A7 is stored as the almost-empty offset value (X) and the almost-full offset value (Y). Holding $\overline{\text{PENA}}$ low for another low-to-high transition of CLKA reprograms Y to the binary value on A0–A7 at the time of the second CLKA low-to-high transition.

During the first two CLKA cycles used for offset programming, $\overline{\text{PENA}}$ can be brought high only when CLKA is low. $\overline{\text{PENA}}$ can be brought high at any time after the second CLKA pulse used for offset programming returns low. A maximum value of 255 can be programmed for either X or Y (see Figure 9). To use the default values of X = Y = 128, $\overline{\text{PENA}}$ must be tied high. No data is stored in FIFOA–B while the AF/AEA offsets are programmed. The AF/AEB flag is programmed in the same manner, with $\overline{\text{PENB}}$ enabling CLKB to program the offset values taken from B0–B7.

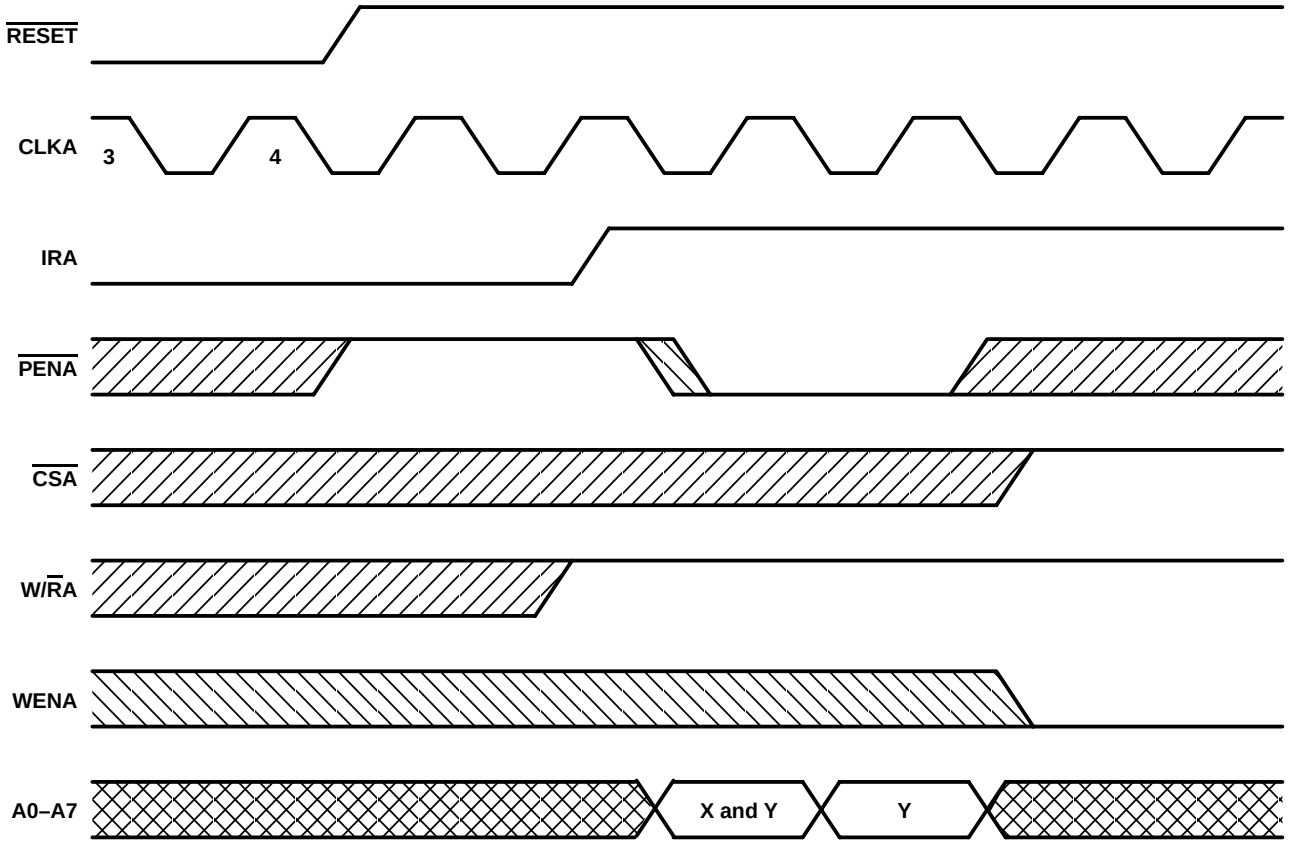


Figure 9. Programming X and Y Separately for AF/AEA

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Voltage range applied to any output in the high state or power-off state, V_O . . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O . . . . . 48 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 2): PH package . . . . . 72°C/W
PN package . . . . . 62°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51–7.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
I_{OH}	High-level output current			–12	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate			5	ns/V
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = –3 mA	2.5			V
		V_{CC} = 5 V,	I_{OH} = –3 mA	3			
		V_{CC} = 4.5 V,	I_{OH} = –12 mA	2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.5		V
I_I		V_{CC} = 5.5 V,	V_I = V_{CC} or GND			±1	µA
I_{OZH}§		V_{CC} = 5.5 V,	V_O = 2.7 V			50	µA
I_{OZL}§		V_{CC} = 5.5 V,	V_O = 0.5 V			–50	µA
I_O¶		V_{CC} = 5.5 V,	V_O = 2.5 V	–40	–100	–180	mA
I_{CC}		V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			15	mA
			Outputs low			95	
			Outputs disabled			15	
C_i	Control inputs	V_I = 2.5 V or 0.5 V			12		pF
C_{io}	A or B ports	V_O = 2.5 V or 0.5 V			14		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 10)

			’7819A-10		’7819A-12		’7819A-15		’7819A-20		’7819A-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			100		80		67		50		33.3	MHz
t_w	Pulse duration	CLKA, CLKB high or low	4.5		4.5		6		8		11		ns
t_{su}	Setup time	A0–A17 before CLKA↑ and B0–B17 before CLKB↑	2		3		4		5		5		ns
		$\overline{CSA}$ before CLKA↑ and $\overline{CSB}$ before CLKB↑	6		6		6		7		7		
		W/$\overline{R}$A before CLKA↑ and W/$\overline{R}$B before CLKB↑	6		6		6		7		7		
		WENA before CLKA↑ and WENB before CLKB↑	4		4		4		5		5		
		RENA before CLKA↑ and RENB before CLKB↑	5		5		5		5		6		
		$\overline{PENA}$ before CLKA↑ and $\overline{PENB}$ before CLKB↑	3		3		4		5		5		
		$\overline{RSTA}$ or $\overline{RSTB}$ low before first CLKA↑ and CLKB↑†	3		3		4		5		5		
t_h	Hold time	A0–A17 after CLKA↑ and B0–B17 after CLKB↑	0		0		0		0		0		ns
		$\overline{CSA}$ after CLKA↑ and $\overline{CSB}$ after CLKB↑	0		0		0		0		0		
		W/$\overline{R}$A after CLKA↑ and W/$\overline{R}$B after CLKB↑	0		0		0		0		0		
		WENA after CLKA↑ and WENB after CLKB↑	0		0		0		0		0		
		RENA after CLKA↑ and RENB after CLKB↑	0		0		0		0		0		
		PENA after CLKA low and PENB after CLKB low	2		2		2		2		2		
		$\overline{RSTA}$ or $\overline{RSTB}$ low after fourth CLKA↑ and CLKB↑†	3		3		3		4		4		

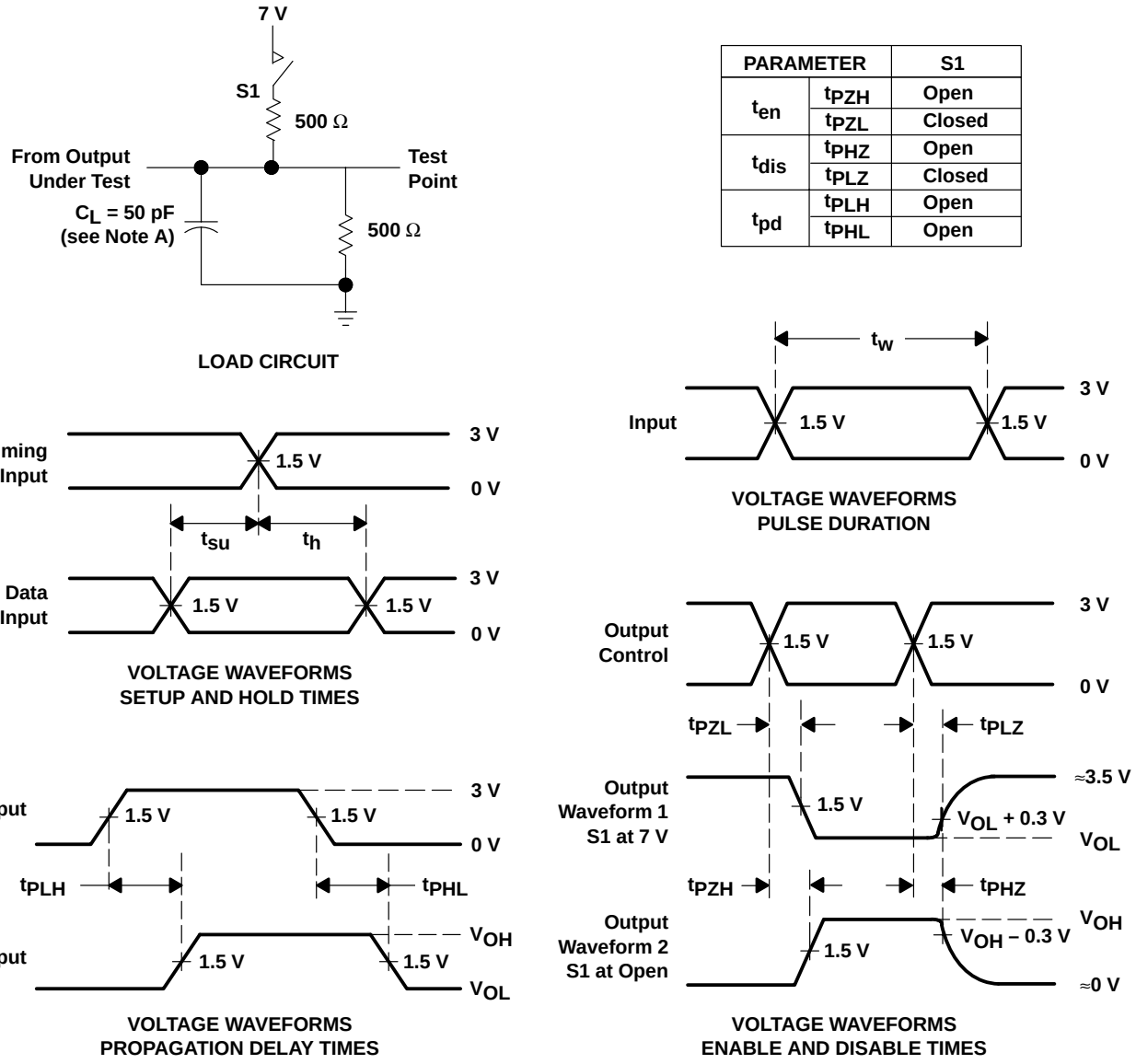
† To permit the clock pulse to be utilized for reset purposes

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	’7819A-10			’7819A-12		’7819A-15		’7819A-20		’7819A-30		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	CLKA or CLKB		100			80		67		50		33.3		MHz
t_{pd}	CLKA↑	A0–A17	3	6	8	4	9	4	10	4	12	4	14	ns
	CLKB↑	B0–B17	3	6	8	4	9	4	10	4	12	4	14	
t_{pd}‡	CLKA↑	A0–A17		5										ns
	CLKB↑	B0–B17		5										
t_{pd}	CLKA↑	IRA	4		9	4	9	4	10	4	12	4	14	ns
	CLKB↑	IRB	4		9	4	9	4	10	4	12	4	14	
	CLKA↑	ORA	3.5		9	3.5	9	3.5	10	3.5	12	3.5	14	
	CLKB↑	ORB	3.5		9	3.5	9	3.5	10	3.5	12	3.5	14	
	CLKA↑	AF/AEA	8		17	8	17	8	17	8	18	8	20	
	CLKB↑		8		17	8	17	8	17	8	18	8	20	
t_{PLH}	$\overline{RSTA}$	AF/AEA	4		12	4	12	4	14	4	15	4	16	ns
t_{pd}	CLKA↑	AF/AEB	8		17	8	17	8	17	8	18	8	20	ns
	CLKB↑		8		17	8	17	8	17	8	18	8	20	
t_{PLH}	$\overline{RSTB}$	AF/AEB	4		12	4	12	4	14	4	15	4	16	
	CLKA↑	HFA	8		17	8	17	8	17	8	18	8	20	
t_{PHL}	CLKB↑	HFA	8		17	8	17	8	17	8	18	8	20	ns
	$\overline{RSTA}$		4		12	4	12	4	14	4	15	4	16	
	CLKA↑	HFB	8		17	8	17	8	17	8	18	8	20	
t_{PLH}	CLKB↑	HFB	8		17	8	17	8	17	8	18	8	20	ns
t_{PHL}	$\overline{RSTB}$		4		12	4	12	4	14	4	15	4	16	
t_{en}	$\overline{CSA}$	A0–A17	2.5		8	2.5	8	2.5	9	2.5	10	2.5	11	ns
	W/$\overline{R}$A		2.5		8	2.5	8	2.5	9	2.5	10	2.5	11	
	$\overline{CSB}$	B0–B17	2.5		8	2.5	8	2.5	9	2.5	10	2.5	11	
	W/$\overline{R}$B		2.5		8	2.5	8	2.5	9	2.5	10	2.5	11	
t_{dis}	$\overline{CSA}$	A0–A17	2.5		8	2.5	8	2.5	9	2.5	10	2.5	11	ns
	W/$\overline{R}$A		2.5		8	2.5	8	2.5	9	2.5	10	2.5	11	
	$\overline{CSB}$	B0–B17	2.5		8	2.5	8	2.5	9	2.5	10	2.5	11	
	W/$\overline{R}$B		2.5		8	2.5	8	2.5	9	2.5	10	2.5	11	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This parameter is measured with a 30-pF load (see Figure 11).

PARAMETER MEASUREMENT INFORMATION



PARAMETER		S1
t_{en}	t_{PZH}	Open
	t_{PZL}	Closed
t_{dis}	t_{PHZ}	Open
	t_{PLZ}	Closed
t_{pd}	t_{PLH}	Open
	t_{PHL}	Open

NOTE A: C_L includes probe and jig capacitance.

Figure 10. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

**PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE**

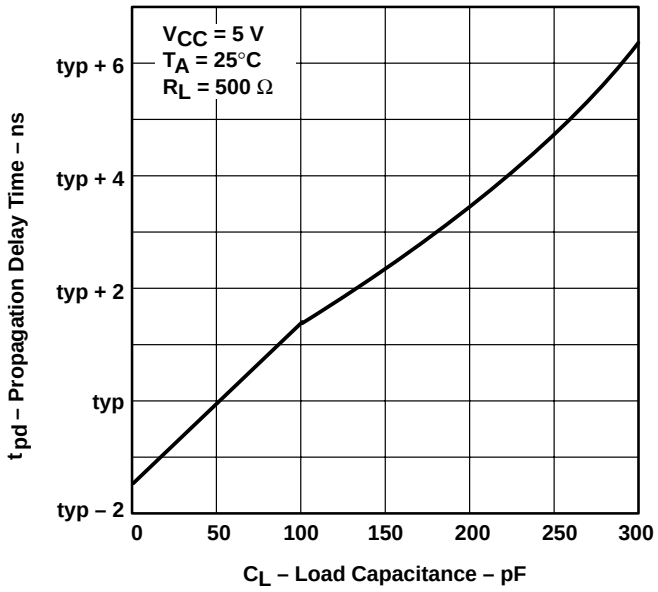


Figure 11

**SUPPLY CURRENT
vs
CLOCK FREQUENCY**

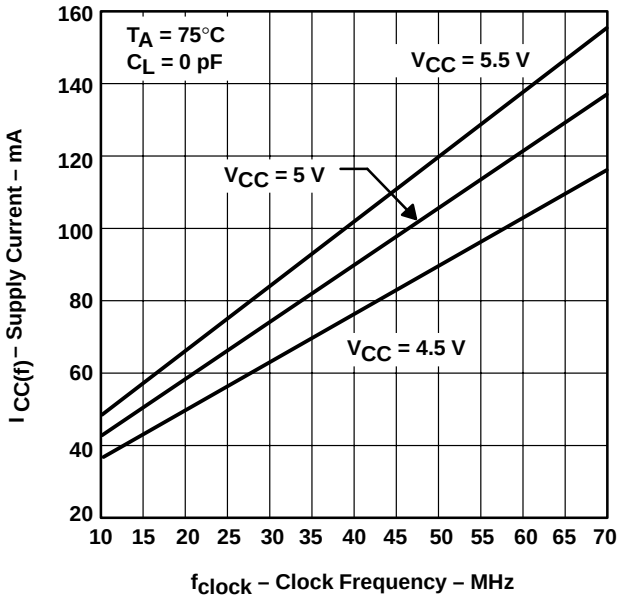


Figure 12

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265