MN3611

2160-Bit CCD Linear Image Sensor

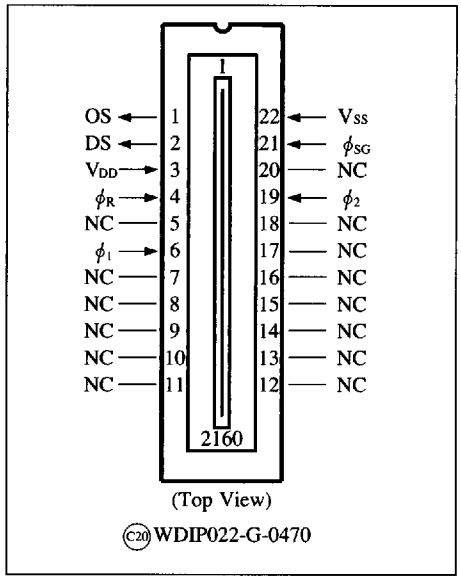
■Overview

The MN3611 is a 2160-pixel high sensitivity CCD linear image sensor combining photo-sites using low dark output floating photodiodes and CCD analog shift registers for read out. It provides large output at a high S/N ratio for visible light inputs over a wide range of wavelength.

■Features

- 2160 floating photodiodes and n-channel buried type CCD shift registers for read out are integrated in a single chip.
- Extremely high sensitivity has been obtained by employing an on-chip voltage amplifier circuit.
- Use of photodiodes with a new structure has made the dark output voltage very low.
- All the input pulses can be driven by CMOS 5V-type logics.
- Has a smooth spectral characteristics that is close to the sensitivity of the human eye in the entire visible region.
- Large signal output of typically 1700mV at saturation can be obtained.
- Operation with a single +12V positive power supply.

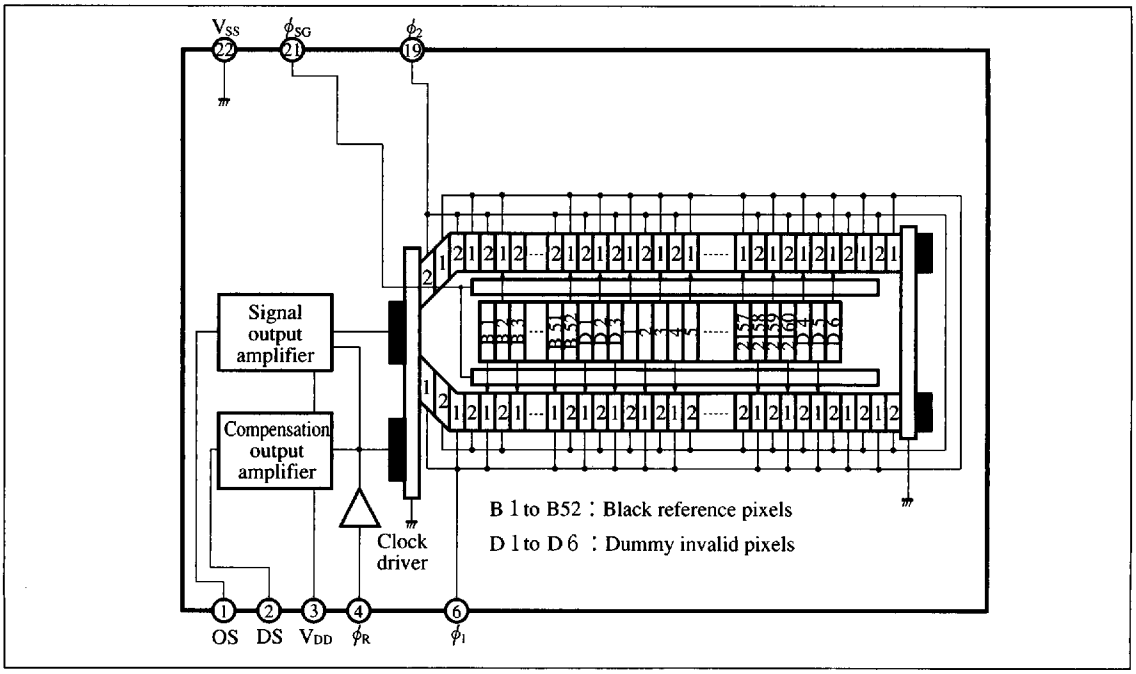
■Pin Assignments



■Application

- Graphic and character read out in fax machines, image scanners, etc.
- Measurement of position and dimensions of objects.

■Block Diagram



■Absolute Maximum Ratings (Ta=25℃, V_{SS}=0V)

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	−0.3 to +15	V
Input pin voltage	V_I	−0.3 to +15	V
Output pin voltage	V_O	−0.3 to +15	V
Operating temperature range	T_{opr}	−25 to +60	℃
Storage temperature range	T_{stg}	−40 to +100	℃

■Operating Conditions

●Voltage conditions (Ta=−25 to +60℃, V_{SS}=0V)

Parameter	Symbol	Condition	min	typ	max	Unit
Power supply voltage	V_{DD}		11.4	12.0	13.0	V
CCD shift register clock High level	$V_{\phi H}$		4.5	5.0	5.5	V
CCD shift register clock Low level	$V_{\phi L}$		0	0.2	0.5	V
Shift gate clock High level	V_{SH}		4.5	5.0	5.5	V
Shift gate clock Low level	V_{SL}		0	0.2	0.5	V
Reset gate clock High level	V_{RH}		4.5	5.0	5.5	V
Reset gate clock Low level	V_{RL}		0	0.2	0.5	V

●Timing conditions (Ta=−25 to +60℃)

Parameter	Symbol	Condition	min	typ	max	Unit
Shift register clock (ϕ_1,ϕ_2) frequency	f_C	See drive timing diagram. f_C=1/2T	—	0.5	1.0	MHz
Reset clock (ϕ_R) frequency	f_R	See drive timing diagram. f_R=1/T	—	1.0	2.0	MHz
Shift register clock (ϕ_1,ϕ_2) rise time	t_{Cr}	See drive timing diagram	0	60	100	ns
Shift regisster clock (ϕ_1,ϕ_2) fall time	t_{Cf}		0	60	100	ns
Shift clock (ϕ_{SG}) rise time	t_{Sr}	See drive timing diagram	0	50	100	ns
Shift clock (ϕ_{SG}) fall time	t_{Sf}		0	50	100	ns
Shift clock set up time	t_{Ss}		0	100	—	ns
Shift clock pulse width	t_{Sw}		200	1000	—	ns
Shift clock hold time	t_{Sh}		0	100	—	ns
Reset clock rise time	t_{Rr}	See drive timing diagram	0	15	30	ns
Reset clock fall time	t_{Rf}		0	15	30	ns
Reset clock pulse width	t_{Rw}		40	250	—	ns
Reset clock hold time	t_{Rh}		100	125	—	ns

■Electrical Characteristics

●Clock input capacitance (Ta=−25 to +60℃)

Parameter	Symbol	Condition	min	typ	max	Unit
Shift register clock input capacitance	C_1,C_2	V_{IN}=12V f=1MHz	—	350	400	pF
Reset clock input capacitance	C_R		—	15	30	pF
Shift clock input capacitance	C_S		—	130	200	pF

●DC characteristics

Parameter	Symbol	Condition	min	typ	max	Unit
Power supply current	I_{DD}	V_{DD}=+12V	—	8	15	mA

●AC characteristics

Parameter	Symbol	Condition	min	typ	max	Unit
Signal output delay time	t_{OS}		—	100	—	ns

■Optical Characteristics

<Inspection conditions>

- Ta=25℃, V_{DD}=12V, $V_{\phi H}$=V_{SH}=V_{RH}=5V (pulse), f_C=0.5MHz, f_R=1MHz, T_{int} (accumulation time)=10ms
- Light source: Daylight type fluorescent lamp
- Optical system: A slit with an aperture dimensions of 20mm×20mm is used at a distance of 200mm from the sensor (equivalent to F=10).
- Load resistance = 100k Ohms
- These specifications apply to the 2160 valid pixels excluding the dummy pixels D1 to D6.

Parameter	Symbol	Condition	min	typ	max	Unit
Responsivity	R		38	45	52	V/lx·s
Photo response non-uniformity	PRNU	Note 1	—	—	10	%
Odd/even bit non-uniformity	O/E	Note 2	—	—	3	%
Saturation output voltage	V_{SAT}	Note 3	1.5	1.7	—	V
Saturation exposure	SE	Note 3	0.029	0.038	—	lx·s
Dark signal output voltage	V_{DRK}	Dark condition, see Note 4	—	0.8	2.0	mV
Dark signal output non-uniformity	DSNU	Dark condition, see Note 4	—	0.2	3.0	mV
Shift register total transfer efficiency	STTE		92	—	—	%
Output impedance	Zo		—	—	1	kΩ
Dynamic range	DR	Note 5	—	2125	—	
Signal output pin DC level	V_{OS}	Note 6	3.5	4.5	6.0	V
Compensation output pin DC level	V_{DS}	Note 6	3.5	4.5	6.0	V
Signal and compensation output pin DC level difference	$\lvert V_{OS}-V_{DS}\rvert$	Note 6	—	50	100	mV

Note 1) The photo response non-uniformity (PRNU) is defined by the following equation, where X_{ave} is the average output voltage of the 2160 valid pixels and Δx is the absolute value of the difference between X_{ave} and the voltage of the maximum (or minimum) output pixel, when the surface of the photo-sites is illuminated with light having a uniform distribution over the entire surface.

$$PRNU=\frac{\triangle x}{X_{ave.}}\times 100\ (\%)$$

The incident light intensity shall be 50% of the standard saturation light intensity.

Note 2) The odd/even bit non-uniformity (O/E) is defined by the following equation, where X_{ave} is the average output voltage of the 2048 valid pixels and Xn is the output voltage of the 'n'th pixel, when the surface of the photo-sites is illuminated with light having a uniform distribution over the entire surface.

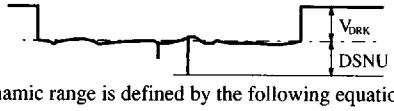
$$O/E=\frac{\sum_{n=1}^{2159}\lvert Xn-Xn_{+1}\rvert}{2159\times X_{ave}}\times 100\ (\%)$$

In other words, this is the value obtained by dividing the average of the output difference between the odd and even pixels by the average output voltage of all the valid pixels. The incident light intensity shall be 50% of the standard saturation light intensity.

Note 3) The Saturation output voltage (V_{SAT}) is defined as the output voltage at the point when the linearity of the photoelectric characteristics cannot be maintained as the incident light intensity is increased. (The light intensity of exposure at this point is called the saturation exposure.)

Note 4) The dark signal output voltage (V_{DRK}) is defined as the average output voltage of the 2160 pixels in the dark condition at Ta=25℃ and T_{int}=10ms. Normally, the dark output voltage doubles for every 8 to 10℃ rise in Ta, and is proportional to T_{int}.

The dark signal output non-uniformity (DSNU) is defined as the difference between the maximum output voltage among all the valid pixels and V_{DRK} in the dark condition at Ta=25℃ and T_{int}=10ms.



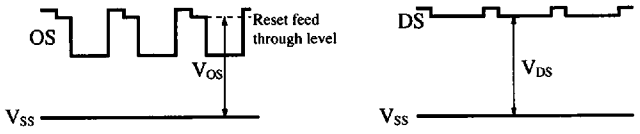
Note 5) The dynamic range is defined by the following equation.

Since the dark signal voltage is proportional to the accumulation time, the dynamic range becomes wider when the accumulation time is shorter.

$$DR=\frac{V_{SAT}}{V_{DRK}}$$

■Optical Characteristics (continued)

Note 6) The signal output pin DC level (V_{OS}) and the compensation output pin DC level (V_{DS}) are the voltage values shown in the following figure.



■Pin Descriptions

Pin No.	Symbol	Pin name	Condition
1	OS	Signal output	
2	DS	Compensation output	
3	V_{DD}	Power supply	
4	ϕ_R	Reset clock	
5	NC	Non connection	
6	ϕ_1	CCD Clock (Phase 1)	
7	NC	Non connection	
8	NC	Non connection	
9	NC	Non connection	
10	NC	Non connection	
11	NC	Non connection	
12	NC	Non connection	
13	NC	Non connection	
14	NC	Non connection	
15	NC	Non connection	
16	NC	Non connection	
17	NC	Non connection	
18	NC	Non connection	
19	ϕ_2	CCD Clock (Phase 2)	
20	NC	Non connection	
21	ϕ_{SG}	Shift gate clock	
22	V_{SS}	Ground	

Note) Connect all NC pins externally to V_{SS}.

■Construction of the Image Sensor

The MN3611 can be made up of the three sections of—a) photo detector region, b) CCD transfer region (shift register), and c) output region.

a) Photo detector region

- The photoelectric conversion device consists of an 11 μm floating photodiode and a 3 μm channel stopper for each pixel, and 2160 of these devices are linearly arranged side by side at a pitch of 14 μm.
- The photo detector's windows are 14 μm × 14 μm squares and light incident on areas other than these windows is optically shut out.
- The photo detector is provided with 52 optically shielded pixels (black dummy pixels) which serve as the black reference.

b) CCD Transfer region (shift register)

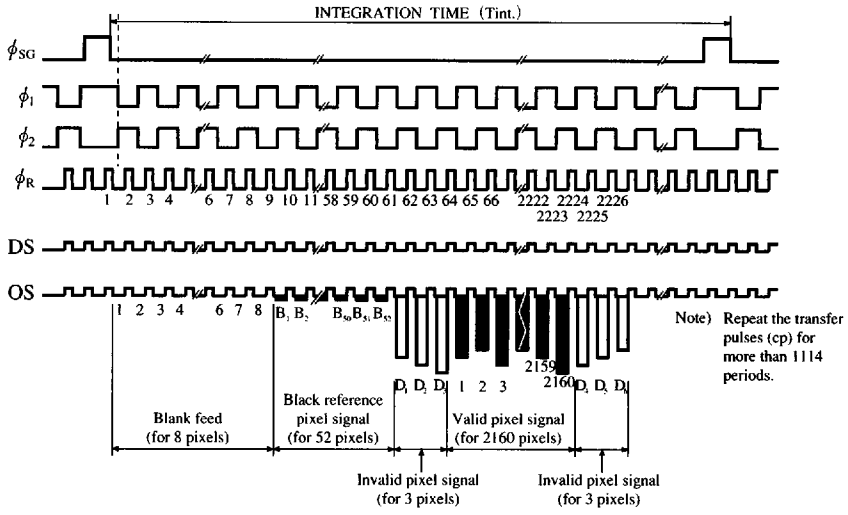
- The light output that has been photoelectrically converted is transferred to the CCD transfer for each odd and even pixel at the timing of the shift clock (ϕ_{SG}). The optical signal electric charge transferred to this analog shift register is successively transferred out and guided to the output region.
- A buried type CCD that can be driven by a two phase clock (ϕ_1, ϕ_2) is used for the analog shift register.

c) Output region

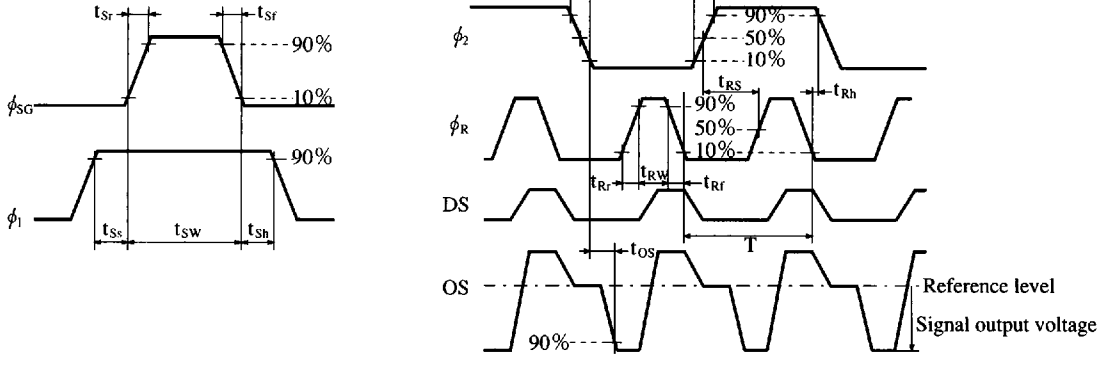
- The signal charge that is transferred to the output region is sent to the detector where voltage amplification is executed and impedance transformation is done using source follower stage.
- The DC level component and the clock noise component not containing optical signals are output from the DS pin.
- By carrying out differential amplification of the two outputs OS and DS externally, it is possible to obtain an output signal with a high S/N ratio by reducing the clock noise, etc.

■Timing Diagram

(1) I/O timing



(2) Drive timing



■Graphs and Characteristics

Spectral Response Characteristics