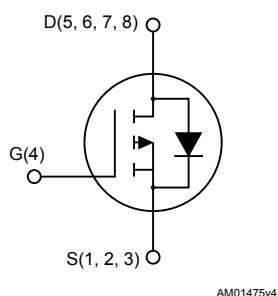
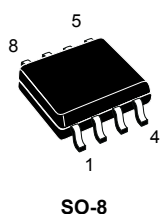


P-channel 40 V, 17.5 mΩ typ., 7 A, STripFET F6 Power MOSFET in an SO-8 package



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STS7P4LLF6	40 V	20.5 mΩ	7 A

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is a P-channel Power MOSFET developed using the STripFET F6 technology, with a new trench gate structure. The resulting Power MOSFET exhibits very low R_{DS(on)} in all packages.



Product status link

[STS7P4LLF6](#)

Product summary

Order code	STS7P4LLF6
Marking	7K4L
Package	SO-8
Packing	Tape and reel

Note: For the P-channel Power MOSFET, current polarity of voltages and current have to be reversed.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_{amb} = 25\text{ }^{\circ}\text{C}$	7	A
	Drain current (continuous) at $T_{amb} = 100\text{ }^{\circ}\text{C}$	4.2	
$I_{DM}^{(1)}$	Drain current (pulsed)	28	A
P_{TOT}	Total power dissipation at $T_{amb} = 25\text{ }^{\circ}\text{C}$	2.7	W
T_{stg}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$
T_J	Maximum junction temperature	150	$^{\circ}\text{C}$

1. Pulse width limited by safe operating area.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient	47	$^{\circ}\text{C/W}$

1. When mounted on 1 inch² FR-4 board, 2 oz. Cu., $t \leq 10\text{ s}$.

Note: For the P-channel Power MOSFET, current polarity of voltages and current have to be reversed.

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 3. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	40			V
I_{DSS}	Zero gate voltage Drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 40\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 40\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}$			10	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1			V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 3.5\text{ A}$		17.5	20.5	m Ω
		$V_{GS} = 4.5\text{ V}$, $I_D = 3.5\text{ A}$		20.5	29.0	

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	2850	-	pF
C_{oss}	Output capacitance		-	270	-	pF
C_{rss}	Reverse transfer capacitance		-	180	-	pF
Q_g	Total gate charge	$V_{DD} = 20\text{ V}$, $I_D = 7\text{ A}$, $V_{GS} = 4.5\text{ V}$ (see Figure 13. Gate charge test circuit)	-	22	-	nC
Q_{gs}	Gate-source charge		-	9.4	-	nC
Q_{gd}	Gate-drain charge		-	7.3	-	nC
R_G	Gate input resistance	$I_D = 0\text{ A}$, gate DC bias = 0 V , $f = 1\text{ MHz}$, magnitude of alternative signal = 20 mV	-	1.4	-	Ω

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 20\text{ V}$, $I_D = 3.5\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	43	-	ns
t_r	Rise time		-	47	-	ns
$t_{d(off)}$	Turn-off-delay time	(see Figure 12. Switching times test circuit for resistive load)	-	148	-	ns
t_f	Fall time		-	19	-	ns

Note: For the P-channel Power MOSFET, current polarity of voltages and current have to be reversed.

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 3.5\text{ A}$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 3.5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 32\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	26		ns
Q_{rr}	Reverse recovery charge		-	21		nC
I_{RRM}	Reverse recovery current		-	1.7		A

1. Pulse test: pulse duration = 300 μs , duty cycle 1.5%

Note: For the P-channel Power MOSFET, current polarity of voltages and current have to be reversed.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

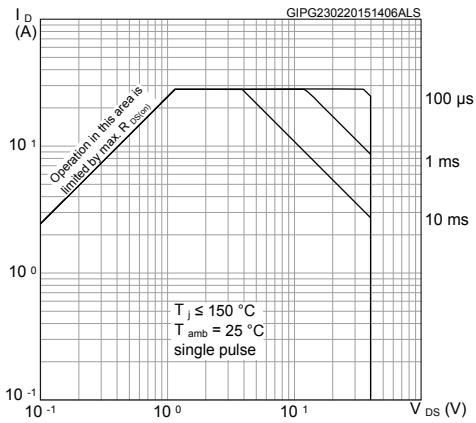


Figure 2. Thermal impedance

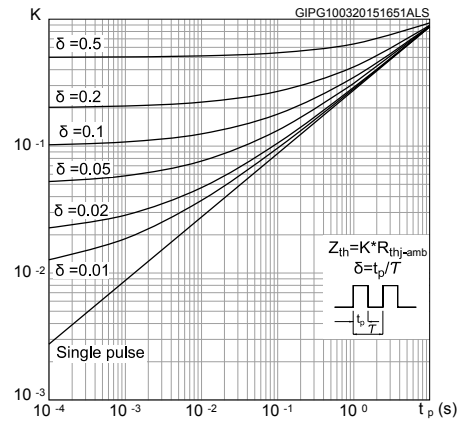


Figure 3. Output characteristics

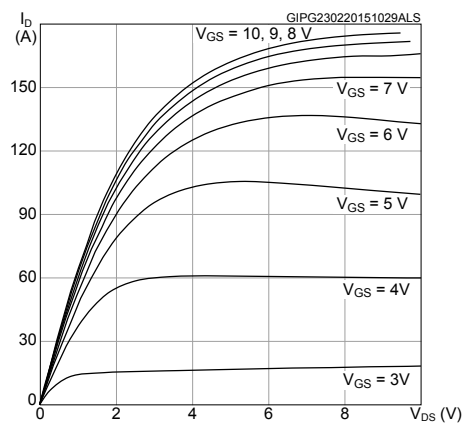


Figure 4. Transfer characteristics

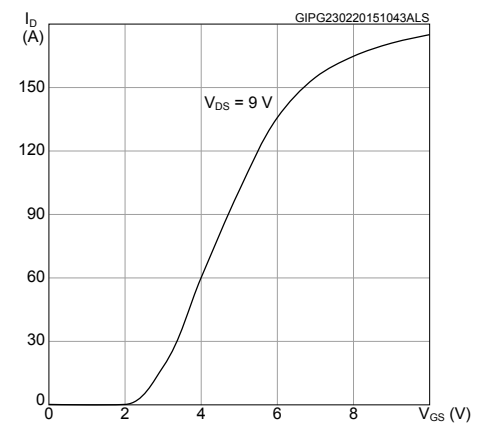


Figure 5. Normalized gate threshold voltage vs temperature

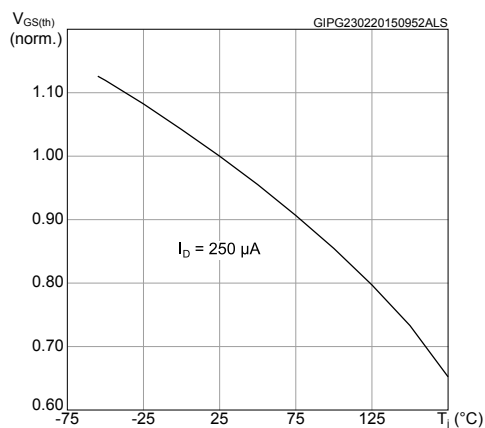


Figure 6. Normalized $V_{(BR)DSS}$ vs temperature

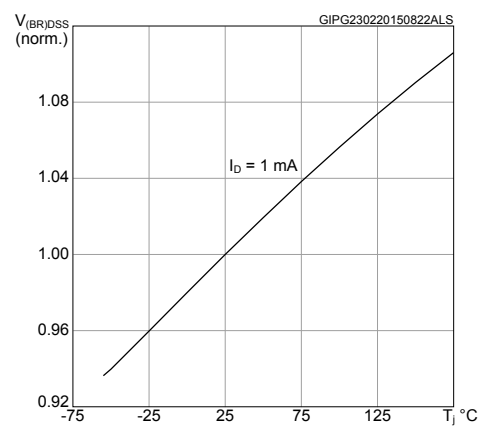


Figure 7. Static drain-source on-resistance

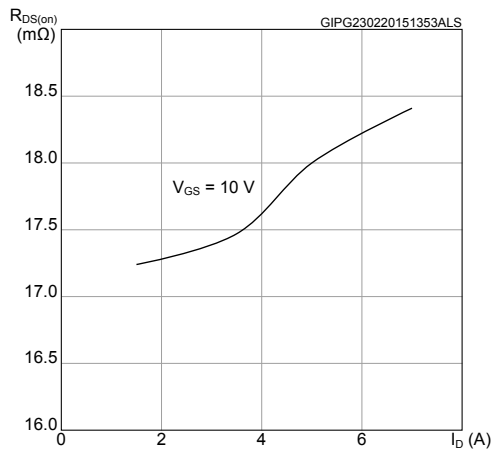


Figure 8. Normalized on-resistance vs. temperature

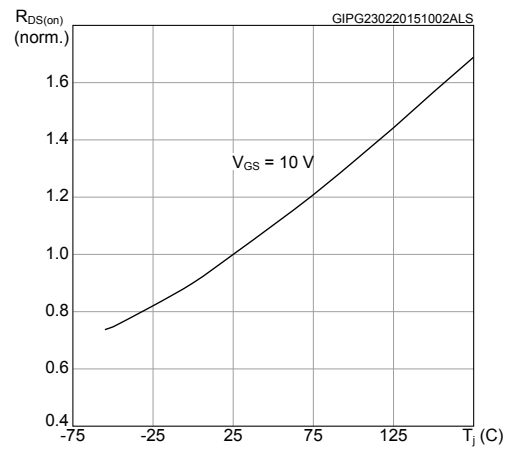


Figure 9. Gate charge vs gate-source voltage

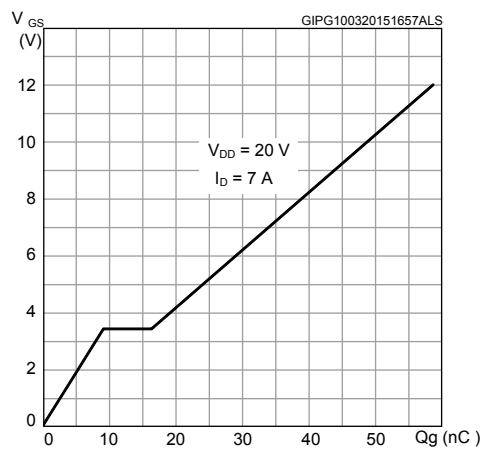


Figure 10. Capacitance variations voltage

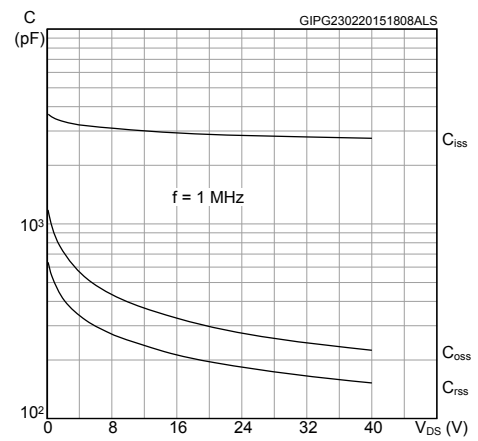
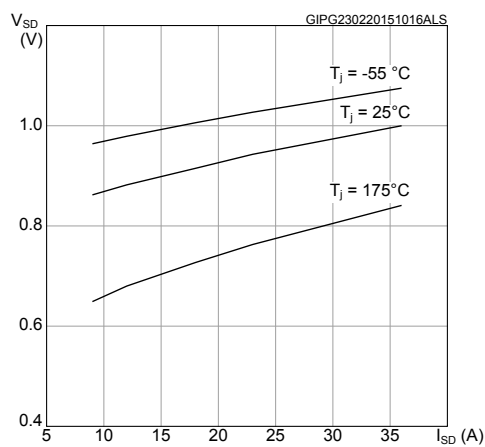


Figure 11. Source-drain diode forward characteristics



3 Test circuits

Figure 12. Switching times test circuit for resistive load

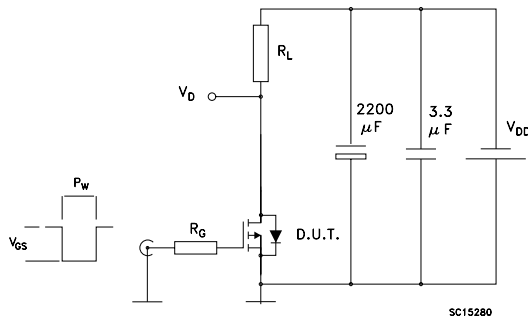


Figure 13. Gate charge test circuit

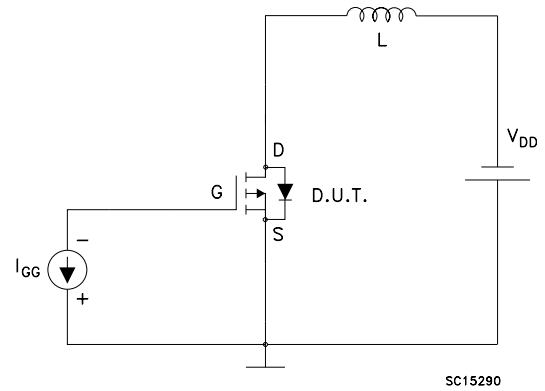
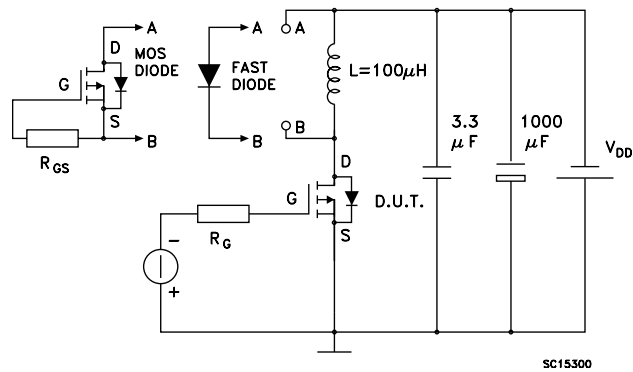


Figure 14. Test circuit for inductive load switching and diode recovery times

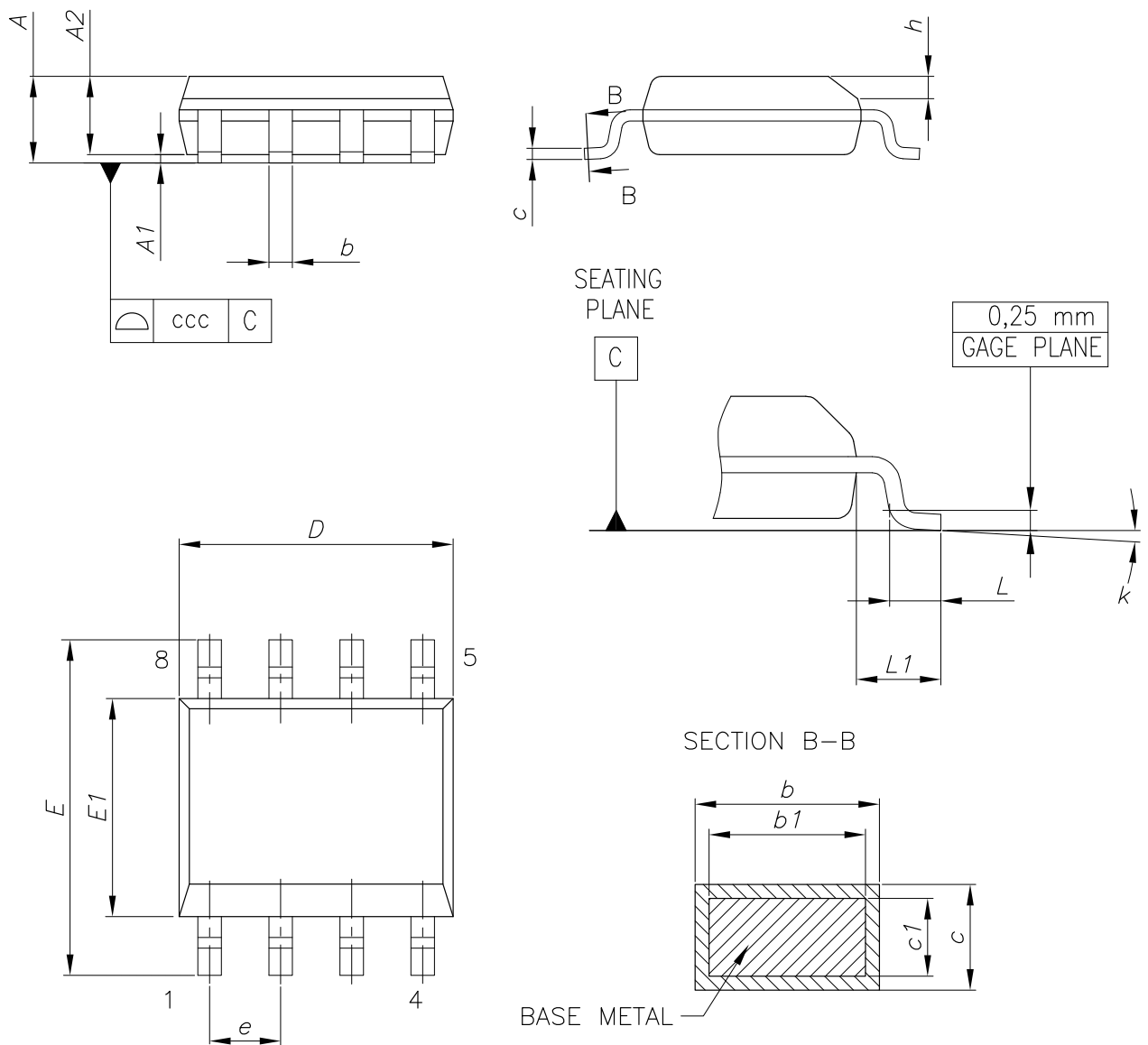


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 SO-8 package information

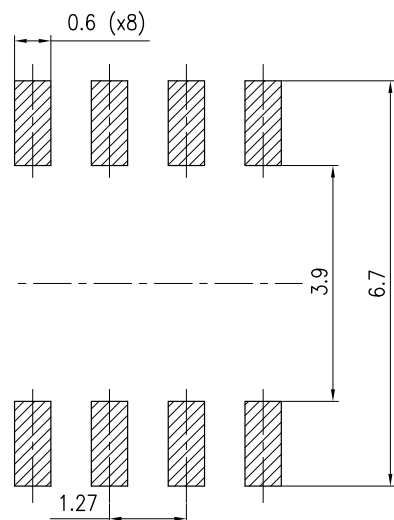
Figure 15. SO-8 package outline



0016023_So-807_fig2_Rev10

Table 7. SO-8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
b1	0.28		0.48
c	0.10		0.25
c1	0.10		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
k	0°		8°
ccc			0.10

Figure 16. SO-8 recommended footprint (dimensions are in mm)


0016023_So-807_footprint_Rev10

4.2 SO-8 packing information

Figure 17. SO-8 tape and reel dimensions

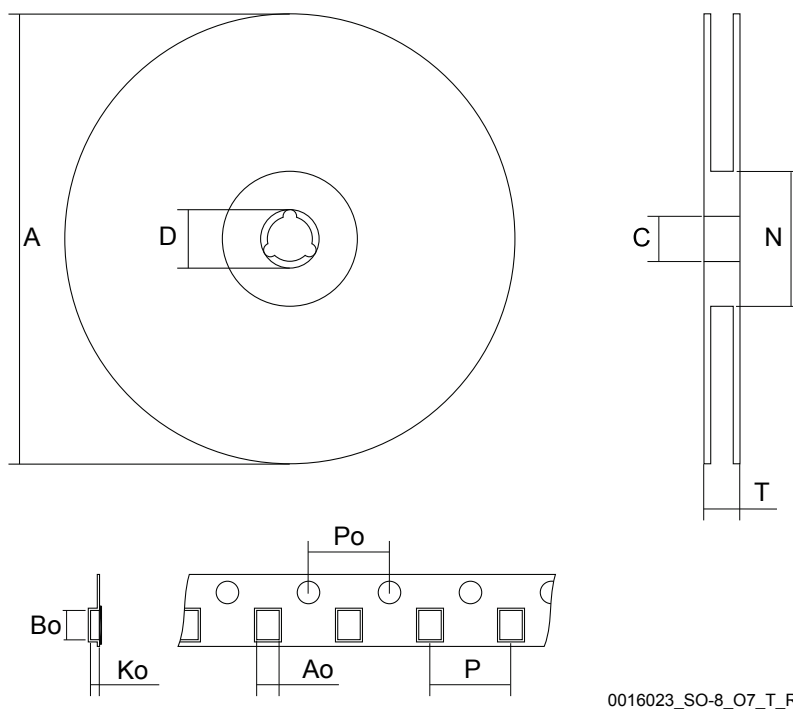


Figure 18. Tape orientation

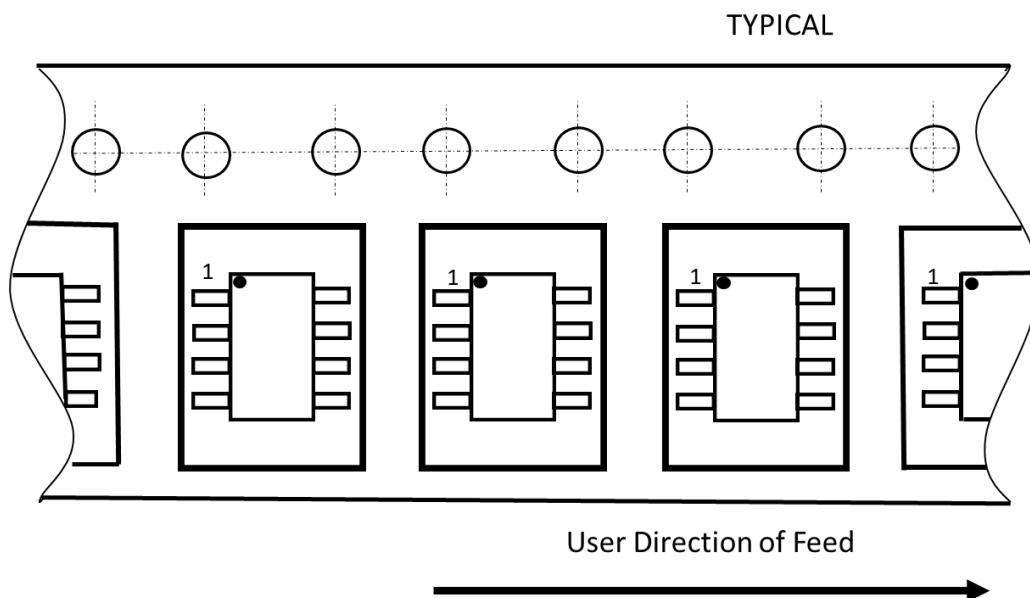


Table 8. SO-8 tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A		-	330
C	12.8		13.2
D	20.2		
N	60		
T			22.4
Ao	6.5		6.7
Bo	5.4		5.6
Ko	2.0		2.2
Po	3.9		4.1
P	7.9		8.1

Revision history

Table 9. Document revision history

Date	Version	Changes
10-Dec-2013	1	First revision.
10-Mar-2015	2	Text edits throughout document On cover page, updated title, description and features table Updated and renamed Table 4: Static Updated Table 5: Dynamic Updated Table 6: Switching times Updated Table 7: Source-drain diode Added Section 2.1: Electrical characteristics (curves) Minor text changes.
17-Feb-2021	3	Updated Internal schematic . Updated Section 4.2 SO-8 packing information . Minor text changes.

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