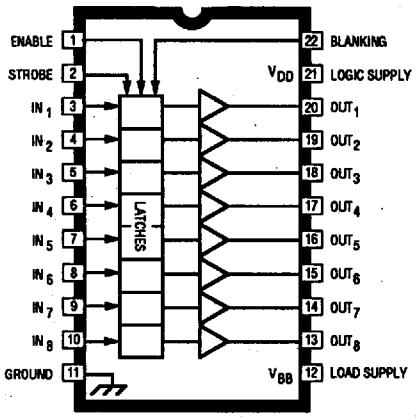
5815

T-52-13-09

BiMOS II 8-BIT LATCHED SOURCE DRIVERS

UCN5815A



Dwg. No. A-10,987

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature

Output Voltage, V_{OUT} . . . . . **60 V**
(Suffix '-1') . . . . . **80 V**
Logic Supply Voltage Range,
V_{DD} . . . . . **4.5 V to 15 V**
Load Supply Voltage Range,
V_{BB} . . . . . **5.0 V to 60 V**
(Suffix '-1') . . . . . **5.0 V to 80 V**
Input Voltage Range,
V_{IN} . . . . . **-0.3 V to V_{DD} + 0.3 V**
Continuous Output Current,
I_{OUT} . . . . . **-40 mA**
Package Power Dissipation, P_D
(UCN5815A/A-1) . . . . . **2.5 W***
(UCN5815EP/EP-1) . . . . . **2.27 W***
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

* Derate linearly to 0 W at +150°C.

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Designed primarily for use with high-voltage vacuum-fluorescent displays, the UCN5815A and UCN5815EP BiMOS II integrated circuits consist of eight NPN Darlington source drivers with output pull-down resistors, a CMOS latch for each driver, and common STROBE, BLANKING, and ENABLE functions. Selected devices (suffix "-1") have maximum output ratings of 80 V and 40 mA per driver. In all other respects, they are identical to the 60 V devices without the suffix.

BiMOS II devices have considerably better data-input rates than the original BiMOS circuits. With a 5 V logic supply, they will typically operate above 5 MHz. With a 12 V supply, significantly higher speeds are obtained. The CMOS inputs cause minimum loading and are compatible with standard CMOS and NMOS logic commonly found in microprocessor designs. TTL circuits may require the use of appropriate pull-up resistors.

The bipolar outputs may be used as segment, dot (matrix), bar, or digit drivers in vacuum-fluorescent displays. All eight outputs can be activated simultaneously at ambient temperatures in excess of 75°C. To simplify printed wiring board layout, output connections are opposite the inputs. A minimum component display subsystem, requiring few or no discrete components, can be assembled using the UCN5815A/EP with the UCN5810AF/EPF/LWF, UCN5812AF/EPF, or UCN5818AF/EPF serial-to-parallel latched driver.

Suffix 'A' devices are furnished in a standard 22-pin plastic DIP; suffix 'EP' indicates a 28-lead PLCC.

FEATURES

- 4.4 MHz Minimum Date-Input Rate
- High-Voltage Source Outputs
- CMOS, NMOS, TTL Compatible Inputs
- Low-Power CMOS Latches
- Internal Pull-Down Resistors
- Wide Supply-Voltage Range

Always order by complete part number:

Part Number	Package	Max V_{OUT}
UCN5815A	22-Pin DIP	60 V
UCN5815A-1		80 V
UCN5815EP	28-Lead PLCC	60 V
UCN5815EP-1		80 V

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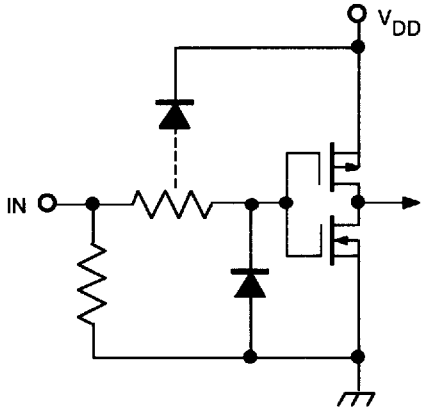
BiMOS II 8-BIT LATCHED SOURCE DRIVERS

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 60 V, V_{DD} = 5 V and 12 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage	V_{OUT}	I_{OUT} = -25 mA, V_{BB} = 60 V	57.5	—	V
		I_{OUT} = -25 mA, V_{BB} = 80 V, Suffix "-1" only	77.5	—	V
Output Pull-Down Current	I_{OUT}	V_{OUT} = V_{BB}	400	850	µA
		V_{BB} = V_{OUT} = 80 V, Suffix "-1" only	550	1150	µA
Output Leakage Current	I_{OUT}	T_A = 70°C	—	-15	µA
Input Voltage	$V_{IN(1)}$	V_{DD} = 5.0 V	3.5	5.3	V
		V_{DD} = 12 V	10.5	12.3	V
	$V_{IN(0)}$		-0.3	+0.8	V
Input Current	$I_{IN(1)}$	V_{DD} = V_{IN} = 5.0 V	—	100	µA
		V_{DD} = V_{IN} = 12 V	—	240	µA
Input Impedance	Z_{IN}	V_{DD} = 5.0 V	50	—	kΩ
Supply Current	I_{BB}	All outputs ON, All outputs open	—	10.5	mA
		All outputs OFF, All outputs open	—	100	µA
	I_{DD}	V_{DD} = 5.0 V, All outputs OFF, All inputs = 0 V	—	100	µA
		V_{DD} = 12 V, All outputs OFF, All inputs = 0 V	—	200	µA
		V_{DD} = 5.0 V, One output ON, All inputs = 0 V	—	1.0	mA
		V_{DD} = 12 V, One output ON, All inputs = 0 V	—	3.0	mA

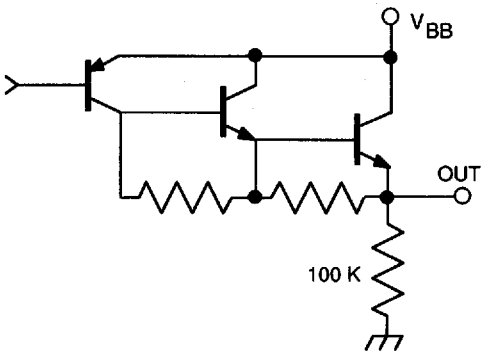
NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.

TYPICAL INPUT CIRCUIT



Dwg. No. EP-010-4A

TYPICAL OUTPUT DRIVER



Dwg. No. EP-021-3

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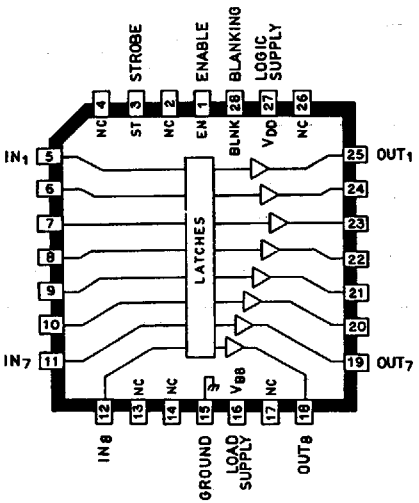
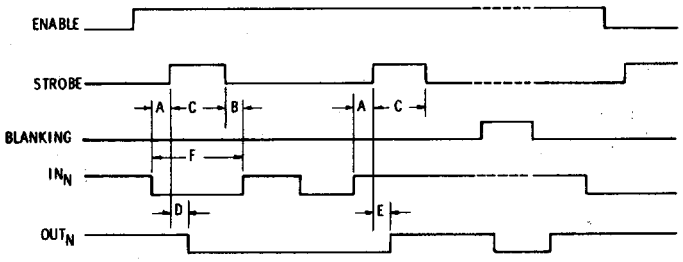
BiMOS II 8-BIT LATCHED SOURCE DRIVERS

UCN5815EP



Dwg. No. A-14,357



Dwg. No. A-10,991

TIMING CONDITIONS

(V_{DD} = 5 V, T_A = +25°C, Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Strobe Enabled (Data Set-Up Time) ..... 50 ns
B. Minimum Data Active Time After Strobe Disabled (Data Hold Time) ..... 50 ns
C. Minimum Strobe Pulse Width ..... 125 ns
D. Typical Time Between Strobe Activation and Output ON to OFF Transition ..... 5.0 µs
E. Typical Time Between Strobe Activation and Output OFF to ON Transition ..... 500 ns
F. Minimum Data Pulse Width ..... 225 ns

Information present at an input is transferred to its latch when the STROBE and ENABLE are high. The latches will continue to accept new data as long as both STROBE and ENABLE are held high. With either STROBE or ENABLE in the low state, no information can be loaded into the latches.

When the BLANKING input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches. With the BLANKING input low, the outputs are controlled by the state of the latches.

The timing conditions shown above guarantee a 4.4 MHz minimum data input rate with a 5 V supply. Typically, input rates above 5 MHz are permitted. With a 12 V supply, rates in excess of 10 MHz are possible.

TRUTH TABLE

INPUTS				OUT_N	
IN_N	STROBE	ENABLE	BLANK	T-1	T
0	1	1	0	X	0
1	1	1	0	X	1
X	X	X	1	X	0
X	0	X	0	1	1
X	0	X	0	0	0
X	X	0	0	1	1
X	X	0	0	0	0

X = irrelevant
T-1 = previous output state
T = present output state