

# 74LCX244

## Low Voltage Buffer/Line Driver with 5V Tolerant Inputs and Outputs

### Features

- 5V tolerant inputs and outputs
- 2.3V to 3.6V  $V_{CC}$  specifications provided
- 6.5ns  $t_{PD}$  max. ( $V_{CC} = 3.3V$ ), 10 $\mu$ A  $I_{CC}$  max.
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal<sup>(1)</sup>
- $\pm 24mA$  output drive ( $V_{CC} = 3.0V$ )
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500mA
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V
- Leadless DQFN package

### Note:

1. To ensure the high-impedance state during power up or down, OE should be tied to  $V_{CC}$  through a pull-up resistor: the minimum value of the resistor is determined by the current-sourcing capability of the driver.

### General Description

The LCX244 contains eight non-inverting buffers with 3-STATE outputs. The device may be employed as a memory address driver, clock driver and bus-oriented transmitter/receiver. The LCX244 is designed for low voltage (2.5V or 3.3V)  $V_{CC}$  applications with capability of interfacing to a 5V signal environment.

The LCX244 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

### Ordering Information

Order Number	Package Number	Package Description
74LCX244WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LCX244SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LCX244BQX <sup>(2)</sup>	MLP20B	20-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 4.5mm
74LCX244MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
74LCX244MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

### Note:

2. DQFN package available in Tape and Reel only.

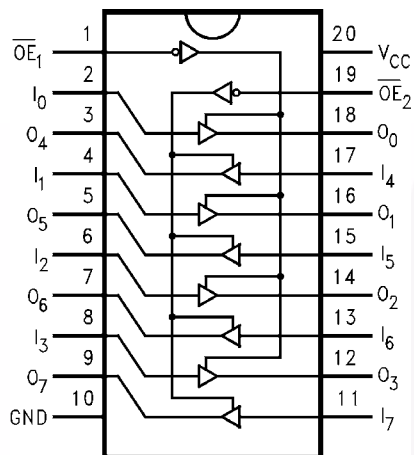
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.



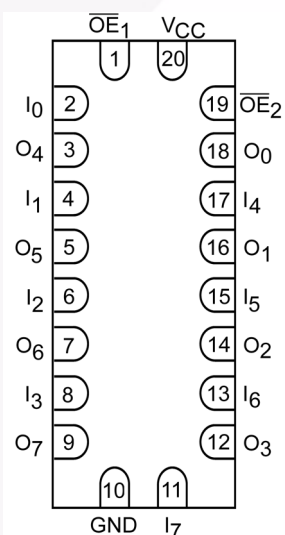
All packages are lead free per JEDEC: J-STD-020B standard.

## Connection Diagram

Pin Assignments for SOIC, SOP, SSOP, and TSSOP



Pad Assignments for DQFN

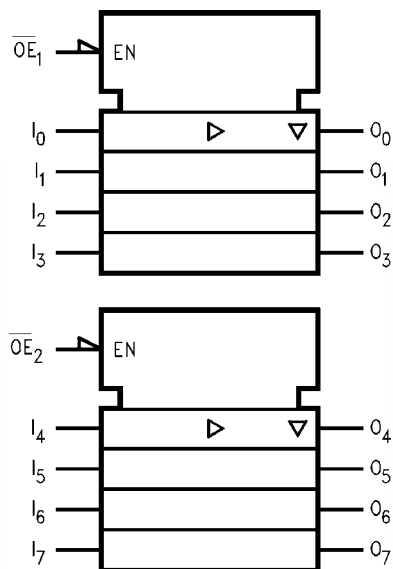


(Top Through View)

## Pin Description

Pin Names	Description
$\overline{OE}_1, \overline{OE}_2$	3-STATE Output Enable Inputs
$I_0-I_7$	Inputs
$\overline{O}_0-\overline{O}_7$	Outputs

## Logic Diagram



## Truth Tables

Inputs		Outputs
$\overline{OE}_1$	$I_n$	(Pins 12, 14, 16, 18)
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	$I_n$	(Pins 3, 5, 7, 9)
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	−0.5V to +7.0V
$V_I$	DC Input Voltage	−0.5V to +7.0V
$V_O$	DC Output Voltage Output in 3-STATE	−0.5V to +7.0V
	Output in HIGH or LOW State <sup>(3)</sup>	−0.5V to $V_{CC} + 0.5V$
$I_{IK}$	DC Input Diode Current, $V_I < GND$	−50mA
$I_{OK}$	DC Output Diode Current $V_O < GND$	−50mA
	$V_O > V_{CC}$	+50mA
$I_O$	DC Output Source/Sink Current	±50mA
$I_{CC}$	DC Supply Current per Supply Pin	±100mA
$I_{GND}$	DC Ground Current per Ground Pin	±100mA
$T_{STG}$	Storage Temperature	−65°C to +150°C

**Note:**

3.  $I_O$  Absolute Maximum Rating must be observed.

## Recommended Operating Conditions<sup>(4)</sup>

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
$V_{CC}$	Supply Voltage Operating	2.0	3.6	V
	Data Retention	1.5	3.6	
$V_I$	Input Voltage	0	5.5	V
$V_O$	Output Voltage 3-STATE	0	5.5	V
	HIGH or LOW State	0	$V_{CC}$	
$I_{OH} / I_{OL}$	Output Current $V_{CC} = 3.0V-3.6V$		±24	mA
	$V_{CC} = 2.7V-3.0V$		±12	
	$V_{CC} = 2.3V-2.7V$		±8	
$T_A$	Free-Air Operating Temperature	−40	85	°C
$\Delta t / \Delta V$	Input Edge Rate, $V_{IN} = 0.8V-2.0V$ , $V_{CC} = 3.0V$	0	10	ns/V

**Note:**

4. Unused inputs must be held HIGH or LOW. They may not float.

## DC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = -40°C to +85°C		Units
				Min.	Max.	
V <sub>IH</sub>	HIGH Level Input Voltage	2.3–2.7		1.7		V
		2.7–3.6		2.0		
V <sub>IL</sub>	LOW Level Input Voltage	2.3–2.7			0.7	V
		2.7–3.6			0.8	
V <sub>OH</sub>	HIGH Level Output Voltage	2.3–3.6	I <sub>OH</sub> = -100μA	V <sub>CC</sub> - 0.2		V
		2.3	I <sub>OH</sub> = -8mA	1.8		
		2.7	I <sub>OH</sub> = -12mA	2.2		
		3.0	I <sub>OH</sub> = -18mA	2.4		
			I <sub>OH</sub> = -24mA	2.2		
V <sub>OL</sub>	LOW Level Output Voltage	2.3–3.6	I <sub>OL</sub> = 100μA		0.2	V
		2.3	I <sub>OL</sub> = 8mA		0.6	
		2.7	I <sub>OL</sub> = 12mA		0.4	
		3.0	I <sub>OL</sub> = 16mA		0.4	
			I <sub>OL</sub> = 24mA		0.55	
I <sub>I</sub>	Input Leakage Current	2.3–3.6	0 ≤ V <sub>I</sub> ≤ 5.5V		±5.0	μA
I <sub>OZ</sub>	3-STATE Output Leakage	2.3–3.6	0 ≤ V <sub>O</sub> ≤ 5.5V, V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>		±5.0	μA
I <sub>OFF</sub>	Power-Off Leakage Current	0	V <sub>I</sub> or V <sub>O</sub> = 5.5V		10	μA
I <sub>CC</sub>	Quiescent Supply Current	2.3–3.6	V <sub>I</sub> = V <sub>CC</sub> or GND		10	μA
			3.6V ≤ V <sub>I</sub> , V <sub>O</sub> ≤ 5.5V <sup>(5)</sup>		±10	
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	2.3–3.6	V <sub>IH</sub> = V <sub>CC</sub> - 0.6V		500	μA

## Note:

5. Outputs disabled or 3-STATE only.

## AC Electrical Characteristics

Symbol	Parameter	T <sub>A</sub> = -40°C to +85°C, R <sub>L</sub> = 500Ω						Units
		V <sub>CC</sub> = 3.3V ± 0.3V, C <sub>L</sub> = 50pF		V <sub>CC</sub> = 2.7V, C <sub>L</sub> = 50pF		V <sub>CC</sub> = 2.5V ± 0.2V, C <sub>L</sub> = 30pF		
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay, Data to Output	1.5	6.5	1.5	7.5	1.5	7.8	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time	1.5	8.0	1.5	9.0	1.5	10.0	ns
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Output Disable Time	1.5	7.0	1.5	8.0	1.5	8.4	ns
t <sub>OSHL</sub> , t <sub>OSLH</sub>	Output to Output Skew <sup>(6)</sup>		1.0					ns

## Note:

6. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>).

**Dynamic Switching Characteristics**

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = 25°C	Unit
				Typical	
V <sub>OLP</sub>	Quiet Output Dynamic Peak V <sub>OL</sub>	3.3	C <sub>L</sub> = 50pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V	0.8	V
		2.5	C <sub>L</sub> = 30pF, V <sub>IH</sub> = 2.5V, V <sub>IL</sub> = 0V	0.6	
V <sub>OLV</sub>	Quiet Output Dynamic Valley V <sub>OL</sub>	3.3	C <sub>L</sub> = 50pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V	−0.8	V
		2.5	C <sub>L</sub> = 30pF, V <sub>IH</sub> = 2.5V, V <sub>IL</sub> = 0V	−0.6	

**Capacitance**

Symbol	Parameter	Conditions	Typical	Units
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = Open, V <sub>I</sub> = 0V or V <sub>CC</sub>	7.0	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = 3.3V, V <sub>I</sub> = 0V or V <sub>CC</sub>	8.0	pF
C <sub>PD</sub>	Power Dissipation Capacitance	V <sub>CC</sub> = 3.3V, V <sub>I</sub> = 0V or V <sub>CC</sub> , f = 10MHz	25.0	pF

# AC Loading and Waveforms (Generic for LCX Family)

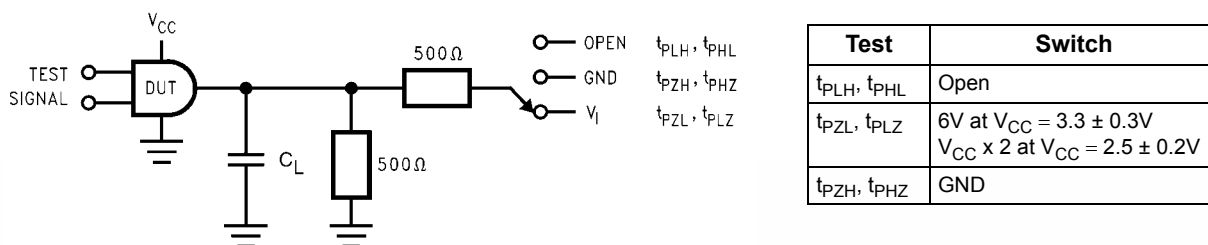
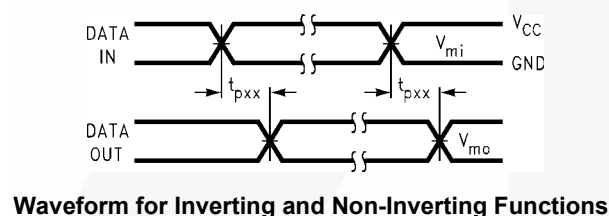
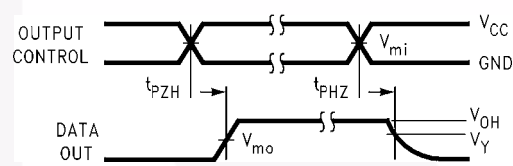


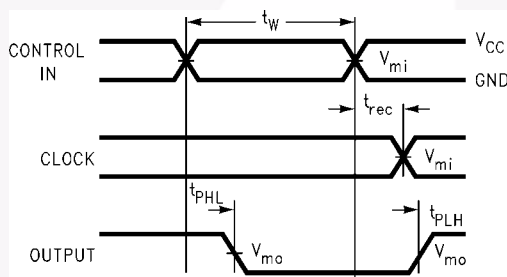
Figure 1. AC Test Circuit ( $C_L$  includes probe and jig capacitance)



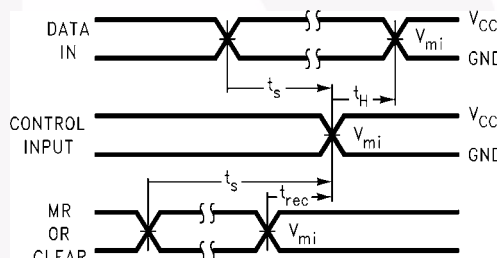
Waveform for Inverting and Non-Inverting Functions



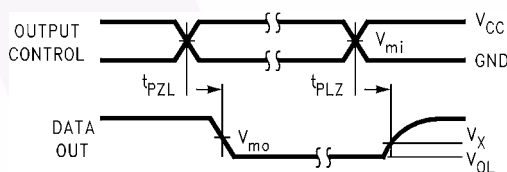
3-STATE Output High Enable and Disable Times for Logic



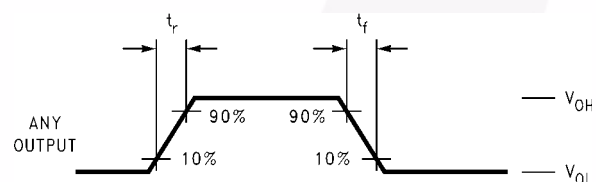
Propagation Delay, Pulse Width and  $t_{rec}$  Waveforms



Setup Time, Hold Time and Recovery Time for Logic



3-STATE Output Low Enable and Disable Times for Logic

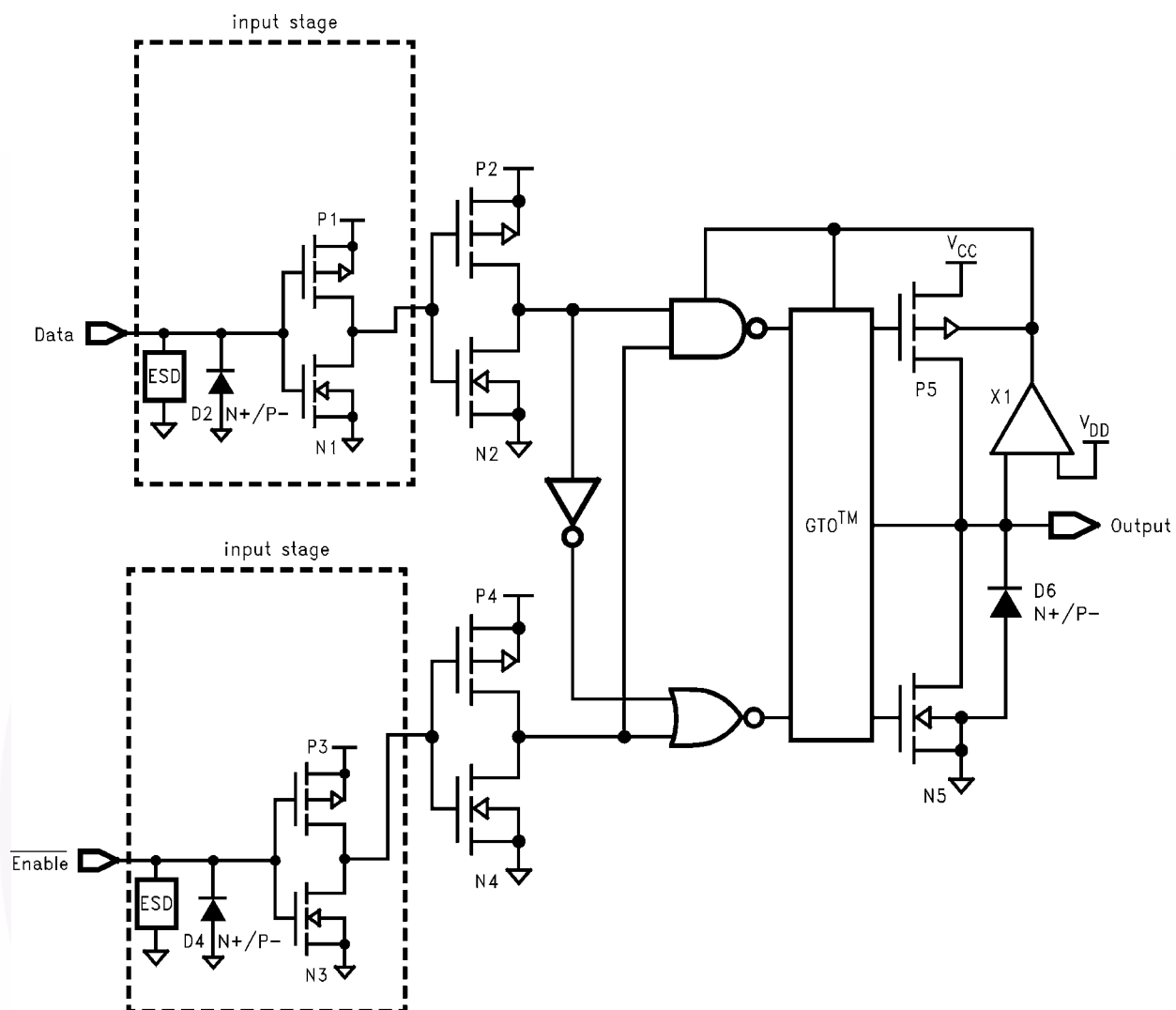


$t_{rise}$  and  $t_{fall}$

Symbol	$V_{CC}$		
	$3.3V \pm 0.3V$	$2.7V$	$2.5V \pm 0.2V$
$V_{mi}$	1.5V	1.5V	$V_{CC}/2$
$V_{mo}$	1.5V	1.5V	$V_{CC}/2$
$V_x$	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$
$V_y$	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$

Figure 2. Waveforms (Input Characteristics;  $f = 1MHz$ ,  $t_r = t_f = 3ns$ )

# **Schematic Diagram** (Generic for LCX Family)

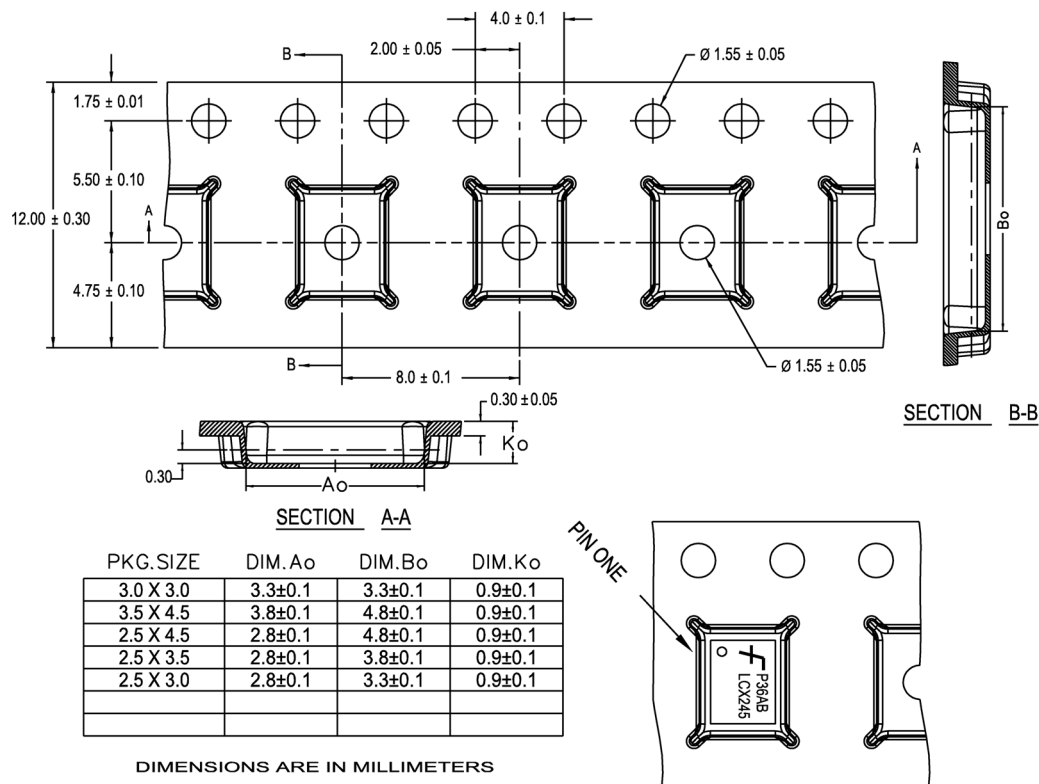


## Tape and Reel Specification

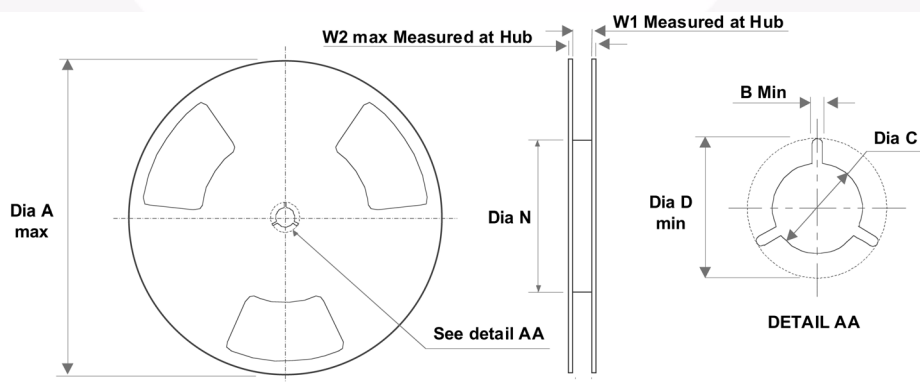
### Tape Format for DQFN

Package Designator	Tape Section	Number of Cavities	Cavity Status	Cover Tape Status
BQX	Leader (Start End)	125 (typ.)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ.)	Empty	Sealed

### Tape Dimension inches (millimeters)



### Reel Dimensions inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2
12mm	13.0 (330.0)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.488 (12.4)	0.724 (18.4)



## Physical Dimensions

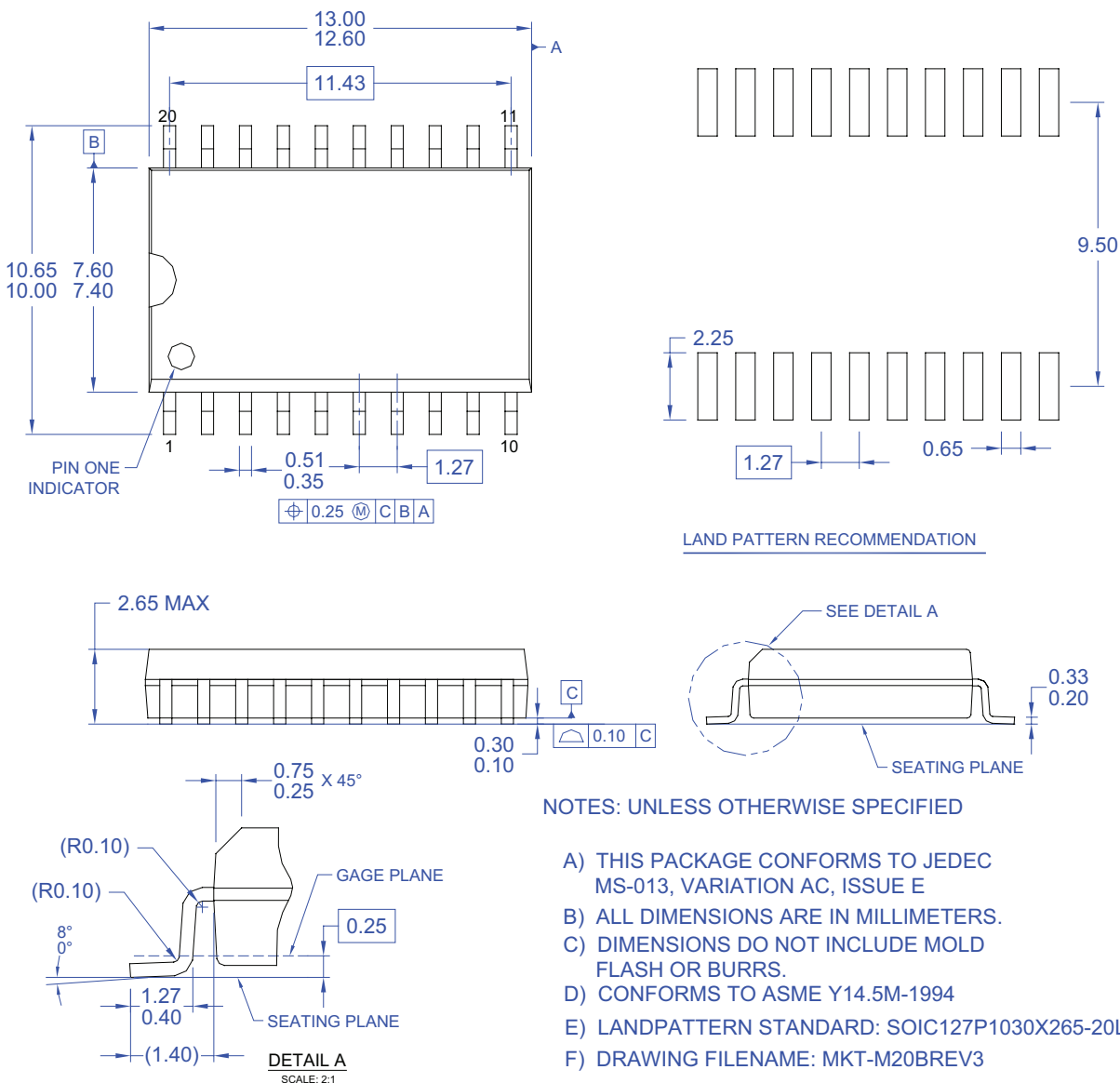


Figure 3. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide

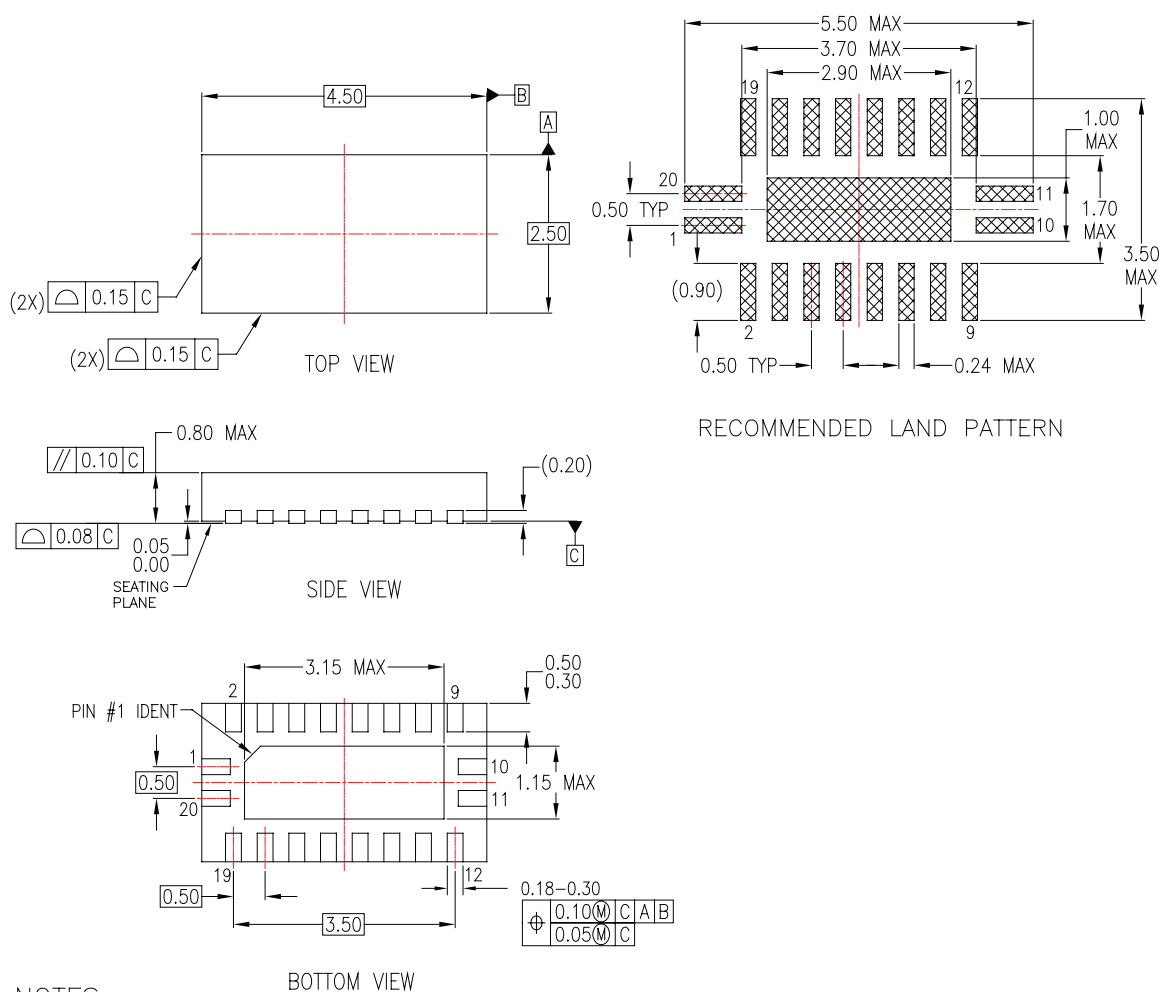
Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>.



## Physical Dimensions (Continued)



## NOTES:

- CONFORMS TO JEDEC REGISTRATION MO-241, VARIATION AC
- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP20BrevA

**Figure 5. 20-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 4.5mm**

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>






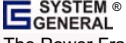






## TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

Build it Now	FRFET®	Programmable Active Droop	the power®
CorePLUS	Global Power Resource <sup>SM</sup>	QFET®	franchise
CorePOWER	Green FPS	QS	TinyBoost
CROSSVOLT	Green FPS   e-Series	Quiet Series	TinyBuck
CTL™	GTO	RapidConfigure	TinyLogic®
Current Transfer Logic™	IntelliMAX	 ™	TINYOPTO
EcoSPARK®	ISOPANAR	Saving our world, 1mW/W/kW at a time™	TinyPower
EfficientMax™	MegaBuck™	SmartMax™	TinyPWM
EZSWITCH™ *	MICROCOUPLER	SMART START	TinyWire
 ™	MicroFET	SPM®	TriFault Detect
 ®	MicroPak	STEALTH™	oSerDes
Fairchild®	MillerDrive™	SuperFET	 SerDes®
Fairchild Semiconductor®	MotionMax™	SuperSOT   -3	UHC®
FACT Quiet Series™	Motion-SPM™	SuperSOT   -6	Ultra FRFET
FACT®	OPTOLOGIC®	SuperSOT   -8	UniFET
FAST®	OPTOPLANAR®	SupreMOS™	VCX
FastvCore	 PDP SPM™	SyncFET™	VisualMax
FlashWriter® *	Power-SPM	 SYSTEM® GENERAL	XS™
FPS	PowerTrench®	The Power Franchise®	
F-PFS	PowerXS™		

\* EZSWITCH™ and FlashWriter® are trademarks of System General Corporation, used under license by Fairchild Semiconductor.

## DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

## LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, [www.fairchildsemi.com](http://www.fairchildsemi.com), under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I38