SLOS074 - D2785, OCTOBER 1983 - REVISED JUNE 1988

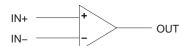
7 OUT

D OR P PACKAGE

(TOP VIEW)

- Matched Gain and Offset Between **Amplifiers**
- Unity-Gain Bandwidth . . . 3 MHz Min
- Slew Rate . . . 1.5 V/ns Min
- Low Equivalent Input Noise Voltage 2 μV/Hz Max (20 Hz to 20 kHz)
- No Frequency Compensation Required
- No Latch Up
- Wide Common-Mode Voltage Range
- **Low Power Consumption**
- Designed to be Interchangeable with Raytheon RC4559

symbol (each amplifier)



#### **AVAILABLE OPTIONS**

SYMBO	LIZATION	OPERATING	
DEVICE	PACKAGE	TEMPERATURE	V <sub>IO</sub> max at 25°C
	SUFFIX	RANGE	at 25 0
RC4559	D, P	−0°C to 70°C	6 mV

The D packages are available taped and reeled. Add the suffix R to the device type when ordering. (i.e., RC4559DR)

### description

The RC4559 is a dual high-performance operational amplifier. The high common-mode input voltage and the absence of latch-up make this amplifier ideal for low-noise signal applications such as audio preamplifiers and signal conditioners. This amplifier features a guaranteed dynamic performance and output drive capability that far exceeds that of the general-purpose type amplifiers.

The RC4559 is characterized for operation from 0°C to 70°C.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V <sub>CC+</sub> (see Note 1)	V
Supply voltage V <sub>CC</sub> (see Note 1)	V
Differential input voltage (see Note 2) ±30	V
Input voltage (any input, see Notes 1 and 3) ±15	V
Duration of output short-circuit to ground, one amplifier at a time (see Note 4) unlimited	эd
Continuous total dissipation	W
Operating free-air temperature range	Ò,
Storage temperature range	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	,C

- NOTES: 1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V<sub>CC+</sub> and V<sub>CC-</sub>.
  - 2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
  - 3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
  - 4. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.



## RC4559 DUAL HIGH-PERFORMANCE OPERATIONAL AMPLIFIER

## electrical characteristics at specified free-air temperature, $V_{CC+}$ = 15 V, $V_{CC-}$ = -15 V

	PARAMETER	TEST CONDITIONS†	T <sub>A</sub> ‡	MIN	TYP	MAX	UNIT
\/	land offert veltage	V- 0	25°C		2	6	mV
VIO	Input offset voltage	VO = 0	Full Range			7.5	IIIV
lio	land offert surrent	V- 0	25°C		5	100	
IIO	Input offset current	VO = 0	Full range			200	nA
lini	nput bias current	V <sub>O</sub> = 0	25°C		40	250	nA
IBI	riput bias current	VO = 0	Full range			500	IIA
$V_{I}$	Input voltage range		25°C	±12	±13		V
		$R_L \ge 3 \text{ k}\Omega$	25°C	±12	±13		
VOM	Maximum peak output voltlage swing	$R_L = 600 \Omega$	25°C	±9.5	±10		V
		$R_L \ge 2 k\Omega$	Full range	±10			
VI		$V_0 = \pm 10 \text{ V},$	25°C 20		300		\//m\/
	Input voltage range	$R_L = 2 k\Omega$	Full range	15			V/mV
ВОМ	Maximum output-swing bandwidth	$V_{OPP} = 20 \text{ V},$ $R_L = 2 \text{ k}\Omega$	25°C	24	32		kHz
B <sub>1</sub>	Unity-gain bandwidth		25°C	3	4		MHz
rį	Input resistance		25°C	0.3	1		MΩ
CMRR	Common-mode rejection ratio	VO = 0	25°C	80	100		dB
ksvs	Supply voltage sensitivity (ΔV <sub>IO</sub> /ΔV <sub>CC</sub> )	V <sub>O</sub> = 0	25°C		10	75	μV/V
V <sub>n</sub>	Equivalent input noise voltage (closed loop)	$A_{VD} = 100,$ $R_{S} = 1 \text{ k}\Omega,$ f = 20  Hz to  20  kHz	25°C		1.4	2	μV
In	Equivalent input noise current	f = 20 Hz to 20 kHz	25°C		25		рΑ
			25°C		3.3	5.6	
ICC	Supply current (both amplifiers)	No load, No signal	0°C		4	6.6	mA
			70°C		3	5	
V <sub>01</sub> /V <sub>02</sub>	Crosstalk attentuation	$A_{VD} = 100,$ $R_{S} = 1 \text{ k}\Omega,$ f = 10  kHz	25°C		90		dB

<sup>†</sup> All characteristics are specified under open-loop operation, unless otherwise noted.

## matching characteristics at $V_{CC+} = 15 \text{ V}$ , $V_{CC-} = -15 \text{ V}$ , $T_A = 25^{\circ}\text{C}$

	301	· A		
	PARAMETER	TEST CONDITIONS	MIN TYP MA	X UNIT
VIO	Input offset voltage	V <sub>O</sub> = 0	±0.2	mV
liO	Input offset current	V <sub>O</sub> = 0	±7.5	nA
I <sub>IB</sub>	Input bias current	V <sub>O</sub> = 0	±15	nA
A <sub>VD</sub>	Large-signal differential voltage amplification	$V_O = \pm 10 \text{ V}, R_L = 2 \text{ k}\Omega$	±1	dB

## operating characteristics, $V_{CC+}$ = 15 V, $V_{CC-}$ = -15 V, $T_A$ = 25°C

	PARAMETER		TEST CONDITION	ONS	MIN	TYP	MAX	UNIT
t <sub>r</sub>	Rise time	$V_{I} = 20 \text{ mV},$	$R_L = 2 k\Omega$ ,	$C_L = 100  pF$		80		μs
	Overshoot	]				18%		
SR	Slew rate at unity gain	$V_{I} = 10 \text{ mV},$	$R_L = 2 k\Omega$ ,	C <sub>L</sub> = 100 pF	1.5	2		V/μs



<sup>‡</sup> Full range operating free-air temperature range is 0°C to 70°C.





ti.com 23-Apr-2007

#### PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
RC4559D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
RC4559DE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
RC4559DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
RC4559DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
RC4559DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
RC4559DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
RC4559P	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
RC4559PE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

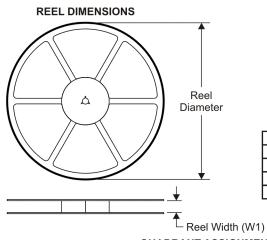
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

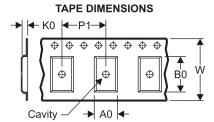
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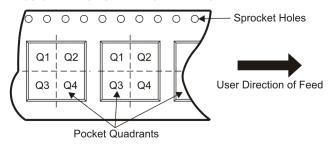
### TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

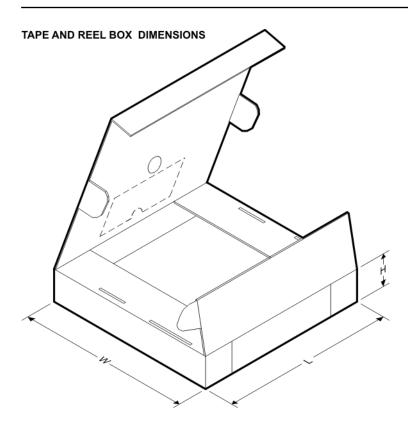
## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

	Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
I	RC4559DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1



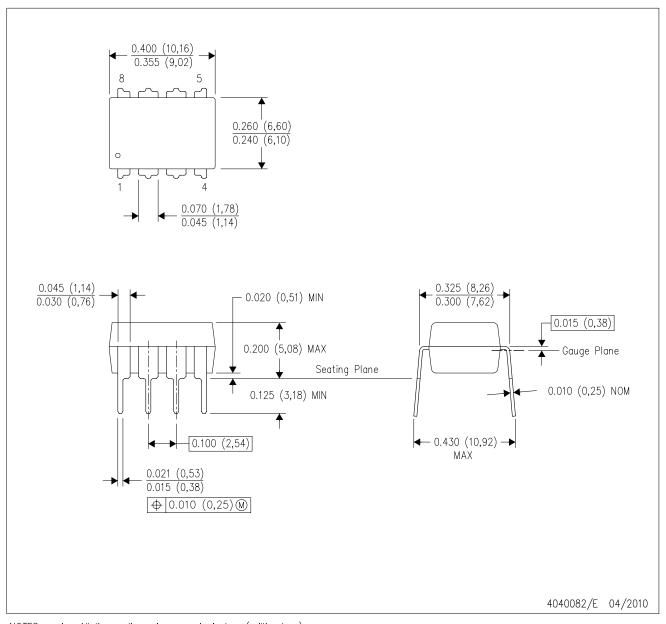


#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
RC4559DR	SOIC	D	8	2500	340.5	338.1	20.6

## P (R-PDIP-T8)

## PLASTIC DUAL-IN-LINE PACKAGE



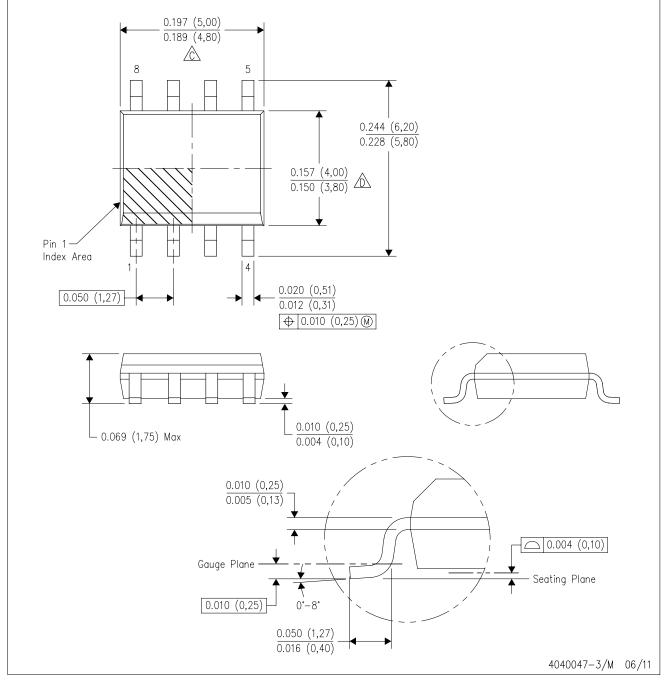
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001 variation BA.



## D (R-PDSO-G8)

## PLASTIC SMALL OUTLINE



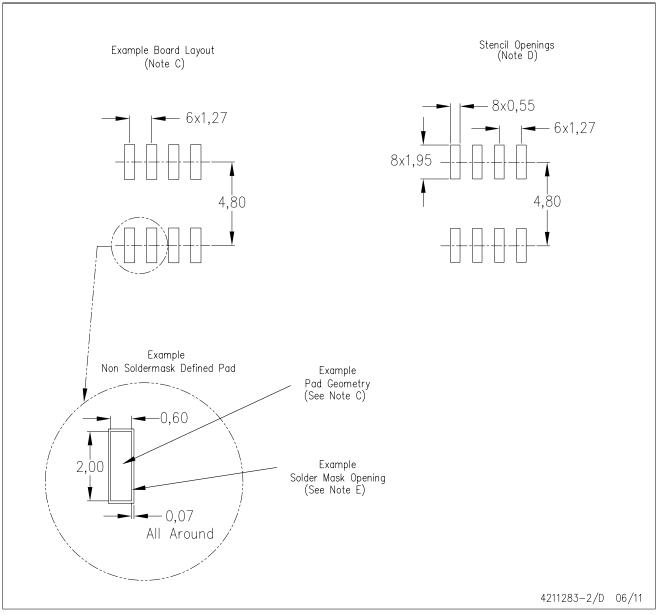
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.



# D (R-PDSO-G8)

## PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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