Freescale Semiconductor
Technical Data

Document Number: MRF7S21210H
Rev. 0, 7/2008

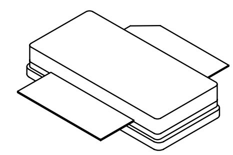
RoHS

RF Power Field Effect Transistor

N-Channel Enhancement-Mode Lateral MOSFET

MRF7S21210HSR3

2110-2170 MHz, 63 W AVG., 28 V
SINGLE W-CDMA
LATERAL N-CHANNEL
RF POWER MOSFET



CASE 465A-06, STYLE 1
NI-780S

Designed for CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for CDMA and multicarrier amplifier applications. To be used in Class AB and Class C for TD-SCDMA, PCN-PCS/cellular radio and WLL applications.

- Typical Single-Carrier W-CDMA Performance: V_{DD} = 28 Volts, I_{DQ} = 1400 mA, P_{out} = 63 Watts Avg., Full Frequency Band, 3GPP Test Model 1, 64 DPCH with 50% Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.
  Power Gain — 18.5 dB
  Drain Efficiency — 29%
  Device Output Signal PAR — 5.9 dB @ 0.01% Probability on CCDF
  ACPR @ 5 MHz Offset — -33 dBc in 3.84 MHz Channel Bandwidth
- Capable of Handling 5:1 VSWR, @ 32 Vdc, 2140 MHz, 190 Watts CW Output Power
- Typical P_{out} @ 1 dB Compression Point ≃ 190 Watts CW

Features

- 100% PAR Tested for Guaranteed Output Power Capability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (1)	T_J	225	°C
CW Operation @ T_C = 25°C Derate above 25°C	CW	253 1.5	W W/°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2)	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 190 W CW Case Temperature 72°C, 63 W CW	$R_{\theta JC}$	 0.33 0.37	°C/W

1. Continuous use at maximum temperature will affect MTTF.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

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Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1C (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Electrical Characteristics (T_C = 25°C unless otherwise noted)

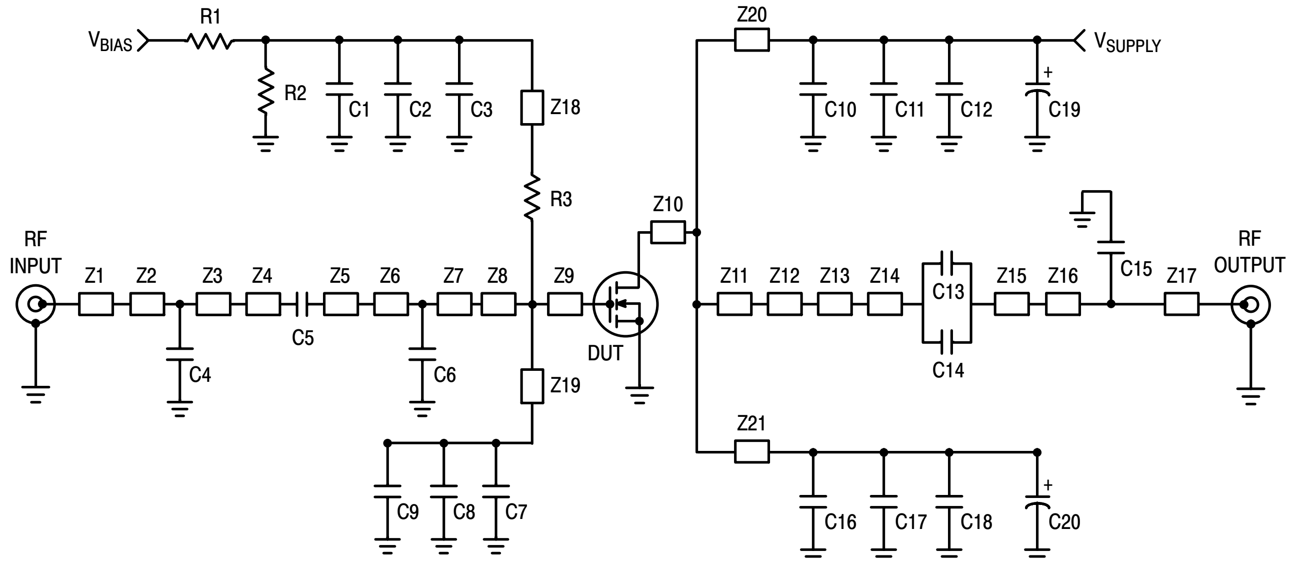
Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 513 μAdc)	$V_{GS(th)}$	1.2	2	2.7	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_D = 1400 mAdc)	$V_{GS(Q)}$	—	2.7	—	Vdc
Fixture Gate Quiescent Voltage (1) (V_{DD} = 28 Vdc, I_D = 1400 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	4	5.4	7	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 5.13 Adc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc
Dynamic Characteristics (2)					
Reverse Transfer Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	2.02	—	pF
Output Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	257	—	pF
Input Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc ± 30 mV(rms)ac @ 1 MHz)	C_{iss}	—	516	—	pF
Functional Tests (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1400 mA, P_{out} = 63 W Avg., f = 2112.5 MHz and f = 2167.5 MHz, Single-Carrier W-CDMA, 3GPP Test Model 1, 64 DPCH, 50% Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	17	18.5	20.5	dB
Drain Efficiency	η_D	26	29	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	5.5	5.9	—	dB
Adjacent Channel Power Ratio	ACPR	—	-33	-31	dBc
Input Return Loss	IRL	—	-15	-8	dB

1. V_{GG} = 2 x $V_{GS(Q)}$. Parameter measured on Freescale Test Fixture, due to resistive divider network on the board. Refer to Test Circuit schematic.
2. Part internally matched both on input and output.

(continued)

Table 4. Electrical Characteristics (T_C = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performances (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1400 mA, 2110-2170 MHz Bandwidth					
IMD Symmetry @ 130 W PEP, P_{out} where IMD Third Order Intermodulation ≅ 30 dBc (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands > 2 dB)	IMD_{sym}	—	15	—	MHz
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	60	—	MHz
Gain Flatness in 60 MHz Bandwidth @ P_{out} = 63 W Avg.	G_F	—	1.2	—	dB
Average Deviation from Linear Phase in 60 MHz Bandwidth @ P_{out} = 190 W CW	Φ	—	1.1	—	°
Average Group Delay @ P_{out} = 190 W CW, f = 2140 MHz	Delay	—	2.5	—	ns
Part-to-Part Insertion Phase Variation @ P_{out} = 190 W CW, f = 2140 MHz, Six Sigma Window	ΔΦ	—	26	—	°
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.019	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	ΔP1dB	—	0.011	—	dBm/°C



Z1	0.402″ x 0.066″ Microstrip	Z12	0.044″ x 0.613″ Microstrip
Z2	0.840″ x 0.076″ Microstrip	Z13	0.398″ x 0.102″ Microstrip
Z3	0.029″ x 0.076″ Microstrip	Z14	0.071″ x 0.220″ Microstrip
Z4	0.059″ x 0.118″ Microstrip	Z15	0.071″ x 0.220″ Microstrip
Z5	0.059″ x 0.118″ Microstrip	Z16	0.439″ x 0.066″ Microstrip
Z6	0.029″ x 0.076″ Microstrip	Z17	0.764″ x 0.066″ Microstrip
Z7	0.194″ x 0.076″ Microstrip	Z18	0.353″ x 0.090″ Microstrip
Z8	0.510″ x 0.533″ Microstrip	Z19	0.797″ x 0.090″ Microstrip
Z9	0.114″ x 0.533″ Microstrip	Z20, Z21	0.660″ x 0.120″ Microstrip
Z10	0.139″ x 1.268″ Microstrip	PCB	Taconic RF35, 0.030”, $\varepsilon_r = 3.5$
Z11	0.304″ x 1.201″ Microstrip		

Figure 1. MRF7S21210HSR3 Test Circuit Schematic

Table 5. MRF7S21210HSR3 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C9, C11, C12, C17, C18	10 μF, 50 V Chip Capacitors	C5750X5R1H106MT	TDK
C2, C8	100 nF Chip Capacitors	12065C104KAT	AVX
C3, C7, C10, C13, C14, C16	6.8 pF Chip Capacitors	ATC100B6R8BT500XT	ATC
C4	0.3 pF Chip Capacitor	ATC100B0R3BT500XT	ATC
C5	5.6 pF Chip Capacitor	ATC100B5R6BT500XT	ATC
C6	0.2 pF Chip Capacitor	ATC100B0R2BT500XT	ATC
C15	0.4 pF Chip Capacitor	ATC100B0R4BT500XT	ATC
C19, C20	470 μF Electrolytic Capacitors	2222 12018471	BC Components
R1, R2	10 KΩ, 1/4 W Chip Resistors	CRCW12061002FKEA	Vishay
R3	10 Ω, 1/4 W Chip Resistor	CRCW12061000FKEA	Vishay

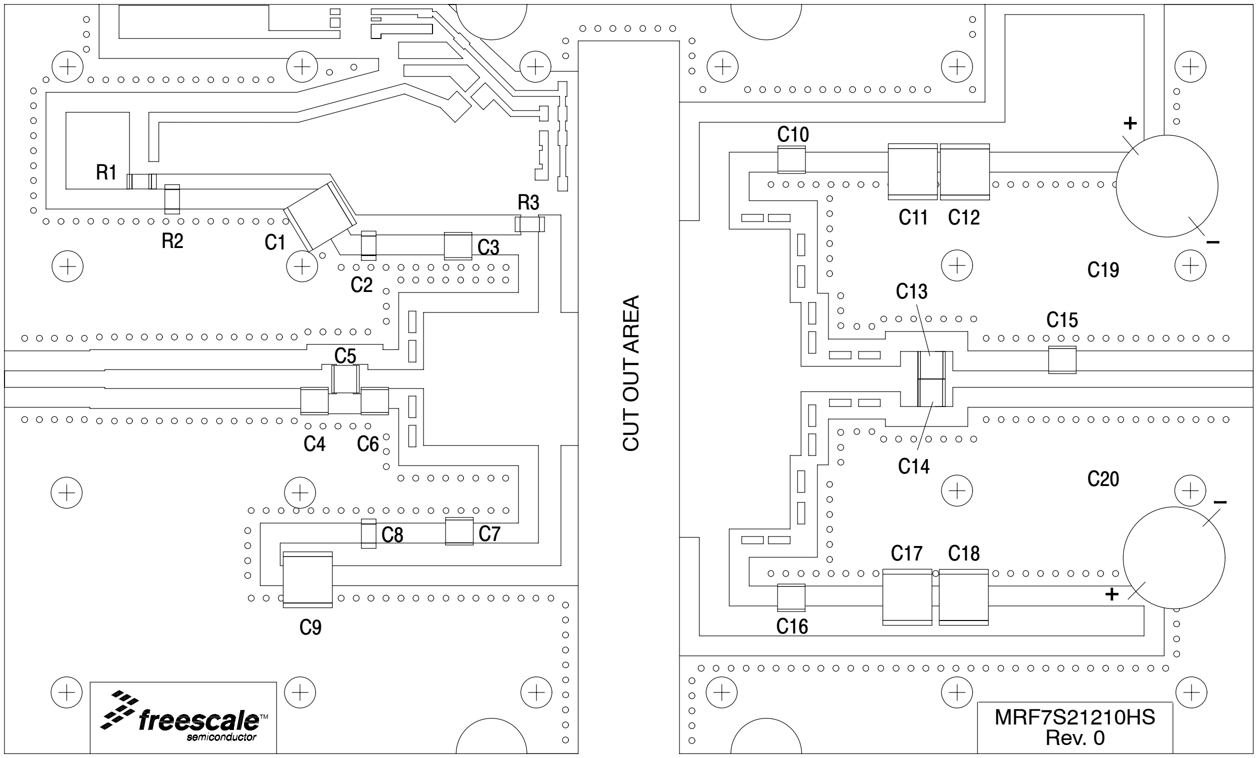
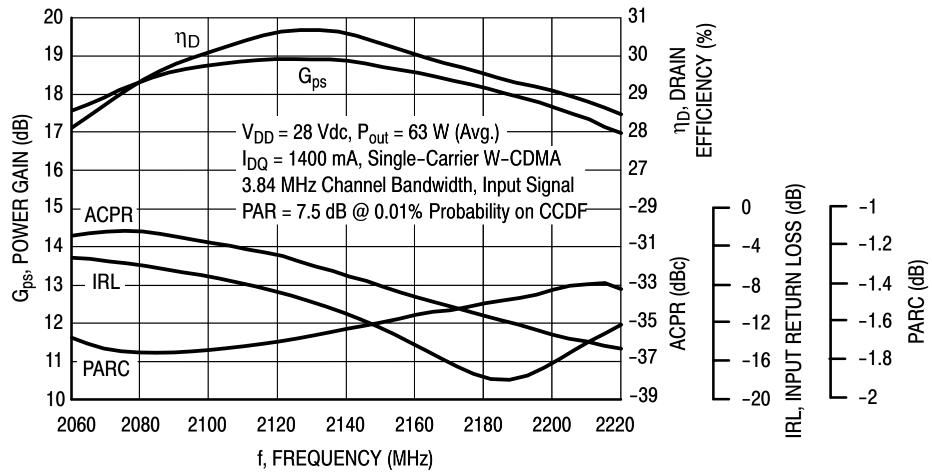


Figure 2. MRF7S21210HSR3 Test Circuit Component Layout

TYPICAL CHARACTERISTICS



Note: Measurement conducted with device soldered on Freescale test fixture.

Figure 3. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 63 Watts Avg.

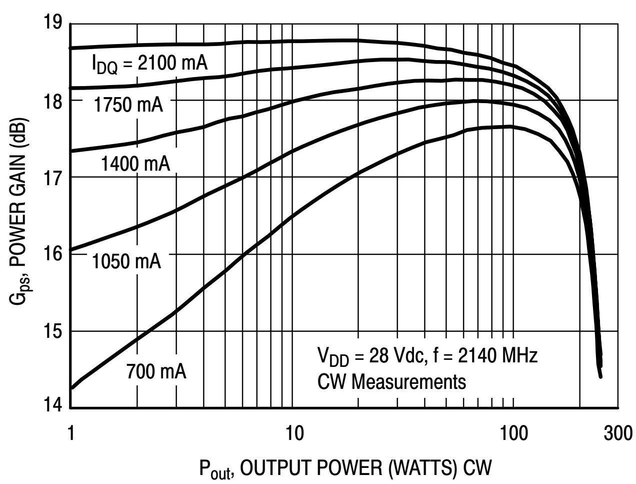


Figure 4. CW Power Gain versus Output Power

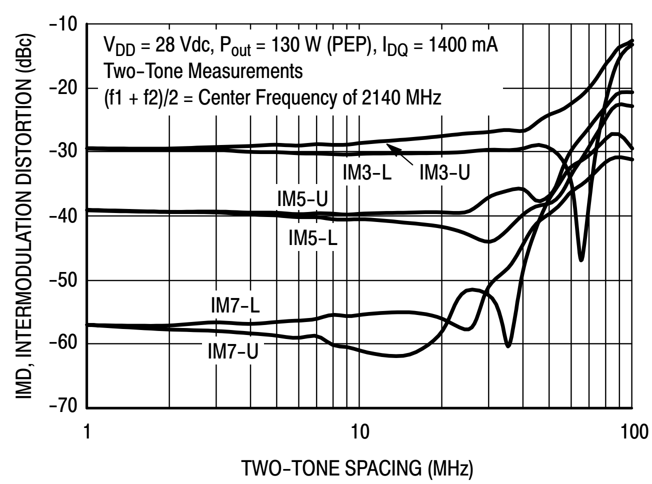


Figure 5. Intermodulation Distortion Products versus Tone Spacing

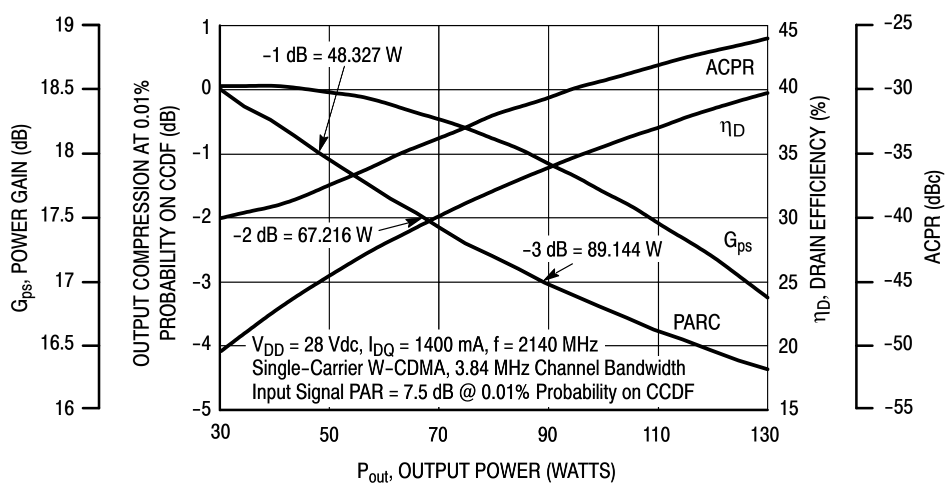


Figure 6. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

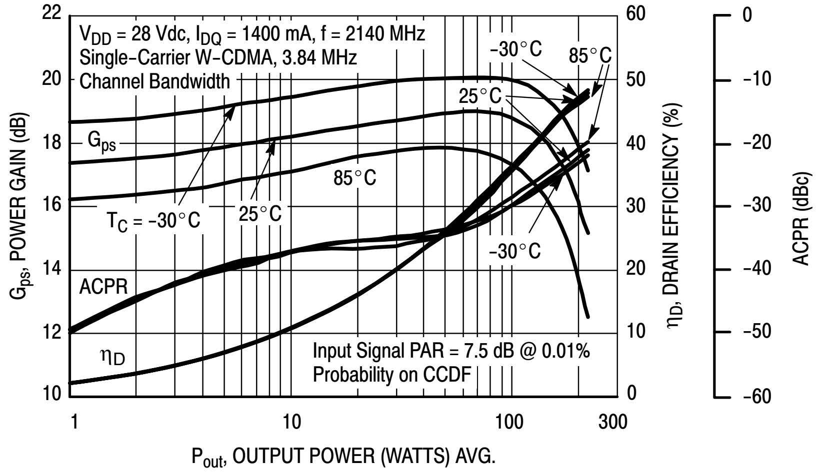


Figure 7. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

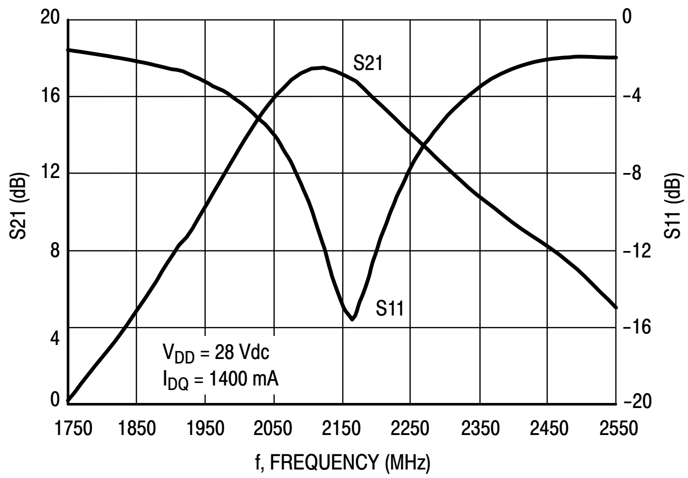


Figure 8. Broadband Frequency Response

W-CDMA TEST SIGNAL

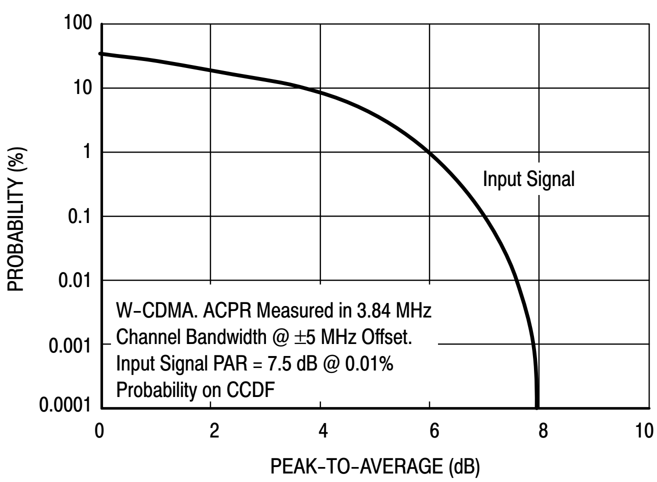


Figure 9. CCDF W-CDMA 3GPP, Test Model 1, 64 DPCH, 50% Clipping, Single-Carrier Test Signal

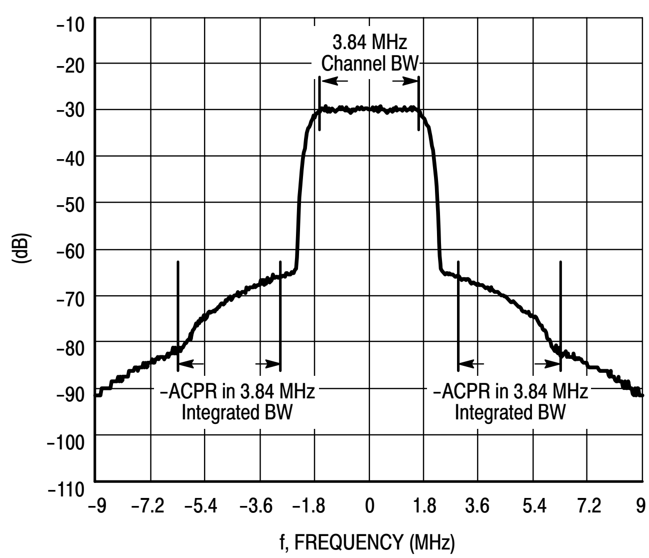
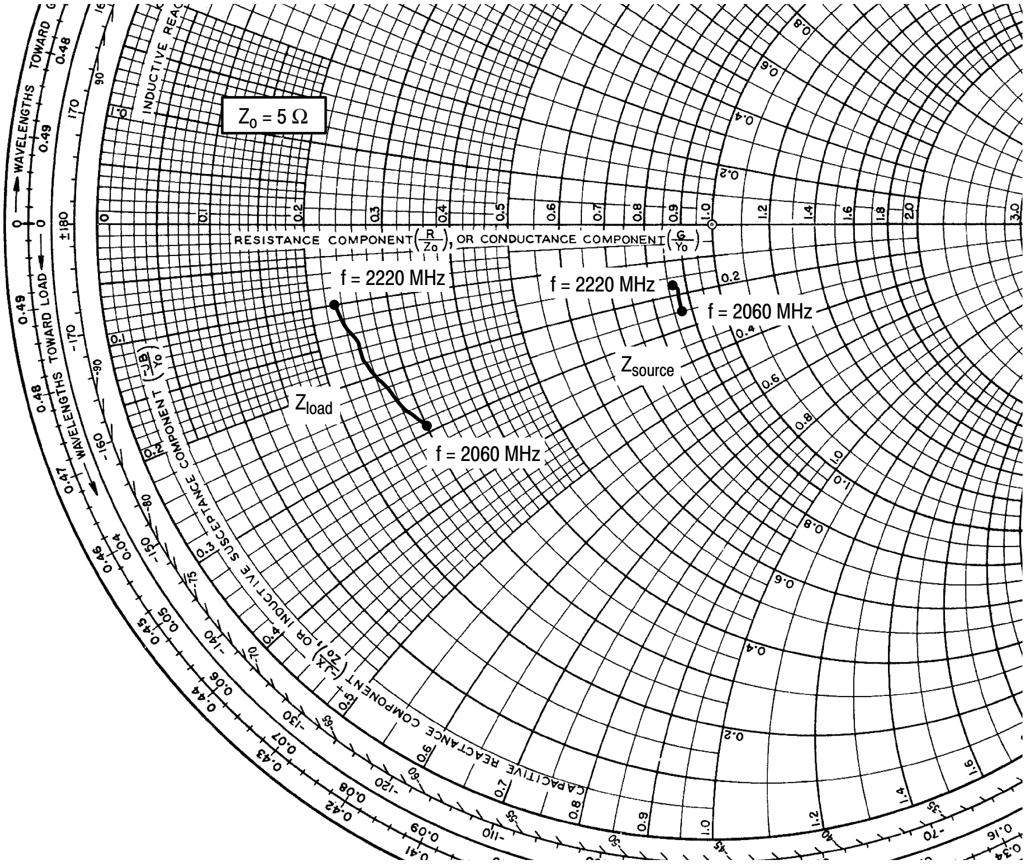


Figure 10. Single-Carrier W-CDMA Spectrum



V_{DD} = 28 Vdc, I_{DQ} = 1400 mA, P_{out} = 63 W Avg.

f MHz	Z_{source} Ω	Z_{load} Ω
2060	4.34 - j1.26	1.52 - j1.46
2080	4.34 - j1.20	1.47 - j1.35
2100	4.34 - j1.14	1.42 - j1.23
2120	4.33 - j1.09	1.37 - j1.11
2140	4.34 - j1.05	1.32 - j0.99
2160	4.33 - j0.96	1.27 - j0.87
2180	4.33 - j0.92	1.23 - j0.75
2200	4.33 - j0.92	1.19 - j0.64
2220	4.32 - j0.87	1.15 - j0.52

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

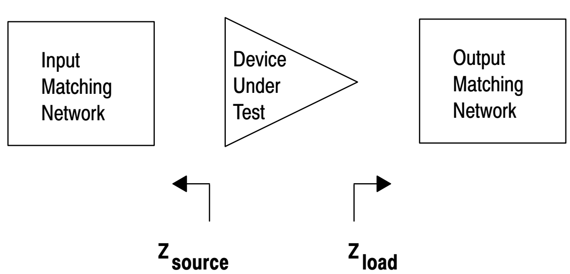
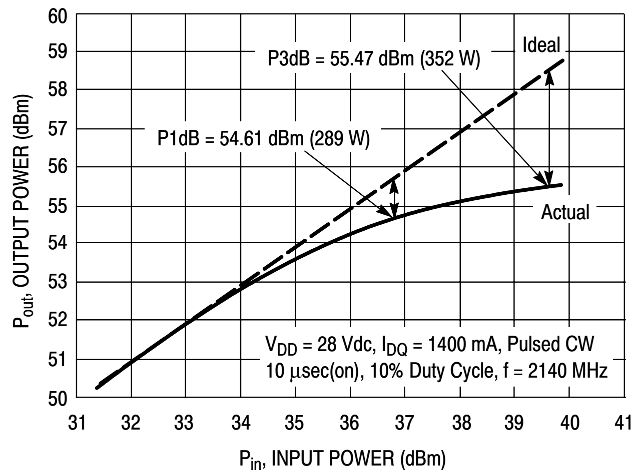


Figure 11. Series Equivalent Source and Load Impedance

ALTERNATIVE PEAK TUNE LOAD PULL CHARACTERISTICS



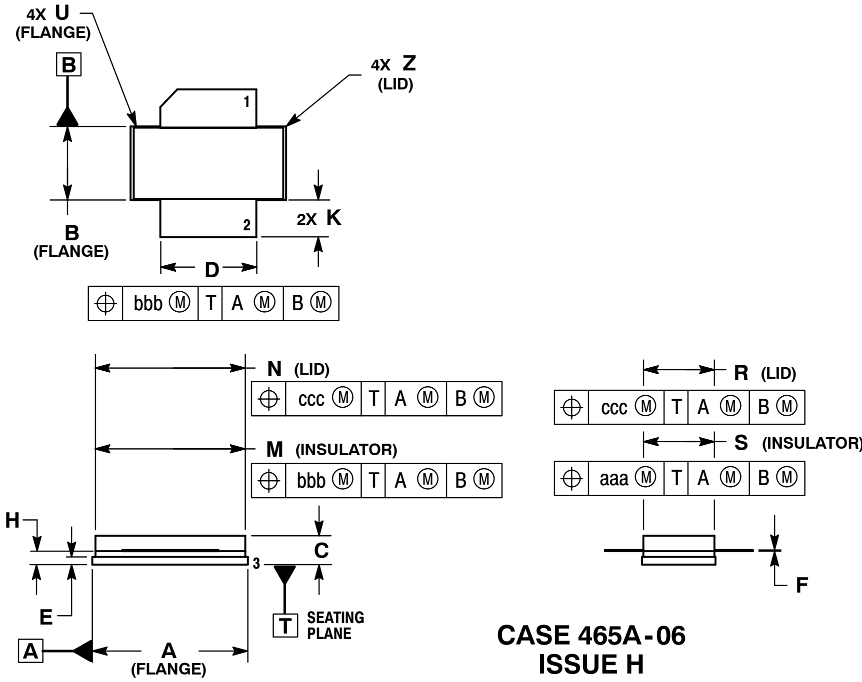
NOTE: Load Pull Test Fixture Tuned for Peak P1dB Output Power @ 28 V

Test Impedances per Compression Level

	Z_{source} Ω	Z_{load} Ω
P1dB	5.21 - j0.31	1.23 - j1.06

Figure 12. Pulsed CW Output Power versus Input Power @ 28 V

PACKAGE DIMENSIONS



CASE 465A-06
ISSUE H
NI-780S
MRF7S21210HSR3

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.805	0.815	20.45	20.70
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.61	20.02
N	0.772	0.788	19.61	20.02
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
U	---	0.040	---	1.02
Z	---	0.030	---	0.76
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
5. SOURCE

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	July 2008	• Initial Release of Data Sheet

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