



# AK8858

## PS/SD Multi Format Video Decoder

### Overview

The AK8858 is a single-chip digital video decoder for composite, s-video, 525i/625i component and 525p/625p component video signals. Its output data is in YCbCr and RGB format. Its pixel clock is generated internally and synchronized with the input signal. Microprocessor access is via I2C interface.

### Features

- Decodes composite and S-Video signals NTSC/ PAL-B, D, G, H, I, N, Nc, M, 60 /SECAM
- Decode 525i / 625i YPbPr component video signals
- Decode 525p / 625p YPbPr component video signals
- 10 input channel
- 10-bit 54MHz ADC 2 channel
- Internally built PLL
- Internal analog bandwidth filter
- Programmable Gain Amp (PGA) (-3.25dB~10dB)
- Adaptive automatic Gain Control (AGC)
- Auto Color Control (Composite and S-Video signals)
- Image adjustment (Contrast, Brightness, Saturation, HUE, Sharpness)
- Automatic input signal detection (NTSC/ PAL/ SECAM detect、 Interlace/ Progressive detect)
- Adaptive 2-D Y/C separation
- Output data format
  - YCbCr 4:2:2 or RGB 8:8:8
- Output interface
  - (YCbCr)
    - Interlace: ITU-R BT.656 (8bit 27MHz) and 16bit 13.5MHz with EAV/ SAV
    - Progressive: 16bit 27MHz and 8bit 54MHz with EAV/ SAV
  - (RGB)
    - Interlace: 8bit:8bit:8bit 13.5MHz with EAV/ SAV
    - Progressive: 8bit:8bit:8bit 27MHz with EAV/ SAV
- \*EAV/ SAV output can be disabled via register
- HD, VD, DVALID and FIELD (VD, DVALID, FIELD can be select up to 2 output via register setting)
- Closed Caption / WSS / CGMS-A signal decoding (output via register).
- Macrovision signal detection (Rovi certification)
- I2C control
- Powerdown function
- Internal VREF
- Core supply voltage: 1.70~2.00V
- I/O power supply: 1.70~3.60V
- Operating temperature: -40°C~105°C
- 80-pin LQFP package (12.0mm x 12.0mm)

(Notice) This device is protected by U.S. patent number 6,600,873 and other intellectual property rights.

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|-----------------|
| <b>Features</b> |
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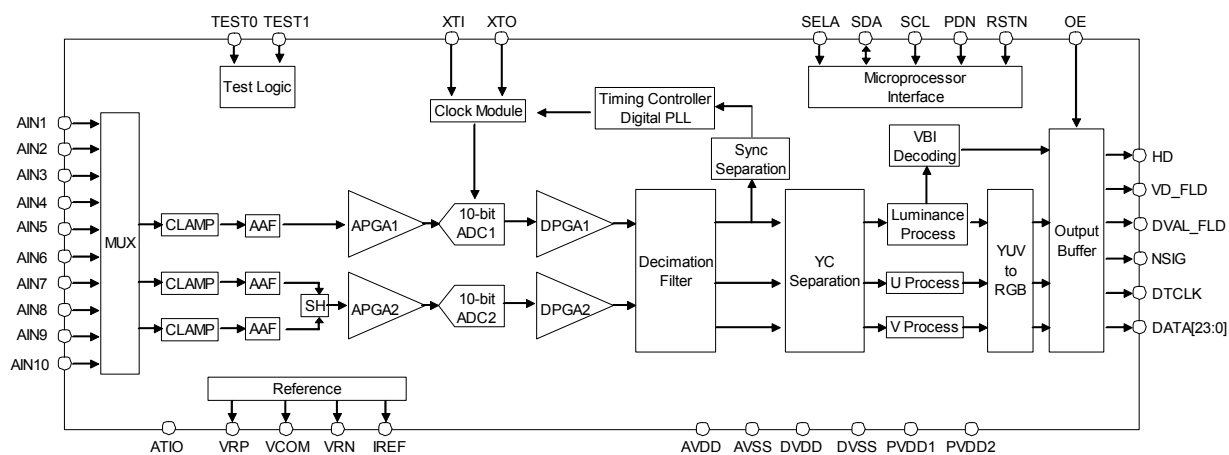
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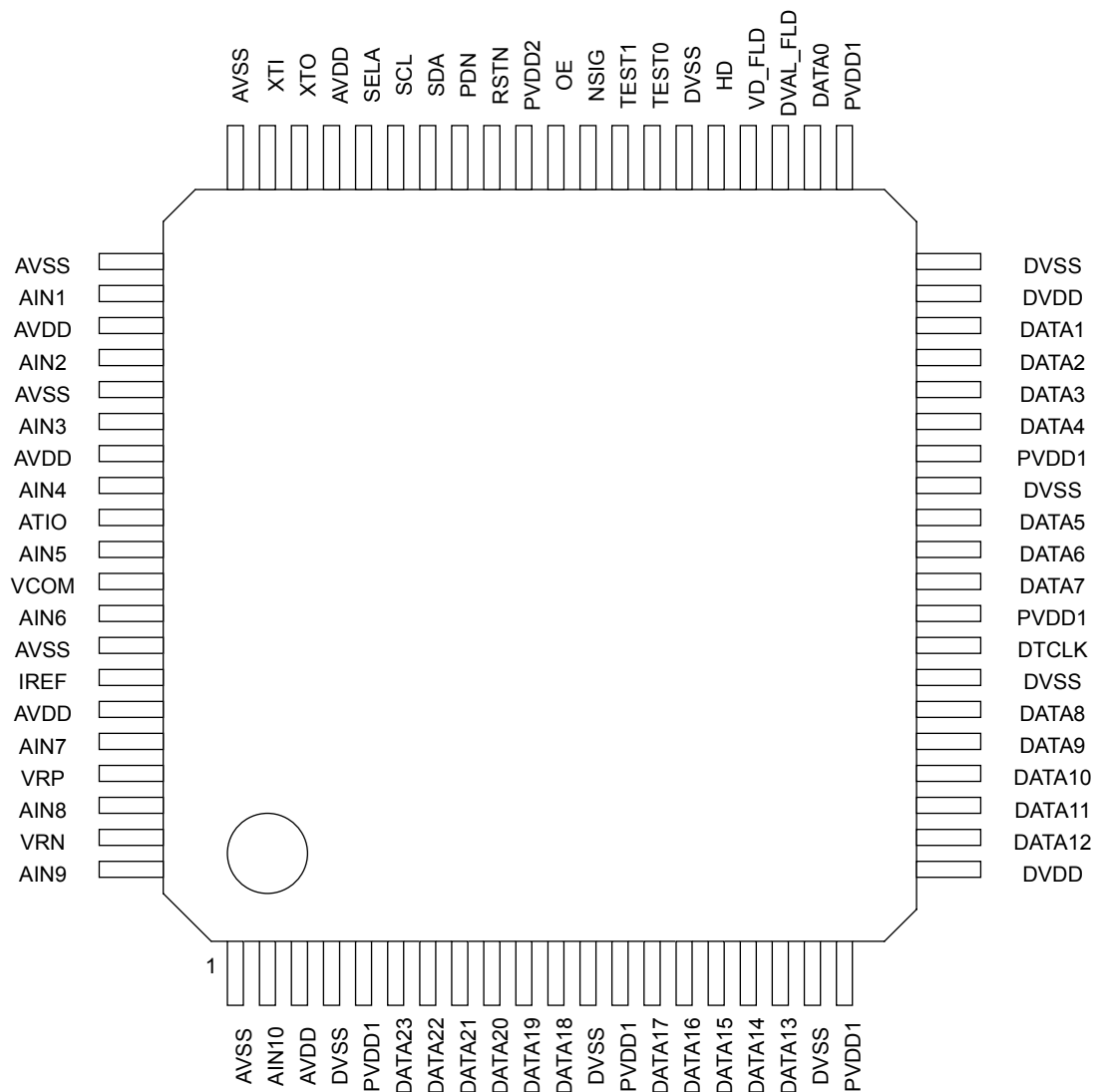
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## [1] Functional block diagram



[2] Pin assignment

80-pin LQFP package (12.0mm x 12.0mm)



**[3] Pin function description****[3.1] Pin function**

| Pin No. | Symbol | P/S | I/O     | Functional Description                                                                                                         |
|---------|--------|-----|---------|--------------------------------------------------------------------------------------------------------------------------------|
| 1       | AVSS   | A   | G       | Analog ground pin.                                                                                                             |
| 2       | AIN10  | A   | I       | Analog video signal input pin. Connect via 0.033μF capacitor and voltage-splitting resistors. If not used, connect to NC.      |
| 3       | AVDD   | A   | P       | Analog power supply pin.                                                                                                       |
| 4       | DVSS   | D   | G       | Digital ground pin.                                                                                                            |
| 5       | PVDD1  | P1  | P       | I/O power supply pin.                                                                                                          |
| 6       | DATA23 | P1  | O (I/O) | DATA output pin. Used as output pin in RGB 8:8:8 output. <sup>(*)</sup><br>If test mode, it is I/O pin.                        |
| 7       | DATA22 | P1  | O (I/O) | DATA output pin. Used as output pin in RGB 8:8:8 output. <sup>(*)</sup><br>If test mode, it is I/O pin.                        |
| 8       | DATA21 | P1  | O (I/O) | DATA output pin. Used as output pin in RGB 8:8:8 output. <sup>(*)</sup><br>If test mode, it is I/O pin.                        |
| 9       | DATA20 | P1  | O (I/O) | DATA output pin. Used as output pin in RGB 8:8:8 output. <sup>(*)</sup><br>If test mode, it is I/O pin.                        |
| 10      | DATA19 | P1  | O (I/O) | DATA output pin. Used as output pin in RGB 8:8:8 output. <sup>(*)</sup><br>If test mode, it is I/O pin.                        |
| 11      | DATA18 | P1  | O (I/O) | DATA output pin. Used as output pin in RGB 8:8:8 output. <sup>(*)</sup><br>If test mode, it is I/O pin.                        |
| 12      | DVSS   | D   | G       | Digital ground pin.                                                                                                            |
| 13      | PVDD1  | P1  | P       | I/O power supply pin.                                                                                                          |
| 14      | DATA17 | P1  | O (I/O) | DATA output pin. Used as output pin in RGB 8:8:8 output. <sup>(*)</sup><br>If test mode, it is I/O pin.                        |
| 15      | DATA16 | P1  | O (I/O) | DATA output pin. Used as output pin in RGB 8:8:8 output. <sup>(*)</sup><br>If test mode, it is I/O pin.                        |
| 16      | DATA15 | P1  | O (I/O) | DATA output pin. Used as output pin in 16-bit output and RGB 8:8:8 output mode. <sup>(*)</sup><br>If test mode, it is I/O pin. |
| 17      | DATA14 | P1  | O (I/O) | DATA output pin. Used as output pin in 16-bit output and RGB 8:8:8 output mode. <sup>(*)</sup><br>If test mode, it is I/O pin. |
| 18      | DATA13 | P1  | O (I/O) | DATA output pin. Used as output pin in 16-bit output and RGB 8:8:8 output mode. <sup>(*)</sup><br>If test mode, it is I/O pin. |
| 19      | DVSS   | D   | G       | Digital ground pin.                                                                                                            |
| 20      | PVDD1  | P1  | P       | I/O power supply pin.                                                                                                          |
| 21      | DVDD   | D   | P       | Digital power supply pin.                                                                                                      |
| 22      | DATA12 | P1  | O (I/O) | DATA output pin. Used as output pin in 16-bit output and RGB 8:8:8 output mode. <sup>(*)</sup><br>If test mode, it is I/O pin. |
| 23      | DATA11 | P1  | O (I/O) | DATA output pin. Used as output pin in 16-bit output and RGB 8:8:8 output mode. <sup>(*)</sup><br>If test mode, it is I/O pin. |
| 24      | DATA10 | P1  | O (I/O) | DATA output pin. Used as output pin in 16-bit output and RGB 8:8:8 output mode. <sup>(*)</sup><br>If test mode, it is I/O pin. |
| 25      | DATA9  | P1  | O       | DATA output pin. Used as output pin in 16-bit output and RGB 8:8:8 output mode. <sup>(*)</sup>                                 |
| 26      | DATA8  | P1  | O       | DATA output pin. Used as output pin in 16-bit output and RGB 8:8:8 output mode. <sup>(*)</sup>                                 |

[Power supply] A: AVDD, D: DVDD, P1: PVDD1, P2: PVDD2

[Input/Output] I: input pin, O: output pin, I/O: input/output pin, P: power supply pin, G: ground connection pin

<sup>(\*)</sup>See {[3.2] Output pin state} for relation of output to OE/PDN and RSTN pin status.



| Pin No. | Symbol   | P/S | I/O     | Functional Description                                                                                                                                             |
|---------|----------|-----|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 27      | DVSS     | D   | G       | Digital ground pin.                                                                                                                                                |
| 28      | DTCLK    | P1  | O       | Data clock output pin. <sup>(*)</sup>                                                                                                                              |
| 29      | PVDD1    | P1  | P       | I/O power supply pin.                                                                                                                                              |
| 30      | DATA7    | P1  | O       | DATA output pin. <sup>(*)</sup>                                                                                                                                    |
| 31      | DATA6    | P1  | O       | DATA output pin. <sup>(*)</sup>                                                                                                                                    |
| 32      | DATA5    | P1  | O       | DATA output pin. <sup>(*)</sup>                                                                                                                                    |
| 33      | DVSS     | D   | G       | Digital ground pin.                                                                                                                                                |
| 34      | PVDD1    | P1  | P       | I/O power supply pin.                                                                                                                                              |
| 35      | DATA4    | P1  | O       | DATA output pin. <sup>(*)</sup>                                                                                                                                    |
| 36      | DATA3    | P1  | O       | DATA output pin. <sup>(*)</sup>                                                                                                                                    |
| 37      | DATA2    | P1  | O       | DATA output pin. <sup>(*)</sup>                                                                                                                                    |
| 38      | DATA1    | P1  | O       | DATA output pin. <sup>(*)</sup>                                                                                                                                    |
| 39      | DVDD     | D   | P       | Digital power supply pin.                                                                                                                                          |
| 40      | DVSS     | D   | G       | Digital ground pin.                                                                                                                                                |
| 41      | PVDD1    | P1  | P       | I/O power supply pin.                                                                                                                                              |
| 42      | DATA0    | P1  | O       | DATA output pin. <sup>(*)</sup>                                                                                                                                    |
| 43      | DVAL_FLD | P1  | O (I/O) | DVALID/ FIELD signal output pin.<br>DVALID signal output / FIELD signal output can be selected by register setting. <sup>(*)</sup><br>If test mode, it is I/O pin. |
| 44      | VD_FLD   | P1  | O (I/O) | VD/ FIELD signal output pin<br>VD signal output / FIELD signal output can be selected by register setting. <sup>(*)</sup><br>If test mode, it is I/O pin.          |
| 45      | HD       | P1  | O (I/O) | HD signal output pin. <sup>(*)</sup><br>If test mode, it is I/O pin.                                                                                               |
| 46      | DVSS     | D   | G       | Digital ground pin.                                                                                                                                                |
| 47      | TEST0    | P2  | I       | Pin for test mode setting. Connect to DVSS.                                                                                                                        |
| 48      | TEST1    | P2  | I       | Pin for test mode setting. Connect to DVSS.                                                                                                                        |
| 49      | NSIG     | P2  | O       | Shows status of synchronization with input signal<br>Low: Signal present (synchronized).<br>High: Signal not present or not synchronized. <sup>(*)</sup>           |
| 50      | OE       | P2  | I       | Output Enable pin.<br>Low: Digital output pin in Hi-z output mode.<br>High: Data output mode.<br>Hi-z input to OE pin is prohibited.                               |
| 51      | PVDD2    | P2  | P       | Microprocessor I/F power supply pin.                                                                                                                               |
| 52      | RSTN     | P2  | I       | Reset signal input pin. Hi-z input is prohibited.<br>Low: Reset.<br>High: Normal operation.                                                                        |
| 53      | PDN      | P2  | I       | Power-down control pin. Hi-z input is prohibited.<br>Low: Power-down.<br>High: Normal operation.                                                                   |
| 54      | SDA      | P2  | I/O     | I2C data pin. Connect to PVDD2 via a pull-up register.<br>Hi-z input possible when PDN=L.                                                                          |
| 55      | SCL      | P2  | I       | I2C clock input pin. Connect to PVDD2 via a pull-up register.<br>Hi-z input possible when PDN=L.                                                                   |
| 56      | SELA     | P2  | I       | I2C bus address selector pin.<br>PVDD2 connection: Slave address [0x8A]<br>DVSS connection: Slave address [0x88]                                                   |
| 57      | AVDD     | A   | P       | Analog power supply pin.                                                                                                                                           |

[Power supply] A: AVDD, D: DVDD, P1: PVDD1, P2: PVDD2

[Input/Output] I: input pin, O: output pin, I/O: input/output pin, P: power supply pin, G: ground connection pin

<sup>(\*)</sup>See {[3.2] Output pin state} for relation of output to OE/PDN and RSTN pin status.

| Pin No. | Symbol | P/S | I/O | Functional Description                                                                                                                                      |
|---------|--------|-----|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 58      | XTO    | A   | O   | Crystal connection pin. Use 24.576 MHz crystal.<br>When PDN=L, output level is AVSS.<br>If crystal is not used, connect to NC or AVSS.                      |
| 59      | XTI    | A   | I   | Crystal connection pin. Use 24.576 MHz crystal resonator.<br>For input from 24.576 MHz crystal oscillator, use this pin.                                    |
| 60      | AVSS   | A   | G   | Analog ground pin.                                                                                                                                          |
| 61      | AVSS   | A   | G   | Analog ground pin.                                                                                                                                          |
| 62      | AIN1   | A   | I   | Analog video signal input pin. Connect via 0.033μF capacitor and voltage-splitting resistors. If not used, connect to NC.                                   |
| 63      | AVDD   | A   | P   | Analog power supply pin.                                                                                                                                    |
| 64      | AIN2   | A   | I   | Analog video signal input pin. Connect via 0.033μF capacitor and voltage-splitting resistors. If not used, connect to NC.                                   |
| 65      | AVSS   | A   | G   | Analog ground pin.                                                                                                                                          |
| 66      | AIN3   | A   | I   | Analog video signal input pin. Connect via 0.033μF capacitor and voltage-splitting resistors. If not used, connect to NC.                                   |
| 67      | AVDD   | A   | P   | Analog power supply pin.                                                                                                                                    |
| 68      | AIN4   | A   | I   | Analog video signal input pin. Connect via 0.033μF capacitor and voltage-splitting resistors. If not used, connect to NC.                                   |
| 69      | ATIO   | A   | I/O | Analog test pin. For normal operation, connect to AVSS.                                                                                                     |
| 70      | AIN5   | A   | I   | Analog video signal input pin. Connect via 0.033μF capacitor and voltage-splitting resistors. If not used, connect to NC.                                   |
| 71      | VCOM   | A   | O   | Common internal voltage for AD converter.<br>Connect to AVSS via 0.1μF ceramic capacitor (±10%).                                                            |
| 72      | AIN6   | A   | I   | Analog video signal input pin. Connect via 0.033μF capacitor and voltage-splitting resistors. If not used, connect to NC.                                   |
| 73      | AVSS   | A   | G   | Analog ground pin.                                                                                                                                          |
| 74      | IREF   | A   | O   | Analog circuit reference current setting pin.<br>Connect to AVSS via 6.8KΩ (±1% accuracy) resistor.                                                         |
| 75      | AVDD   | A   | P   | Analog power supply pin.                                                                                                                                    |
| 76      | AIN7   | A   | I   | Analog video signal input pin. Connect via 0.033μF capacitor and voltage-splitting resistors. If not used, connect to NC.                                   |
| 77      | VRP    | A   | O   | Internal reference positive voltage pin for AD converter.<br>Connect to AVSS via 0.1μF ceramic capacitor (±10%).                                            |
| 78      | AIN8   | A   | I   | Analog video signal input pin. Connect via 0.033μF capacitor and voltage-splitting resistors. If not used, connect to NC.                                   |
| 79      | VRN    | A   | O   | Internal reference negative voltage pin for AD converter.<br>Connect to AVSS via 0.1μF ceramic capacitor (±10%).                                            |
| 80      | AIN9   | A   | I   | Analog video signal input pin.<br>Connect via 0.033 μF capacitor and voltage-splitting resistors as shown in page 107.<br>If it is not used, connect to NC. |

[Power supply] A: AVDD, D: DVDD, P1: PVDD1, P2: PVDD2

[Input/Output] I: input pin, O: output pin, I/O: input/output pin, P: power supply pin, G: ground connection pin

(\*) See {[3.2] Output pin state} for relation of output to OE/PDN and RSTN pin status.

**[3.2] Output pin state**

Relation of output to OE/PDN and RSTN pin status.

| OE | PDN | RSTN | DATA[23:0], DTCLK, HD, VD_FLD, DVAL_FLD | NSIG     |
|----|-----|------|-----------------------------------------|----------|
| L  | x   |      | Hi-Z output                             | L output |
| H  | L   | x    | L output                                | L output |
| H  | H   | L    | L output                                | L output |
| H  | H   | H    | DOUT                                    | DOUT     |

(x: Don't care, DOUT: Data output)

State of DATA pin except for RGB 8:8:8 format output

| YCbCr8bit output |            |           | YCbCr16bit output |            |           |
|------------------|------------|-----------|-------------------|------------|-----------|
| DATA[23:16]      | DATA[15:8] | DATA[7:0] | DATA[23:16]       | DATA[15:8] | DATA[7:0] |
| Low output       | Low output | DOUT      | Low output        | DOUT       | DOUT      |

(DOUT: Data output)

In the absence of AIN signal input, output will be black data (Y=0x10, Cb/Cr=0x80).

(Blueback output can be obtained by register setting).

\*(Sub Address: 0x0D [3:2])

**[4] Electrical specifications****[4.1] Absolute maximum ratings**

| Parameter                             | Min  | Max                        | Unit | Notes                            |
|---------------------------------------|------|----------------------------|------|----------------------------------|
| Supply voltage                        |      |                            |      |                                  |
| DVDD, AVDD                            | -0.3 | 2.2                        | V    |                                  |
| PVDD1, PVDD2                          | -0.3 | 4.2                        | V    |                                  |
| Analog input pin voltage A (VinA)     | -0.3 | AVDD + 0.3 ( $\leq 2.2$ )  | V    | ( <sup>(*)1</sup> )              |
| Digital input pin voltage P1 (VioP1)  | -0.3 | PVDD1 + 0.3 ( $\leq 4.2$ ) | V    | ( <sup>(*)2</sup> )              |
| Digital output pin voltage P2 (VioP2) | -0.3 | PVDD2 + 0.3 ( $\leq 4.2$ ) | V    |                                  |
| Input pin current (IIn)               | -10  | 10                         | mA   | Power supply pin is not included |
| Storage temperature                   | -40  | 150                        | °C   |                                  |

(<sup>(\*)1</sup>) DTCLK, DATA [23:0], HD, VD\_FLD, DVAL\_FLD

(<sup>(\*)2</sup>) OE, SELA, PDN, RSTN, SDA, SCL, NSIG, TEST0, TEST1

The above supply voltages are referenced to ground pins (DVSS=AVSS) at 0V (Reference Voltage).

All power supply grounds (AVSS, DVSS) should be at the same electric potential.

If digital output pins are connected to data bus, the data bus operating voltage should be in the same range as shown above from the digital output pin.

The setting other than above may cause the eternal destruction to the device.

Normal operational is not guaranteed for the above setting.

**[4.2] Recommended operating conditions**

| Parameter                              | Min  | Typ  | Max  | Unit | Condition         |
|----------------------------------------|------|------|------|------|-------------------|
| Analog supply voltage (AVDD)           | 1.70 | 1.80 | 2.00 | V    | AVDD = DVDD       |
| Digital supply voltage (DVDD)          |      |      |      |      |                   |
| MPU I/F supply voltage (PVDD1)         | 1.70 | 1.80 | 3.60 | V    | PVDD1 $\geq$ DVDD |
| Data output i/F supply voltage (PVDD2) |      |      |      |      | PVDD2 $\geq$ DVDD |
| Operating temperature (Ta)             | -40  |      | 85   | °C   |                   |

The above supply voltages are referenced to ground pins (DVSS=AVSS) at 0V (Reference Voltage).

All power supply grounds (AVSS, DVSS) should be at the same electric potential.

**[4.3] DC characteristics**

(Ta: -40°C~85°C / DVDD=AVDD=1.7V~2.0V / PVDD1=DVDD~3.6V / PVDD2=DVDD~3.6V)

| Parameter                                          | Symbol | Min      | Typ | Max              | Units | Condition                              |
|----------------------------------------------------|--------|----------|-----|------------------|-------|----------------------------------------|
| Digital P2 input high voltage <sup>(*)</sup>       | VPIH   | 0.8PVDD2 |     |                  | V     | PVDD2<2.7V                             |
|                                                    |        | 0.7PVDD2 |     |                  | V     | PVDD2≥2.7V                             |
| Digital P2 input low voltage <sup>(*)</sup>        | VPIL   |          |     | 0.2PVDD2         | V     | PVDD2<2.7V                             |
|                                                    |        |          |     | 0.3PVDD2         | V     | PVDD2≥2.7V                             |
| XTI input high voltage                             | VXIH   | 0.8AVDD  |     |                  |       |                                        |
| XTI input low voltage                              | VXIL   |          |     | 0.2AVDD          |       |                                        |
| Digital input leak current <sup>(*)</sup>          | IL     |          |     | ±10              | uA    |                                        |
| Digital P1 output high voltage <sup>(*)</sup>      | VOH1   | 0.7PVDD1 |     |                  | V     | IOH1 = -600uA                          |
| Digital P1 output low voltage <sup>(*)</sup>       | VOL1   |          |     | 0.3PVDD1         | V     | IOL1 = 1mA                             |
| Digital P1 output Hi-z leak current <sup>(*)</sup> | HIL    |          |     | ±10              | uA    |                                        |
| NSIG output high voltage                           | VOH2   | 0.7PVDD2 |     |                  | V     | IOH2 = -600uA                          |
| NSIG output low voltage                            | VOL2   |          |     | 0.3PVDD2         | V     | IOL2 = 1mA                             |
| I2C(SDA)L output                                   | VOLC   |          |     | 0.4<br>0.2 PVDD2 | V     | IOLC = 3mA<br>PVDD2≥2.0V<br>PVDD2<2.0V |

(\*) Collective term for SDA, SCL, SELA, OE, PDN, RSTN, TEST0 and TEST1 pins.

(\*) Collective term for DTCLK, DATA [23:0], HD, VD\_FLD and DVAL\_FLD pins.

**[4.4] Analog characteristics**

(AVDD=1.8V, Ta=25°C)

**[4.4.1] Input Range**

| Parameter   | Symbol | Min | Typ | Max  | Units | Condition |
|-------------|--------|-----|-----|------|-------|-----------|
| Input range | VIMX   | 0   |     | 0.60 | Vpp   |           |

**[4.4.2] AAF (Anti-Aliasing Filter)**

| Parameter          | Symbol | Min | Typ | Max | Units | Condition                                             |
|--------------------|--------|-----|-----|-----|-------|-------------------------------------------------------|
| Pass band ripple   | Gp     | -1  |     | +1  | dB    | Progressive signal: ~12MHz<br>Interlace signal: ~6MHz |
| Stop band blocking | Gs     | 20  | 30  |     | dB    | Progressive signal: 54MHz<br>Interlace signal: 27MHz  |

**[4.4.3] Analog PGA**

| Parameter    | Symbol | Min  | Typ | Max  | Units |
|--------------|--------|------|-----|------|-------|
| Resolution   | RES    |      | 2   |      | bit   |
| Minimum gain | GMN    |      | -3  |      | dB    |
| Maximum gain | GMX    |      | 6   |      | dB    |
| Gain step    | GST    | 2.75 | 3   | 3.25 | dB    |

**[4.4.4] ADC**

| Parameter                   | Symbol | Min | Typ  | Max  | Units | Condition                                                       |
|-----------------------------|--------|-----|------|------|-------|-----------------------------------------------------------------|
| Resolution                  | RES    |     | 10   |      | bit   |                                                                 |
| Operating clock frequency   | FS     |     | 54   |      | MHz   | Progressive decode : Y signal                                   |
|                             |        |     | 27   |      |       | Interlace decode : Y signal<br>Progressive decode : PbPr signal |
| Integral nonlinearity       | INL    |     | ±1.0 | ±2.0 | LSB   |                                                                 |
| Differential nonlinearity   | DNL    |     | ±0.5 | ±1.0 | LSB   |                                                                 |
| S/N                         | SN     |     | 53   |      | dB    | Fin=1MHz*, FS=54MHz,<br>PGA GAIN default setting                |
| S/(N+D)                     | SND    |     | 52   |      | dB    | Fin=1MHz*, FS=54MHz<br>PGA GAIN default setting                 |
| Full scale Gain matching    | IFGM   |     |      | 5    | %     |                                                                 |
| ADC internal common voltage | VCOM   |     | 0.96 |      | V     |                                                                 |
| ADC internal positive VREF  | VRP    |     | 1.26 |      | V     |                                                                 |
| ADC internal negative VREF  | VRN    |     | 0.66 |      | V     |                                                                 |

\*Fin = AIN input signal frequency

**[4.4.5] Current consumption**

(AVDD = DVDD = PVDD1 = PVDD2 = 1.8V, Ta = -40~85°C)

| Parameter         | Symbol | Min | Typ | Max | Units | Condition                                         |
|-------------------|--------|-----|-----|-----|-------|---------------------------------------------------|
| (Active mode)     |        |     |     |     |       |                                                   |
| Total             | IDD    |     | 110 | 151 | mA    | ADC 3ch operational <sup>(*)1</sup>               |
| Analog block      | AIDD   |     | 68  |     | mA    | ADC 3ch operational <sup>(*)1</sup>               |
|                   |        |     | 60  |     | mA    | YC: ADC 2ch operational <sup>(*)2</sup>           |
|                   |        |     | 35  |     | mA    | CVBS: ADC 1ch operational <sup>(*)2</sup>         |
| Digital block     | DIDD   |     | 28  |     | mA    | With crystal connected<br>Load condition: CL=15pF |
| I/O block         | PIDD   |     | 14  |     | mA    |                                                   |
| (Power down mode) |        |     |     |     |       |                                                   |
| Total             | SIDD   |     | ≤1  | 100 | uA    | PDN=L(DVSS) <sup>(*)3</sup>                       |
| Analog block      | ASIDD  |     | ≤1  |     | uA    |                                                   |
| Digital block     | DSIDD  |     | ≤1  |     | uA    |                                                   |
| I/O block         | PSIDD  |     | ≤1  |     | uA    |                                                   |

(\*)1 Progressive YPbPr signal decode

(\*)2 Reference value

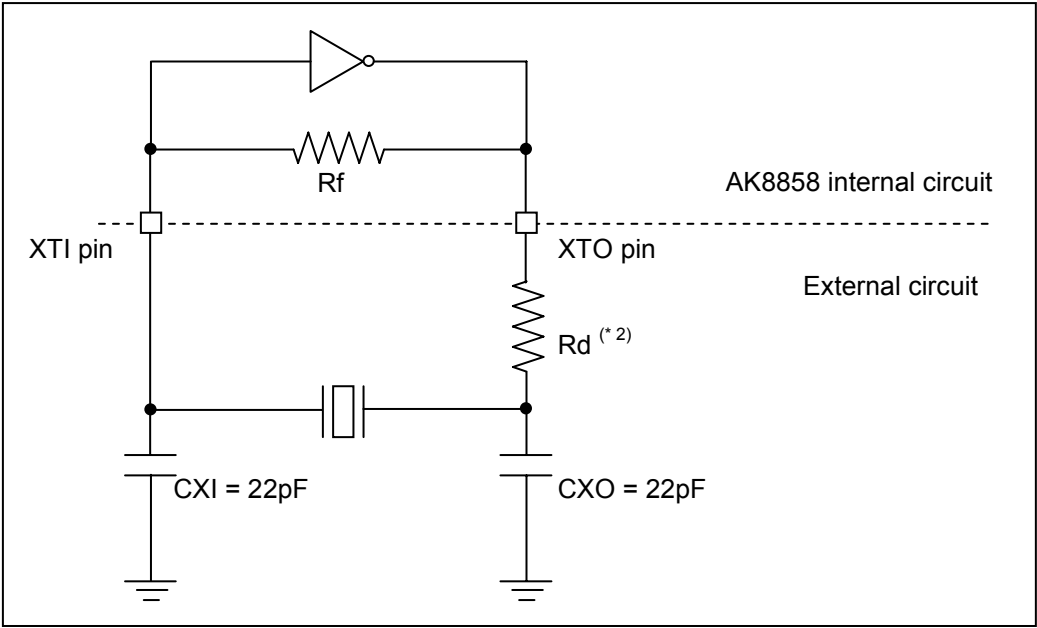
(\*)3 OE pin and RSTN pin must always be brought to the voltage polarity to be used or to ground level

**[4.4.6] Crystal circuit block**

| Parameter                                         | Symbol         | Min | Typ    | Max  | Units | Notes   |
|---------------------------------------------------|----------------|-----|--------|------|-------|---------|
| Frequency                                         | f0             |     | 24.576 |      | MHz   |         |
| Frequency tolerance                               | $\Delta f / f$ |     |        | ±100 | ppm   |         |
| Load capacitance                                  | CL             |     | 15     |      | pF    |         |
| Effective equivalent resistance                   | Re             |     |        | 100  | Ω     | (*)     |
| Crystal parallel capacitance                      | CO             |     | 0.9    |      | pF    |         |
| XTI terminal external connection load capacitance | CXI            |     | 22     |      | pF    | CL=15pF |
| XTO terminal external connection load capacitance | CXO            |     | 22     |      | pF    | CL=15pF |

(\*) Effective equivalent resistance generally may be taken as  $Re = \{R1 \times (1+CO/CL)^2\}$ . (R1 is the crystal series equivalent resistance)

**Example connection**

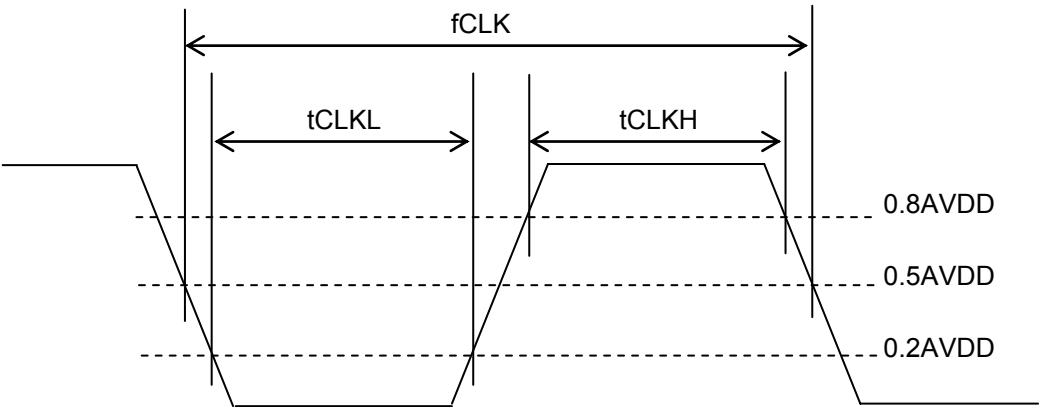


(\*) Determine need for and appropriate value of limiting resistance ( $R_d$ ) in accordance with the crystal specifications.

[5] AC Timing

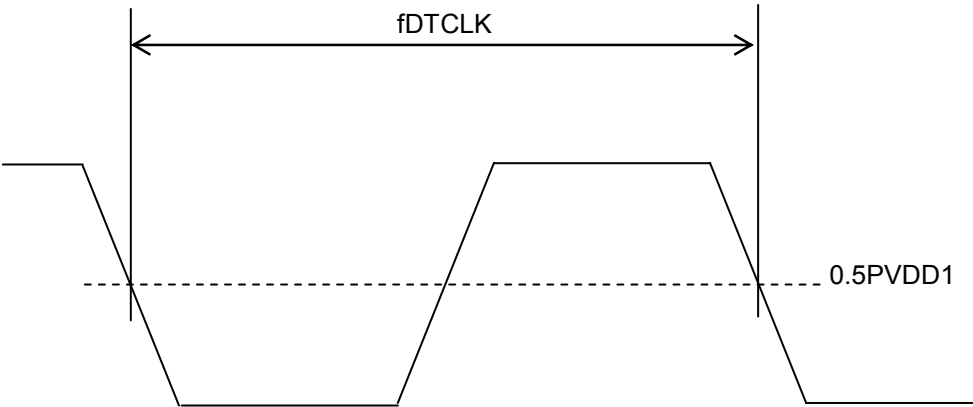
( $1.70 \leq DVDD \leq 2.00$ ,  $DVDD \leq PVDD1 \leq 3.60$ ,  $DVDD \leq PVDD2 \leq 3.60$ )  
( $T_a = -40 \sim 85^\circ\text{C}$ , Load condition:  $CL=15\text{pF}$ )

[5.1] Clock input



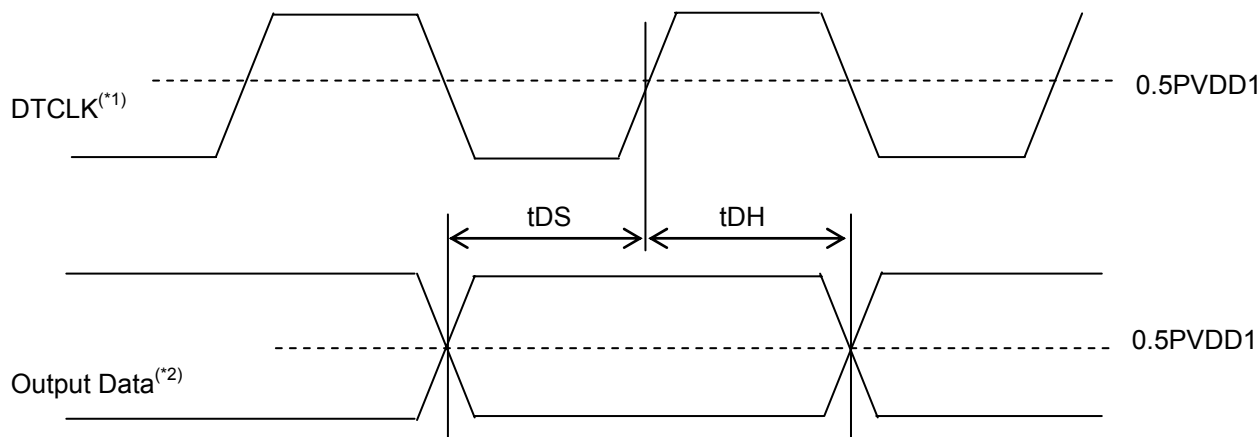
| Parameter           | Symbol | Min | Typ    | Max  | Units |
|---------------------|--------|-----|--------|------|-------|
| Input CLK           | fCLK   |     | 24.576 |      | MHz   |
| CLK pulse width H   | tCLKH  | 16  |        |      | nsec  |
| CLK pulse widthL    | tCLKL  | 16  |        |      |       |
| Frequency tolerance |        |     |        | ±100 | ppm   |

[5.2] Clock output (DTCLK output)



| Parameter | Symbol | Min | Typ  | Max | Units | Condition                                                                                     |
|-----------|--------|-----|------|-----|-------|-----------------------------------------------------------------------------------------------|
| DTCLK     | fDTCLK |     | 13.5 |     | MHz   | (Interlace) 16bit YCbCr output<br>(Interlace) RGB output                                      |
|           |        |     | 27   |     |       | (Interlace) 8bit YCbCr output<br>(Progressive) 16bit YCbCr output<br>(Progressive) RGB output |
|           |        |     | 54   |     |       | (Progressive) 8bit YCbCr output                                                               |

### [5.3] Output data timing

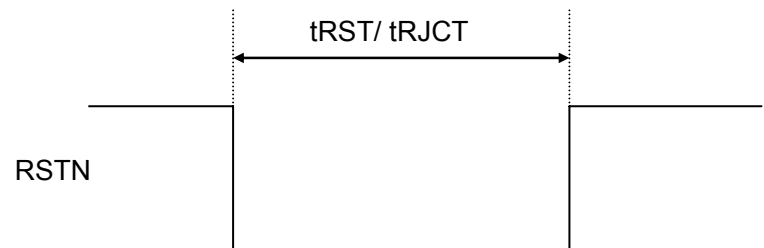


| Parameter              | Symbol | Min | Typ | Max | Units | Condition                                                                                     |
|------------------------|--------|-----|-----|-----|-------|-----------------------------------------------------------------------------------------------|
| Output Data Setup Time | tDS    | 20  |     |     | nsec  | (Interlace) 16bit YCbCr output<br>(Interlace) RGB output                                      |
|                        |        | 10  |     |     |       | (Interlace) 8bit YCbCr output<br>(Progressive) 16bit YCbCr output<br>(Progressive) RGB output |
|                        |        | 5   |     |     |       | (Progressive) 8bit YCbCr output                                                               |
| Output Data Hold Time  | tDH    | 20  |     |     | nsec  | (Interlace) 16bit YCbCr output<br>(Interlace) RGB output                                      |
|                        |        | 10  |     |     |       | (Interlace) 8bit YCbCr output<br>(Progressive) 16bit YCbCr output<br>(Progressive) RGB output |
|                        |        | 5   |     |     |       | (Progressive) 8bit YCbCr output                                                               |

(\*1) It is possible to invert the polarity of DTCLK by setting register. (Sub Address: 0x07[7]).

(\*2) Output Data is general term of DATA [23:0], HD, VD\_FLD and DVAL\_FLD.

### [5.4] Reset pulse

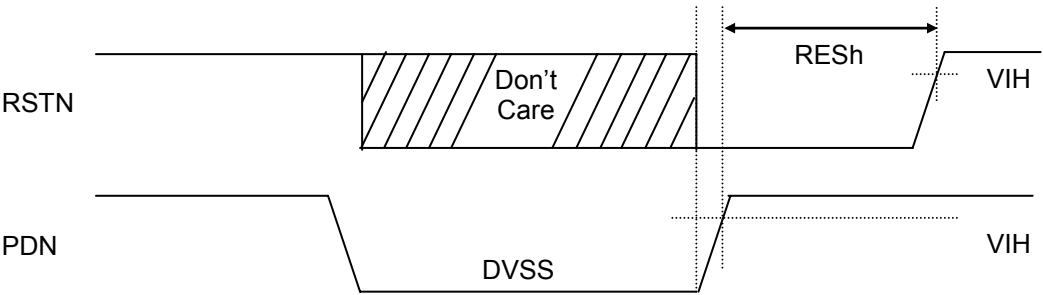


| Parameter        | Symbol | Min | Typ | Max | Units |
|------------------|--------|-----|-----|-----|-------|
| RSTN pulse width | tRST   | 500 |     |     | nsec  |
| RSTN pulse eject | tRJCT  |     |     | 50  |       |



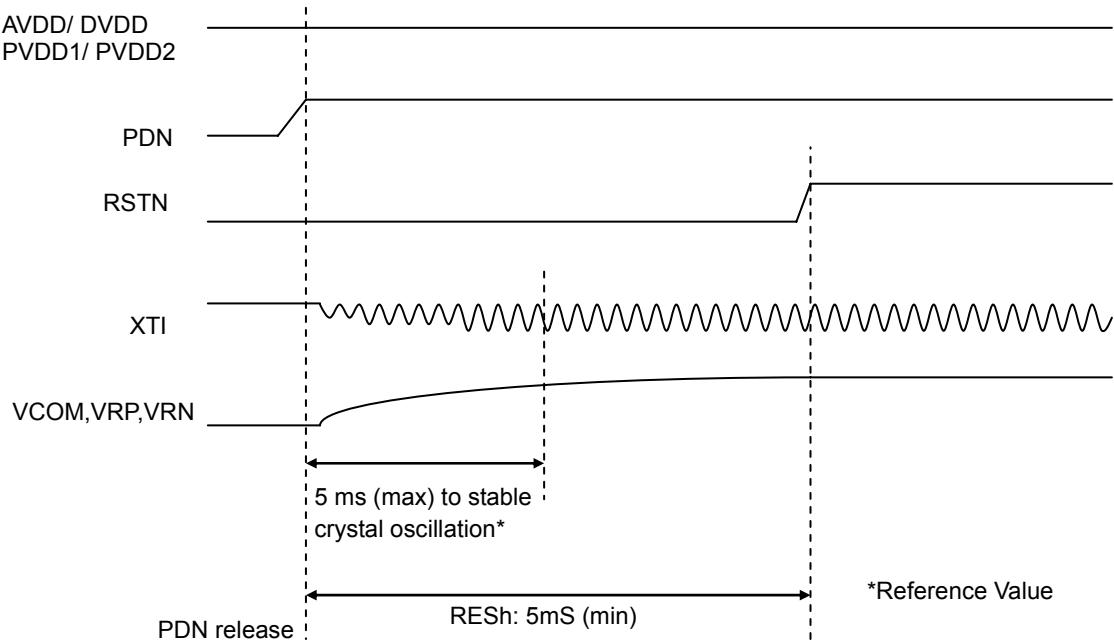
**[5.5] Power-down release sequence**

Reset must be applied after PDN release (PDN=Hi).

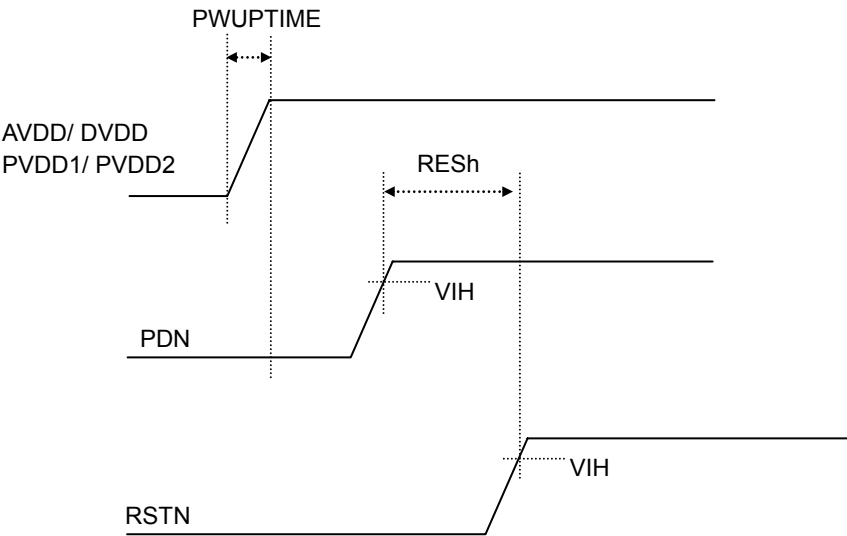


| Parameter                     | Symbol | Min | Typ | Max | Units |
|-------------------------------|--------|-----|-----|-----|-------|
| Reset width after PDN release | RESH   | 5   |     |     | ms    |

To perform power-down, all control signals must always be brought to the voltage polarity to be used or to ground level.



[5.6] Power-on sequence

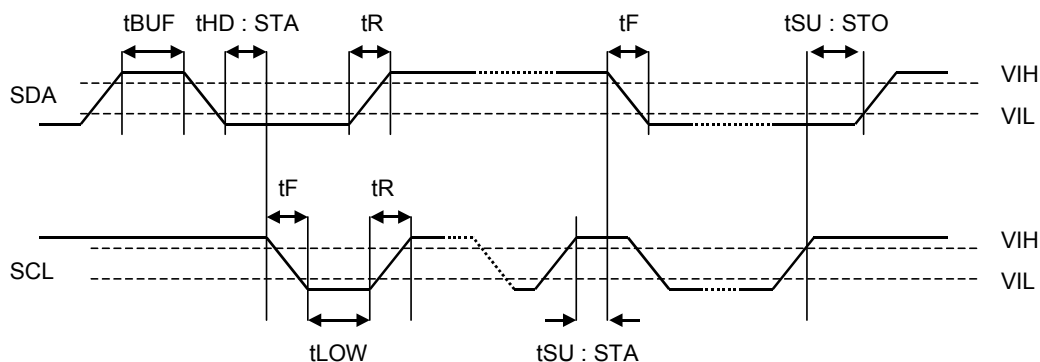


| Parameter                     | Symbol   | Min | Typ | Max | Units |
|-------------------------------|----------|-----|-----|-----|-------|
| POWERUP TIME                  | PWUPTIME |     |     | 100 | msec  |
| Reset width after PDN release | RESh     | 5   |     |     |       |

At power-on, PDN must be set to ground level (PDN=Low).  
AVDD/DVDD/PVDD1/PVDD2 should be raised at power-on less than 100msec.  
After PDN release, RSTN must stay on Low level more than 5msec.

## [5.7] I2C bus input timing

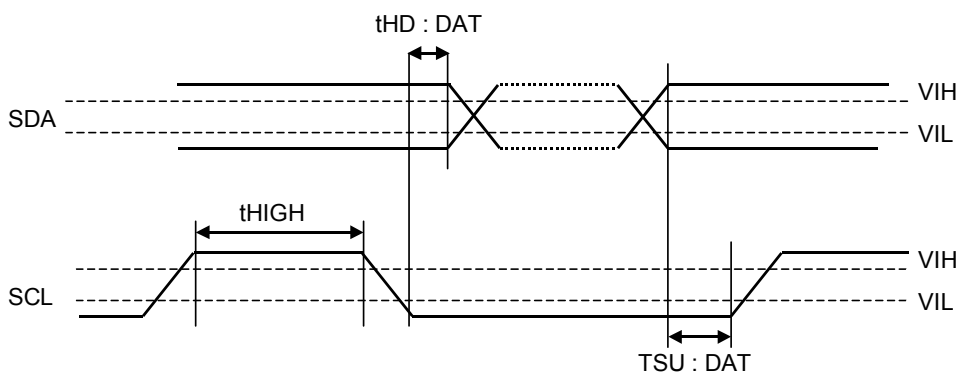
## [5.7.1] Timing 1



| Parameter                   | Symbol       | Min | Max | Units           |
|-----------------------------|--------------|-----|-----|-----------------|
| Bus Free Time               | $t_{BUF}$    | 1.3 |     | $\mu\text{sec}$ |
| Hold Time (Start Condition) | $t_{HD:STA}$ | 0.6 |     | $\mu\text{sec}$ |
| Clock Pulse Low Time        | $t_{LOW}$    | 1.3 |     | $\mu\text{sec}$ |
| Input Signal Rise Time      | $t_R$        |     | 300 | nsec            |
| Input Signal Fall Time      | $t_F$        |     | 300 | nsec            |
| Setup Time(Start Condition) | $t_{SU:STA}$ | 0.6 |     | $\mu\text{sec}$ |
| Setup Time(Stop Condition)  | $t_{SU:STO}$ | 0.6 |     | $\mu\text{sec}$ |

\*The timing relating to the I2C bus is as stipulated by the I2C bus specification, and not determined by the device itself. For details, see I2C bus specification.

## [5.7.2] Timing 2



| Parameter             | Symbol       | Min                 | Max                 | Units           |
|-----------------------|--------------|---------------------|---------------------|-----------------|
| Data Setup Time       | $t_{SU:DAT}$ | 100 <sup>(*)1</sup> |                     | nsec            |
| Data Hold Time        | $t_{HD:DAT}$ | 0.0                 | 0.9 <sup>(*)2</sup> | $\mu\text{sec}$ |
| Clock Pulse High Time | $t_{HIGH}$   | 0.6                 |                     | $\mu\text{sec}$ |

<sup>(\*)1</sup> If I2C is used in standard mode,  $t_{SU:DAT} \geq 250\text{ns}$  is required.

<sup>(\*)2</sup> This condition must be met if the AK8858 is used with a bus that does not extend  $t_{LOW}$  (to use  $t_{LOW}$  at minimum specification).

**[6] Functional overview**

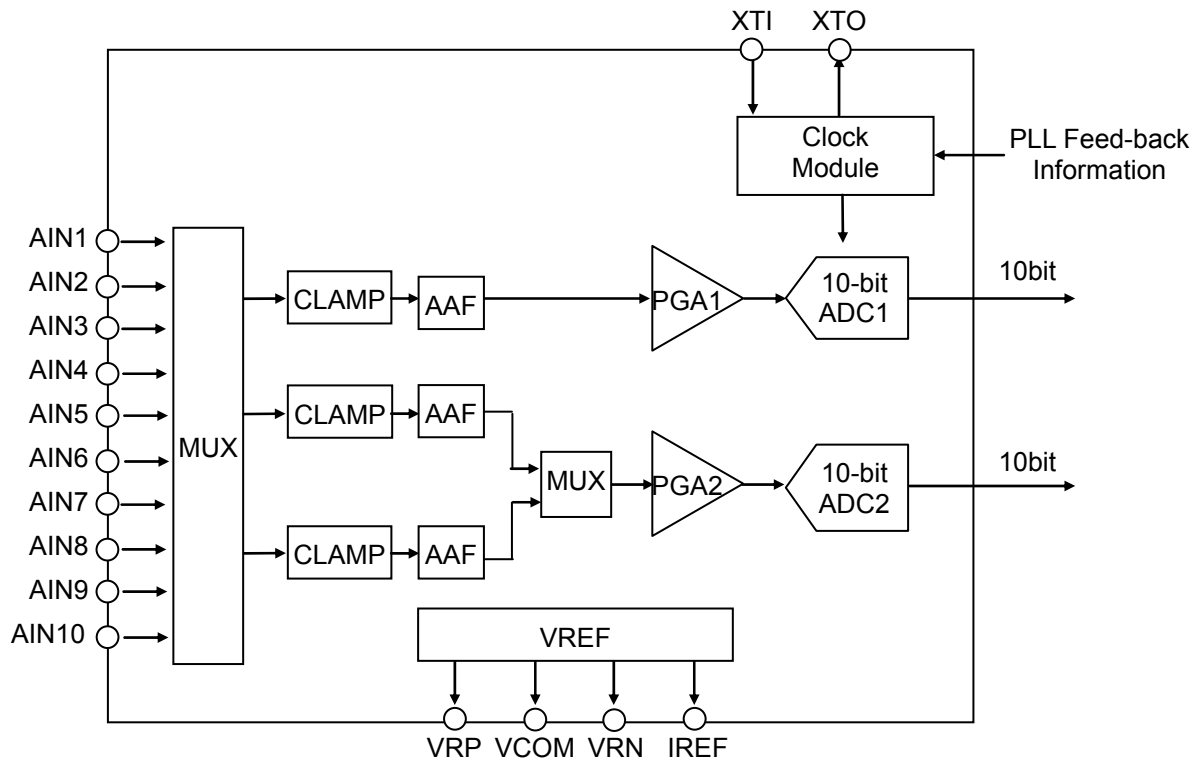
The following key functions are characteristic of the AK8858 and its operational performance.

- (1) It accepts composite video signal (CVBS), S-video and component YPbPr input with 10 input pins available for this purpose. The decode signal is selected via register setting.
- (2) It contains an internal analog band limiting filter (anti-aliasing) in front of the AD converter input.
- (3) Its analog circuit clamps the input signal to the sync tip (analog sync tip clamp). Its digital circuit clamps the digitized input data to the pedestal level (digital pedestal clamp).
- (4) It has auto detection mode via register setting which automatically recognizes the input signal category.
- (5) Its adaptive AGC function enables measurement of the input signal size and determination of the input signal level.
- (6) Its ACC function enables measurement of the input signal color burst size and determination of the appropriate color burst level.
- (7) It performs adaptive two-dimensional Y/C separation, in which its phase detector selects the best correlation from among vertical, horizontal, and diagonal samples and optimum Y/C separation mode.
- (8) Its digital pixel spacing adjuster can align vertical positions by vertical pixel positioning.
- (9) Its operated in line-locked, frame-locked, or fixed clock mode with automatic transition and optimum mode selection by automatic scanning.
- (10) In PAL-B, D, G, H, I and N decoding, it can perform phase-difference correction for each line.
- (11) Its output interface is ITU-R BT.656 (EAV/SAV) compliant. For connection of devices having no ITU-R BT.656 interface, it shows the active video region by HD/ VD/ DVALID/ FIELD signal output.
- (12) Its output data format is in YCbCr format and RGB (8:8:8) format.
- (13) It judges the chroma signal quality from the color burst of the input signal, and can apply color kill if the signal quality is judged insufficient. It can also apply color kill if the color decode PLL clock control.
- (14) Its image quality adjustment function includes contrast, brightness, hue, color saturation, and sharpness adjustment.
- (15) Its luminance and color signal band limiting filter are adjustable via register setting.
- (16) It can decode conflated closed caption data, WSS signals, VBI(CGMS-A) and write them separately to the storage register.
- (17) Its enables Macrovision signal type notification, in cases where the Macrovision signal is included in the decoded data.

## [7] Functional description

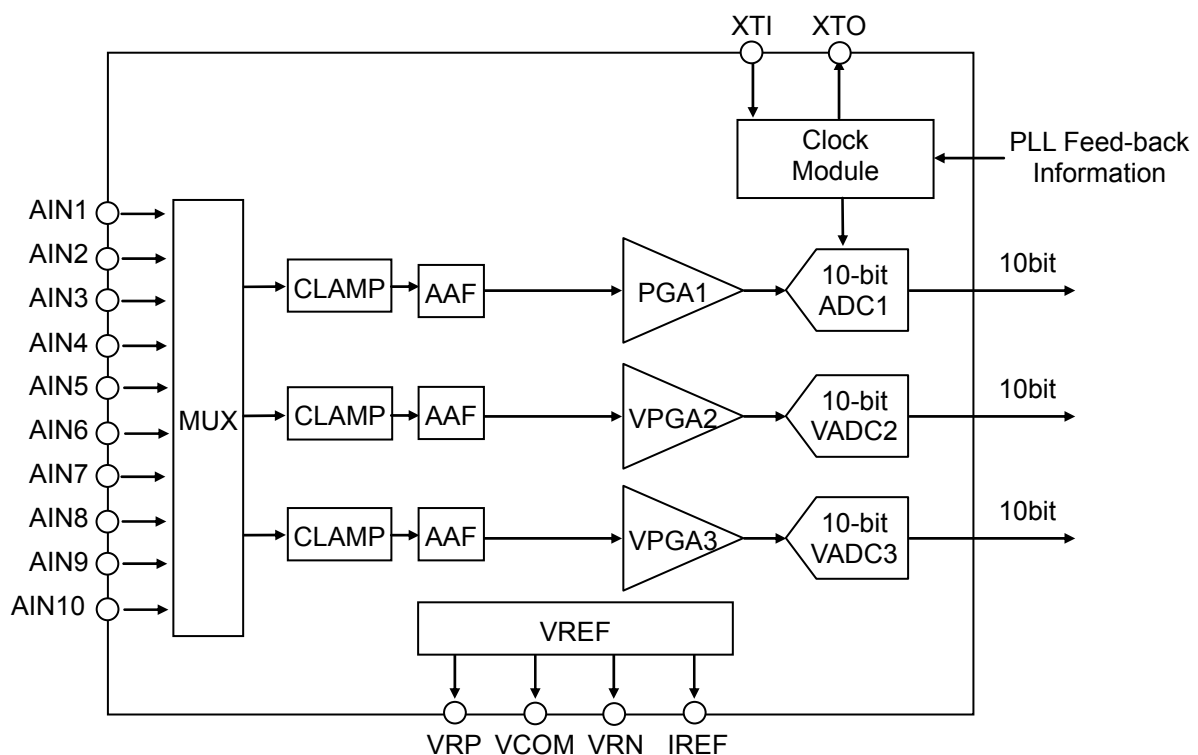
### [7.1] Analog circuit description

Analog circuit block is shown below.



When decode YPbPr component video signal, Pb/Pr signal is converted to digital data by PGA2 and ADC2 after the data was sampled at sample hold circuit.

Time sharing operational status of ADC and PGA is shown below (PGA2 and ADC2 is shown as VPGA2, VADC2, VPGA3 and VADC3).



**[7.1.1] CVBS signal decoding**

The data is converted to digital at PGA1 and ADC1. Sampling clock is 27MHz.

The characteristics of internal analog limiting filter (anti-aliasing), which is in front of the AD converter input, are as follows:  $\pm 1\text{dB}$  ( $\sim 6\text{MHz}$ ),  $-30\text{dB}$  ( $27\text{MHz}$ )

**[7.1.2] S(Y/C) video signal decoding**

Y signal data is converted to digital at PGA1 and ADC1. Sampling clock is 27MHz.

C signal data is converted to digital at PGA2 and ADC2. Sampling clock is 27MHz.

The characteristics of internal analog limiting filter (anti-aliasing), which is in front of the AD converter input, are as follows:  $\pm 1\text{dB}$  ( $\sim 6\text{MHz}$ ),  $-30\text{dB}$  ( $27\text{MHz}$ )

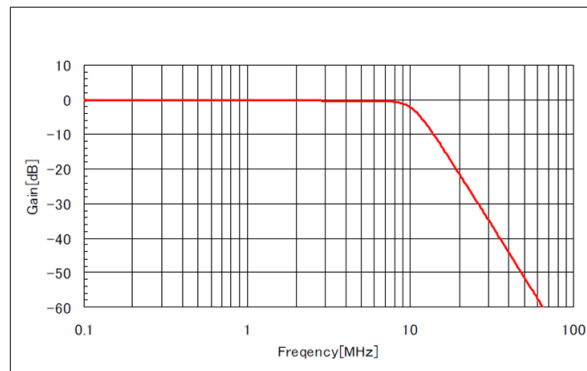
**[7.1.3] 525i/625i YPbPr component video signal decoding**

Y signal data is converted to digital at PGA1 and ADC1. Sampling clock is 27MHz.

Pb signal data is converted to digital at VPGA2 and VADC2. Sampling clock is 27MHz.

Pr signal data is converted to digital at VPGA3 and VADC3. Sampling clock is 27MHz.

The characteristics of internal analog limiting filter (anti-aliasing), which is in front of the AD converter input, are as follows:  $\pm 1\text{dB}$  ( $\sim 6\text{MHz}$ ),  $-30\text{dB}$  ( $27\text{MHz}$ )



AAF Characteristic (except Progressive)

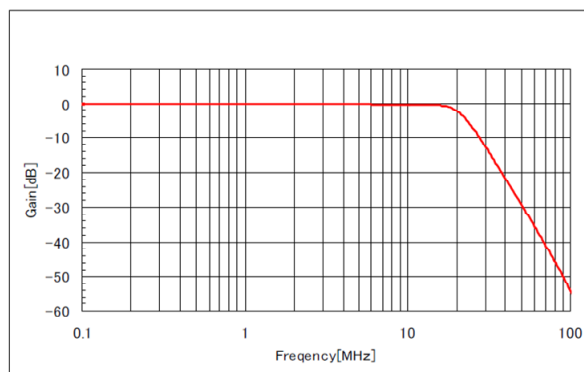
**[7.1.4] 525p/625p YPbPr component video signal decoding**

Y signal data is converted to digital at PGA1 and ADC1. Sampling clock is 54MHz.

Pb signal data is converted to digital at VPGA2 and VADC2. Sampling clock is 27MHz.

Pr signal data is converted to digital at VPGA3 and VADC3. Sampling clock is 27MHz.

The characteristics of internal analog limiting filter (anti-aliasing), which is in front of the AD converter input, are as follows:  $\pm 1\text{dB}$  ( $\sim 12\text{MHz}$ ),  $-30\text{dB}$  ( $54\text{MHz}$ )



AAF Characteristic (Progressive)

**[7.2] Analog Interface**

The AK8858 accepts composite video signal (CVBS), S(Y/C) video signal, YPbPr component video signal (D1/D2) input with 10 input pins available for this purpose.

Sub Address:0x00

Default Value:0x00

| bit 7         | bit 6   | bit 5   | bit 4   | bit 3   | bit 2    | bit 1    | bit 0    |
|---------------|---------|---------|---------|---------|----------|----------|----------|
| CLKMOD        | SELSRC1 | SELSRC0 | ADC3SEL | ADC2SEL | ADC1SEL2 | ADC1SEL1 | ADC1SEL0 |
| Default Value |         |         |         |         |          |          |          |
| 0             | 0       | 0       | 0       | 0       | 0        | 0        | 0        |

The connection settings are shown below.

ADC1SEL[2:0]-bit: Input selection for ADC1. (for CVBS or Y)

| Setting | ADC1 Input |
|---------|------------|
| 000     | AIN1       |
| 001     | AIN2       |
| 010     | AIN3       |
| 011     | AIN4       |
| 100     | AIN5       |
| 101     | AIN6       |

ADC2SEL-bit: Input selection for ADC2 (VADC2). (for C or Pb)

| Setting | ADC2 Input |
|---------|------------|
| 0       | AIN7       |
| 1       | AIN8       |

ADC3SEL-bit: Input selection for ADC3 (VADC2). (for Pr)

| Setting | ADC3 Input |
|---------|------------|
| 0       | AIN9       |
| 1       | AIN10      |

SELSRC[1:0]-bit: Decode signal type setting bit.

| Setting | Input signal                                           |
|---------|--------------------------------------------------------|
| 00      | Composite (CVBS) video signal                          |
| 01      | S-Video signal                                         |
| 10      | Component video signal                                 |
| 11      | Analog power-down (CLAMP, AAF, PGA, ADC is power-down) |

**[7.3] Input Clock mode**

CLKMOD-bit: Input clock setting bit.

| Setting | Input clock                            |
|---------|----------------------------------------|
| 0       | For crystal                            |
| 1       | External clock input (clock generator) |

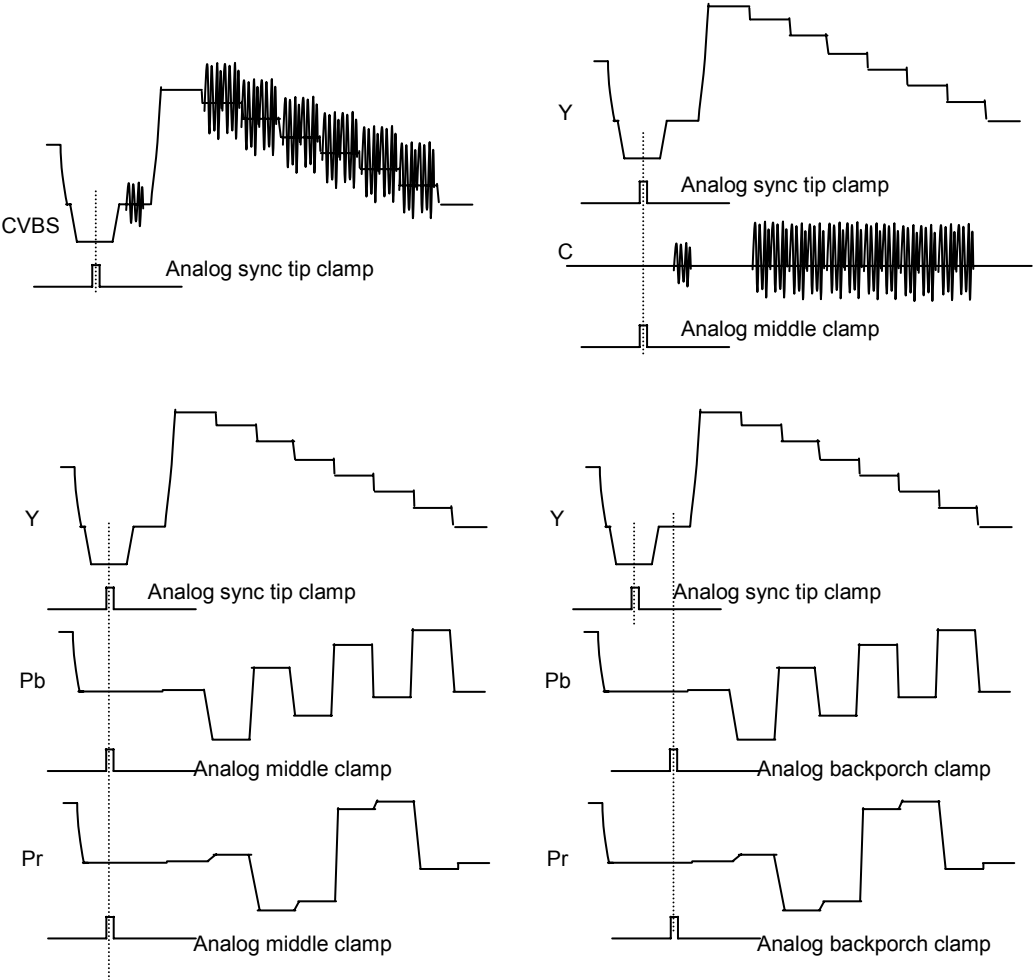
**[7.4] Analog clamp circuit**

The analog circuit of the AK8858 clamps the input signal to the reference level. The way to clamp the input signal is as follows.

The clamp timing pulse, with its origin at the falling edge of the internally synchronized and separated sync signal, is generated at approximately the central position of the sync signal.

| Input signal                  |           | Clamp Level    | Clamp pulse position                                                                                                                        |
|-------------------------------|-----------|----------------|---------------------------------------------------------------------------------------------------------------------------------------------|
| Composite (CVBS) video signal |           | Sync tip level | Sync tip                                                                                                                                    |
| S(Y/C) video signal           | Y signal  | Sync tip level | Sync tip                                                                                                                                    |
|                               | C signal  | Pedestal level | Sync tip of Y                                                                                                                               |
| Component video signal        | Y signal  | Sync tip level | Sync tip                                                                                                                                    |
|                               | Pb signal | Pedestal level | Clamp timing is performs by sync tip clamp or backporch clamp.<br>If Pb and Pr signal have sync signl, set clamp timing to backporch clamp. |
|                               | Pr signal | Pedestal level |                                                                                                                                             |

Clamp Timing Pulse





Additionaly, the AK8858 can change the position, width and current value of clamp pulse via register Clamp Control 1 Register (R/W) [Sub Address 0x01] and Clamp Control 2 Register (R/W) [Sub Address 0x02].

Sub Address: 0x01

Default Value: 0x00

| bit 7         | bit 6      | bit 5     | bit 4     | bit 3    | bit 2      | bit 1      | bit 0      |
|---------------|------------|-----------|-----------|----------|------------|------------|------------|
| CLP-WIDTH1    | CLP-WIDTH0 | CLP-STAT1 | CLP-STAT0 | Reserved | BCLP-STAT2 | BCLP-STAT1 | BCLP-STAT0 |
| Default Value |            |           |           |          |            |            |            |
| 0             | 0          | 0         | 0         | 0        | 0          | 0          | 0          |

Sub Address: 0x02

Default Value: 0x01

| bit 7         | bit 6    | bit 5    | bit 4   | bit 3 | bit 2 | bit 1 | bit 0 |
|---------------|----------|----------|---------|-------|-------|-------|-------|
| Reserved      | Reserved | Reserved | YPBPRCP | UDG1  | UDG0  | CLPG1 | CLPG0 |
| Default Value |          |          |         |       |       |       |       |
| 0             | 0        | 0        | 0       | 0     | 0     | 0     | 1     |

BCLPSTAT[2:0]-bit: Set the position of analog backporch clamp pulse.

| Setting | Clamp position                          | Notes |
|---------|-----------------------------------------|-------|
| 000     | Same position with "CLPSTAT" setting    |       |
| 001     | (1/128)H delay from "CLPSTAT" setting   |       |
| 010     | (2/128)H delay from "CLPSTAT" setting   |       |
| 011     | (3/128)H delay from "CLPSTAT" setting   |       |
| 100     | (4/128)H advance from "CLPSTAT" setting |       |
| 101     | (3/128)H advance from "CLPSTAT" setting |       |
| 110     | (2/128)H advance from "CLPSTAT" setting |       |
| 111     | (1/128)H advance from "CLPSTAT" setting |       |

Set only the position of analog backporch clamp pulse.

CLPSTAT[1:0]-bit: Set the position of clamp pulse.

| Setting | Clamp position                                                                                             | Notes |
|---------|------------------------------------------------------------------------------------------------------------|-------|
| 00      | Sync tip/ middle/ bottom clamp: Center of horizontal sync<br>Backporch clamp: Center of backporch interval |       |
| 01      | (1/128)H delay                                                                                             |       |
| 10      | (2/128)H advance                                                                                           |       |
| 11      | (1/128)H advance                                                                                           |       |

The positions of all clamp pulse are changed.

CLPWIDTH[1:0]-bit: Set the clamp pulse width. Pulse width is change according to sampling clock units.

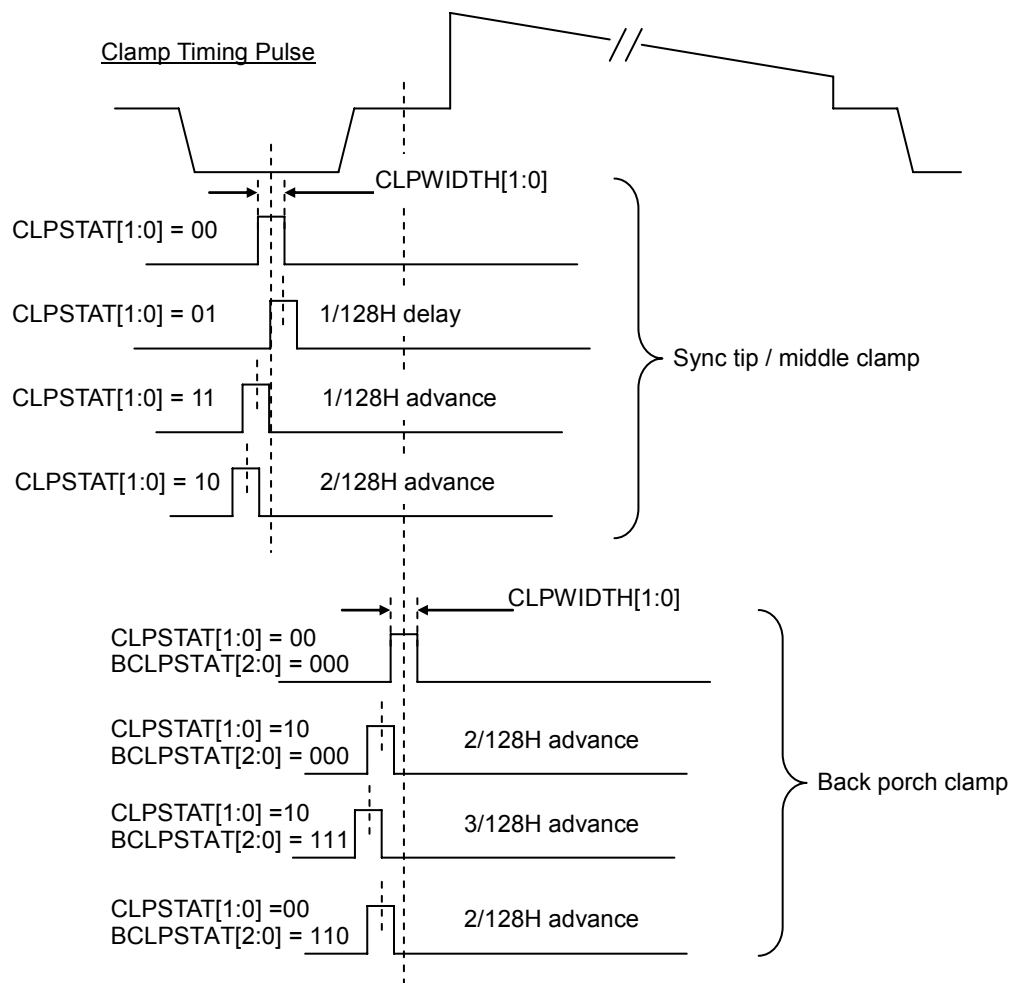
| Setting | Clamp width | Notes                                                 |
|---------|-------------|-------------------------------------------------------|
| 00      | 7 clock     | Clock units<br>525i, 625i: 27MHz<br>525p, 625p: 54MHz |
| 01      | 15 clock    |                                                       |
| 10      | 31 clock    |                                                       |
| 11      | 63 clock    |                                                       |

The width of all clamp pulse is changed.

YPBPRCP-bit: Set the clamp position of PbPr signal of YPbPR component video signal.

| Setting | Clamp position   | Notes |
|---------|------------------|-------|
| 0       | Sync tip timing  |       |
| 1       | Backporch timing |       |

The relation between CLPSTAT and BCLPSTAT is shown as follows.



### Clamp current value setting

CLPG[1:0]: Set the current value of fine clamp in analog block.

| Setting | Clamp current value | Notes                                                                                 |
|---------|---------------------|---------------------------------------------------------------------------------------|
| 00      | Min.                | Middle 1 = (Min. x 3 times)<br>Middle 2 = (Min. x 5 times)<br>Max. = (Min. x 7 times) |
| 01      | Middle 1 (Default)  |                                                                                       |
| 10      | Middle 2            |                                                                                       |
| 11      | Max.                |                                                                                       |

UDG[1:0]: Set the current value of rough clamp in analog block.

| Setting | Clamp current value | Notes                                                                                 |
|---------|---------------------|---------------------------------------------------------------------------------------|
| 00      | Min. (Default)      | Middle 1 = (Min. x 2 times)<br>Middle 2 = (Min. x 3 times)<br>Max. = (Min. x 4 times) |
| 01      | Middle 1            |                                                                                       |
| 10      | Middle 2            |                                                                                       |
| 11      | Max.                |                                                                                       |

Its digital circuit clamps the digitized input data to the pedestal level (digital pedestal clamp).

**[7.5] Input video signal categorization**

Set the input video signal.

Composite (CVBS) video signal, S-Video signal, and Component video signal can be select via register Input Channel Select Register (R/W) [Sub Address 0x00].

When decode composite (CVBS) video signal and S-Video signal, it is necessary to set subcarrier frequency, color encode format, line frequency, and Setup ON/OFF of input signal via register Input Video Standard Register (R/W) [Sub Address 0x04].

When decode component video signal, it is necessary to set line frequency and Setup ON/OFF. It is also necessary to set sync signal and signal ratio of input video signal via register Miscellaneous Setting Register (R/W) [Sub Address 0x03].

Sub Address: 0x04

Default Value:0x00

| bit 7         | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---------------|-------|-------|-------|-------|-------|-------|-------|
| AUTODET       | SETUP | BW    | VLF   | VCEN1 | VCEN0 | VSCF1 | VCSF0 |
| Default Value |       |       |       |       |       |       |       |
| 0             | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

Sub Address: 0x03

Default Value: 0x00

| bit 7         | bit 6 | bit 5    | bit 4  | bit 3    | bit 2 | bit 1 | bit 0    |
|---------------|-------|----------|--------|----------|-------|-------|----------|
| VERTS         | CSCAN | Reserved | CMPSEL | Reserved | CSCL  | CSSL  | Reserved |
| Default Value |       |          |        |          |       |       |          |
| 0             | 0     | 0        | 0      | 0        | 0     | 0     | 0        |

VCSF[1:0]-bit: Setting for subcarrier frequency of input signal.

| Setting | Subcarrier frequency | Formats                                   |
|---------|----------------------|-------------------------------------------|
| 00      | 3.57954545 MHz       | NTSC                                      |
| 01      | 3.57561149 MHz       | PAL-M                                     |
| 10      | 3.58205625 MHz       | PAN-Nc                                    |
| 11      | 4.43361875 MHz       | PAL-B,D,G,H,I,N, NTSC-4.43, PAL60, SECAM* |

\*For SECAM input signal, set VCSF[1:0] to 11.

For component video signal input, VCSF[1:0] setting is not necessary.

VCEN[1:0]-bit: Setting for color encode format of input signal.

| Setting | Color encode format | Notes                                  |
|---------|---------------------|----------------------------------------|
| 00      | NTSC                |                                        |
| 01      | PAL                 |                                        |
| 10      | SECAM               | In case of YPbPr, SECAM is prohibited. |
| 11      | Reserved            |                                        |

For component video signal input, VCEN[1:0] setting is not necessary.

VLF-bit: Setting for line frequency of each input frame.

| Setting | Number of lines | Notes                               |
|---------|-----------------|-------------------------------------|
| 0       | 525             | NTSC-M, J, NTSC-4.43, PAL-M, PAL-60 |
| 1       | 625             | PAL-B, D, G, H, I, N, Nc, SECAM     |

BW-bit: Setting for decoding of input signal as monochrome signal (monochrome mode)

| Setting | Signal type                                      | Notes |
|---------|--------------------------------------------------|-------|
| 0       | Not monochrome (monochrome mode OFF)             |       |
| 1       | Decode as monochrome signal (monochrome mode ON) |       |

In the monochrome mode (BW=1), the input signal is treated as a monochrome signal, and all sampling data digitized the AD converter passes through the luminance process and is processed as luminance signal, and the CbCr code is output as 0x80 regardless of the input.

SETUP-bit: Setting for presence or absence of input signal SETUP.

| Setting | ON/OFF        | Notes                                                                                                                                                                                                                                                                                                                                                                                            |
|---------|---------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0       | Setup absent  |                                                                                                                                                                                                                                                                                                                                                                                                  |
| 1       | Setup present | <p>With the Setup present setting, the luminance and color signals are processed as follows:<br/> <math>Y_{out} = (Y_{IN} - 7.5IRE) / 0.925</math><br/> <math>U_{out} = U_{IN} / 0.925</math>, <math>V_{out} = V_{IN} / 0.925</math></p> <p>YOUT: Y after setup<br/> YIN: Y before setup<br/> UOUT: U after setup<br/> UIN: U before setup<br/> VOUT: V after setup<br/> VIN: V before setup</p> |

In auto detection mode, the default setting of Setup processing via register STUPATOFF-bit of Control 2 Register (R/W) [Sub Address 0x0D]-bit6 is shows as follows.

| Detected signal                                     | Register setting |               | Setup present/ absent |
|-----------------------------------------------------|------------------|---------------|-----------------------|
|                                                     | Setup-bit        | STUPATOFF-bit |                       |
| NTSC-M,J<br>PAL-B,D,G,H,I,N<br>PAL-Nc , 60<br>SECAM | 0                | 0             | Setup absent          |
|                                                     |                  | 1             | Setup absent          |
|                                                     | 1                | 0             | Setup present         |
|                                                     |                  | 1             | Setup present         |
| PAL-M<br>NTSC-4.43                                  | 0                | 0             | Setup present         |
|                                                     |                  | 1             | Setup absent          |
|                                                     | 1                | 0             | Setup present         |
|                                                     |                  | 1             | Setup present         |

In case of YPbPr signal input, auto Setup processing is not performed.

AUTODET-bit: Settings for auto detection of input signal (auto detection mode)

| Setting | ON/OFF | Notes          |
|---------|--------|----------------|
| 0       | OFF    | Manual setting |
| 1       | ON     |                |

CSSL-bit: Settings for sync and video signal ratio of input signal.

| Setting | S/V ratio | Notes     |
|---------|-----------|-----------|
| 0       | 300/700   | EIA-770.2 |
| 1       | 286/714   | EIA-770.1 |

Only available when component input signal is selected.

CSCL-bit: Settings for color level of component input signal.

| Setting | Video level | Notes     |
|---------|-------------|-----------|
| 0       | 700mV       | EIA-770.2 |
| 1       | 714mV       | EIA-770.1 |

Only available when component input signal is selected.

CMPSEL-bit: Interlace and Progressive setting for YPbPr component input signal.

| Setting | YPbPr component video signal |
|---------|------------------------------|
| 0       | Interlace (525i/ 625i)       |
| 1       | Progressive (525P/ 625P)     |

VERTS-bit: Select of VLOCK or Direct Lock

| Setting | SYNC mechanism        | Notes |
|---------|-----------------------|-------|
| 0       | VLOCK mechanism       |       |
| 1       | Direct LOCK mechanism |       |

**[7.6] Auto detection mode of input signal**

The video input signal can be automatically detected (auto detection mode) via register.

Settings for auto detection of input signal (auto detection mode)

Sub Address: 0x04 [7]

| Name    | Setting | ON/OFF              | Notes |
|---------|---------|---------------------|-------|
| AUTODET | 0       | OFF(Manual setting) |       |
|         | 1       | ON                  |       |

The auto detection recognizes the following parameters (AUTODET-bit=1).

Number of lines per frame:

525/626

Subcarrier frequency:

3.57954545 (MHz)

3.57561149 (MHz)

3.58205625 (MHz)

4.43361875 (MHz)

Color encoding formats:

NTSC/PAL/SECAM

Progressive setting:

Interlace / Progressive

Monochrome signal\*:

Not monochrome/monochrome.

\*Note: Automatic monochrome detection is active if the color kill setting is ON.

The detected result of auto detection mode is reflected to Input Video Status Register. The input signal status can be recognized by reading this register.

Sub Address: 0x25

| bit 7 | bit 6 | bit 5 | bit 4  | bit 3    | bit 2    | bit 1    | bit 0    |
|-------|-------|-------|--------|----------|----------|----------|----------|
| FIXED | UNDEF | ST_BW | ST_VLF | ST_VCEN1 | ST_VCEN0 | ST_VSCF1 | ST_VCSF0 |

In addition, auto detection function of the input signal is recognized by the changing of internal status.

If FIXED-bit changed from 0 to 1, the detection is completed. During FIXED-bit is 0, the AK8858 may attempt to recognize the input signal and the output code during this period cannot be trusted. If the AK8858 cannot recognize the input signal, UNDEF-bit is changed from 0 to 1 to indicate the status of the input signal.

**[7.7] Auto detection restriction of input signal**

In auto detection mode, the candidates for detection can be limited via register NDMODE Register.

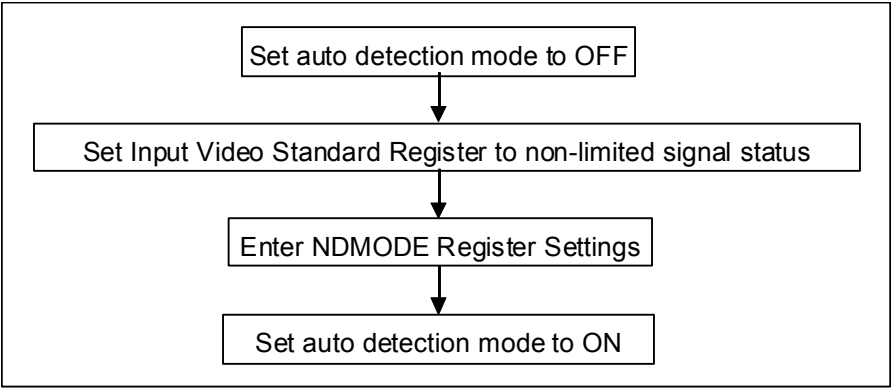
Sub Address:0x06

Default Value: 0x00

| bit 7         | bit 6  | bit 5   | bit 4     | bit 3    | bit 2   | bit 1   | bit 0  |
|---------------|--------|---------|-----------|----------|---------|---------|--------|
| ND625L        | ND525L | NDPAL60 | NDNTSC443 | Reserved | NDSECAM | NDPALNC | NDPALM |
| Default Value |        |         |           |          |         |         |        |
| 0             | 0      | 0       | 0         | 0        | 0       | 0       | 0      |

In making the above register settings, the following restrictions apply.

1. Setting both NDNTSC443-bit and NDPAL60-bit to 1 is prohibited.
2. Setting both ND525L-bit and ND625L-bit to 1 is prohibited.
3. To limit candidate formats, it is necessary to have the auto detection mode OFF while first setting the register to non-limited signal status and next the NDMODE settings, and then setting the auto detection mode to ON.



**[7.8] Output data blanking interval**

Setting vertical blanking intervals.

Sub Address: 0x05[2:0]

| VBIL[2:0]-bit | 525/625  | Vertical blanking interval             | Notes   |
|---------------|----------|----------------------------------------|---------|
| 001           | 525i     | Line1~Line20 and Line263.5~Line283.5   | +1Line  |
|               | 625i     | Line623.5~Line24.5 and Line311~Line336 |         |
|               | 525p     | Line1~Line43                           |         |
|               | 625p     | Line 621~Line625 and Line1~Line45      |         |
| 010           | 525i     | Line1~Line21 and Line263.5~Line284.5   | +2Lines |
|               | 625i     | Line623.5~Line25.5 and Line311~Line337 |         |
|               | 525p     | Line1~Line44                           |         |
|               | 625p     | Line 621~Line625 and Line1~Line46      |         |
| 011           | 525i     | Line1~Line22 and Line263.5~Line285.5   | +3Lines |
|               | 625i     | Line623.5~Line26.5 and Line311~Line338 |         |
|               | 525p     | Line1~Line45                           |         |
|               | 625p     | Line 621~Line625 and Line1~Line47      |         |
| 000           | 525i     | Line1~Line19 and Line263.5~Line282.5   | Default |
|               | 625i     | Line623.5~Line23.5 and Line311~Line335 |         |
|               | 525p     | Line1~Line42                           |         |
|               | 625p     | Line 621~Line625 and Line1~Line44      |         |
| 101           | 525i     | Line1~Line16 and Line263.5~Line279.5   | -3Lines |
|               | 625i     | Line623.5~Line20.5 and Line311~Line332 |         |
|               | 525p     | Line1~Line39                           |         |
|               | 625p     | Line 621~Line625 and Line1~Line41      |         |
| 110           | 525i     | Line1~Line17 and Line263.5~Line280.5   | -2Lines |
|               | 625i     | Line623.5~Line21.5 and Line311~Line333 |         |
|               | 525p     | Line1~Line40                           |         |
|               | 625p     | Line 621~Line625 and Line1~Line42      |         |
| 111           | 525i     | Line1~Line18 and Line263.5~Line281.5   | -1Line  |
|               | 625i     | Line623.5~Line22.5 and Line311~Line334 |         |
|               | 525p     | Line1~Line41                           |         |
|               | 625p     | Line 621~Line625 and Line1~Line43      |         |
| 100           | Reserved | Reserved                               |         |

As indicated in this table, the default values are:

(525i) Line1~Line19 and Line263.5~Line282.5

(625i) Line623.5~Line23.5 and Line311~Line335

(525P) Line1~Line42

(625P) Line 621~Line625 and Line1~Line44

The other specific values are set by entering the difference from these default values.

**[7.9] Output data code Min/Max setting**

LIMIT601-bit: Setting for output data code Min/Max

Sub Address: 0x05[3]

| LIMIT601-bit | Output data code Min~Max                       | EAVSAV-bit | Notes |
|--------------|------------------------------------------------|------------|-------|
| 0            | Y: 1~254<br>Cb, Cr: 1~254<br>R, G, B: 1~254    | 0          | (*1)  |
|              | Y: 0~255<br>Cb, Cr: 0~255<br>R, G, B: 0~255    | 1          |       |
| 1            | Y: 16~235<br>Cb, Cr: 16~240<br>R, G, B: 16~235 | X          | (*2)  |

All internal calculating operations are made with Min = 1, Max = 254.

(\*1)In case of LIMIT601-bit = 0, the output code Min and Max values is set according to EAVSAV-bit status.

(\*2)In case of LIMIT601-bit = 1, codes 1~15 and 236~254 are respectively clipped to 16,235(Cb, Cr is 240).

**[7.10] Output Pin state**

DATA[23:0], HD, VD\_FLD, DVAL\_FLD and NSIG pins can be Low output by register.

Sub Address: 0x07 [4:0]

| Name   | Setting | Definition                        | 備考                     |
|--------|---------|-----------------------------------|------------------------|
| DL     | [0]     | Normal output                     | Default: Normal output |
|        | [1]     | [D23: D0] pin output fixed at low |                        |
| VDFL   | [0]     | Normal output                     | Default: Normal output |
|        | [1]     | VDFL pin output fixed at low      |                        |
| DVALFL | [0]     | Normal output                     | Default: Normal output |
|        | [1]     | DVALFL pin output fixed at low    |                        |
| NL     | [0]     | Normal output                     | Default: Normal output |
|        | [1]     | NL pin output fixed at low        |                        |
| HL     | [0]     | Normal output                     | Default: Normal output |
|        | [1]     | HL pin output fixed at low        |                        |

OE, PDN and RSTN pins are prior to these register.



# [7.11] Slice function

The results of VBI slicing by the AK8858 slicing function are output as ITU-R BT.601 digital data. The VBI interval is set via VBIL[2:0]-bits. VBI slicing is performed in the luminance in the luminance signal processing path, so that the Cb/Cr value of the effective line 601 output code is output at the same level as the corresponding luminance signal.

Setting for slice level Sub Address: 0x05 [5]

| Name  | Definition               |
|-------|--------------------------|
| SLLVL | [0]: 25IRE<br>[1]: 50IRE |

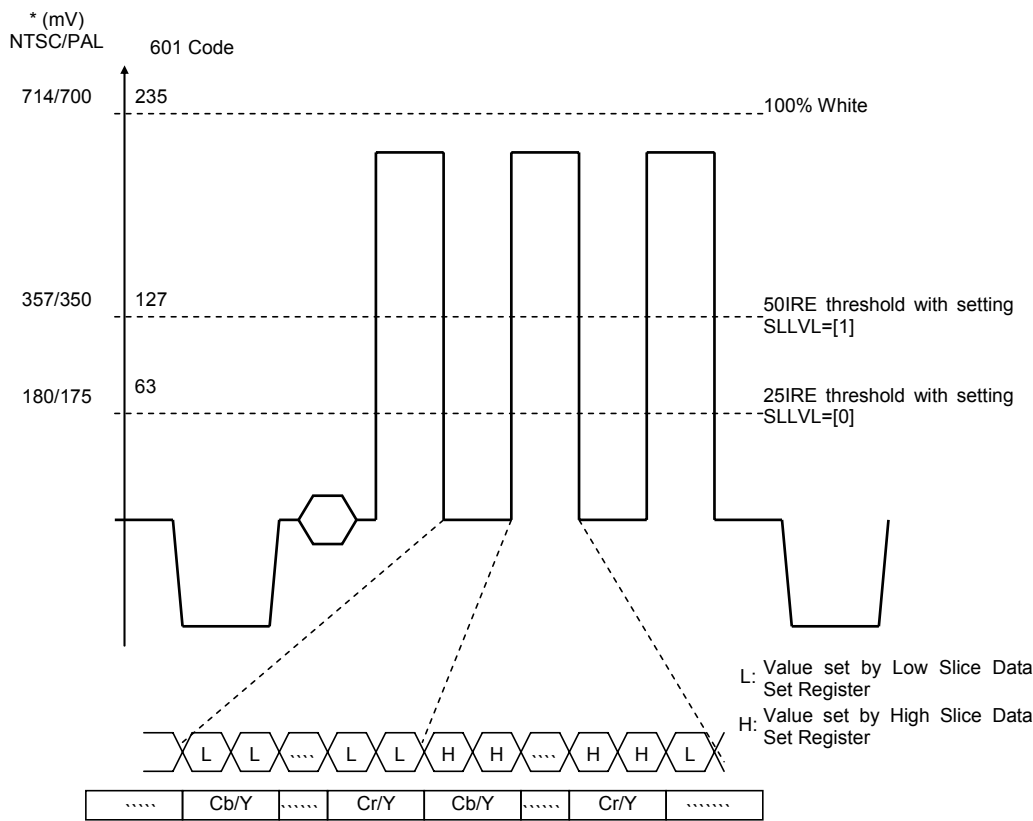
Hi/Low Slice Data Set Register of output data, as follows.

Setting for higher of two values resulting from slicing Sub Address: 0x18

| Name          | Definition                                                                                   |
|---------------|----------------------------------------------------------------------------------------------|
| H0<br>~<br>H7 | Default: 0xEB(235)<br>Note that a setting of 0x00 or 0xFF corresponds to a special 601 code. |

Setting for lower of two values resulting from slicing Sub Address: 0x19

| Name          | Definition                                                                                  |
|---------------|---------------------------------------------------------------------------------------------|
| L0<br>~<br>L7 | Default: 0x10(16)<br>Note that a setting of 0x00 or 0xFF corresponds to a special 601 code. |



\*Threshold values (mV) are approximate

High/Low conversion is performed for either the Cb/Y or the Cr/Y combination. The above figure is an example of the conversion points for Cb/Y.

**[7.12] VBI period decode data**

The AK8858 decode data during VBI period can be selected via register.

Settings for decode data in the VBI period

Sub Address: 0x05 [7:6]

| Name                    | Setting value | Decode data        | Notes                                                                                         |
|-------------------------|---------------|--------------------|-----------------------------------------------------------------------------------------------|
| VBIDEC0<br>~<br>VBIDEC1 | [00]          | Black level output | Y = 0x10<br>Cb/Cr = 0x80                                                                      |
|                         | [01]          | Monochrome mode    | Y = data converted to 601 level<br>Cb/Cr = 0x80                                               |
|                         | [10]          | Sliced data output | Y/Cb/Cr = value corresponding to slice level<br>(Value set at Hi/Low Slice Data Set Register) |
|                         | [11]          | Reserved           | Reserved                                                                                      |

Note: (525i) Line1~Line9 and Line263.5~Line272.5

(625i) Line623.5~Line6.5 and Line311~Line388

(525p) Line1~Line18

(625p) Line621~Line10

During the above period, these values are unaffected by the VBIDEC[1:0]-bits setting.

The output code during this period is black level code (Y=0x10, Cb/Cr=0x80).

**[7.13] VLOCK mechanism**

The AK8858 synchronizes internal operation with the input signal frame structure. If, for example, the frame structure of the input signal comprises 524 lines, the internal operation will have structure of 524 lines per frame. This mechanism is termed the VLOCK mechanism. If an input signal changes from a structure of 525 lines per frame to one of 524 lines per frame, internal operation will change accordingly, and the VLOCK mechanism will go to UnLock via a pull-in process. In such case, the UnLock status can be confirmed via the control register [VLOCK-bit\*]. Note that the time required for locking of the VLOCK mechanism upon channel or other input signal switching will be about 4 frames (\*Sub-address:0x22-“bit1”)

Furthermore, the AK8858 synchronizes internal operation with the vertical SYNC of the input signal. This mechanism is termed the direct LOCK mechanism.

Setting for Vertical SYNC mechanism

Sub Address: 0x03 [7]

| Name  | Definition                                                                    |
|-------|-------------------------------------------------------------------------------|
| VERTS | Vertical SYNC mechanism<br>[0]: VLOCK mechanism<br>[1]: Direct LOCK mechanism |

**[7.14] Adjustment of Y and C timing**

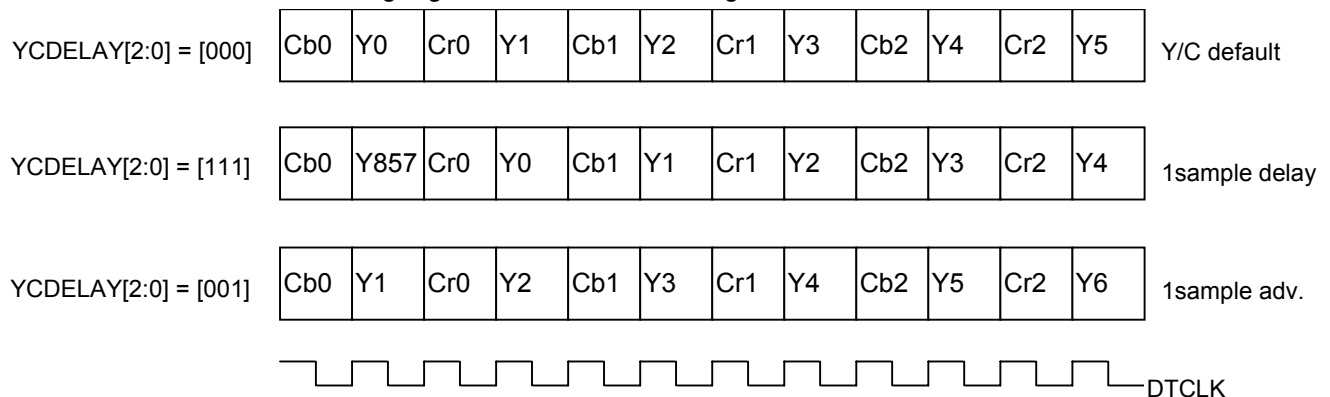
Adjustment of the position between Y and C signal

Sub Address: 0x08 [2:0]

| YCDELAY[2:0]-bit | Y and C timing                    | Notes   |
|------------------|-----------------------------------|---------|
| 001              | Y advance 1 sample toward Cb, Cr. |         |
| 010              | Y advance 2 sample toward Cb, Cr. |         |
| 011              | Y advance 3 sample toward Cb, Cr. |         |
| 000              | No delay and advance.             | Default |
| 101              | Y delay 3 sample toward Cb, Cr.   |         |
| 110              | Y delay 2 sample toward Cb, Cr.   |         |
| 111              | Y delay 1 sample toward Cb, Cr.   |         |
| 100              | Reserved                          |         |

Note: 1sample of Interlace output is about 74ns / 1 sample of progressive output is about 37ns.

Relation between Y and C timing regardless the above setting is shown as follows.

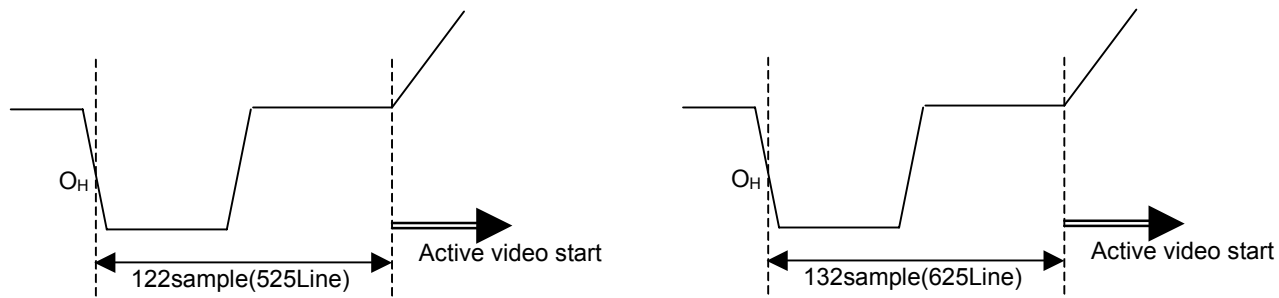
**[7.15] Adjustment of active video start position**

Adjustment of the active video start position

Sub Address: 0x08 [6:4]

| ACTSTA[2:0]-bit | Line and active video start |              | Notes                     |
|-----------------|-----------------------------|--------------|---------------------------|
| 001             | 525 Line                    | 124th sample | D1 decode: 74ns delay     |
|                 | 625 Line                    | 134th sample | D2 decode: 37ns delay     |
| 010             | 525 Line                    | 125th sample | D1 decode: 148ns delay    |
|                 | 625 Line                    | 135th sample | D2 decode: 74ns delay     |
| 011             | 525 Line                    | 126th sample | D1 decode: 222ns delay    |
|                 | 625 Line                    | 136th sample | D2 decode: 111ns delay    |
| 000             | 525 Line                    | 123th sample | Default (Normal position) |
|                 | 625 Line                    | 133th sample |                           |
| 101             | 525 Line                    | 120th sample | D1 decode: 222ns advance  |
|                 | 625 Line                    | 130th sample | D2 decode: 111ns advance  |
| 110             | 525 Line                    | 121th sample | D1 decode: 148ns advance  |
|                 | 625 Line                    | 131th sample | D2 decode: 74ns advance   |
| 111             | 525 Line                    | 122th sample | D1 decode: 74ns advance   |
|                 | 625 Line                    | 132th sample | D2 decode: 37ns advance   |
| 100             | Reserved                    | Reserved     |                           |

With the default value, the start position is as follows (with ITU-R BT.601 format compliance).



### [7.16] PGA

The AK8858 analog PGA and digital PGA are built internally.  
 The analog PGA value can be set in range of -3dB to 6dB, and the gain step is 3dB/step.  
 The digital PGA value can be set in range -0.25dB to 4dB, and the gain step is not log scale.

Digital PGA gain equation:

$$\text{Gain(dB)} = 20\text{LOG}\left(\frac{(5 \times \text{PGA}) + 497}{512}\right)$$

\*PGA: PGA1 or PGA2 register value (Decimal)

Default gain setting is 0x54(HEX)=1.3dB. (Analog:0dB + Digital:1.3dB)  
 At the default setting, when the composite video signal input with 0.5Vpp is input to the AIN pin, the decode gain setting is set to appropriate range.

PGA1 is used for CVBS and Y signals gain processing.

Setting for PGA1 value Sub Address: 0x0E [7:0]

| Name                    | Definition                                                                       |
|-------------------------|----------------------------------------------------------------------------------|
| DPGA1_0<br>~<br>DPGA1_5 | Digital PGA1 gain setting.<br>PGA gain is set by above equation.                 |
| APGA1_0<br>~<br>APGA1_1 | Analog PGA1 gain setting.<br>[00]: -3dB<br>[01]: 0dB<br>[10]: +3dB<br>[11]: +6dB |

PGA2 is used for C, Pb, and Pr signals gain processing.

Setting for PGA2 value Sub Address: 0x0F [7:0]

| Name                    | Definition                                                                       |
|-------------------------|----------------------------------------------------------------------------------|
| DPGA2_0<br>~<br>DPGA2_5 | Digital PGA2 gain setting.<br>PGA gain is set by above equation.                 |
| APGA2_0<br>~<br>APGA2_1 | Analog PGA2 gain setting.<br>[00]: -3dB<br>[01]: 0dB<br>[10]: +3dB<br>[11]: +6dB |

This register also can be used to read the current setting of the AGC setting.  
 If AGC is enable, the Gain1/2 Control Register[7:0]-bit setting value has no effect.  
 If AGC is disable, the Gain1/2 Control Register setting can be manually entered.

**[7.17] AGC (Auto Gain Control)**

The AGC function amplifies the input signal to the appropriate size and enables input to the AD converter. The AGC function in the AK8858 is adaptive, and thus includes peak AGC as well as sync AGC.

The AGC of the AK8858 measures the size of the input signal (i.e. the difference between the sync tip and pedestal levels), and adjusts the PGA value to bring the sync signal level to 286mV/300mV (525/625).

Peak AGC is effective for input signals in which the sync signal level is appropriate and only the active video signal is large.

In case of component video signal and S-Video signal inputs, AGC are adjust by Y sync level.

When AGC function is enables, the setting values of AGC can be read via register Gain Control Register.

Settings for AGC time constant

Sub Address: 0x0A [1:0]

| AGCT[1:0]-bit | Time constant | Notes                          |
|---------------|---------------|--------------------------------|
| 00            | Disable       | AGC OFF, PGA register enabled. |
| 01            | Fast          | T= 1Field                      |
| 10            | Middle        | T= 7Fields                     |
| 11            | Slow          | T= 29Fields                    |

T is the time constant.

Settings for AGC non-sensing range

Sub Address: 0x0A [3:2]

| AGCC[1:0]-bit | Non-sensing range | Notes |
|---------------|-------------------|-------|
| 00            | ±2LSB             |       |
| 01            | ±3LSB             |       |
| 10            | ±4LSB             |       |
| 11            | None              |       |

Settings for freezing AGC function

Sub Address: 0x0A [4]

| AGCFRZ-bit | AGC status | Notes |
|------------|------------|-------|
| 0          | Non-frozen |       |
| 1          | Frozen     |       |

Settings for selection of quick or slow transition between peak and sync AGC

Sub Address: 0x0B [0]

| AGCTL-bit | AGC transition | Notes |
|-----------|----------------|-------|
| 0         | Quick          |       |
| 1         | Slow           |       |

**[7.18] ACC (Auto Color Control)**

The ACC of the AK8858 measures the level of the input signal color burst and adjusts to the appropriate level. The ACC is not applicable to SECAM, and YPbPr input signals.

The ACC and Color saturation functions operate independently. If ACC is enabled, the color saturation adjustment is applied to the signal that has been adjusted to the appropriate level by the ACC.

Settings for ACC time constant

Sub Address: 0x0A [6:5]

| ACCT[1:0]-bit | Time constant | Notes       |
|---------------|---------------|-------------|
| 00            | Disable       | ACC OFF     |
| 01            | Fast          | T= 2Fields  |
| 10            | Middle        | T= 8Fields  |
| 11            | Slow          | T= 30Fields |

Settings for freezing ACC function

Sub Address: 0x0A [7]

| ACCFRZ-bit | ACC status | Notes |
|------------|------------|-------|
| 0          | Non-frozen |       |
| 1          | Frozen     |       |

**[7.19] Y/C separation**

The adaptive two-dimensional Y/C separation of the AK8858 utilizes a co-relation detector to select the best-correlated direction from among vertical, horizontal, and diagonal samples, and selects the optimum Y/C separation mode.

For NTSC-4.43, PAL-60, and SECAM inputs, the Y/C separation is one-dimensional only, regardless of the setting.

Setting for Y/C separation

Sub Address: 0x0C [1:0]

| Name                  | Setting Value | YC separation mode | Notes                                                             |
|-----------------------|---------------|--------------------|-------------------------------------------------------------------|
| YCSEP0<br>~<br>YCSEP1 | [00]          | Adaptive           |                                                                   |
|                       | [01]          | 1-D                | 1-D (BPF)                                                         |
|                       | [10]          | 2-D                | (NTSC-M,J, PAL-M): 3 Line 2-D<br>(PAL-B,D,G,H,I,N,Nc): 5 Line 2-D |
|                       | [11]          | Reserved           |                                                                   |

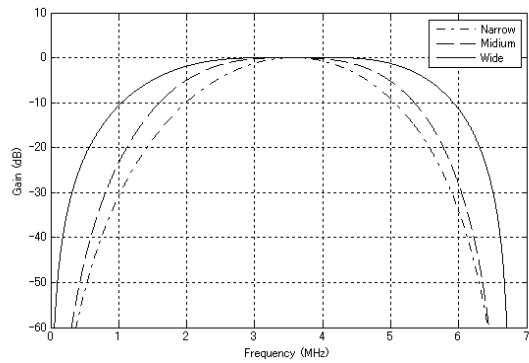
**[7.20] C Filter**

The bandwidth of the C filter can be set via register, as follows.

Settings for C filter bandwidth, for input signal with 3.58 MHz subcarrier wave.

Sub Address: 0x0B [2:1]

| C358FIL[1:0] -bit | C filter bandwidth | Notes                     |
|-------------------|--------------------|---------------------------|
| 00                | Narrow             | NTSC-M,J , PAL-M , PAL-Nc |
| 01                | Medium             |                           |
| 10                | Wide               |                           |
| 11                | Reserved           |                           |

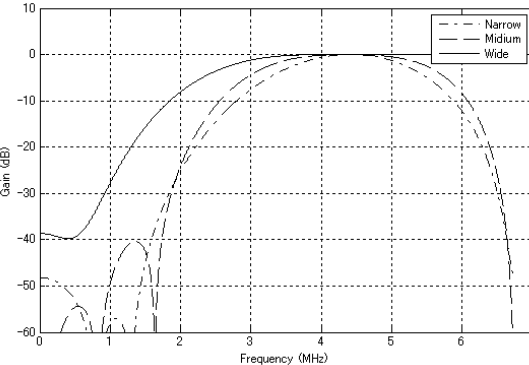


Settings for C filter bandwidth, for input signal with 4.43 MHz subcarrier wave.

Sub Address: 0x0B [4:3]

| C443FIL[1:0] -bit | C filter bandwidth | Notes                                |
|-------------------|--------------------|--------------------------------------|
| 00                | Narrow             | PAL-B,D,G,H,I,N , NTSC-4.43 , PAL-60 |
| 01                | Medium             |                                      |
| 10                | Wide               |                                      |
| 11                | Reserved           |                                      |

\*Note: No bandwidth selection is possible for SECAM input.



**[7.21] Clock generation**

The AK8858 operates in the following three clock modes:

1. Line-locked clock mode.
2. Frame-locked clock mode
3. Fixed clock mode

The clock mode can be set via register.

**[7.21.1] Line-locked clock mode**

The “line-locked clock” is generated by PLL using horizontal sync signal within the input signal. If no input signal is present, the AK8858 will switch from this mode to fixed-clock mode.

**[7.21.2] Frame-locked mode**

The “frame-locked clock” is generated by PLL using vertical sync signal within the input signal. If no signal is present, the AK8858 will switch from this mode to fixed-clock mode.

**[7.21.3] Fixed-clock mode**

No PLL control is applied in this mode, which is enabled only when either it is set via the register or no input signal is present. The sampling clock in this mode is 27MHz or 54MHz. In this mode, data capture cannot be performed in EAV (end of active video), and must be performed in SAV (start of active video) format. The number of pixels per line is not guarantee in this mode, but data guarantee is performed in the interval from SAV to EAV.

In the line-locked and frame-locked clock modes, the clock is synchronized with the input signal and the output is ITU-R BT.656 compliant. It should be noted that ITU-R BT.656 compliant output may not be possible with low-quality input signals.

It should be noted that in the fixed-clock mode the sample number will be insufficient for ITU-R BT.656 compliance, due to non-synchronization of the input data.

**[7.21.4] Auto transition mode**

The AK8858 transition function automatically switches among the above modes and selects the optimum one, and when no input signal is present, it switches to the fixed-clock mode.

Settings for selection of clock generation mode.

Sub Address 0x0C [7:6]

| CLKMODE[1:0]-bit | Clock generation mode | Notes |
|------------------|-----------------------|-------|
| 00               | Automatic             |       |
| 01               | Line-locked           |       |
| 10               | Frame-locked          |       |
| 11               | Fixed-clock           |       |



**[7.22] Digital Pixel Interpolar**

The digital pixel interpolator of the AK8858 aligns vertical pixel positions in both frame-lock and fixed-clock operating modes. The pixel interpolator can be set to ON or OFF via register. With a register setting of AUTO, the pixel interpolator is OFF or ON depending on the clock mode, as follows.

|                         |     |
|-------------------------|-----|
| Line-locked clock mode  | OFF |
| Frame-locked clock mode | ON  |
| Fixed-clock mode        | ON  |

Settings for pixel interpolator operation

Sub Address: 0x0C [5:4]

| INTPOL[1:0]-bit | Interpolar operation | Notes                   |
|-----------------|----------------------|-------------------------|
| 00              | Auto                 | Dependent on clock mode |
| 01              | ON                   |                         |
| 10              | OFF                  |                         |
| 11              | Reserved             |                         |

**[7.23] Phase correction**

In PAL-B, D, G, H, I, N, Nc, 60, and M decoding, the AK8858 performs phase correction for each line. With this function ON, color averaging is performed for each line. In the adaptive phase correction mode, interline phase correlation is sampled and color averaging is performed for correlated samples.

Interline color averaging is also performed in NTSC-M and J decoding.

No phase correction or color averaging is performed in SECAM decoding.

Settings for phase correction

Sub Address: 0x0D [1:0]

| DPAL[1:0]-bit | Status                         | Notes |
|---------------|--------------------------------|-------|
| 00            | Adaptive phase correction mode |       |
| 01            | Phase correction ON            |       |
| 10            | Phase correction OFF           |       |
| 11            | Reserved                       |       |

**[7.24] No-signal output**

If no input signal is found (as shown by control bit NOSIG-bit), the output signal is black-level, blue-level (blueback), or input-state (sandstorm), depending on the register setting.

Settings for output signals for no input signal

Sub Address: 0x0D [3:2]

| NSIGMD [1:0]-bit | Output                  | Notes |
|------------------|-------------------------|-------|
| 00               | Black-level             |       |
| 01               | Blue-level (blueback)   |       |
| 10               | Input-state (sandstorm) |       |
| 11               | Reserved                |       |

**[7.25] Output data format**

AK8858 output YCbCr or RGB data.

| Output format | bit   |
|---------------|-------|
| YCbCr         | 8bit  |
|               | 16bit |
| RGB           | 24bit |

Settings for YCbCr output data width

Sub Address: 0x09 [0]

| Name  | Definition | Notes                                  |
|-------|------------|----------------------------------------|
| ODFMT | [0]: 8bit  | If RGBCNV = [1], output data is 24bit. |
|       | [1]: 16bit |                                        |

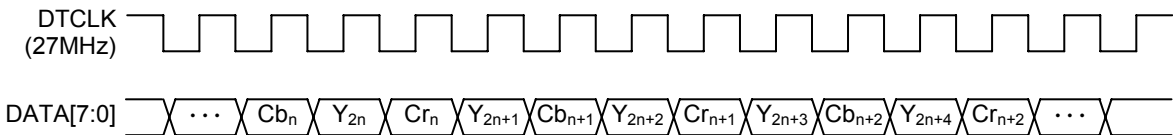
Settings for RGB output

Sub Address: 0x09 [2]

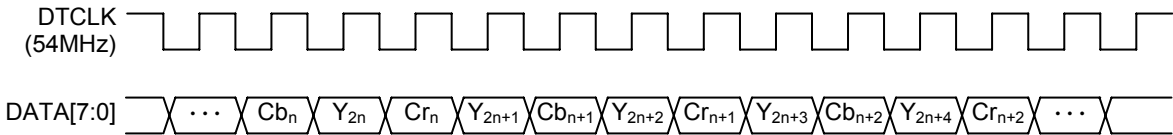
| Name   | Definition             | Notes                                  |
|--------|------------------------|----------------------------------------|
| RGBCNV | [0]: YCbCr<br>[1]: RGB | If RGBCNV = [1], output data is 24bit. |

**[7.25.1] YCbCr 8bit output format**

Interlace



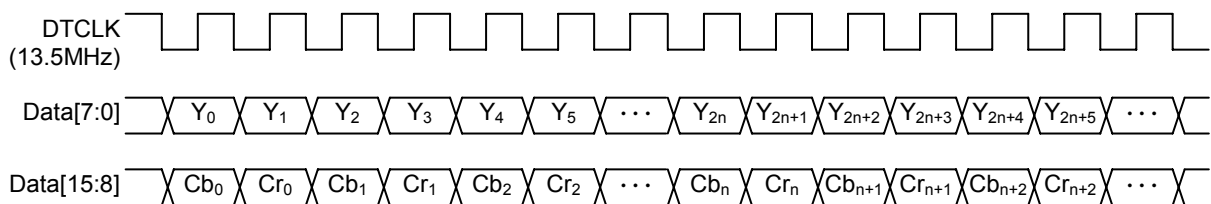
Progressive



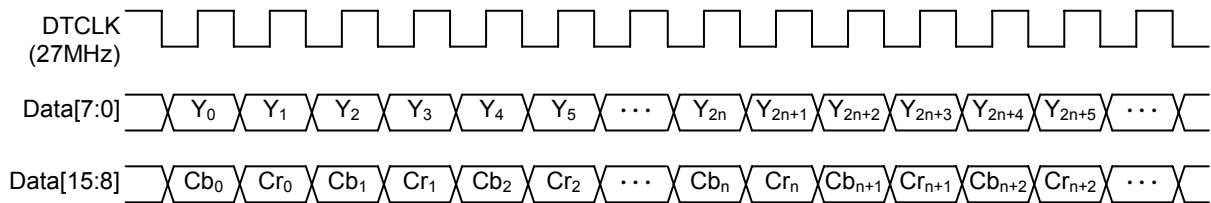
DATA[23:8] is low output.

**[7.25.2] YCbCr 16bit output format**

Interlace



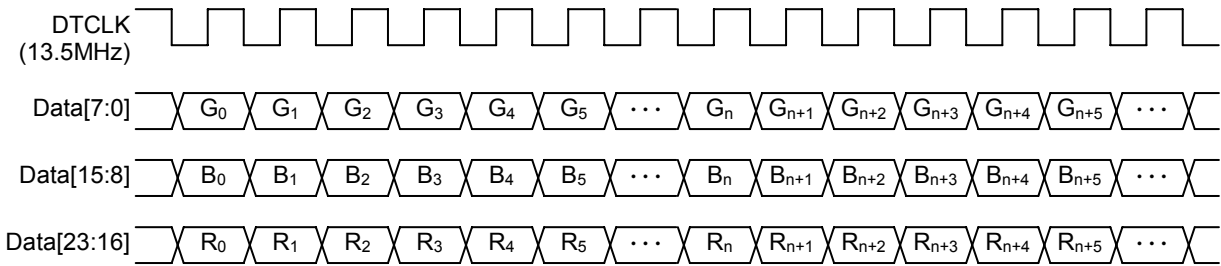
Progressive



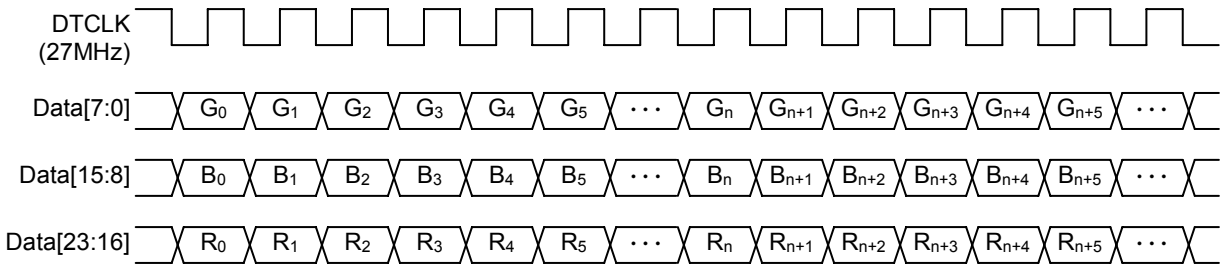
DATA[23:16] is low output.

**[7.25.3] RGB 24bit output format**

Interlace



Progressive



**[7.26] Output Interface****[7.26.1] Interface with EAV/SAV**

SYNC code is output with the output data.

**[7.26.1.1] EAV/ SAV code**

Those code succeeding 0xFF – 0x00 – 0x00 which are fed as input data become EAV/SAV codes.

EAV/SAV codes have following meanings, started with MSB.

| Bit Number |                 | MSB |   |   |   |    |    |    |    | LSB |  |
|------------|-----------------|-----|---|---|---|----|----|----|----|-----|--|
| WORD       | VALUE           | 7   | 6 | 5 | 4 | 3  | 2  | 1  | 0  |     |  |
| 0          | 0xFF            | 1   | 1 | 1 | 1 | 1  | 1  | 1  | 1  |     |  |
| 1          | 0x00            | 0   | 0 | 0 | 0 | 0  | 0  | 0  | 0  |     |  |
| 2          | 0x00            | 0   | 0 | 0 | 0 | 0  | 0  | 0  | 0  |     |  |
| 3          | 0xXX (EAV/ SAV) | 1   | F | V | H | P3 | P2 | P1 | P0 |     |  |

F=0: Field1

F=1: Field2

\*In case of Progressive (525P/ 625P) output, F-bit output is always 0.

V=0: Exept for Field Blanking

V=1: Field Blanking

H=0: SAV

H=1: EAV

P3, P2, P1, P0: Protection bit

Following is a relation between protection bit and F/V/H-bit.

| F | V | H | P3 | P2 | P1 | P0 |
|---|---|---|----|----|----|----|
| 0 | 0 | 0 | 0  | 0  | 0  | 0  |
| 0 | 0 | 1 | 1  | 1  | 0  | 1  |
| 0 | 1 | 0 | 1  | 0  | 1  | 1  |
| 0 | 1 | 1 | 0  | 1  | 1  | 0  |
| 1 | 0 | 0 | 0  | 1  | 1  | 1  |
| 1 | 0 | 1 | 1  | 0  | 1  | 0  |

**Reference standards**

| Input format | Reference     |
|--------------|---------------|
| 525i         | ITU-R.BT656   |
| 625i         | ITU-R.BT656   |
| 525p         | SMPTE 293M    |
| 625p         | ITU-R. BT1358 |

**[7.26.1.2] EAV/SAV code position**

## YCbCr 8bit 525Line

|           |          |           |          |           |          |           |          |     |           |          |           |          |         |        |         |        |
|-----------|----------|-----------|----------|-----------|----------|-----------|----------|-----|-----------|----------|-----------|----------|---------|--------|---------|--------|
| Cb<br>359 | Y<br>718 | Cr<br>359 | Y<br>719 | Cb<br>360 | Y<br>720 | Cr<br>360 | Y<br>721 | ... | Cb<br>428 | Y<br>856 | Cr<br>428 | Y<br>857 | Cb<br>0 | Y<br>0 | Cr<br>0 | Y<br>1 |
|           |          |           |          | 0xFF      | 0x00     | 0x00      | EAV      |     | 0xFF      | 0x00     | 0x00      | SAV      |         |        |         |        |

## YCbCr 8bit 625Line

|           |          |           |          |           |          |           |          |     |           |          |           |          |         |        |         |        |
|-----------|----------|-----------|----------|-----------|----------|-----------|----------|-----|-----------|----------|-----------|----------|---------|--------|---------|--------|
| Cb<br>359 | Y<br>718 | Cr<br>359 | Y<br>719 | Cb<br>360 | Y<br>720 | Cr<br>360 | Y<br>721 | ... | Cb<br>431 | Y<br>862 | Cr<br>431 | Y<br>863 | Cb<br>0 | Y<br>0 | Cr<br>0 | Y<br>1 |
|           |          |           |          | 0xFF      | 0x00     | 0x00      | EAV      |     | 0xFF      | 0x00     | 0x00      | SAV      |         |        |         |        |

## YCbCr 16bit 525Line

|          |          |          |          |          |          |     |          |          |          |          |        |        |
|----------|----------|----------|----------|----------|----------|-----|----------|----------|----------|----------|--------|--------|
| Y<br>718 | Y<br>719 | Y<br>720 | Y<br>721 | Y<br>722 | Y<br>723 | ... | Y<br>854 | Y<br>855 | Y<br>856 | Y<br>857 | Y<br>0 | Y<br>1 |
|          |          | 0xFF     | 0x00     | 0x00     | EAV      |     | 0xFF     | 0x00     | 0x00     | SAV      |        |        |

Only Y signal with EAV/SAV

## YCbCr 16bit 625Line

|          |          |          |          |          |          |     |          |          |          |          |        |        |
|----------|----------|----------|----------|----------|----------|-----|----------|----------|----------|----------|--------|--------|
| Y<br>718 | Y<br>719 | Y<br>720 | Y<br>721 | Y<br>722 | Y<br>723 | ... | Y<br>860 | Y<br>861 | Y<br>862 | Y<br>863 | Y<br>0 | Y<br>1 |
|          |          | 0xFF     | 0x00     | 0x00     | EAV      |     | 0xFF     | 0x00     | 0x00     | SAV      |        |        |

Only Y signal with EAV/SAV

## RGB 24bit 525Line

|            |            |            |            |            |            |     |            |            |            |            |          |          |
|------------|------------|------------|------------|------------|------------|-----|------------|------------|------------|------------|----------|----------|
| RGB<br>718 | RGB<br>719 | RGB<br>720 | RGB<br>721 | RGB<br>722 | RGB<br>723 | ... | RGB<br>854 | RGB<br>855 | RGB<br>856 | RGB<br>857 | RGB<br>0 | RGB<br>1 |
|            |            | 0xFF       | 0x00       | 0x00       | EAV        |     | 0xFF       | 0x00       | 0x00       | SAV        |          |          |

All of RGB signal with EAV/SAV

## RGB 24bit 625Line

|            |            |            |            |            |            |     |            |            |            |            |          |          |
|------------|------------|------------|------------|------------|------------|-----|------------|------------|------------|------------|----------|----------|
| RGB<br>718 | RGB<br>719 | RGB<br>720 | RGB<br>721 | RGB<br>722 | RGB<br>723 | ... | RGB<br>860 | RGB<br>861 | RGB<br>862 | RGB<br>863 | RGB<br>0 | RGB<br>1 |
|            |            | 0xFF       | 0x00       | 0x00       | EAV        |     | 0xFF       | 0x00       | 0x00       | SAV        |          |          |

All of RGB signal with EAV/SAV

**[7.26.1.3] F-bit, V-bit**

Code relation between F-bit in EAV/SAV and line number.

| F-bit | 525i                           | 625i            | 525P/625P |
|-------|--------------------------------|-----------------|-----------|
| 0     | Line4~Line265                  | Line1~Line312   | F-bit = 0 |
| 1     | Line266~Line525<br>Line1~Line3 | Line313~Line625 |           |

Code relation between V-bit in EAV/SAV and line number.

Interlace

Sub Address: 0x05 [4]

| Name    | Setting                          | 525i                              |                                 | 625i                              |                                                    |
|---------|----------------------------------|-----------------------------------|---------------------------------|-----------------------------------|----------------------------------------------------|
|         |                                  | V-bit=0                           | V-bit=1                         | V-bit=0                           | V-bit=1                                            |
| TRSVSEL | [0]<br>BT. 656-3                 | Line10~Line263<br>Line273~Line525 | Line1~Line9<br>Line264~Line272  | Line23~Line310<br>Line336~Line623 | Line1~Line22<br>Line311~Line335<br>Line624~Line625 |
|         | [1]<br>BT. 656-4 or<br>SMPTE125M | Line20~Line263<br>Line283~Line525 | Line1~Line19<br>Line264~Line282 |                                   |                                                    |

Not affected by VBIL[2:0]-bit

Progressive

Sub Address: 0x05 [4]

| Name    | Setting                               | 525p           |              | 625p           |                                 |
|---------|---------------------------------------|----------------|--------------|----------------|---------------------------------|
|         |                                       | V-bit=0        | V-bit=1      | V-bit=0        | V-bit=1                         |
| TRSVSEL | [0]<br>SMPTE293M<br>or<br>EIA-770.2-A | Line43~Line525 | Line1~Line42 | Line45~Line620 | Line1~Line44<br>Line621~Line625 |
|         | [1]<br>EIA-770.2-C                    | Line46~Line525 | Line1~Line45 |                |                                 |

Not affected by VBIL[2:0]-bit

**[7.26.1.4] exclude EAV/SAV flag**

Sub Address: 0x09 [3]

| Name   | Definition                                                                    |
|--------|-------------------------------------------------------------------------------|
| EAVSAV | [0]: Output data with EAV/SAV flag.<br>[1]: Output data without EAV/SAV flag. |

If LIMIT601\* = [0], output code range are 0~255 (\*Sub Address: 0x05 [3])

**[7.26.1.5] Operating used EAV/SAV****[7.26.1.5.1] Line-locked and frame-locked clock modes**

In both of these modes, the output data are compliant with ITU-R BT.656 (525i/625i), SMPTE293M (525p), and ITU-R. BT1358 (625p), which requires the following samples and line numbers.

- Number of samples for 1 line:  
858 samples (525i/525) / 864 samples (625i/625p)
- Number of lines for 1 frame:  
525 lines / 625 lines

It may not be possible, however, to meet these requirements if the input signal quality is poor.

**[Line drop/repeat processing]**

A line drop or a line repeat will result in output signal with 524/624 or 526/626 lines per frame respectively.

Line drop/repeat processing may be performed at any line in the frame.

**[Pixel drop/repeat processing]**

A pixel drop or a pixel repeat will result in output signals less or more than the required 858/864 samples in the last line of the frame or field respectively.

Note: In the event of output-stage buffer failure, line drop/repeat processing will be performed even if the register is for pixel drop/ repeat processing.

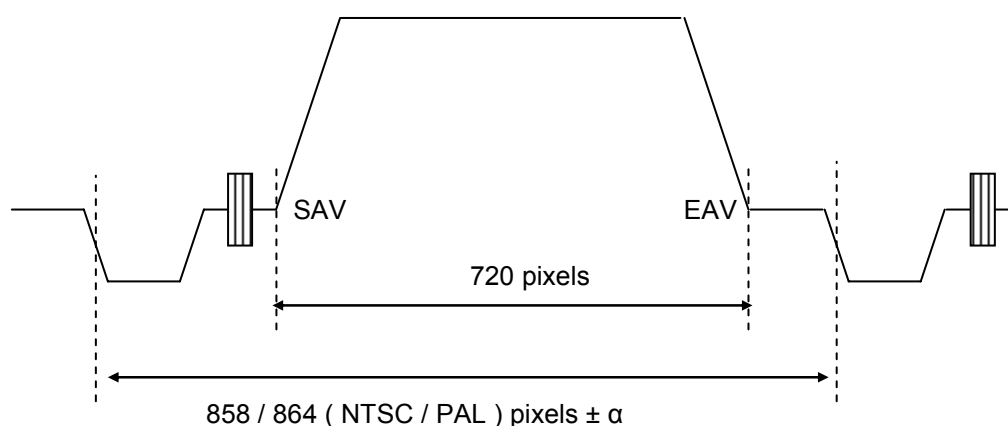
Line or pixel drop/repeat

Sub Address: 0x0D [5:4]

| ERRHND-bit | Processing mode                    | Notes   |
|------------|------------------------------------|---------|
| 00         | Line Drop / Line Repeat            | Default |
| 01         | Pixel Drop / Pixel Repeat by Field |         |
| 10         | Pixel Drop / Pixel Repeat by Frame |         |
| 11         | Reserved                           |         |

**[7.26.1.5.2] Fixed clock mode**

In fixed-clock mode, operation is at an internally generated 27 MHz clock, from a 24.576 MHz input clock. The output signal is therefore not synchronized with the input signal, and thus not ITU-R BT.656 compliant. Data is output in SAV format. As shown in the following figure, EAV is guaranteed for 720 pixels from SAV, but the number of pixels from EAV to SAV is not.



**[7.26.2] Interface used timing signal**

For connection with devices having no ITU-R BT.656 interface, the AK8858 DVALID signal output identifies the active video interval by remaining low throughout that period, as shown in the following figure.

In RGB output mode, it is suggest to use this interface when output the valid data

**[7.26.2.1] HD pin output**

AK8858 output HD signal for horizontal synchronization.

| Pin name | Interlace / Progressive | 525-Line                               | 625-Line                               |
|----------|-------------------------|----------------------------------------|----------------------------------------|
| HD       | Interlace               | Low for 4.7us at 15.734 kHz interval.  | Low for 4.7us at 15.625 kHz interval.  |
|          | Progressive             | Low for 2.35us at 31.468 kHz interval. | Low for 2.35us at 31.250 kHz interval. |

**[7.26.2.2] VD\_FLD or DVAL\_FLD pin output**

AK8858 output VD, FIELD and DVALID signal.

| Pin name | Interlace / Progressive | Output | 525-Line                                         | 625-Line                                         |
|----------|-------------------------|--------|--------------------------------------------------|--------------------------------------------------|
| VD_FLD   | Interlace               | VD     | Low output at Line4~Line6 or Line266.5~Line269.5 | Low output at Line1~Line3.5 or Line313.5~Line315 |
|          |                         | FIELD  | ODD-Field: Low, EVEN-Field: High                 |                                                  |
|          | Progressive             | VD     | Low output at Line7~Line12                       | Low output at Line1~Line5                        |
|          |                         | FIELD  | Toggle by each flame                             |                                                  |
| DVAL_FLD | Interlace               | DVALID | Low during active video interval                 |                                                  |
|          |                         | FIELD  | ODD-Field: Low, EVEN-Field: High                 |                                                  |
|          | Progressive             | DVALID | Low during active video interval                 |                                                  |
|          |                         | FIELD  | Toggle by each flame                             |                                                  |

Select output from VD\_FLD pin

Sub Address: 0x07 [5]

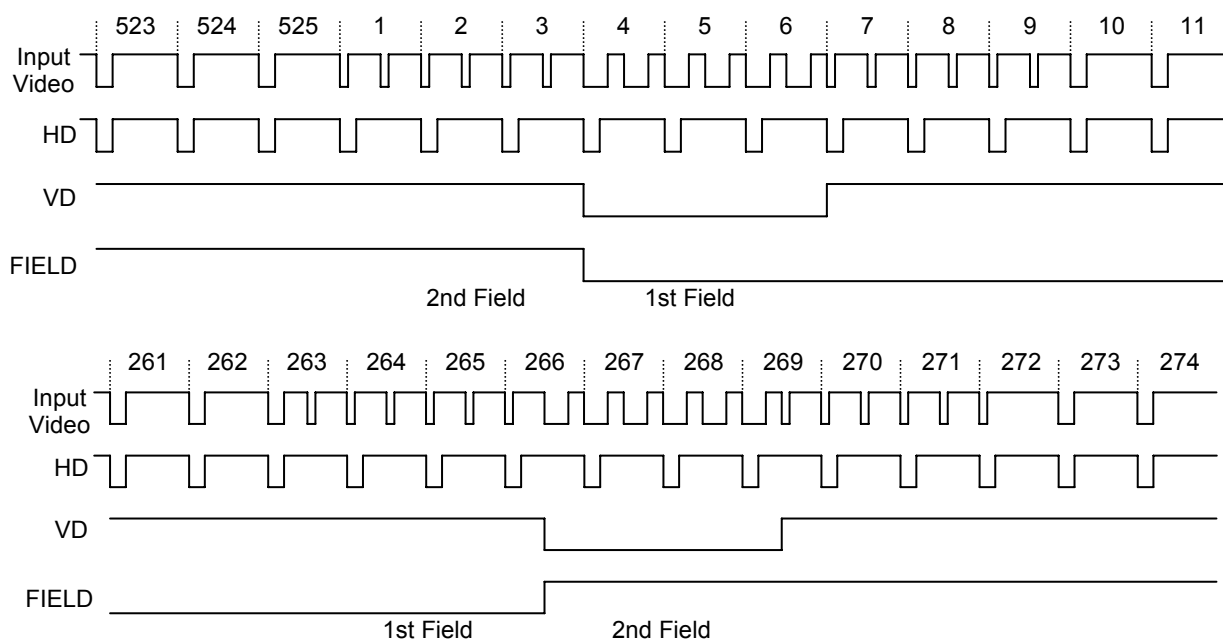
| Name   | Definition            | Notes |
|--------|-----------------------|-------|
| VDFSEL | [0]: VD<br>[1]: FIELD |       |

Select output from DVAL\_FLD pin

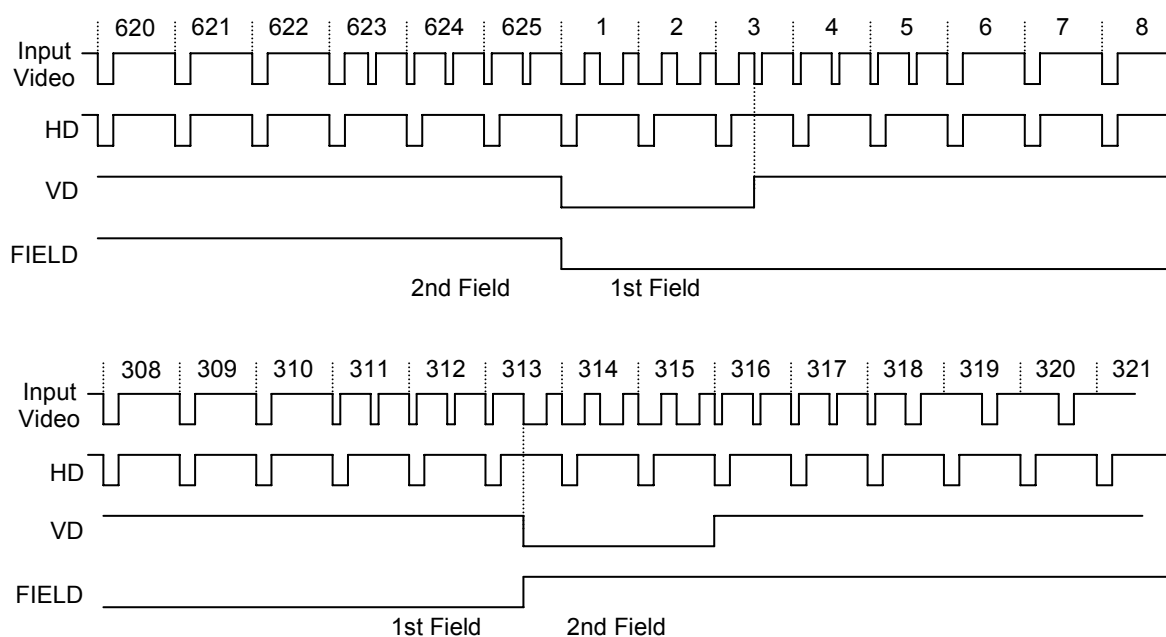
Sub Address: 0x07 [6]

| Name     | Definition                | Notes |
|----------|---------------------------|-------|
| DVALFSEL | [0]: DVALID<br>[1]: FIELD |       |



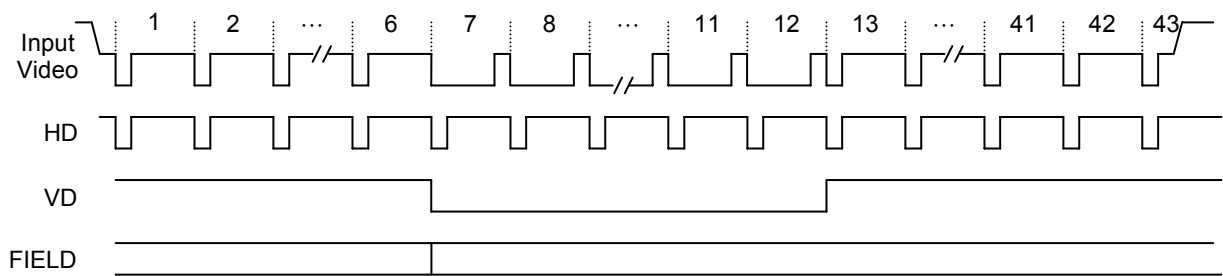
**[7.26.2.3] Position of HD, VD and FIELD****[7.26.2.3.1] 525Line Interlace**

If 262 or 263 line signal input, FIELD signal is toggled.

**[7.26.2.3.2] 625Line Interlace**

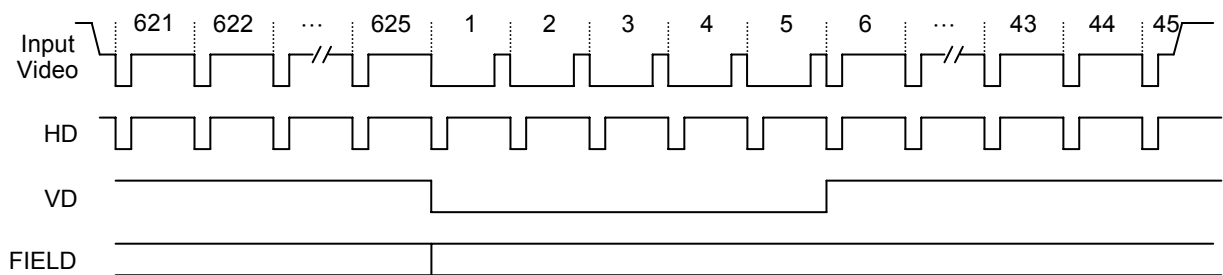
If 312 or 313 line signal input, FIELD signal is toggled.

**[7.26.2.3.3] 525Line Progressive**



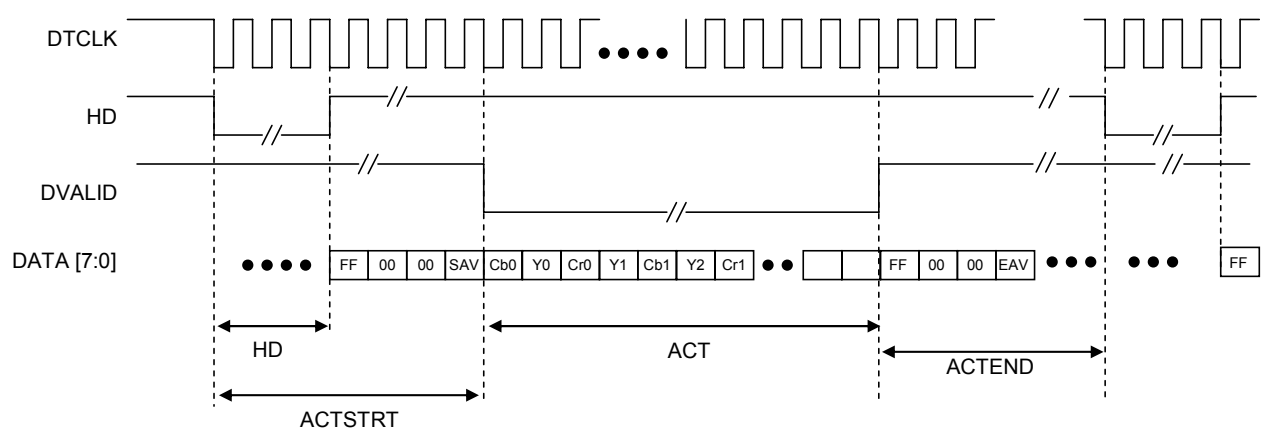
FIELD signal is toggled.

**[7.26.2.3.4] 625Line Progressive**



FIELD signal is toggled.

**[7.26.2.4] Position of HD, DVALID and EAV/SAV code**



| Input signal | bit         | HD (CLK) | ACTSTRT (CLK) | ACT (CLK) | ACTEND (CLK) | Notes             |
|--------------|-------------|----------|---------------|-----------|--------------|-------------------|
| 525Line      | YCbCr 8bit  | 128      | 244           | 1440      | 32           | 1CLK = DTCLK rate |
|              | YCbCr 16bit | 64       | 122           | 720       | 16           |                   |
|              | RGB 24bit   | 64       | 122           | 720       | 16           |                   |
| 625Line      | YCbCr 8bit  | 128      | 264           | 1440      | 24           |                   |
|              | YCbCr 16bit | 64       | 132           | 720       | 12           |                   |
|              | RGB 24bit   | 64       | 132           | 720       | 12           |                   |

**[7.26.2.5] Pin polarity**

Sub Address: 0x0B [7:5]

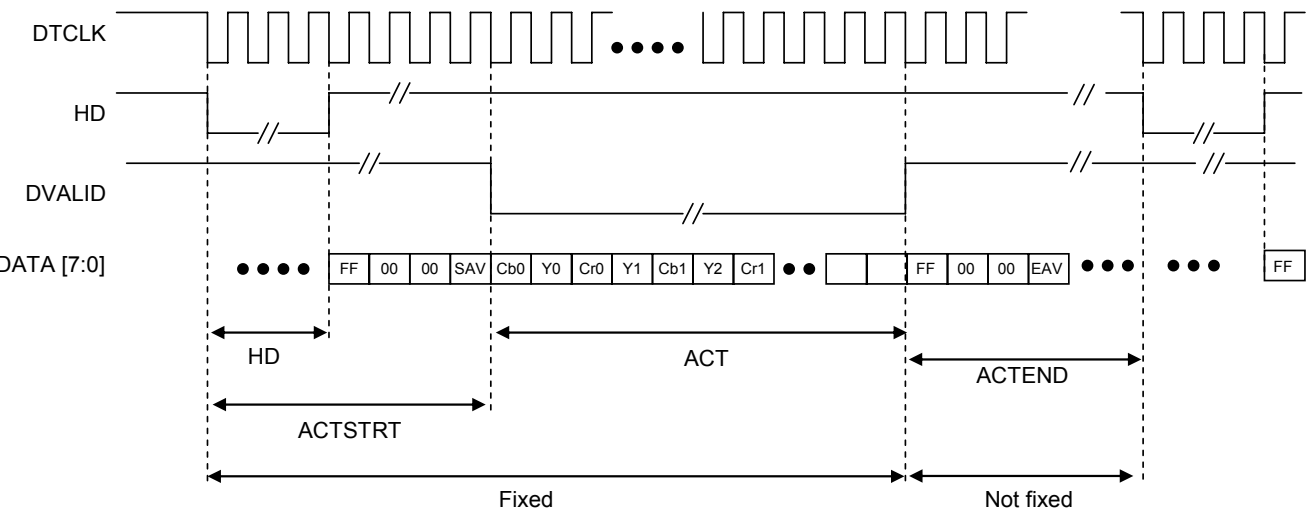
| Register Name | Pin name | Signal | Setting                            |                                    |
|---------------|----------|--------|------------------------------------|------------------------------------|
|               |          |        | [0]                                | [1]                                |
| HDP           | HD       | HD     | Active Low                         | Active High                        |
| VD_FP         | VD_FLD   | VD     | Active Low                         | Active High                        |
|               |          | Field  | Low: Odd-Field<br>High: Even-Field | Low: Even-Field<br>High: Odd-Field |
| DVAL_FP       | DVAL_FLD | DVALID | Active Low                         | Active High                        |
|               |          | Field  | Low: Odd-Field<br>High: Even-Field | Low: Even-Field<br>High: Odd-Field |

**DTCLK polarity**

Sub Address: 0x07 [7]

| Name   | Definition                                                                   |
|--------|------------------------------------------------------------------------------|
| CLKINV | [0]: Normal output ( rise edge to data)<br>[1]: Inverted( fall edge to data) |

**[7.26.2.6] Timing signal on fixed clock mode**



**[7.27] Sync separation, sync detection, black-level detection and digital pedestal clamp**

The AK8858 performs sync separation and sync detection on the digitized input signal, uses the detected sync signal as the timing reference for the decoding process, and calculates the phase error from the separated sync signal and applies it to control of the sampling clock.

The digitally converted input signal is clamped in the digital signal processing block. The internal clamp position depends on the input signal type (either 286 mV sync or 300 mV sync), but pedestal position is output as code 16 (8-Bit, ITU-R BT.601) for both types. The digital pedestal clamp function can adjust the time constant and set the coring level.

Black-level tuning can be performed in the sync separation block. The black-level fine-tuning band, which is 10 bits wide before REC 601 conversion, can be adjusted -8~+7 LSB in 1-LSB steps, with one step resulting in a change of about 0.4 LSB in the output code

Settings for digital pedestal clamp time constant

Sub Address: 0x10 [5:4]

| DPCT[1:0]-bit | Transition time constant | Notes                      |
|---------------|--------------------------|----------------------------|
| 00            | Fast                     |                            |
| 01            | Middle                   |                            |
| 10            | Slow                     |                            |
| 11            | Disable                  | Digital pedestal clamp OFF |

Settings for digital clamp pedestal coring level

Sub Address: 0x10 [7:6]

| DPCC[1:0]-bit | Transition time constant (bit) | Notes |
|---------------|--------------------------------|-------|
| 00            | ±1bit                          |       |
| 01            | ±2bit                          |       |
| 10            | ±3bit                          |       |
| 11            | Non-coring                     |       |

Settings for black-level fine tuning

Sub Address: 0x10 [3:0]

| BKLVL[3:0]-bit | Code adjustment of black level | Approx. change in 601 level (LSB) |
|----------------|--------------------------------|-----------------------------------|
| 0001           | +1                             | +0.4LSB                           |
| 0010           | +2                             | +0.8LSB                           |
| 0011           | +3                             | +1.2LSB                           |
| 0100           | +4                             | +1.6LSB                           |
| 0101           | +5                             | +2.0LSB                           |
| 0110           | +6                             | +2.4LSB                           |
| 0111           | +7                             | +2.8LSB                           |
| 0000           | Default                        | None                              |
| 1000           | -8                             | -3.2LSB                           |
| 1001           | -7                             | -2.8LSB                           |
| 1010           | -6                             | -2.4LSB                           |
| 1011           | -5                             | -2.0LSB                           |
| 1100           | -4                             | -1.6LSB                           |
| 1101           | -3                             | -1.2LSB                           |
| 1110           | -2                             | -0.8LSB                           |
| 1111           | -1                             | -0.4LSB                           |

The black level is adjusted upward or downward by the value of the setting, which must be in 2's-complement form. Black-level adjustment is also enabled during the vertical blanking interval.

**[7.28] Color killer**

In CVBS or S-video input, the chroma signal quality of the input signal is determined by comparison of its color burst level against the threshold setting in the color killer control register. If the level is below the threshold, the color killer is activated, resulting in processing of the input as a monochrome signal and thus with CbCr data fixed at 0x80. Depending on the register setting, the color killer may also be activated by failure of the color decode PLL lock.

Settings for color killer ON and OFF

Sub Address: 0x11 [7]

| COLKILL-bit |         | Notes |
|-------------|---------|-------|
| 0           | Enable  |       |
| 1           | Disable |       |

Settings for color killer activation

Sub Address: 0x11 [6]

| CKILSEL-bit | Condition for activation                                                                       | Notes |
|-------------|------------------------------------------------------------------------------------------------|-------|
| 0           | Burst level below threshold setting in CKLVL[3:0]-bits                                         |       |
| 1           | Burst level below threshold setting in CKLVL[3:0]-bits, or<br>Failure of color decode PLL lock |       |

For threshold setting

Sub Address: 0x11 [3:0]

| Name                  | Definition                                                                                                                                                                                                                                                                                                                                   |
|-----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CKLVL0<br>~<br>CKLVL3 | [CKLVL3 : CKLVL0 ]<br>[0000]: -29.7dB<br>[0001]: -28.4dB<br>[0010]: -27.2dB<br>[0011]: -26.2dB<br>[0100]: -25.3dB<br>[0101]: -24.5dB<br>[0110]: -23.7dB<br>[0111]: -23.0dB<br>[1000]: -22.4dB (Default)<br>[1001]: -21.8dB<br>[1010]: -21.2dB<br>[1011]: -20.7dB<br>[1100]: -20.2dB<br>[1101]: -19.7dB<br>[1110]: -19.3dB<br>[1111]: -18.9dB |

Used for threshold setting with SECAM input.

Sub Address: 0x11 [5:4]

| Name                  | Definition                                                                                                                                |
|-----------------------|-------------------------------------------------------------------------------------------------------------------------------------------|
| CKSCM0<br>~<br>CKSCM1 | [CKSCM1 : CKSCM0 ]<br>[00]: {CKLVL[3:0]}<br>[01]: {0, CKLVL[3:1]} (1bit shift)<br>[10]: {0, 0, CKLVL[3:2]} (2bit shift)<br>[11]: Reserved |

**[7.29] Image quality adjustment**

Image quality adjustments consist of contrast, brightness, color saturation, and hue adjustment.

**[7.29.1] Contrast adjustment**

Setting for contrast adjustment inclination

Sub Address: 0x12 [7:0]

| Register            | Definition                                                                                                                                |
|---------------------|-------------------------------------------------------------------------------------------------------------------------------------------|
| CONT0<br>~<br>CONT7 | [CONTSEL-bit =[0]*]<br>$YOUT = (CONT / 128) \times (YIN - 128) + 128$                                                                     |
|                     | [CONTSEL-bit =[1]*]<br>$YOUT = (CONT / 128) \times YIN$                                                                                   |
|                     | YOUT: Contrast obtained by the calculation<br>YIN: Contrast before the calculation<br>CONT: Contrast gain factor (register setting value) |
|                     | The gain factor can be set in the range {0~ (255 / 128)} in 1/128 step.<br>Default setting value is 0x80.                                 |

As the register setting shown in the above table, contrast adjustment inclination can be selected between 50% and 0%.

Setting for contrast adjustment inclination

Sub Address: 0x0D [7]

| Register | Definition          |
|----------|---------------------|
| CONTSEL  | [0]: 50%<br>[1]: 0% |

**[7.29.2] Brightness adjustment**

Setting for brightness adjustment

Sub Address: 0x13 [7:0]

| Name            | Definition                                                                                                                                    |
|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| BR0<br>~<br>BR7 | $YOUT = YIN + BR$                                                                                                                             |
|                 | YOUT: Brightness obtained by the calculation<br>YIN: Brightness before the calculation<br>BR: Brightness gain factor (register setting value) |
|                 | The gain factor can be set in the range {-128 ~ 127} in 1 step.<br>The setting is in 2's complement.                                          |
|                 |                                                                                                                                               |

Settings for brightness and contrast adjustment status (ON/OFF) during VBI

Sub Address: 0x14 [7]

| Register  | Status during VBI           |
|-----------|-----------------------------|
| VBIIMGCTL | [0]: Disable<br>[1]: Enable |

**[7.29.3] Color saturation adjustment**

In composite (CVBS) or S-Video signals mode, saturation adjustment involves multiplication of the color signal by the gain factor setting in this register. The calculated result is U/V demodulated.

In YPbPr mode, U and V value can be adjusted individually.

Sub Address: 0x15 [7:0]

| Name              |                       | Definition                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------------------|-----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SAT0<br>~<br>SAT7 | UTONE0<br>~<br>UTONE7 | <p>[composite (CVBS) or S-Video signals]<br/> <math>COUT = (SAT / 128) \times CIN</math><br/>           COUT: C signal after calculation<br/>           CIN: C signal before calculation<br/>           SAT: Satulation factor (register setting value)</p> <p>[Component video signal]<br/> <math>UOUT = (UTONE / 128) \times UIN</math><br/>           UOUT: U signal after calculation<br/>           UIN: U signal before calculation<br/>           UTONE: Satulation factor (register setting value)</p> <p>The gain factor can be set in the range 0 to 255/128, in steps of 1/128.<br/>           The default value is 0x80.</p> |

Sub Address: 0x16 [7:0]

| Name                  |  | Definition                                                                                                                                                                                                                                                                                                                                                                   |
|-----------------------|--|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VTONE0<br>~<br>VTONE7 |  | <p>[Component video signal]<br/> <math>VOUT = (VTONE / 128) \times VIN</math><br/>           VOUT: V signal after calculation<br/>           VIN: V signal before calculation<br/>           VTONE: Satulation factor (register setting value)</p> <p>The gain factor can be set in the range 0 to 255/128, in steps of 1/128.<br/>           The default value is 0x80.</p> |

(Notice)

If component mode, UTONE and VTONE default value should be changed to following parameter.

UTONE [7:0] =0x70

VTONE [7:0] =0x9D

**[7.29.4] HUE adjustment**

Setting for HUE adjustment

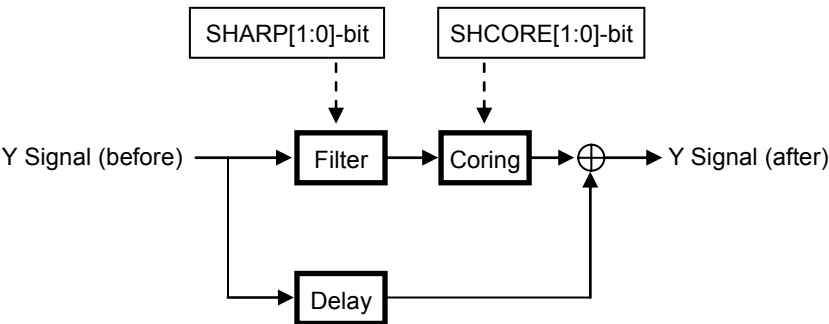
Sub Address: 0x17 [7:0]

| Name               | Definition                                                                                                                                                     |
|--------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| HUE0<br>~<br>HUE 7 | <p>The phase rotation can be set in the range of <math>\pm 45^\circ</math> in 1/256step (about 0.35step).<br/>           The setting is in 2's complement.</p> |

HUE adjustment only valid for composite (CVBS) and S-Video signals input.

[7.29.5] Sharpness adjustment

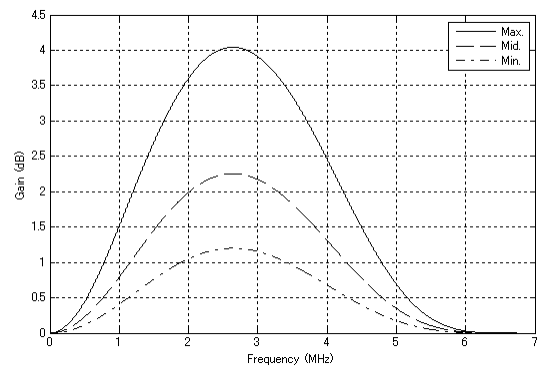
Sharpness adjustment is performed on the luminance signal. The filter characteristic is shown in the following diagram. A sharp image can be obtained by selection of the filter with the appropriate characteristics.



Settings for filter characteristics selection

Sub Address: 0x14 [1:0]

| SHARP[1:0]-bit | Filter characteristics | Notes           |
|----------------|------------------------|-----------------|
| 00             | No filtering           | Filter disabled |
| 01             | Min                    |                 |
| 10             | Middle                 |                 |
| 11             | Max                    |                 |



Settings for coring level after sharpness filtering

Sub Address: 0x14 [3:2]

| SHCORE[1:0]-bit | Coring level (LSB) | Notes                                   |
|-----------------|--------------------|-----------------------------------------|
| [00]            | No coring          | Settings apply only to filtered signal. |
| [01]            | ±1LSB              |                                         |
| [10]            | ±2LSB              |                                         |
| [11]            | ±3LSB              |                                         |

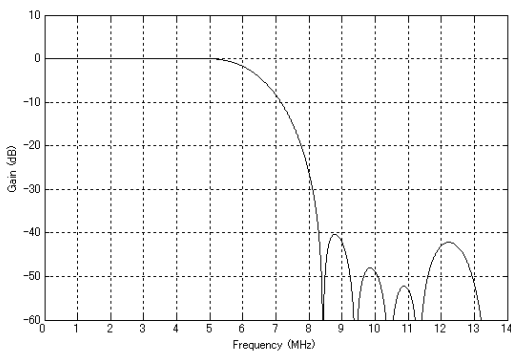


### [7.29.6] Luminance bandwidth adjustment

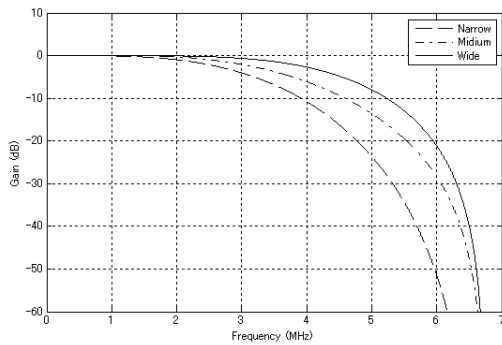
Luminance bandwidth adjustment can be performed for MPEG compression etc. The band-limiting filters for pre-compression limiting can be selected by the following register settings. Without these filters, the frequency response of the luminance signal is determined by the decimation filter.

Settings for luminance bandwidth filter Sub Address: 0x14 [5:4]

| LUMFIL [1:0]-bit | Filter characteristic           | Notes                                               |
|------------------|---------------------------------|-----------------------------------------------------|
| 00               | No filter<br>No bandwidth limit | Decimation filter characteristic<br>-3dB at 6.29MHz |
| 01               | Narrow                          | -3dB at 2.94MHz                                     |
| 10               | Mid                             | -3dB at 3.30MHz                                     |
| 11               | Wide                            | -3dB at 4.00MHz                                     |



Luminance signal decimation filter



Luminance bandwidth filter

For 525/626p input signal, the bandwidth for each filter characteristic is expands about 2 times.

### [7.29.7] Sepia output

Sepia-colored output of the decoded signal can be obtained by the following register setting.

Settings for sepia output of decoded signal Sub Address: 0x14 [6]

| SEPIA -bit | Output        | Notes |
|------------|---------------|-------|
| [0]        | Normal output |       |
| [1]        | Sepia output  |       |

**[7.29.8] U/ V Filter**

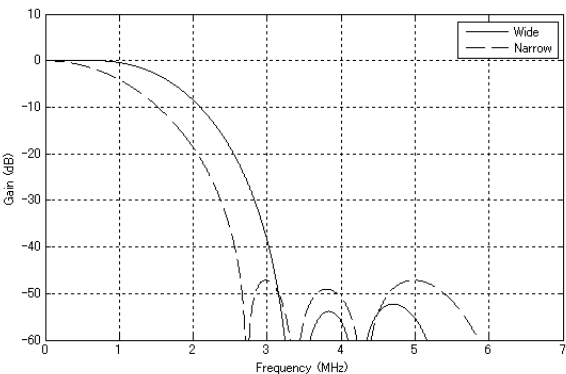
U/V signal bandwidth can be set via register

[Composite (CVBS) and S-Video signal input]

Setting for U/ V filter characteristic

Sub Address: 0x0C [2]

| UVFILSEL0-bit | U/V filter bandwidth | Notes |
|---------------|----------------------|-------|
| 0             | Wide                 |       |
| 1             | Narrow               |       |

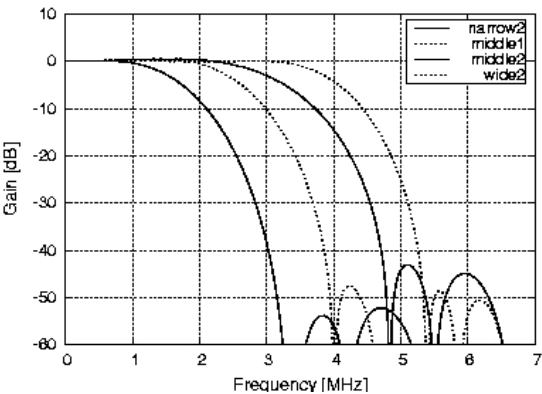


[YPbPr signal input]

Setting for U/ V filter characteristic

Sub Address: 0x0C [3:2]

| UVFILSEL[1:0] -bit | U/V filter bandwidth | Range                                   |
|--------------------|----------------------|-----------------------------------------|
| 00                 | Middle 1             | Narrow 2 < Middle 1 < Middle 2 < Wide 2 |
| 01                 | Middle 2             |                                         |
| 10                 | Wide 2               |                                         |
| 11                 | Narrow 2             |                                         |



For 525/626p input signal, the bandwidth for each filter characteristic is expands about 2 times.

**[7.30] VBI information decoding**

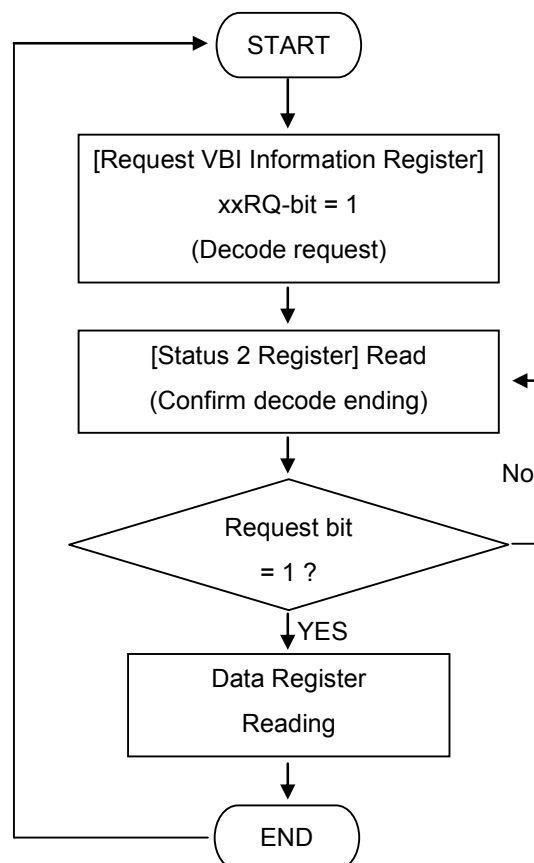
The AK8858 decodes closed-caption, closed-caption-extended, VBI(CGMS), and WSS signals on the vertical blanking signal, and writes the decoded data into a storage register. The AK8858 reads each data bit in Request VBI Information register (Sub Address 0x1A [3:0]) as a decoding request and thereupon enters a data wait state. Data detection and decoding to the storage register are then performed which indicates the presence or absence of data at STATUS 2 register (Sub Address 0x23 [3:0]) for host. The host can therefore determine the stored values by reading the respective storage registers. The value in each storage register is retained until a new value is written in by data renewal. For VBI data (CGMS-A), the CRCC code is decoded and only the arithmetic result is stored in the register.

| Signal                       | Line Number                            | Notes                |
|------------------------------|----------------------------------------|----------------------|
| Closed Caption               | Line21                                 | 525i                 |
| Closed Caption Extended Data | Line284                                | 525i                 |
| VBID                         | Line20 / 283<br>Line20 / 333<br>Line41 | 525i<br>625i<br>525p |
| WSS                          | Line23<br>Line43                       | 625i<br>625p         |

Following are store registers. (Sub Address: 0x26 ~ 0x2D)

Closed Caption 1 Register, Closed Caption 2 Register, WSS 1 Register, WSS 2 Register, Extended Data 1 Register, Extended Data 2 Register, VBI 1 Register and VBI 2 Register

Reading data flow chart



**[7.31] Internal status indicators Register****[7.31.1] No signal detect**

Indicates presence or absence of signal

Sub Address: 0x22 [0]

| Name  | Setting | Definition         | Notes |
|-------|---------|--------------------|-------|
| NOSIG | [0]     | Signal detected    |       |
|       | [1]     | No signal detected |       |

**[7.31.2] VLOCK status**

Indicates status of VLOCK

Sub Address: 0x22 [1]

| Name  | Setting | Definition       | Notes |
|-------|---------|------------------|-------|
| VLOCK | [0]     | Synchronized     |       |
|       | [1]     | Not synchronized |       |

**[7.31.3] Interlace Status**

Indicate interlace or not of input video signal

Sub Address: 0x22 [2]

| Name   | Setting | Definition            | Notes |
|--------|---------|-----------------------|-------|
| FRMSTD | [0]     | 525/625 interlace     |       |
|        | [1]     | not 525/625 interlace |       |

**[7.31.4] Status of color killer operation**

Indicates status of color killer

Sub Address: 0x22 [3]

| Name     | Setting | Definition                 | Notes |
|----------|---------|----------------------------|-------|
| COLKILON | [0]     | Not color killer operation |       |
|          | [1]     | Color killer operation     |       |

**[7.31.5] Status of clock mode**

Indicates status of clock modeko

Sub Address: 0x22 [5:4]

| Name                        | Setting | Definition                   | Notes |
|-----------------------------|---------|------------------------------|-------|
| SCLKMODE0<br>~<br>SCLKMODE1 | [00]    | Fixed clock operation        |       |
|                             | [01]    | Line lock clocked operation  |       |
|                             | [10]    | Frame lock clocked operation |       |
|                             | [11]    | Reserved                     |       |

**[7.31.6] Luminance over flow**

Indicates status of luminance decode result after passage through AGC block

Sub Address: 0x22 [6]

| Name    | Setting | Definition | Notes |
|---------|---------|------------|-------|
| PKWHITE | [0]     | Normal     |       |
|         | [1]     | Overflow   |       |

**[7.31.7] Chrominance over flow**

Indicates status of color decode result after passage through ACC block

Sub Address: 0x22 [7]

| Name  | Setting | Definition | Notes |
|-------|---------|------------|-------|
| OVCOL | [0]     | Normal     |       |
|       | [1]     | Overflow   |       |

**[7.31.8] Field status**

Indicates decoding signal field status

Sub Address: 0x23 [4]

| Name    | Setting | Definition | Notes |
|---------|---------|------------|-------|
| REALFLD | [0]     | EVEN field |       |
|         | [1]     | ODD field  |       |

**[7.31.9] AGC status**

Indicates status of adaptive AGC

Sub Address: 0x23 [5]

| Name   | Setting | Definition         | Notes |
|--------|---------|--------------------|-------|
| AGCSTS | [0]     | Sync AGC operation |       |
|        | [1]     | Peak AGC operation |       |

**[7.32] Macrovision signal detection**

The AK8858 can detect a decode signal contains Macrovision signal.

The detection result can be confirmed via register.

Indicate signal contains Macrovision signal

Sub Address: 0x24 [2:0]

| Name   | Definition                                                                       |
|--------|----------------------------------------------------------------------------------|
| AGCDET | 0: No Macrovision AGC process detected<br>1: Macrovision AGC process detected    |
| CSDET  | 0: No Color Stripe Process detected<br>1: Color Stripe Process detected          |
| CSTYPE | 0: Color Stripe Type 2 in input signal<br>1: Color Stripe Type 3 in input signal |

If detect macrovision signal on progressive decoding, AGCDET-bit = [1].

**[7.32.1] Macrovision Color Stripe Cancel**

This function is cancellor for macrovision color stripe.

Set CSCAN bit to [1] only when Sub=Address 0x04[7:0] is [XXX00000] setting.

Set CSCAN bit to [0] when Sub=Address 0x04[7:0] is not [XXX00000] setting.

(X: Don't care)

Color stripe cancel

Sub Address: 0x03 [6]

| Name  | Definition                                                                                                                            |
|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| CSCAN | Set to [1] only when Sub=Address 0x04[7:0] is [XXX00000] setting.<br>Set to [0] when Sub=Address 0x04[7:0] is not [XXX00000] setting. |

**[7.33] Auto detection result of input video signal**

In auto detection mode, the result can be acknowledged by reading the following register.

Indicates result and status of auto detection mode

Sub Address: 0x25 [7:0]

| Name                      | Definition                                                                                                                                                                                                                                                                                                                                                                                                                         |
|---------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ST_VSCF0<br>~<br>ST_VSCF1 | (CVBS or S-video signal decoding)<br>Input video signal subcarrier frequency indicator<br>[ ST_VSCF1 : ST_VSCF0 ] ( MHz )<br>[00]: 3.57954545 (NTSC-M,J)<br>[01]: 3.57561149 (PAL-M)<br>[10]: 3.58205625 (PAL-Nc)<br>[11]: 4.43361875 (PAL-B,D,G,H,I,N,60 , NTSC-4.43, SECAM)<br><br>(Component signal decoding)<br>Interlace or Progressive indicator<br>[00]: Interlace<br>[01]: Progressive<br>[10]: Reserved<br>[11]: Reserved |
| ST_VCEN0<br>~<br>ST_VCEN1 | Input signal color encode format indicator<br>[ST_VCEN1 : ST_VCEN0]<br>[00]: NTSC<br>[01]: PAL<br>[10]: SECAM<br>[11]: Component setting*                                                                                                                                                                                                                                                                                          |
| ST_VLF                    | Input signal line number indicator<br>[0]: 525-Line (NTSC-M,J , NTSC-4.43 , PAL-M,60)<br>[1]: 625-Line (PAL-B,D,G,H,I,N,Nc , SECAM)                                                                                                                                                                                                                                                                                                |
| ST_BW                     | Input signal monochrome indicator*<br>[0]: Not monochrome<br>[1]: Monochrome                                                                                                                                                                                                                                                                                                                                                       |
| UNDEF                     | Input signal detection indicator<br>[0]: Input signal detected<br>[1]: Input signal not detected                                                                                                                                                                                                                                                                                                                                   |
| FIXED                     | Input signal detection process status<br>[0]: Detection process in progress<br>[1]: Detection process completed                                                                                                                                                                                                                                                                                                                    |

\*Monochrome auto detection is enabled if the color killer setting is ON (COLKILL-bit = [1]).

\* ST\_VCEN[1:0] is [11] when Sub-Address 0x00[6:5] is set to [10] (Component video input).

## [8] Device control interface

The AK8858 is controlled via I2C bus control interface, as described below.

### [8.1] I2C bus SLAVE Address

|                 | Slave Address |   |   |   |   |   |   |     |
|-----------------|---------------|---|---|---|---|---|---|-----|
| SELA pin status | MSB           |   |   |   |   |   |   | LSB |
| Pulldown [Low]  | 1             | 0 | 0 | 0 | 1 | 0 | 0 | R/W |
| Pullup [High]   | 1             | 0 | 0 | 0 | 1 | 0 | 1 | R/W |

### [8.2] I2C control sequence

#### [8.2.1] Write sequence

After receiving a write-mode slave address first byte, the AK8858 receives the sub-address in the second byte and data in the subsequent bytes. The write sequence may be single-byte or multi-byte.

(a) Single-byte write sequence

|   |               |   |       |             |       |       |       |     |
|---|---------------|---|-------|-------------|-------|-------|-------|-----|
| S | Slave Address | w | A     | Sub Address | A     | Data  | A     | Stp |
|   | 8-bit         |   | 1-bit | 8-bit       | 1-bit | 8-bit | 1-bit |     |

(b) Multi-byte writes sequence (Sequential Write Operation)

|   |               |   |       |                |       |         |       |            |       |       |            |       |     |
|---|---------------|---|-------|----------------|-------|---------|-------|------------|-------|-------|------------|-------|-----|
| S | Slave Address | w | A     | Sub Address(n) | A     | Data(n) | A     | Data (n+1) | A     | ..... | Data (n+m) | A     | stp |
|   | 8-bit         |   | 1-bit | 8-bit          | 1-bit | 8-bit   | 1-bit | 8-bit      | 1-bit |       | 8-bit      | 1-bit |     |

#### [8.2.2] Read sequence

After receiving a read-mode slave address as first byte, the AK8858 sends data in the second and subsequent bytes.

|   |               |   |   |                |   |    |               |   |   |       |   |       |   |       |   |       |
|---|---------------|---|---|----------------|---|----|---------------|---|---|-------|---|-------|---|-------|---|-------|
| S | Slave Address | w | A | Sub Address(n) | A | rS | Slave Address | R | A | Data1 | A | Data2 | A | Data3 | A | ..... |
|   | 8-bit         |   | 1 | 8-bit          | 1 |    | 8-bit         |   | 1 | 8-bit | 1 | 8-bit | 1 | 8-bit | 1 |       |

|       |        |    |     |
|-------|--------|----|-----|
| ..... | Data n | !A | stp |
|       | 8-bit  | 1  |     |

S : Start Condition

rS : repeated Start Condition

A : Acknowledge (SDA Low )

!A : Not Acknowledge (SDA High)

stp : Stop Condition

R/W 1 : Read 0 : Write

: Received from master device (normally microprocessor)

: Output by slave device (AK8858)

**[9] Register Definitions**

| Sub-Address       | Register                            | Default | R/W | Function                            |
|-------------------|-------------------------------------|---------|-----|-------------------------------------|
| 0x00              | Input Channel Select Register       | 0x00    | R/W | Input channel setting               |
| 0x01              | Clamp Control 1                     | 0x00    | R/W | Clamp pulse setting register 1      |
| 0x02              | Clamp Control 2                     | 0x01    | R/W | Clamp pulse setting register 2      |
| 0x03              | Miscellaneous Setting               | 0x00    | R/W |                                     |
| 0x04              | Input Video Standard                | 0x00    | R/W | Input video signal setting          |
| 0x05              | Output Format                       | 0x00    | R/W | Output format setting               |
| 0x06              | NDMODE                              | 0x00    | R/W | Auto detection limit setting        |
| 0x07              | Output Control                      | 0x00    | R/W | Output pin status setting           |
| 0x08              | Output Data Start and Delay Control | 0x00    | R/W | Output data timing setting          |
| 0x09              | Output Data Format (YUV/RGB)        | 0x00    | R/W | Output data format setting          |
| 0x0A              | AGC & ACC Control                   | 0x00    | R/W | AGC and ACC setting                 |
| 0x0B              | Control 0                           | 0x00    | R/W | Control register type               |
| 0x0C              | Control 1                           | 0x00    | R/W | Control register type               |
| 0x0D              | Control 2                           | 0x00    | R/W | Control register type               |
| 0x0E              | PGA1 Control                        | 0x54    | R/W | PGA1 gain setting                   |
| 0x0F              | PGA2 Control                        | 0x54    | R/W | PGA2 gain setting                   |
| 0x10              | Pedestal Level Control              | 0x00    | R/W | Pedestal level adjustment           |
| 0x11              | Color Killer Control                | 0x08    | R/W | Color killer setting                |
| 0x12              | Contrast Control                    | 0x80    | R/W | Contrast adjustment                 |
| 0x13              | Brightness Control                  | 0x00    | R/W | Brightness adjustment               |
| 0x14              | Image Control                       | 0x00    | R/W | Image control setting               |
| 0x15              | Saturation / U Tone Control         | 0x80    | R/W | Saturation (Y) / Color (U) control  |
| 0x16              | V Tone Control                      | 0x80    | R/W | Color (V) control                   |
| 0x17              | HUE Control                         | 0x00    | R/W | Hue adjustment                      |
| 0x18              | High Slice Data Set                 | 0xEB    | R/W | VBI Slice Data High setting         |
| 0x19              | Low Slice Data Set                  | 0x10    | R/W | VBI Slice Data Low setting          |
| 0x1A              | Request VBI Information             | 0x00    | R/W | VBI interval decode request setting |
| 0x1B<br>~<br>0x21 | Reserved                            | 0x00    | —   | Reserved register                   |
| 0x22              | Status 1 Register                   |         | R   | Internal status indicator           |
| 0x23              | Status 2 Register                   |         | R   | Internal status indicator           |
| 0x24              | Macrovision Status Register         |         | R   | Input Macrovision signal indicator  |
| 0x25              | Input Video Status Register         |         | R   | Input signal detection indicator    |
| 0x26              | Closed Caption 1 Register           |         | R   | Closed caption data indicator       |
| 0x27              | Closed Caption 2 Register           |         | R   | Closed caption data indicator       |
| 0x28              | WSS 1 Register                      |         | R   | WSS data indicator                  |
| 0x29              | WSS 2 Register                      |         | R   | WSS data indicator                  |
| 0x2A              | Extended Data 1 Register            |         | R   | CC-Extended data indicator          |
| 0x2B              | Extended Data 2 Register            |         | R   | CC-Extended data indicator          |
| 0x2C              | VBID 1 Register                     |         | R   | VBID data indicator                 |
| 0x2D              | VBID 2 Register                     |         | R   | VBID data indicator                 |
| 0x2E              | Device and Revision ID              | 0x3A    | R   | Device ID / Revision ID             |
| 0x2F<br>~<br>0x3F | Reserved                            | 0x00    | —   | Reserved register                   |

For all other registers, write-in is prohibited.

For all reserved registers, write-in must be limited to the default value.



**[9.1] Register setting overview****[9.1.1] Input Channel Select Register (R/W) [Sub Address 0x00]**

Input signal channel selection and clock mode selection register.

Sub Address: 0x00

Default Value: 0x00

| bit 7         | bit 6   | bit 5   | bit 4   | bit 3   | bit 2    | bit 1    | bit 0    |
|---------------|---------|---------|---------|---------|----------|----------|----------|
| CLKMOD        | SELSRC1 | SELSRC0 | ADC3SEL | ADC2SEL | ADC1SEL2 | ADC1SEL1 | ADC1SEL0 |
| Default Value |         |         |         |         |          |          |          |
| 0             | 0       | 0       | 0       | 0       | 0        | 0        | 0        |

## Input Channel Select Register

| BIT                 | Register Name             |               | R/W | Definition                                                                                                                                 |
|---------------------|---------------------------|---------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------|
| bit 0<br>~<br>bit 2 | ADC1SEL0<br>~<br>ADC1SEL2 | ADC 1 Select  | R/W | ADC1 input signal selection<br>000: AIN1<br>001: AIN2<br>010: AIN3<br>011: AIN4<br>100: AIN5<br>101: AIN6                                  |
| bit 3               | ADC2SEL                   | ADC 2 Select  | R/W | Virtual ADC2 input signal selection<br>0: AIN7<br>1: AIN8                                                                                  |
| bit 4               | ADC3SEL                   | ADC 3 Select  | R/W | Virtual ADC3 input signal selection<br>0: AIN9<br>1: AIN10                                                                                 |
| bit 5<br>~<br>bit 6 | SELSRC0<br>~<br>SELSRC1   | Select Source | R/C | Decode signal selection<br>00: Composite (CVBS)<br>01: S-Video<br>10: Component (YPbPr)<br>11: No input signal (Analog block is powerdown) |
| bit 7               | CLKMOD                    | Clock Mode    | R/W | Clock mode selection<br>0: For crystal<br>1: External clock input (clock generator etc.)                                                   |

**[9.1.2] Clamp Control 1 Register (R/W) [Sub Address 0x01]**

Clamp pulse setting.

Sub Address: 0x01

Default Value: 0x00

| bit 7         | bit 6      | bit 5     | bit 4     | bit 3    | bit 2      | bit 1      | bit 0      |
|---------------|------------|-----------|-----------|----------|------------|------------|------------|
| CLP-WIDTH1    | CLP-WIDTH0 | CLP-STAT1 | CLP-STAT0 | Reserved | BCLP-STAT2 | BCLP-STAT1 | BCLP-STAT0 |
| Default Value |            |           |           |          |            |            |            |
| 0             | 0          | 0         | 0         | 0        | 0          | 0          | 0          |

**Clamp Control 1 Register**

| BIT                 | Register Name               |                           | R/W | Definition                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|---------------------|-----------------------------|---------------------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| bit 0<br>~<br>bit 2 | BCLPSTAT0<br>~<br>BCLPSTAT2 | Back Porch<br>Clamp Start | R/W | Backporch clamp start position setting.<br>The default position is at the center of Sync signal.<br>[ BCLPSTAT2 : BCLPSTAT0 ]<br>[000]: Same position as default "CLPSTAT"<br>[001]: (1/128)H delay from "CLPSTAT"<br>[010]: (2/128)H delay from "CLPSTAT"<br>[011]: (3/128)H delay from "CLPSTAT"<br>[100]: (4/128)H advance from "CLPSTAT"<br>[101]: (3/128)H advance from "CLPSTAT"<br>[110]: (2/128)H advance from "CLPSTAT"<br>[111]: (1/128)H advance from "CLPSTAT" |
| bit 3               | Reserved                    | Reserved                  | R/W | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| bit 4<br>~<br>bit 5 | CLPSTAT0<br>~<br>CLPSTAT1   | Clamp Start               | R/W | Clamp pulse start position setting.<br>The default position is at the center of horizontal Sync signal.<br>[ CLPSTAT1 : CLPSTAT0 ]<br>[00]: Center of horizontal sync (default position)<br>[01]: (1/128)H delay<br>[10]: (2/128)H advance<br>[11]: (1/128)H advance                                                                                                                                                                                                       |
| bit 6<br>~<br>bit 7 | CLPWIDTH0<br>~<br>CLPWIDTH1 | Clamp Pulse<br>Width      | R/W | Clamp pulse width setting.<br>Pulse width is change according to sampling clock units.<br>[ CLPWIDTH1 : CLPWIDTH0 ]<br>[00]: 7-clk<br>[01]: 15-clk<br>[10]: 31-clk<br>[11]: 63-clk                                                                                                                                                                                                                                                                                         |

**[9.1.3] Clamp Control 2 Register (R/W) [Sub Address 0x02]**

Clamp pulse control setting.

Sub Address: 0x02

Default Value: 0x01

| bit 7         | bit 6    | bit 5    | bit 4   | bit 3 | bit 2 | bit 1 | bit 0 |
|---------------|----------|----------|---------|-------|-------|-------|-------|
| Reserved      | Reserved | Reserved | YPBPRCP | UDG1  | UDG0  | CLPG1 | CLPG0 |
| Default Value |          |          |         |       |       |       |       |
| 0             | 0        | 0        | 0       | 0     | 0     | 0     | 1     |

## Clamp Control 2 Register

| BIT                 | Register Name       |              | R/W | Definition                                                                                                                                |
|---------------------|---------------------|--------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------|
| bit 0<br>~<br>bit 1 | CLPG0<br>~<br>CLPG1 | Clamp Gain   | R/W | Current value of fine clamp in analog circuit setting<br>CLPG[1:0]<br>00: Min<br>01: Middle 1 (default)<br>10: Middle 2<br>11: Max        |
| bit 2<br>~<br>bit 3 | UDG0<br>~<br>UDG1   | Up Down Gain | R/W | Current value of rough clamp in analog circuit setting<br>[ UDG1 : UDG0 ]<br>00: Min (default)<br>01: Middle 1<br>10: Middle 2<br>11: Max |
| bit 4               | YPBPRCP             | YPbPr Clamp  | R/W | Clamp position of PbPr signal input setting<br>0: YPbPr sync tip timing<br>1: Y sync tip timing / PbPr backporch                          |
| bit 5<br>~<br>bit 7 | Reserved            | Reserved     | R/W | Reserved                                                                                                                                  |

**[9.1.4] Miscellaneous Setting Register (R/W) [Sub Address 0x03]**

Sub Address: 0x03

Default Value: 0x00

| bit 7         | bit 6 | bit 5    | bit 4  | bit 3 | bit 2 | bit 1    | bit 0    |
|---------------|-------|----------|--------|-------|-------|----------|----------|
| VERTS         | CSCAN | Reserved | CMPSEL | CSCL  | CSSL  | Reserved | Reserved |
| Default Value |       |          |        |       |       |          |          |
| 0             | 0     | 0        | 0      | 0     | 0     | 0        | 0        |

**Miscellaneous Setting Register**

| BIT                 | Register Name |                                    | R/W | Definition                                                                                                                                             |
|---------------------|---------------|------------------------------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| bit 0<br>~<br>bit 1 | Reserved      | Reserved                           | R/W | Reserved                                                                                                                                               |
| bit 2               | CSSL          | Component<br>Signal<br>Sync Level  | R/W | YPbPr signal sync / luminance ratio level setting<br>0: 300/700<br>1: 286/714                                                                          |
| bit 3               | CSCL          | Component<br>Signal<br>Color Level | R/W | Color (PbPr) signal level setting<br>0: 700mV<br>1: 714mV                                                                                              |
| bit 4               | CMPSEL        | Component<br>Signal Select         | R/W | Component signal input, interlace / progressive setting<br>(auto detection mode is disable).<br>0: Interlace (525i/625i)<br>1: Progressive (525p/625p) |
| bit 5               | Reserved      | Reserved                           | R/W | Reserved                                                                                                                                               |
| bit 6               | CSCAN         | Color stripe<br>cancel             | R/W | Color stripe cancel operation<br>Set to [1] only when Sub=Address 0x04[7:0] is [XXX00000]<br>Set to [0] when Sub=Address 0x04[7:0] is not [XXX00000]   |
| bit 7               | VERTS         | Vertical<br>SYNC way               | R/W | Vertical sync mechanism setting<br>0: VLOCK mechanism<br>1: Direct lock mechanism                                                                      |

**[9.1.5] Input Video Standard Register (R/W) [Sub Address 0x04]**

Input signal setting.

Sub Address: 0x04

Default Value: 0x00

| bit 7         | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---------------|-------|-------|-------|-------|-------|-------|-------|
| AUTODET       | SETUP | BW    | VLF   | VCEN1 | VCEN0 | VSCF1 | VCSF0 |
| Default Value |       |       |       |       |       |       |       |
| 0             | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

## Input Video Standard Register

| BIT                 | Register Name       |                                | R/W | Definition                                                                                                                                                                                          |
|---------------------|---------------------|--------------------------------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| bit 0<br>~<br>bit 1 | VSCF0<br>~<br>VSCF1 | Video<br>Sub-Carrier Frequency | R/W | Input video signal subcarrier frequency setting<br>[VSCF1:VSCF0]<br>00: 3.57954545 MHz (NTSC)<br>01: 3.57561149 MHz (PAL-M)<br>10: 3.58205625 MHz (PAL-Nc)<br>11: 4.43361875 MHz (PAL-B,D,G,H,I,N)* |
| bit 2<br>~<br>bit 3 | VCEN0<br>~<br>VCEN1 | Video Color Encode             | R/W | Input signal color encode format setting<br>[VCEN1:VCEN0]<br>00: NTSC<br>01: PAL<br>10: SECAM<br>11: Reserved (prohibited)                                                                          |
| bit 4               | VLF                 | Video Line Frequency           | R/W | Input signal line frequency setting<br>0: 525<br>1: 625                                                                                                                                             |
| bit 5               | BW                  | Black & White                  | R/W | Monochrome mode (ON/OFF) setting *2<br>[0] : Monochrome mode OFF<br>[1] : Monochrome mode ON                                                                                                        |
| bit 6               | SETUP               | Setup                          | R/W | Setup process setting<br>[0] : Process as input signal with no setup<br>[1] : Process as input signal with setup                                                                                    |
| bit 7               | AUTODET             | Video Standard<br>Auto Detect  | R/W | Input signal auto detection setting<br>[0]: OFF (auto detection disabled; set manually)<br>[1]: ON (auto detection enabled)                                                                         |

\* For SECAM input signal, change VSCF[1:0] setting to [11]

**[9.1.6] Output Format Register (R/W) [Sub Address 0x05]**

Output data format setting.

Sub Address: 0x05

Default Value: 0x00

| bit 7         | bit 6   | bit 5 | bit 4   | bit 3    | bit 2 | bit 1 | bit 0 |
|---------------|---------|-------|---------|----------|-------|-------|-------|
| VBIDEC1       | VBIDEC0 | SLLVL | TRSVSEL | 601LIMIT | VBIL2 | VBIL1 | VBIL0 |
| Default Value |         |       |         |          |       |       |       |
| 0             | 0       | 0     | 0       | 0        | 0     | 0     | 0     |

## Output Format Register

| BIT                 | Register Name           |                                         | R/W | Definition                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|---------------------|-------------------------|-----------------------------------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| bit 0<br>~<br>bit 2 | VBIL0<br>~<br>VBIL2     | Vertical<br>Blanking<br>Interval Length | R/W | <p>Vertical blanking interval length setting,<br/>entered as difference from the default settings<br/>The default settings are:<br/>           (525i) Line1~Line19 and Line263.5~Line282.5<br/>           (625i) Line623.5~Line23.5 and Line311~Line335<br/>           (525p) Line1~Line42<br/>           (625p) Line 621~Line625 and Line1~Line44</p> <p>Examples of lengthening and shortening:<br/>           If lengthened 1 line, the interval becomes<br/>           (525i) Line1~Line20 and Line263.5~Line283.5<br/>           (625i) Line623.5~Line24.5 and Line311~Line336<br/>           (525p) Line1~Line43<br/>           (625p) Line 621~Line625 and Line1~Line45<br/>           If shortened 1 line, the interval becomes<br/>           (525i) Line1~Line18 and Line263.5~Line281.5<br/>           (625i) Line623.5~Line22.5 and Line311~Line334<br/>           (525p) Line1~Line41<br/>           (625p) Line 621~Line625 and Line1~Line43</p> <p>[ VBIL2 : VBIL0 ]<br/>           [001]: VBI lengthened 1 line<br/>           [010]: VBI lengthened 2 lines<br/>           [011]: VBI lengthened 3 lines<br/>           [000]: Default<br/>           [101]: VBI shortened 3 lines<br/>           [110]: VBI shortened 2 lines<br/>           [111]: VBI shortened 1 line<br/>           [100]: Reserved</p> |
| bit 3               | 601LIMIT                | 601 Output Limit                        | R/W | <p>Output data code limit (Min-Max) setting<br/>           0: 1-254 (Y/CbCr)<br/>           1: 16-235 (Y), 16-240 (Cb/Cr)</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| bit 4               | TRSVSEL                 | Time<br>Reference<br>Signal<br>V Select | R/W | <p>Setting of lines for "Time reference signal"<br/>           V-bit value change in ITU-R BT.656 format<br/>           0: ITU-R Bt.656-3<br/>           1: ITU-R Bt.656-4 and SMPTE125M</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| bit 5               | SLLVL                   | Slice Level                             | R/W | <p>Slice level setting<br/>           0: Slice level approx. 25 IRE<br/>           1: Slice level approx. 50 IRE</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| bit 6<br>~<br>bit 7 | VBIDEC0<br>~<br>VBIDEC1 | VBI Decode                              | R/W | <p>Setting for type of data output during interval<br/>           set in Vertical Blanking Interval register *<br/>           [ VBIDEC1: VBIDEC0 ]<br/>           [00]: Black level data output<br/>           [01]: Monochrome data output<br/>           [10]: Slice result data output<br/>           [11]: Reserved</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |

**[9.1.7] NDMODE Register (R/W) [Sub Address 0x06]**

Limiting auto input video signal detection candidates register setting

Sub Address: 0x06

Default Value: 0x00

| bit 7         | bit 6  | bit 5   | bit 4     | bit 3    | bit 2   | bit 1   | bit 0  |
|---------------|--------|---------|-----------|----------|---------|---------|--------|
| ND625L        | ND525L | NDPAL60 | NDNTSC443 | Reserved | NDSECAM | NDPALNC | NDPALM |
| Default Value |        |         |           |          |         |         |        |
| 0             | 0      | 0       | 0         | 0        | 0       | 0       | 0      |

## NDMODE Register

| BIT   | Register Name |                     | R/W | Definition                                           |
|-------|---------------|---------------------|-----|------------------------------------------------------|
| bit 0 | NDPALM        | No Detect PAL-M     | R/W | 0: PAL-M candidate<br>1: PAL-M non-candidate         |
| bit 1 | NOPALNC       | No Detect PAL-NC    | R/W | 0: PAL-Nc candidate<br>1: PAL-Nc non-candidate       |
| bit 2 | NDSECAM       | No Detect SECAM     | R/W | 0: SECAM candidate<br>1: SECAM non-candidate         |
| bit 3 | Reserved      | Reserved            | R/W | Reserved                                             |
| bit 4 | NDNTSC443     | No Detect NTSC-4.43 | R/W | 0: NTSC-4.43 candidate<br>1: NTSC-4.43 non-candidate |
| bit 5 | NDPAL60       | No Detect PAL60     | R/W | 0: PAL-60 candidate<br>1: PAL-60 non-candidate       |
| bit 6 | ND525L        | No Detect 525 Line  | R/W | 0: 525 line candidate<br>1: 525 line non-candidate   |
| bit 7 | ND625L        | No Detect 625 Line  | R/W | 0: 625 line candidate<br>1: 625 line non-candidate   |

In making the above register settings, the following restrictions apply,

1. Setting both NDNTSC443(bit 4) and NDPAL60(bit 5) to [1] (High) is prohibited.
2. Setting both ND525L(bit 6) and ND625L(bit 7) to [1] (High) is prohibited.
3. To limit candidate formats, it is necessary to have the auto detection mode OFF while first setting the register to non-limited signal status and next the NDMODE settings, and then setting the auto detection mode to ON.

**[9.1.8] Output Control Register (R/W) [Sub Address 0x07]**

Output pin status register setting.

Sub Address: 0x07

Default Value: 0x00

| bit 7         | bit 6    | bit 5  | bit 4 | bit 3 | bit 2  | bit 1 | bit 0 |
|---------------|----------|--------|-------|-------|--------|-------|-------|
| CLKINV        | DVALFSEL | VDFSEL | HL    | NL    | DVALFL | VDFL  | DL    |
| Default Value |          |        |       |       |        |       |       |
| 0             | 0        | 0      | 0     | 0     | 0      | 0     | 0     |

## Output Control Register

| BIT   | Register Name |                         | R/W | Definition                                                                                                    |
|-------|---------------|-------------------------|-----|---------------------------------------------------------------------------------------------------------------|
| bit 0 | DL            | Data Output Low bit     | R/W | 0: Normal output<br>1: [D17: D0] pin output fixed at Low                                                      |
| bit 1 | VDFL          | VD_FLD Output Low bit   | R/W | 0: Normal output<br>1: VD_FLD pin output fixed at Low                                                         |
| bit 2 | DVALFL        | DVAL_FLD Output Low bit | R/W | 0: Normal output<br>1: DVAL_FLD pin output fixed at Low                                                       |
| bit 3 | NL            | NSIG Output Low bit     | R/W | 0: Normal output<br>1: NSIG pin output fixed at Low                                                           |
| bit 4 | HL            | HD Output Low bit       | R/W | 0: Normal output<br>1: HD pin output fixed at Low                                                             |
| bit 5 | VDFSEL        | VD_FLD Select bit       | R/W | 0: VD signal output<br>1: FIELD signal output                                                                 |
| bit 6 | DVALFSEL      | DVAL_FLD Select bit     | R/W | 0: DVALID signal output<br>1: FIELD signal output                                                             |
| bit 7 | CLKINV        | Clock Invert Setting    | R/W | 0: Normal output (write in data at rising edge)<br>1: Data and clock reversed (write in data at falling edge) |

Note: Output control via pins OE, PDN, and RSTN takes priority, regardless of the above settings.



**[9.1.9] Output Data Start and Delay Control Register (R/W) [Sub Address 0x08]**

Output data timing setting register.

Sub Address: 0x08

Default Value: 0x00

| bit 7         | bit 6    | bit 5    | bit 4    | bit 3    | bit 2    | bit 1    | bit 0    |
|---------------|----------|----------|----------|----------|----------|----------|----------|
| Reserved      | ACTSTAT2 | ACTSTAT1 | ACTSTAT0 | Reserved | YCDELAY2 | YCDELAY1 | YCDELAY0 |
| Default Value |          |          |          |          |          |          |          |
| 0             | 0        | 0        | 0        | 0        | 0        | 0        | 0        |

**Output Data Start and Delay Control Register**

| BIT                 | Register Name             |                               | R/W | Definition                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|---------------------|---------------------------|-------------------------------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| bit 0<br>~<br>bit 2 | YCDEALY0<br>~<br>YCDELAY2 | YC Delay<br>Control           | R/W | Adjustment of Y and C timing.<br>In D1 decode, delay or advance 1 sample unit is about 74ns<br>In D2 decode, delay or advance 1 sample unit is about 37ns.<br><br>YCDELAY[2:0]<br>[001]: Y advance 1-sample toward C.<br>[010]: Y advance 2-sample toward C.<br>[011]: Y advance 3-sample toward C.<br>[000]: No Delay and advance.<br>[101]: Y delay 3-sample toward C.<br>[110]: Y delay 2-sample toward C.<br>[111]: Y delay 1-sample toward C.<br>[100]: Reserved |
| bit 3               | Reserved                  | Reserved                      | R/W | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| bit 4<br>~<br>bit 6 | ACTSTA0<br>~<br>ACTSTA2   | Active Video<br>Start Control | R/W | Fine-tuning video data decode start position<br>In D1 decode, delay or advance 1 sample unit is about 74ns<br>In D2 decode, delay or advance 1 sample unit is about 37ns.<br><br>ACTSTA[2:0]<br>[001]: 1-sample delay<br>[010]: 2-sample delay<br>[011]: 3-sample delay<br>[000]: Normal start position<br>[101]: 3-sample advance<br>[110]: 2-sample advance<br>[111]: 1-sample advance<br>[100]: Reserved                                                           |
| bit 7               | Reserved                  | Reserved                      | R/W | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

**[9.1.10] Output Data Format Register (R/W) [Sub Address 0x09]**

Output data format setting register.

Sub Address: 0x09

Default Value: 0x00

| bit 7         | bit 6    | bit 5    | bit 4    | bit 3  | bit 2 | bit 1    | bit 0 |
|---------------|----------|----------|----------|--------|-------|----------|-------|
| Reserved      | Reserved | Reserved | Reserved | EAVSAV | RGBO  | Reserved | ODFMT |
| Default Value |          |          |          |        |       |          |       |
| 0             | 0        | 0        | 0        | 0      | 0     | 0        | 0     |

## Output Data Format Register

| BIT                 | Register Name |                    | R/W | Definition                                                                                                         |
|---------------------|---------------|--------------------|-----|--------------------------------------------------------------------------------------------------------------------|
| bit 0               | ODFMT         | Output Data Format | R/W | YCbCr output bit-width setting<br>0: 8-bit output<br>1: 16-bit output                                              |
| bit 1               | Reserved      | Reserved           | R/W | Reserved                                                                                                           |
| bit 2               | RGBO          | RGB Convert        | R/W | RGB convert output selection:<br>0: YCbCr data is output<br>1: RGB data is output                                  |
| bit 3               | EAVSAV        | EAVSAV Disable     | R/W | EAV/SAV output (ON/OFF) setting.<br>0: EAV/SAV ON<br>EAV/SAV is superimposed to Y or R/G/B data.<br>1: EAV/SAV OFF |
| bit 4<br>~<br>bit 7 | Reserved      | Reserved           | R/W | Reserved                                                                                                           |

**[9.1.11] AGC & ACC Control Register (R/W) [Sub Address 0x0A]**

AGC and ACC setting register.

Sub Address: 0x0A

Default Value: 0x00

| bit 7         | bit 6 | bit 5 | bit 4  | bit 3 | bit 2 | bit 1 | bit 0 |
|---------------|-------|-------|--------|-------|-------|-------|-------|
| ACCFRZ        | ACC1  | ACC0  | AGCFRZ | AGCC1 | AGCC0 | AGCT1 | AGCT0 |
| Default Value |       |       |        |       |       |       |       |
| 0             | 0     | 0     | 0      | 0     | 0     | 0     | 0     |

## AGC &amp; ACC Control Register

| BIT                 | Register Name       |                    | R/W | Definition                                                                                                                                                                         |
|---------------------|---------------------|--------------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| bit 0<br>~<br>bit 1 | AGCT0<br>~<br>AGCT1 | AGC Time Constance | R/W | AGC time constant (T) setting<br>(if disabled, PGA can be set manually).<br>AGCT[1:0]<br>00: Disable<br>01: Fast [T = 1Filed]<br>10: Middle [T = 7Filed]<br>11: Slow [T = 28Filed] |
| bit 2<br>~<br>bit 3 | AGCC0<br>~<br>AGCC1 | AGC Coring Control | R/W | AGC non-sensing bandwidth (LSB) setting<br>AGCC[1:0]<br>00: $\pm 2$ LSB<br>01: $\pm 3$ LSB<br>10: $\pm 4$ LSB<br>11: No non-sensing band                                           |
| bit 4               | AGCFRZ              | AGC Freeze         | R/W | AGC freeze function (ON/OFF) setting<br>(AGC set values are saved during freeze)<br>0: Non-frozen<br>1: Frozen                                                                     |
| bit 5<br>~<br>bit 6 | ACCT0<br>~<br>ACCT1 | ACC Time Constance | R/W | ACC time constant (T) setting<br>ACCT[1: 0]<br>00: Disable<br>01: Fast [T = 2Fields]<br>10: Middle [T = 8Fields]<br>11: Slow [T = 30Fields]                                        |
| bit 7               | ACCFRZ              | ACC Freeze         | R/W | ACC freeze function (ON/OFF) setting<br>(ACC set values are saved during freeze)<br>0: Non-frozen<br>1: Frozen                                                                     |

**[9.1.12] Control 0 Register (R/W) [Sub Address 0x0B]**

Sub Address: 0x0B

Default Value: 0x00

| bit 7         | bit 6 | bit 5 | bit 4    | bit 3    | bit 2    | bit 1    | bit 0 |
|---------------|-------|-------|----------|----------|----------|----------|-------|
| DVAL_FP       | VD_FP | HDP   | C443FIL1 | C443FIL0 | C358FIL1 | C358FIL0 | AGCTL |
| Default Value |       |       |          |          |          |          |       |
| 0             | 0     | 0     | 0        | 0        | 0        | 0        | 0     |

**Control 0 Register**

| BIT                 | Register Name             |                       | R/W | Definition                                                                                                                                                                                        |
|---------------------|---------------------------|-----------------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| bit 0               | AGCTL                     | AGC Transition Level  | R/W | Transition speed setting,<br>between peak AGC and sync AGC<br>0: QUICK<br>1: SLOW                                                                                                                 |
| bit 1<br>~<br>bit 2 | C358FIL0<br>~<br>C358FIL1 | C Filter 358 Select   | R/W | C-filter bandwidth setting,<br>for 3.58 MHz subcarrier system signal<br>C358FIL[1:0]<br>00: Narrow<br>01: Middle<br>10: Wide<br>11: Reserved                                                      |
| bit 3<br>~<br>bit 4 | C443FIL0<br>~<br>C443FIL1 | C Filter 443 Select   | R/W | C-filter bandwidth setting,<br>for 4.43 MHz subcarrier system signal<br>C443FIL[1:0]<br>00: Narrow<br>01: Middle<br>10: Wide<br>11: Reserved                                                      |
| bit 5               | HDP                       | HD pin Polarity       | R/W | HD signal polarity setting<br>0: ACTIVE LOW<br>1: ACTIV HIGH                                                                                                                                      |
| bit 6               | VD_FP                     | VD_F Pin Polarity     | R/W | VD_FLD pin output signal polarity setting<br><br>If VD signal is output<br>0: ACTIVE LOW<br>1: ACTVIE HIGH<br>If FIELD signal is output<br>0: LOW=ODD / HIGH=EVEN<br>1: LOW=EVEN / HIGH=ODD       |
| bit 7               | DVAL_FP                   | DVAL_FLD pin Polarity | R/W | DVAL_FLD pin output signal polarity setting<br><br>If DVALID signal is output<br>0: ACTIVE LOW<br>1: ACTVIE HIGH<br>If FIELD signal is output<br>0: LOW=ODD / HIGH=EVEN<br>1: LOW=EVEN / HIGH=ODD |

**[9.1.13] Control 1 Register (R/W) [Sub Address 0x0C]**

Sub Address: 0x0C

Default Value: 0x00

| bit 7         | bit 6    | bit 5   | bit 4   | bit 3     | bit 2     | bit 1  | bit 0  |
|---------------|----------|---------|---------|-----------|-----------|--------|--------|
| CLKMODE1      | CLKMODE0 | INTPOL1 | INTPOL0 | UVFILSEL1 | UVFILSEL0 | YCSEP1 | YCSEP0 |
| Default Value |          |         |         |           |           |        |        |
| 0             | 0        | 0       | 0       | 0         | 0         | 0      | 0      |

## Control 1 Register

| BIT                 | Register Name               |                          | R/W | Definition                                                                                                                                                              |
|---------------------|-----------------------------|--------------------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| bit 0<br>~<br>bit 1 | YCSEP0<br>~<br>YCSEP1       | YC Separation Control    | R/W | Y/C separation setting YCSEP[1:0]<br>00: Adaptive Y/C separation<br>01: 1-dimensional Y/C separation<br>10: 2-dimensional Y/C separation<br>11: Reserved                |
| bit 2<br>~<br>bit 3 | UVFILSEL0<br>~<br>UVFILSEL1 | UV Filter Select         | R/W | UV filter setting<br>(CVBS or S-video input)<br>UVFILSEL0<br>0: Wide 1<br>1 Narrow 1<br><br>(YPbPr input)<br>00: Middle 1<br>01: Middle 2<br>10: Wide 2<br>11: Narrow 2 |
| bit 4<br>~<br>bit 5 | INTPOL0<br>~<br>INTPOL1     | Interpolator Mode Select | R/W | Pixel interpolator setting<br>INTPOL[1:0]<br>00: Auto<br>01: ON<br>10: OFF<br>11: Reserved                                                                              |
| bit 6<br>~<br>bit 7 | CLKMODE0<br>~<br>CLKMODE1   | Clock Mode Select        | R/W | Clock mode setting<br>CLKMODE[1:0]<br>00: Automatic transition mode<br>01: Line-locked clock mode<br>10: Frame-locked clock mode<br>11: Fixed-clock mode                |

**[9.1.14] Control 2 Register (R/W) [Sub Address 0x0D]**

Sub Address: 0x0D

Default Value: 0x00

| bit 7         | bit 6     | bit 5   | bit 4   | bit 3   | bit 2   | bit 1 | bit 0 |
|---------------|-----------|---------|---------|---------|---------|-------|-------|
| CONTSEL       | STUPATOFF | ERRHND1 | ERRHND0 | NSIGMD1 | NSIGMD0 | DPAL1 | DPAL0 |
| Default Value |           |         |         |         |         |       |       |
| 0             | 0         | 0       | 0       | 0       | 0       | 0     | 0     |

**Control 2 Register**

| BIT                 | Register Name           |                        | R/W | Definition                                                                                                                                                                                                                     |
|---------------------|-------------------------|------------------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| bit 0<br>~<br>bit 1 | DPAL0<br>~<br>DPAL1     | Deluxe PAL             | R/W | Setting for color averaging (PAL phase correction block)<br>Also applicable to NTSC.<br>DPAL[1:0]<br>00: Adaptive phase correction ON<br>01: Phase correction ON<br>10: Phase correction OFF<br>11: Reserved                   |
| bit 2<br>~<br>bit 3 | NSIGMD0<br>~<br>NSIGMD1 | NSIG mode select       | R/W | Setting for output on no-signal detection<br>NSIGMD[1:0]<br>00: Black-level output (Y=0x10/CbCr=0x80)<br>01: Blue-level (Blueback) output (Y=0x29/Cb=0xF0/Cr=0x6E)<br>10: Input status (sandstorm) output<br>11: Reserved      |
| bit 4<br>~<br>bit 5 | ERRHND0<br>~<br>ERRHND1 | 656 Error Handling     | R/W | Setting for processing if ITU-R Bt.656 output is not possible<br>ERRHND[1:0]<br>00: Line drop or repeat<br>01: Pixel drop or repeat, in final line of field<br>10: Line drop or repeat, in final line of frame<br>11: Reserved |
| bit 6               | STUPATOFF               | Setup Auto Control Off | R/W | Setup auto switching setting (ON/OFF) in auto signal detection mode<br>0: Auto setup switching ON<br>1: Auto setup switching OFF                                                                                               |
| bit 7               | CONTSEL                 | Contrast Select        | R/W | Contrast selector<br>0: 50%<br>1: 0%                                                                                                                                                                                           |

**[9.1.15] PGA1 Control Register (R/W) [Sub Address 0x0E]**

PGA1 gain control register setting.

Sub Address: 0x0E

Default Value: 0x54

| bit 7         | bit 6   | bit 5   | bit 4   | bit 3   | bit 2   | bit 1   | bit 0   |
|---------------|---------|---------|---------|---------|---------|---------|---------|
| APGA1_1       | APGA1_0 | DPGA1_5 | DPGA1_4 | DPGA1_3 | DPGA1_2 | DPGA1_1 | DPGA1_0 |
| Default Value |         |         |         |         |         |         |         |
| 0             | 1       | 0       | 1       | 0       | 1       | 0       | 0       |

| BIT                 | Register Name           |                      | R/W | Definition                                                                       |
|---------------------|-------------------------|----------------------|-----|----------------------------------------------------------------------------------|
| bit 0<br>~<br>bit 5 | DPGA1_0<br>~<br>DPGA1_5 | Digital PGA1 Control | R/W | Digital PGA1 gain setting.<br>PGA gain is set by following equation.             |
| bit 6<br>~<br>bit 7 | APGA1_0<br>~<br>APGA1_1 | Analog PGA1 Control  | R/W | Analog PGA1 gain setting.<br>[00]: -3dB<br>[01]: 0dB<br>[10]: +3dB<br>[11]: +6dB |

Digital PGA gain equation:

$$\text{Gain(dB)} = 20 \text{LOG} \left( \frac{(5 \times \text{PGA}) + 497}{512} \right)$$

\*PGA: PGA1 or PGA2 register value (Decimal)

Default gain setting is 0x54(HEX)=1.3dB. (Analog:0dB + Digital:1.3dB)

**[9.1.16]PGA2 Control Register (R/W) [Sub Address 0x0F]**

PGA2 gain control register setting.

Sub Address: 0x0F

Default Value: 0x54

| bit 7         | bit 6   | bit 5   | bit 4   | bit 3   | bit 2   | bit 1   | bit 0   |
|---------------|---------|---------|---------|---------|---------|---------|---------|
| APGA2_1       | APGA2_0 | DPGA2_5 | DPGA2_4 | DPGA2_3 | DPGA2_2 | DPGA2_1 | DPGA2_0 |
| Default Value |         |         |         |         |         |         |         |
| 0             | 1       | 0       | 1       | 0       | 1       | 0       | 0       |

| BIT                 | Register Name           |                      | R/W | Definition                                                                       |
|---------------------|-------------------------|----------------------|-----|----------------------------------------------------------------------------------|
| bit 0<br>~<br>bit 5 | DPGA2_0<br>~<br>DPGA2_5 | Digital PGA1 Control | R/W | Digital PGA2 gain setting.<br>PGA gain is set by above equation.                 |
| bit 6<br>~<br>bit 7 | APGA2_0<br>~<br>APGA2_1 | Analog PGA1 Control  | R/W | Analog PGA2 gain setting.<br>[00]: -3dB<br>[01]: 0dB<br>[10]: +3dB<br>[11]: +6dB |

**[9.1.17] Pedestal Level Control Register (R/W) [Sub Address 0x10]**

Pedestal level control register setting.

Sub Address: 0x10

Default Value: 0x00

| bit 7         | bit 6 | bit 5 | bit 4 | bit 3  | bit 2  | bit 1  | bit 0  |
|---------------|-------|-------|-------|--------|--------|--------|--------|
| DPCC1         | DPCC0 | DPCT1 | DPCT0 | BKLVL3 | BKLVL2 | BKLVL1 | BKLVL0 |
| Default Value |       |       |       |        |        |        |        |
| 0             | 0     | 0     | 0     | 0      | 0      | 0      | 0      |

## Pedestal Level Control Register

| BIT                 | Register Name         |                                | R/W | Definition                                                                                                                                                                                                                                                                                                                                                                                            |
|---------------------|-----------------------|--------------------------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| bit 0<br>~<br>bit 3 | BKLVL0<br>~<br>BKLVL3 | Black Level                    | R/W | Setting for change from current pedestal level by adding to or subtracting from black level<br>BKLVL[3 : 0]<br>0001: Add 1<br>0010: Add 2<br>0011: Add 3<br>0100: Add 4<br>0101: Add 5<br>0110: Add 6<br>0111: Add 7<br>0000: Default<br>1000: Subtract 8<br>1001: Subtract 7<br>1010: Subtract 6<br>1011: Subtract 5<br>1100: Subtract 4<br>1101: Subtract 3<br>1110: Subtract 2<br>1111: Subtract 1 |
| bit 4<br>~<br>bit 5 | DPCT0<br>~<br>DPCT1   | Digital Pedestal Clamp Control | R/W | Time-constant setting for digital pedestal clamp<br>DPCT[1:0]<br>00: Fast<br>01: Middle<br>10: Slow<br>11: Disable                                                                                                                                                                                                                                                                                    |
| bit 6<br>~<br>bit 7 | DPCC0<br>~<br>DPCC1   | Digital Pedestal Clamp Coring  | R/W | Non-sensing bandwidth setting for digital pedestal clamp<br>DPCC[1: 0]<br>00: +/-1bit<br>01: +/-2bit<br>10: +/-3bit<br>11: No non-sensing band                                                                                                                                                                                                                                                        |



**[9.1.18] Color Killer Control Register (R/W) [Sub Address 0x11]**

Color killer register.

Sub Address: 0x11

Default Value: 0x08

| bit 7         | bit 6   | bit 5  | bit 4  | bit 3  | bit 2  | bit 1  | bit 0  |
|---------------|---------|--------|--------|--------|--------|--------|--------|
| COLKIL        | CKILSEL | CKSCM1 | CKSCM0 | CKLVL3 | CKLVL2 | CKLVL1 | CKLVL0 |
| Default Value |         |        |        |        |        |        |        |
| 0             | 0       | 0      | 0      | 1      | 0      | 0      | 0      |

## Color Killer Control Register

| BIT                 | Register Name         |                                 | R/W | Definition                                                                                                                                                                                                                                                    |
|---------------------|-----------------------|---------------------------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| bit 0<br>~<br>bit 3 | CKLVL0<br>~<br>CKLVL3 | Color Killer<br>Level           | R/W | Burst level setting for color killer activation<br>Default value, approx. -23 dB.                                                                                                                                                                             |
| bit 4<br>~<br>bit 5 | CKSCM0<br>~<br>CKSCM1 | Color Killer<br>Lever for SECAM | R/W | Burst level setting for color killer activation in<br>SECAM mode Adds 2 bits to CKLVL[3:0]                                                                                                                                                                    |
| bit 6               | CKILSEL               | Color Killer<br>Select          | R/W | Color killer operational mode setting<br>0: Activation when burst color level is below<br>than CKLVL[3:0]-bit threshold setting.<br>1: Activation when burst color level is below<br>than CKLVL[3:0]-bit threshold setting<br>or color decode PLL lock fails. |
| bit 7               | COLKIL                | Color Killer<br>Set             | R/W | Color killer ON/OFF setting<br>0: Enable<br>1: Disable                                                                                                                                                                                                        |

**[9.1.19] Contrast Control Register (R/W) [Sub Address 0x12]**

Contrast adjustment setting register.

Sub Address: 0x12

Default Value: 0x80

| bit 7         | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---------------|-------|-------|-------|-------|-------|-------|-------|
| CONT7         | CONT6 | CONT5 | CONT4 | CONT3 | CONT2 | CONT1 | CONT0 |
| Default Value |       |       |       |       |       |       |       |
| 1             | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

## Contrast Control Register

| BIT                 | Register Name       |                  | R/W | Definition                                                                                       |
|---------------------|---------------------|------------------|-----|--------------------------------------------------------------------------------------------------|
| bit 0<br>~<br>bit 7 | CONT0<br>~<br>CONT7 | Contrast Control | R/W | Register for contrast adjustment in steps of 1/128 in range 1~255/128 from default value of 0x80 |

**[9.1.20] Brightness Control Register (R/W) [Sub Address 0x13]**

Brightness adjustment setting register

Sub Address: 0x13

Default Value: 0x00

| bit 7         | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---------------|-------|-------|-------|-------|-------|-------|-------|
| BR7           | BR6   | BR5   | BR4   | BR3   | BR2   | BR1   | BR0   |
| Default Value |       |       |       |       |       |       |       |
| 0             | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

## Brightness Control Register

| BIT                 | Register Name   |                    | R/W | Definition                                                                               |
|---------------------|-----------------|--------------------|-----|------------------------------------------------------------------------------------------|
| bit 0<br>~<br>bit 7 | BR0<br>~<br>BR7 | Brightness Control | R/W | Register for brightness adjustment in steps of 1 by 8-bit code setting in 2's complement |

**[9.1.21] Image Control Register (R/W) [Sub Address 0x14]**

Sharpness control, Luminance bandwidth filter control, Sepia color output setting and VBI interval setting register.

Sub Address: 0x14

Default Value: 0x00

| bit 7         | bit 6 | bit 5   | bit 4   | bit 3   | bit 2   | bit 1  | bit 0  |
|---------------|-------|---------|---------|---------|---------|--------|--------|
| VBIIMGCTL     | SEPIA | LUMFIL1 | LUMFIL0 | SCCORE1 | SHCORE0 | SHARP1 | SHARP0 |
| Default Value |       |         |         |         |         |        |        |
| 0             | 0     | 0       | 0       | 0       | 0       | 0      | 0      |

**Image Control Register**

| BIT                 | Register Name           |                   | R/W | Definition                                                                                                                                                                 |
|---------------------|-------------------------|-------------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| bit 0<br>~<br>bit 1 | SHARP0<br>~<br>SHARP1   | Sharpness Control | R/W | Sharpness control (filter effect) setting<br>SHARP[1: 0]<br>00: No filtering<br>01: Min effect<br>10: Middle effect<br>11: Max effect                                      |
| bit 2<br>~<br>bit 3 | SHCORE0<br>~<br>SHCORE1 | Sharpness Coring  | R/W | Setting for level of coring after passage<br>through sharpness filter<br>SHCORE[1:0]<br>00: No coring<br>01: ±1LSB<br>10: ±2LSB<br>11: ±3LSB                               |
| bit 4<br>~<br>bit 5 | LUMFIL0<br>~<br>LUMFIL1 | Luminance Filter  | R/W | Setting for luminance band limit filter<br>LUMFIL[1:0]<br>00: No filtering<br>01: Narrow<br>10: Mid<br>11: WIDE                                                            |
| bit 6               | SEPIA                   | Sepia Output      | R/W | Setting (ON/OFF) for sepia coloring of decode results<br>0: Normal output<br>1: Sepia output                                                                               |
| bit 7               | VBIIMGCTL               | VBI Image Control | R/W | Setting (ON/OFF) for image adjustment<br>during brightness and contrast adjustment VBI<br>0: Image adjustment inactive during VBI<br>1: Image adjustment active during VBI |

**[9.1.22] Saturation / U Tone Control Register (R/W) [Sub Address 0x15]**

Saturation adjustment registers setting.

If YPbPr signal input, U tone level adjustment register setting.

Sub Address: 0x15

Default Value: 0x80

| bit 7         | bit 6  | bit 5  | bit 4  | bit 3  | bit 2  | bit 1  | bit 0  |
|---------------|--------|--------|--------|--------|--------|--------|--------|
| SAT7          | SAT6   | SAT5   | SAT4   | SAT3   | SAT2   | SAT1   | SAT0   |
| UTONE7        | UTONE6 | UTONE5 | UTONE4 | UTONE3 | UTONE2 | UTONE1 | UTONE0 |
| Default Value |        |        |        |        |        |        |        |
| 1             | 0      | 0      | 0      | 0      | 0      | 0      | 0      |

**Saturation / U TONE Control Register**

| BIT                 | Register Name         |                    | R/W | Definition                                                                                                                       |
|---------------------|-----------------------|--------------------|-----|----------------------------------------------------------------------------------------------------------------------------------|
| bit 0<br>~<br>bit 7 | SAT0<br>~<br>SAT7     | Saturation Control | R/W | Register for saturation level adjustment in steps of 1/128 in range 1~255/128 from default value of 0x80 (CVBS or S-video input) |
| bit 0<br>~<br>bit 7 | UTONE0<br>~<br>UTONE7 | U Tone Control     | R/W | Register for U tone level adjustment in steps of 1/128 in range 1~255/128 from default value of 0x80 (YPbPr input)               |

If component mode, UTONE default value should be changed to following parameter.

UTONE [7:0] =0x70

**[9.1.23] V Tone Control Register (R/W) [Sub Address 0x16]**

YPbPr signal input, V tone level adjustment register setting.

Sub Address: 0x16

Default Value: 0x80

| bit 7         | bit 6  | bit 5  | bit 4  | bit 3  | bit 2  | bit 1  | bit 0  |
|---------------|--------|--------|--------|--------|--------|--------|--------|
| VTONE7        | VTONE6 | VTONE5 | VTONE4 | VTONE3 | VTONE2 | VTONE1 | VTONE0 |
| Default Value |        |        |        |        |        |        |        |
| 1             | 0      | 0      | 0      | 0      | 0      | 0      | 0      |

**V TONE Control Register**

| BIT                 | Register Name         |                | R/W | Definition                                                                                                                |
|---------------------|-----------------------|----------------|-----|---------------------------------------------------------------------------------------------------------------------------|
| bit 0<br>~<br>bit 7 | VTONE0<br>~<br>VTONE7 | V Tone Control | R/W | Register for V tone level adjustment in steps of 1/128 in range 1~255/128 from default value of 0x80 (YPbPr or RGB input) |

If component mode, VTONE default value should be changed to following parameter.

VTONE [7:0] =0x9D

**[9.1.24] HUE Control Register (R/W) [Sub Address 0x17]**

HUE adjustment register setting.

Sub Address: 0x17

Default Value: 0x00

| bit 7         | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---------------|-------|-------|-------|-------|-------|-------|-------|
| HUE7          | HUE6  | HUE5  | HUE4  | HUE3  | HUE2  | HUE1  | HUE0  |
| Default Value |       |       |       |       |       |       |       |
| 0             | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

HUE Control Register

| BIT                 | Register Name     |             | R/W | Definition                                                                              |
|---------------------|-------------------|-------------|-----|-----------------------------------------------------------------------------------------|
| bit 0<br>~<br>bit 7 | HUE0<br>~<br>HUE7 | HUE Control | R/W | Register for hue adjustment in steps of 1/256 in range $\pm 45^\circ$ in 2's complement |

**[9.1.25] High Slice Data Set Register (R/W) [Sub Address 0x18]**

Sub Address: 0x18

Default Value: 0xEB

| bit 7         | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---------------|-------|-------|-------|-------|-------|-------|-------|
| H7            | H6    | H5    | H4    | H3    | H2    | H1    | H0    |
| Default Value |       |       |       |       |       |       |       |
| 1             | 1     | 1     | 0     | 1     | 0     | 1     | 1     |

High Slice Data Set Register

| BIT                 | Register Name |                   | R/W | Definition                                                                                                                        |
|---------------------|---------------|-------------------|-----|-----------------------------------------------------------------------------------------------------------------------------------|
| bit 0<br>~<br>bit 7 | H0<br>~<br>H7 | High Data 0~7 Set | R/W | Register for setting sliced data from VBI slicer to High value. Important: Corresponds to 601 special code if set to 0x00 or 0xFF |

**[9.1.26] Low Slice Data Set Register (R/W) [Sub Address 0x19]**

Sub Address: 0x19

Default Value: 0x10

| bit 7         | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---------------|-------|-------|-------|-------|-------|-------|-------|
| L7            | L6    | L5    | L4    | L3    | L2    | L1    | L0    |
| Default Value |       |       |       |       |       |       |       |
| 0             | 0     | 0     | 1     | 0     | 0     | 0     | 0     |

Low Slice Data Set Register

| BIT                 | Register Name |                  | R/W | Definition                                                                                                                       |
|---------------------|---------------|------------------|-----|----------------------------------------------------------------------------------------------------------------------------------|
| bit 0<br>~<br>bit 7 | L0<br>~<br>L7 | Low Data 0~7 Set | R/W | Register for setting sliced data from VBI slicer to Low value. Important: Corresponds to 601 special code if set to 0x00 or 0xFF |

**[9.1.27] Request VBI Information Register (R/W) [Sub Address 0x1A]**

Request decode data during VBI interval setting register.

Sub Address: 0x1A

Default Value: 0x00

| bit 7         | bit 6    | bit 5    | bit 4    | bit 3 | bit 2  | bit 1 | bit 0 |
|---------------|----------|----------|----------|-------|--------|-------|-------|
| Reserved      | Reserved | Reserved | Reserved | WSSRQ | VBIDRQ | EXTRQ | CCRQ  |
| Default Value |          |          |          |       |        |       |       |
| 0             | 0        | 0        | 0        | 0     | 0      | 0     | 0     |

## Request VBI Information Register

| BIT                 | Register Name |                               | R/W | Definition                                                                                   |
|---------------------|---------------|-------------------------------|-----|----------------------------------------------------------------------------------------------|
| bit 0               | CCRQ          | Closed Caption Decode Request | R/W | Setting (ON/OFF) for closed caption decode request<br>0: No request (OFF)<br>1: Request (ON) |
| bit 1               | EXTRQ         | Extended Data Decode Request  | R/W | Setting (ON/OFF) for Extended Data decode request<br>0: No request (OFF)<br>1: Request (ON)  |
| bit 2               | VBIDRQ        | VBID Decode Request           | R/W | Setting (ON/OFF) for VBID decode request<br>0: No request (OFF)<br>1: Request (ON)           |
| bit 3               | WSSRQ         | WSS Decode Request            | R/W | Setting (ON/OFF) for WSS decode request<br>0: No request (OFF)<br>1: Request (ON)            |
| bit 4<br>~<br>bit 7 | Reserved      | Reserved                      | R/W | Reserved                                                                                     |

**[9.1.28] Sub Address 0x1B~0x21 “Reserved Register (R/W)”**

Reserved register.

**[9.1.29] Status 1 Register (R) [Sub Address 0x22]**

The AK8858 internal status register.

Sub Address: 0x22

| bit 7 | bit 6   | bit 5    | bit 4    | bit 3   | bit 2  | bit 1 | bit 0 |
|-------|---------|----------|----------|---------|--------|-------|-------|
| OVCOL | PKWHITE | SCLKMOD1 | SCLKMOD0 | COLKLON | FRMSTD | VLOCK | NOSIG |

## Status 1 Register

| BIT                 | Register Name             |                      | R/W | Definition                                                                                                                                     |
|---------------------|---------------------------|----------------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------|
| bit 0               | NOSIG                     | No Signal            | R   | Input signal indicator<br>0: Input signal present<br>1: Input signal absent                                                                    |
| bit 1               | VLOCK                     | VLOCK                | R   | Input signal VLOCK synchronization status indicator<br>0: Input signal synchronized<br>1: Input signal non-synchronized                        |
| bit 2               | FRMSTD                    | Frame Standard       | R   | Input signal interlace status indicator<br>0: Input signal 525/625 interlaced<br>1: Input signal not 525/625 interlaced                        |
| bit 3               | COLKILON                  | Color Killer ON      | R   | Color killer status indicator<br>0: Color killer not operation<br>1: Color killer operation<br>In component decode mode, this bit is always 0. |
| bit 4<br>~<br>bit 5 | SCLKMOD0<br>~<br>SCLKMOD1 | Clock Mode           | R   | Clock mode indicator<br>SCLKMOD[1:0]<br>00: Fixed-clock mode<br>01: Line-locked clock mode<br>10: Frame-locked clock mode<br>11: Reserved      |
| bit 6               | PKWHITE                   | Peak White Detection | R   | Luminance decode result flow status indicator,<br>after passage through AGC block<br>0: Normal<br>1: Overflow                                  |
| bit 7               | OVCOL                     | Over Color Level     | R   | Color decode result flow status indicator,<br>after passage through ACC block<br>0: Normal<br>1: Overflow (excessive color signal input)       |

**[9.1.30] Status 2 Register (R) [Sub Address 0x23]**

The AK8858 internal status register.

Sub Address: 0x23

| bit 7    | bit 6    | bit 5 | bit 4   | bit 3  | bit 2   | bit 1  | bit 0 |
|----------|----------|-------|---------|--------|---------|--------|-------|
| Reserved | Reserved | AGSTS | REALFLD | WSSDET | VBIDDET | EXTDET | CCDET |

## Status 2 Register

| BIT                 | Register Name |                       | R/W | Definition                                                                                                                                   |
|---------------------|---------------|-----------------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------|
| bit 0               | CCDET         | Closed Caption Detect | R   | Indicator for presence of decoded data in Closed Caption 1/2 Register<br>0: No closed caption data present<br>1: Closed caption Data present |
| bit 1               | EXTDET        | Extended Data Detect  | R   | Indicator for presence of decoded data in Extended Data 1/2 Register<br>0: No extended data present<br>1: Extended data present              |
| bit 2               | VBIDDET       | VBID Data Detect      | R   | Indicator for presence of decoded data in VBID 1/2 Register<br>0: No VBID data present<br>1: VBID data present                               |
| bit 3               | WSSDET        | WSS Data Detect       | R   | Indicator for presence of decoded data in WSS 1/2 Register<br>0: No WSS data present<br>1: WSS data present                                  |
| bit 4               | REALFLD       | Real Filed            | R   | Input signal field status (even/odd) indicator<br>0: EVEN field<br>1: ODD field                                                              |
| bit 5               | AGCSTS        | AGC Status bit        | R   | AGC status indicator<br>0: Sync AGC active<br>1: Peak AGC active                                                                             |
| bit 6<br>~<br>bit 7 | Reserved      | Reserved              | R   | Reserved                                                                                                                                     |



**[9.1.31] Macrovision Status Register (R) [Sub Address 0x24]**

Macrovision signal status register.

Sub Address: 0x24

| bit 7    | bit 6    | bit 5    | bit 4    | bit 3    | bit 2  | bit 1 | bit 0  |
|----------|----------|----------|----------|----------|--------|-------|--------|
| Reserved | Reserved | Reserved | Reserved | Reserved | CSTYPE | CSDet | AGCDET |

## Macrovision Status Register

| BIT                 | Register Name |                     | R/W | Definition                                                                                                                  |
|---------------------|---------------|---------------------|-----|-----------------------------------------------------------------------------------------------------------------------------|
| bit 0               | AGCDET        | AGC Process Detect  | R   | Indicator for presence of Macrovision AGC in input signal<br>0: No Macrovision AGC present<br>1: Macrovision AGC present    |
| bit 1               | CSDet         | Color Stripe Detect | R   | Indicator for presence of Macrovision Color Stripe in input signal<br>0: No Color Stripe present<br>1: Color Stripe present |
| bit 2               | CSTYPE        | Color Stripe Type   | R   | Indicator for type of Color Stripe included in input signal<br>0: Color Stripe Type 2<br>1: Color Stripe Type 3             |
| bit 3<br>~<br>bit 7 | Reserved      | Reserved            | R   | Reserved                                                                                                                    |

**[9.1.32] Input Video Status Register (R) [Sub Address 0x25]**

Input video status register for auto detection mode.

Sub Address: 0x25

| bit 7 | bit 6 | bit 5 | bit 4  | bit 3    | bit 2    | bit 1    | bit 0    |
|-------|-------|-------|--------|----------|----------|----------|----------|
| FIXED | UNDEF | ST_BW | ST_VLF | ST_VCEN1 | ST_VCEN0 | ST_VSCF1 | ST_VSCF0 |

## Input Video Status Register

| BIT                 | Register Name             |                                       | R/W | Definition                                                                                                                                                                                                                                                                                                                                                                                              |
|---------------------|---------------------------|---------------------------------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| bit 0<br>~<br>bit 1 | ST_VSCF0<br>~<br>ST_VSCF1 | Status of Video Sub-Carrier Frequency | R   | Input video signal subcarrier frequency indicator<br><br>For CVBS and S (Y/C) signal decode results shows as follows:<br>ST_VSCF[1:0]<br>00: 3.57954545 MHz<br>01: 3.57561149 MHz<br>10: 3.58205625 MHz<br>11: 4.43361475 MHz (SECAM detected result)<br>For D1/D2 signal decode results shows as follows (this result also apply if auto detection mode is OFF)<br>00: D1<br>01: D2<br>10/11: Reserved |
| bit 2<br>~<br>bit 3 | ST_VCEN0<br>~<br>ST_VCEN1 | Status of Video Color Encode          | R   | Input signal color encode format indicator<br>ST_VCEN[1:0]<br>00: NTSC<br>01: PAL<br>10: SECAM<br>[11]: Component setting*                                                                                                                                                                                                                                                                              |
| bit 4               | ST_VLF                    | Status of Video Line Frequency        | R   | Input signal line number indicator<br>0: 525 line<br>1: 625 line                                                                                                                                                                                                                                                                                                                                        |
| bit 5               | ST_BW                     | Status of B/W                         | R   | Input signal monochrome indicator<br>0: Not monochrome<br>1: Monochrome                                                                                                                                                                                                                                                                                                                                 |
| bit 6               | UNDEF                     | Un-Define                             | R   | Input signal detection indicator<br>0: Input signal detected<br>1: Input signal not detected                                                                                                                                                                                                                                                                                                            |
| bit 7               | FIXED                     | Input Video Standard Fixed            | R   | Input signal detection process status<br>0: Detection process in progress<br>1: Detection process completed                                                                                                                                                                                                                                                                                             |

\* ST\_VCEN[1:0] is [11] when Sub-Address 0x00[6:5] is set to [10] (Component video input).

**[9.1.33] Closed Caption1 Register (R) [Sub Address 0x26]**

Closed Caption data storage register

Sub Address: 0x26

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| CC7   | CC6   | CC5   | CC4   | CC3   | CC2   | CC1   | CC0   |

**[9.1.34] Closed Caption2 Register (R) [Sub Address 0x27]**

Closed Caption data storage register

Sub Address: 0x27

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| CC15  | CC14  | CC13  | CC12  | CC11  | CC10  | CC9   | CC8   |

**[9.1.35] WSS 1 Register (R) [Sub Address 0x28]**

WSS data storage register

Sub Address: 0x28

| bit 7  | bit 6  | bit 5  | bit 4  | bit 3  | bit 2  | bit 1  | bit 0  |
|--------|--------|--------|--------|--------|--------|--------|--------|
| WSS2-7 | WSS2-6 | WSS2-5 | WSS2-4 | WSS1-3 | WSS1-2 | WSS1-1 | WSS1-0 |

**[9.1.36] WSS 2 Register (R) [Sub Address 0x29]**

WSS data storage register

Sub Address: 0x29

| bit 7    | bit 6    | bit 5   | bit 4   | bit 3   | bit 2   | bit 1  | bit 0  |
|----------|----------|---------|---------|---------|---------|--------|--------|
| Reserved | Reserved | WSS4-13 | WSS4-12 | WSS4-11 | WSS3-10 | WSS3-9 | WSS3-8 |

**[9.1.37.] Extended Data 1 Register (R) [Sub Address 0x2A]**

Closed Caption Extended data storage register

Sub Address: 0x2A

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| EXT7  | EXT6  | EXT5  | EXT4  | EXT3  | EXT2  | EXT1  | EXT0  |

**[9.1.38.] Extended Data 2 Register (R) [Sub Address 0x2B]**

Closed Caption Extended data storage register

Sub Address: 0x2B

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| EXT15 | EXT14 | EXT13 | EXT12 | EXT11 | EXT10 | EXT9  | EXT8  |

**[9.1.39] VBID 1 Register (R) [Sub Address 0x2C]**

VBID data storage register

Sub Address: 0x2C

| bit 7    | bit 6    | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|----------|----------|-------|-------|-------|-------|-------|-------|
| Reserved | Reserved | VBID1 | VBID2 | VBID3 | VBID4 | VBID5 | VBID6 |

**[9.1.40] VBID 2 Register (R) [Sub Address 0x2D]**

VBID data storage register

Sub Address: 0x2D

| bit 7 | bit 6 | bit 5 | bit 4  | bit 3  | bit 2  | bit 1  | bit 0  |
|-------|-------|-------|--------|--------|--------|--------|--------|
| VBID7 | VBID8 | VBID9 | VBID10 | VBID11 | VBID12 | VBID13 | VBID14 |

**[9.1.41] Device and Revision ID Register (R) [Sub Address 0x2E]**

Device ID and Revision indicator

Device ID: [0x3A]

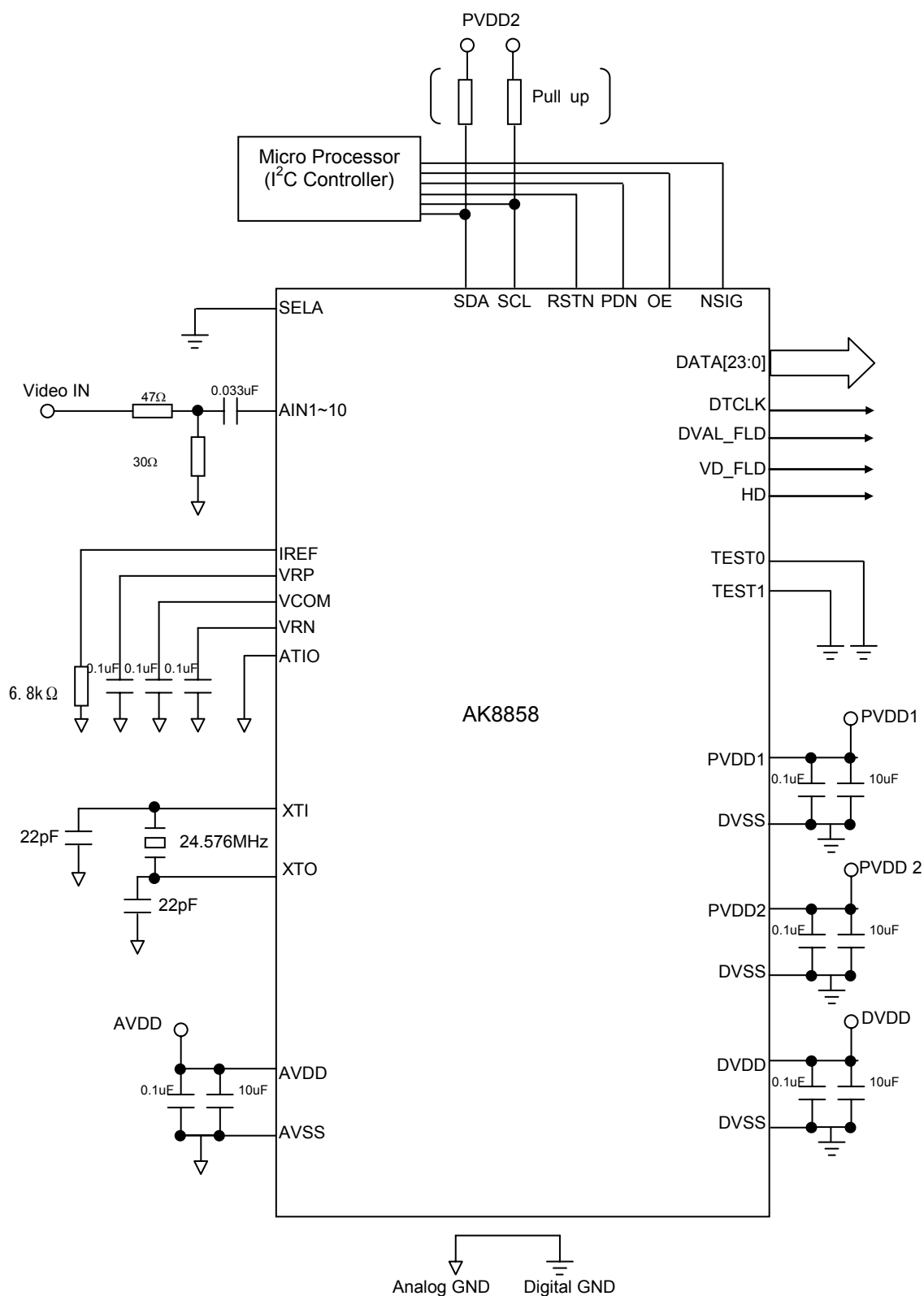
Revision ID: Initially 0x00; revision number changes only when control software should be modified.

Sub Address: 0x2E

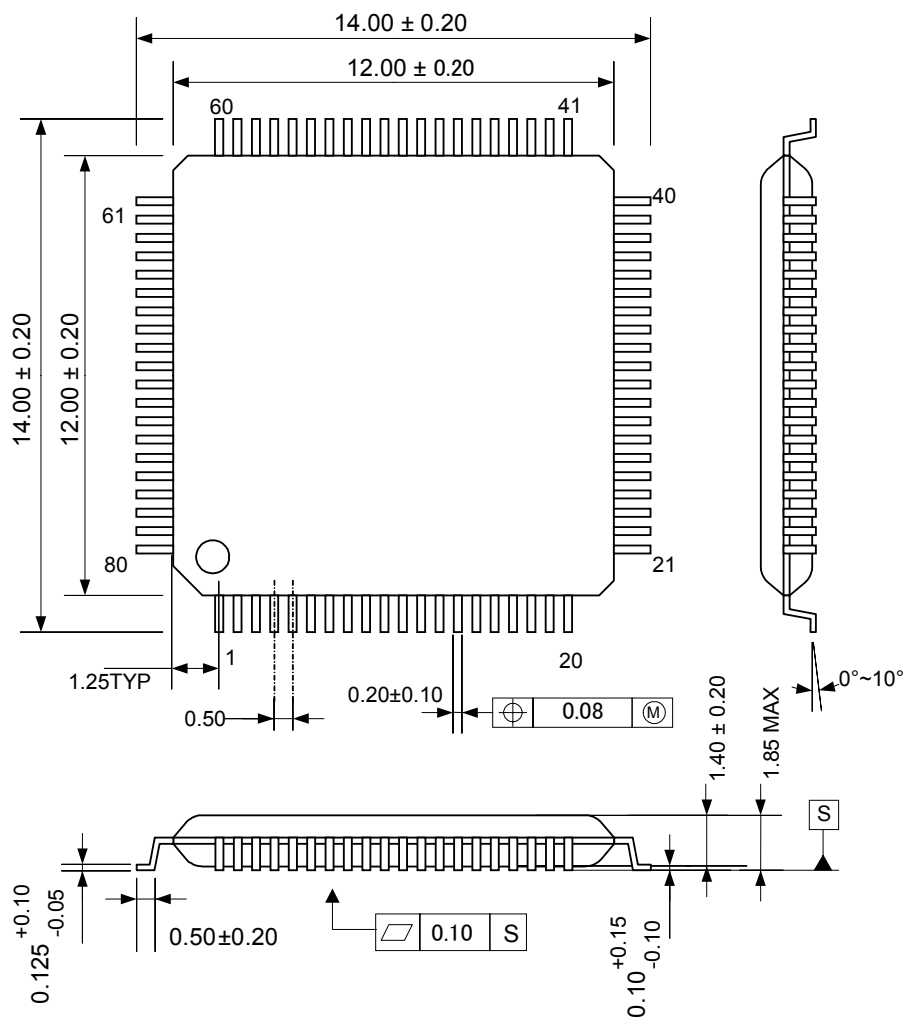
| bit 7         | bit 6 | bit 5  | bit 4  | bit 3  | bit 2  | bit 1  | bit 0  |
|---------------|-------|--------|--------|--------|--------|--------|--------|
| REV1          | REV0  | DEVID5 | DEVID4 | DEVID3 | DEVID2 | DEVID1 | DEVID0 |
| Default Value |       |        |        |        |        |        |        |
| 0             | 0     | 1      | 1      | 1      | 0      | 1      | 0      |

## Device and Revision ID Register

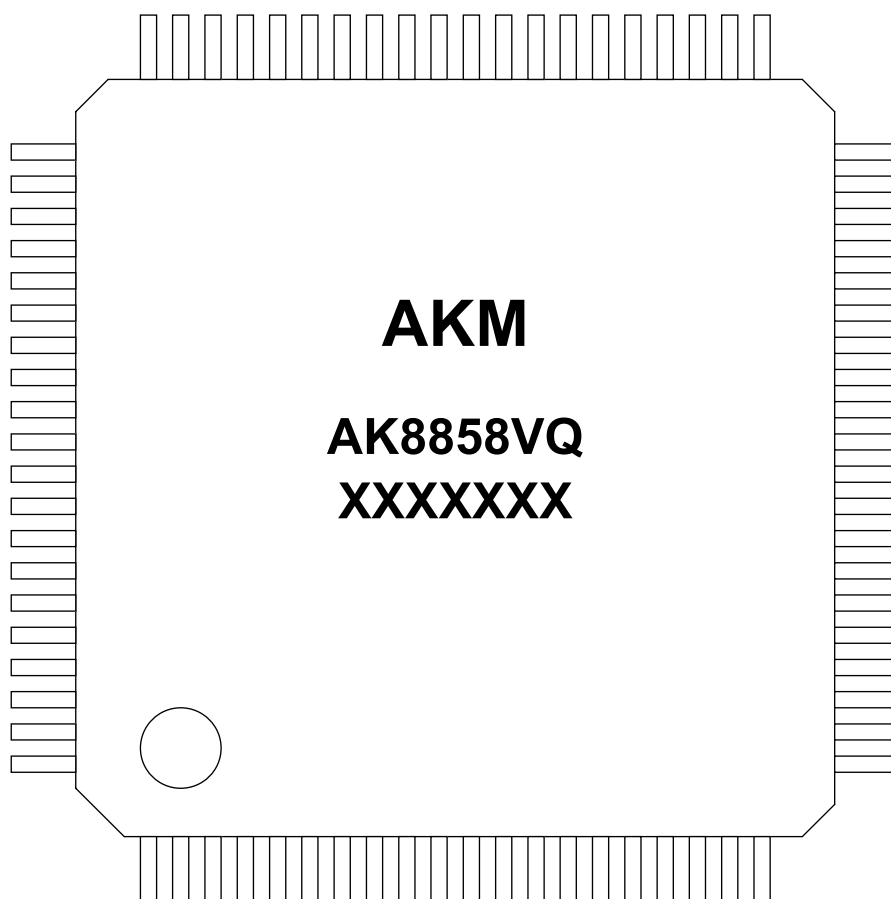
| BIT                 | Register Name         |             | R/W | Definition                             |
|---------------------|-----------------------|-------------|-----|----------------------------------------|
| bit 0<br>~<br>bit 5 | DEVID0<br>~<br>DEVID1 | Device ID   | R   | Device ID indicator (0x3A)             |
| bit 6<br>~<br>bit 7 | REV0<br>~<br>REV1     | Revision ID | R   | Revision ID indicator (initially 0x00) |

**[10] System connection example**

[11] Package  
80-pin LQFP



[12] Marking



AKM: AKM Logo  
AK8858VQ: Marketing Code  
XXXXXXX (7 digits): Date Code

**[13] Revision history**

&lt;MS1230-E-00 → MS1230-E-01&gt;

**[Writeing error, P.27]**

–Before

Sub Address: 0x03

Default Value: 0x00

| bit 7         | bit 6    | bit 5    | bit 4    | bit 3    | bit 2 | bit 1 | bit 0    |
|---------------|----------|----------|----------|----------|-------|-------|----------|
| Reserved      | Reserved | Reserved | Reserved | Reserved | CSSL  | CSSL  | Reserved |
| Default Value |          |          |          |          |       |       |          |
| 0             | 0        | 0        | 0        | 0        | 0     | 0     | 0        |

–After

Sub Address: 0x03

Default Value: 0x00

| bit 7         | bit 6        | bit 5    | bit 4         | bit 3    | bit 2 | bit 1 | bit 0    |
|---------------|--------------|----------|---------------|----------|-------|-------|----------|
| <b>VERTS</b>  | <b>CSCAN</b> | Reserved | <b>CMPSEL</b> | Reserved | CSSL  | CSSL  | Reserved |
| Default Value |              |          |               |          |       |       |          |
| 0             | 0            | 0        | 0             | 0        | 0     | 0     | 0        |

**[Writeing error, P.32]**

–Before

DATA[23:0], HD, VD\_FLD, DVAL\_FLD and NSIG pins can be Low output by register.

Sub Address: 0x17 [4:0]

–After

DATA[23:0], HD, VD\_FLD, DVAL\_FLD and NSIG pins can be Low output by register.

Sub Address: **0x07** [4:0]**[Writeing error, P.41]**

–Before

Settings for output signals for no input signal

Sub Address: 0x07 [3:2]

–After

Settings for output signals for no input signal

Sub Address: **0x0D** [3:2]



**[Writeing error, P.54]**

–Before

| Name            | Definition                                                                                                                                                                                                                                                                            |
|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| BR0<br>~<br>BR7 | $YOUT = YIN + BR$<br>YOUT: Brightness obtained by the calculation<br>YIN: Brightness before the calculation<br>BR: Brightness gain factor (register setting value)<br><br>The gain factor can be set in the range $\{-128 \sim 126\}$ in 1 step.<br>The setting is in 2's complement. |

–After

| Name            | Definition                                                                                                                                                                                                                                                                                     |
|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| BR0<br>~<br>BR7 | $YOUT = YIN + BR$<br>YOUT: Brightness obtained by the calculation<br>YIN: Brightness before the calculation<br>BR: Brightness gain factor (register setting value)<br><br>The gain factor can be set in the range $\{-128 \sim \mathbf{127}\}$ in 1 step.<br>The setting is in 2's complement. |

**[Writeing error, P.62, 90]**

–Before

|                           |                                                                                                                                 |
|---------------------------|---------------------------------------------------------------------------------------------------------------------------------|
| ST_VCEN0<br>~<br>ST_VCEN1 | Input signal color encode format indicator<br>[ST_VCEN1 : ST_VCEN0]<br>[00]: NTSC<br>[01]: PAL<br>[10]: SECAM<br>[11]: Reserved |
|---------------------------|---------------------------------------------------------------------------------------------------------------------------------|

–After

|                           |                                                                                                                                                  |
|---------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| ST_VCEN0<br>~<br>ST_VCEN1 | Input signal color encode format indicator<br>[ST_VCEN1 : ST_VCEN0]<br>[00]: NTSC<br>[01]: PAL<br>[10]: SECAM<br>[11]: <b>Component setting*</b> |
|---------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------|

\* ST\_VCEN[1:0] is [11] when Sub-Address 0x00[6:5] is set to [10] (Component video input).

**[Spec. revise, P.61]**

–Before

This function is cancellor for macrovision color stripe. Set CSCAN bit to [1].

Color stripe cancel

Sub Address: 0x03 [6]

| Name  | Definition                                                                                                                    |
|-------|-------------------------------------------------------------------------------------------------------------------------------|
| CSCAN | [0]: Color stripe on screen (Cancel function is not operated)<br>[1]: No Color stripe on screen (Cancel function is operated) |

–After

This function is cancellor for macrovision color stripe.

**Set CSCAN bit to [1] only when Sub=Address 0x04[7:0] is [XXX00000] setting.****Set CSCAN bit to [0] when Sub=Address 0x04[7:0] is not [XXX00000] setting.****(X: Don't care)**

Color stripe cancel

Sub Address: 0x03 [6]

| Name  | Definition                                                                                                                                          |
|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| CSCAN | <b>Set to [1] only when Sub=Address 0x04[7:0] is [XXX00000] setting.</b><br><b>Set to [0] when Sub=Address 0x04[7:0] is not [XXX00000] setting.</b> |

**[Spec. revise, P.68]**

–Before

|       |       |                     |     |                                                                  |
|-------|-------|---------------------|-----|------------------------------------------------------------------|
| bit 6 | CSCAN | Color stripe cancel | R/W | Color stripe cancel operation*<br>0: not operated<br>1: operated |
|-------|-------|---------------------|-----|------------------------------------------------------------------|

–After

|       |       |                     |     |                                                                                                                                                                    |
|-------|-------|---------------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| bit 6 | CSCAN | Color stripe cancel | R/W | Color stripe cancel operation<br><b>Set to [1] only when Sub=Address 0x04[7:0] is [XXX00000]</b><br><b>Set to [0] when Sub=Address 0x04[7:0] is not [XXX00000]</b> |
|-------|-------|---------------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|

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