19-0324; Rev 2; 12/97

MAXIM

1Gbps, High-Speed Limiting Amplifier with Chatter-Free Loss-of-Signal Detection

General Description

The MAX3262 limiting amplifier with its high gain and wide bandwidth is ideal for use as a post amplifier in fiber-optic receivers with data rates up to 1Gbps. The amplifier's gain can be adjusted between 33dB and 48dB. At maximum gain, signals as small as 6mVp-p can be amplified to drive devices with PECL inputs.

The MAX3262 has complementary loss-of-signal outputs for interfacing with open-fiber-control (OFC) circuitry. These outputs can be programmed to assert with input levels between 9mVp-p and 48mVp-p. LOS hysteresis for any programmed level is nominally 3.0dB, preserving a balance between noise immunity and dynamic range.

Applications

1062Mbps Fibre Channel

622Mbps SONET

Features

- **900MHz Bandwidth**
- **48dB Maximum Gain**
- **Chatter-Free LOS**
- **Programmable LOS Threshold**
- **Single +5V Power Supply**
- **Fully Differential Architecture**

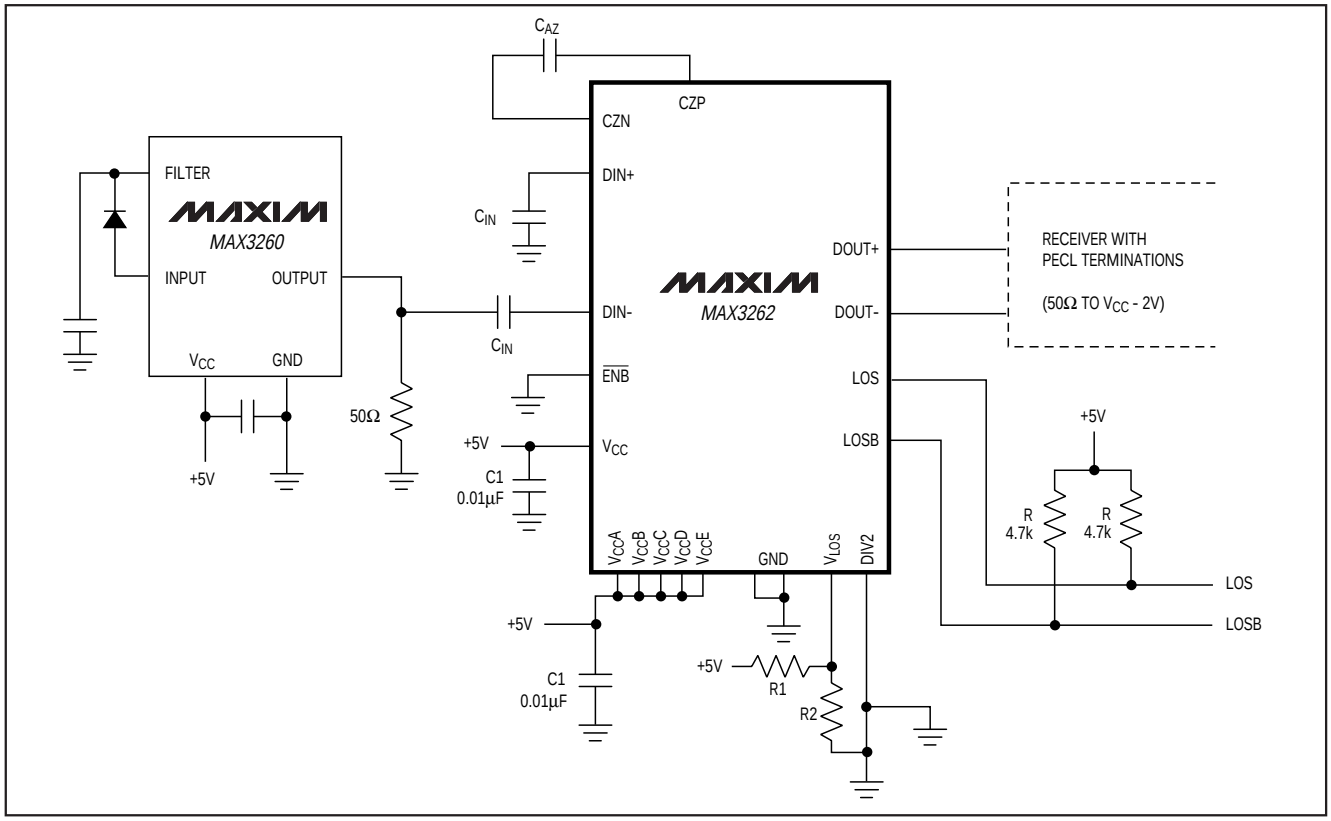
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3262CAG	0°C to +70°C (T_A)	24 SSOP
MAX3262C/D	0°C to +100°C (T_J)	Dice*

**Dice are designed to operate over this range but are tested and guaranteed only at T_A = +25°C.*

Pin Configuration appears at end of data sheet.

Typical Operating Circuit



1Gbps, High-Speed Limiting Amplifier with Chatter-Free Loss-of-Signal Detection

ABSOLUTE MAXIMUM RATINGS

Power Supply, V_{CC} - V_{EE} 6.0V
Input Voltage, DIN+, DIN- 6.0V
CZN, CZP, ENB, VLOS, DIV2, LOS+, LOS- .....-0.3V, V_{CC} + 0.3V
DOUT+, DOUT- (with 50Ω load) .....2.5V, V_{CC} + 0.3V

Continuous Power Dissipation (T_A = +70°C)
SSOP (derate 10mW/°C above +70°C) .....500mW°C
Junction Operating Temperature .....-55°C to +150°C
Storage Temperature Range .....-55°C to +175°C
Processing Temperature (Die).....+400°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, R_{LOAD} = 50Ω to V_{CC} - 2V (equivalent), T_A = 0°C to +70°C. Typical values are at V_{CC} = 5V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Current	I_{VCC}	No output load			60	mA
Enable Input Current	$I_{\overline{ENB}}$				150	µA
V_{LOS} Input Current	I_{LOS}			120		µA
Common-Mode Output Voltage		V_{CC} = 5.0V	3.5	3.7	3.8	V
LOS+, LOS- Output Low Voltage		I_{OUT} = -1.0mA			0.5	V
DIV2 Short-Circuit Current		DIV2 = 0V		0.5		mA
Differential Output Offset, DOUT+ to DOUT-					±35	mV
Input Bias Voltage	V_{DIN}		2.5		3.0	V

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, R_{LOAD} = 50Ω to 3V, AC parameters are not tested, T_A = +25°C, unless otherwise noted.)

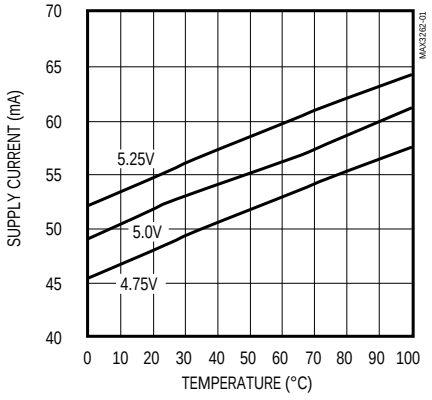
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power-Supply Rejection Ratio	PSRR	Input referred, 55MHz			35		dB
LOS Release Time, Minimum Input	t_{OFFL}	(Note 1)		0.020		0.5	µs
LOS Release Time, Maximum Input	t_{OFFH}	(Note 2)				0.5	µs
LOS Assert Time	t_{ONL}	(Note 1)			0.2	0.5	µs
Input Voltage Range	V_{ID}	Peak-to-peak		0.006		1.8	V
LOS Sensitivity Range	V_{SR}	Differential inputs, peak-to-peak	MAX3262C/D	9		48	mV
			MAX3262CAG	10		48	
LOS Hysteresis	HYS	V_{LOS} = 5V, Pattern 2^7 - 1PRBS		1.5	3.0	5.0	dB
Differential Input Noise	V_n	V_{LOS} = 5V, DIV2 = GND (Note 3)			80		µV
Pulse-Width Distortion	PWD	1Gbps, 8mVp-p input				40	ps
Output Edge Speed	t_R, t_F					250	ps
Output Voltage Amplitude	V_{OUT}	V_{OH} - V_{OL}		400	600	730	mV
Small-Signal Bandwidth	BW	MAX3262C/D		800	925		MHz
		MAX3262CAG		750	810		

Note 1: Input is a 200MHz square wave, t_R < 300ps, 8mVp-p.
Note 2: Input is a 200MHz square wave, t_R < 300ps, 1.8Vp-p.
Note 3: Input-referred noise = RMS output noise/low-frequency gain.

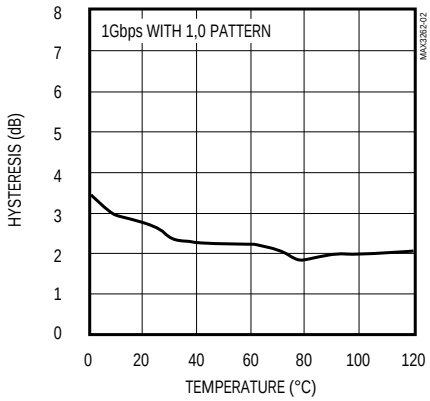
Typical Operating Characteristics

(V_{CC} = 5V, T_A = +25°C, unless otherwise noted.)

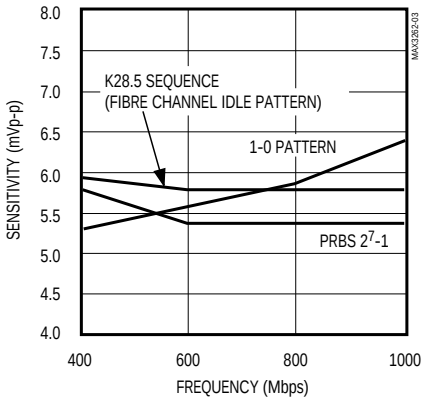
V_{CC} SUPPLY CURRENT (NO OUTPUT LOAD) vs. TEMPERATURE



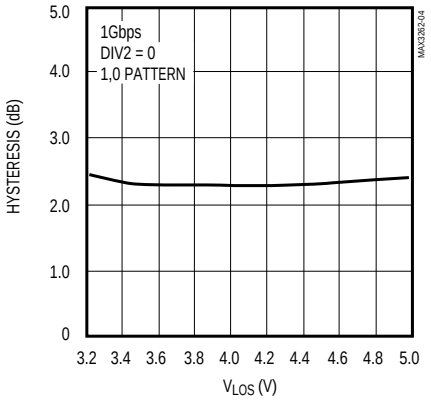
LOS HYSTERESIS vs. TEMPERATURE



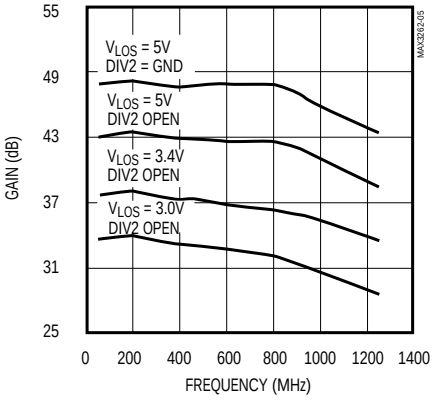
LOS SENSITIVITY vs. FREQUENCY



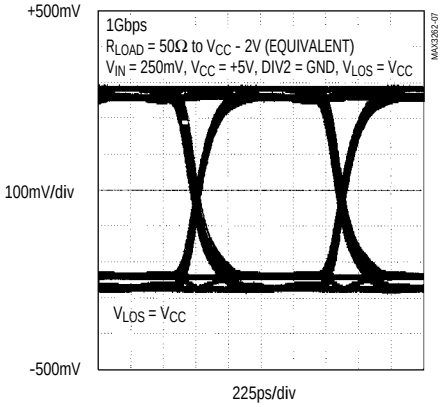
LOS HYSTERESIS vs. V_{LOS}



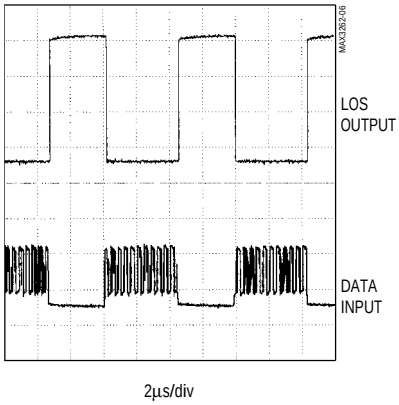
FREQUENCY RESPONSE



EYE DIAGRAM



LOS OPERATION



1Gbps, High-Speed Limiting Amplifier with Chatter-Free Loss-of-Signal Detection

Pin Description

PIN	NAME	FUNCTION
1	$V_{CC}B$	Positive supply for internal gain stages
2	V_{LOS}	Power detect/LOS level set. Use this input to program the required threshold level for LOS assertion.
3	CZP	Offset-correction loop compensation capacitor. This pin should be connected to the CZN pin through a 100nF to 330nF capacitor, which provides the dominant pole for the offset-correction loop.
4	CZN	Offset-correction loop compensation capacitor. This pin should be connected to the CZP pin through a 100nF to 330nF capacitor, which provides the dominant pole for the offset-correction loop.
5	$V_{CC}A$	Power supply for the input stage amplifier
6	DIN+	Data Input
7	DIN-	Inverting Data Input
8	GND	Ground for the input stage amplifier
9	$\overline{ENB}$	Output Enable. Output gain stage is disabled and LOS circuitry remains functional.
10	DIV2	Input stage gain adjust. Grounding this pin forces the input stage gain to maximum (11dB) for applications where the LOS threshold level will be set for input signals in the 9mVp-p to 20mVp-p range. Leaving this pin open forces the gain of the input stage to be divided by two (6dB) for applications where the LOS threshold level will be set for input signal levels in the 15mVp-p to 48mVp-p range.
11	VTH	Comparator threshold voltage for test only. Leave unconnected.
12	$V_{CC}E$	Positive supply for the power detect/LOS circuitry
13	GND	Ground for the power detect/LOS circuitry
14	GND	Ground for the LOS+/LOS- buffer circuitry
15	$V_{CC}D$	Positive supply for the LOS+/LOS- buffer circuitry
16	LOS-	Loss-of-Signal detect. This pin is asserted low when input power drops below the LOS threshold level.
17	LOS+	Loss-of-Signal detect. This pin is asserted high when input power drops below the LOS threshold level.
18	DOUT-	Inverting Data Output
19	DOUT+	Data Output
20	GND	Substrate Ground
21	$V_{CC}C$	Positive supply for bias generators
22	GND	Ground for bias generators
23	V_{CC}	Positive supply for output buffers
24	GND	Ground for internal gain stages

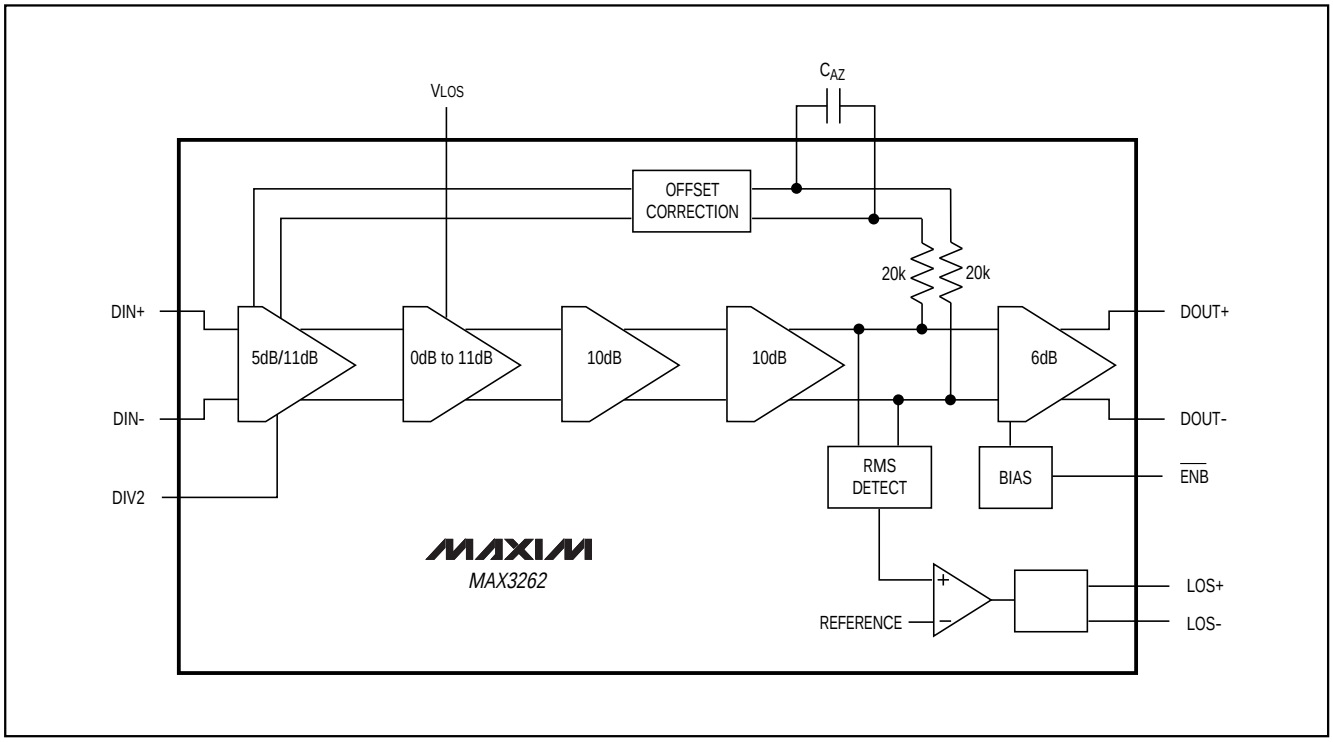


Figure 1. Functional Diagram

Detailed Description

The MAX3262 is an integrated limiting amplifier intended for high-frequency fiber-optic applications. The circuit connects to typical transimpedance amplifiers found within a fiber-optic link. The linear signal output from a transimpedance amplifier can contain significant amounts of noise, and may vary in amplitude over time. The MAX3262 limiting amplifier quantizes the signal, and outputs a voltage-limited waveform over a 48dB input dynamic range.

The MAX3262 provides an offset correction function that effectively reduces the offset voltage to negligible levels. In communications systems using NRZ data with a 50% duty cycle, pulse-width distortion present in the signal or generated by the transimpedance amplifier appears as input offset and is partially removed by the offset correction function. An external capacitor is required between CZP and CZN to compensate the offset correction loop, determining the lower 3dB point.

Loss-of-Signal Function

The MAX3262 incorporates a chatter-free loss-of-signal function, which is used to detect that the input signal has dropped below the level necessary for acceptable bit error rate performance, or to indicate an open-fiber condition. The loss-of-signal function is implemented with a rectifying peak detector, which samples the signal entering the output stage. The output from the peak detector is compared against an internally generated threshold, and is used to assert the LOS+ and LOS- outputs.

The loss-of-signal threshold is adjusted by varying the amplifier gain. The MAX3262 is configurable for gains between 33dB and 48dB, allowing LOS thresholds between 9mVp-p and 48mVp-p. Figure 2 shows the LOS threshold as a function of the DIV2 and V_{LOS} pins. The DIV2 pin provides a coarse adjustment of 6dB of gain, while the V_{LOS} pin provides a fine gain adjustment between 0dB and 11dB.

1Gbps, High-Speed Limiting Amplifier with Chatter-Free Loss-of-Signal Detection

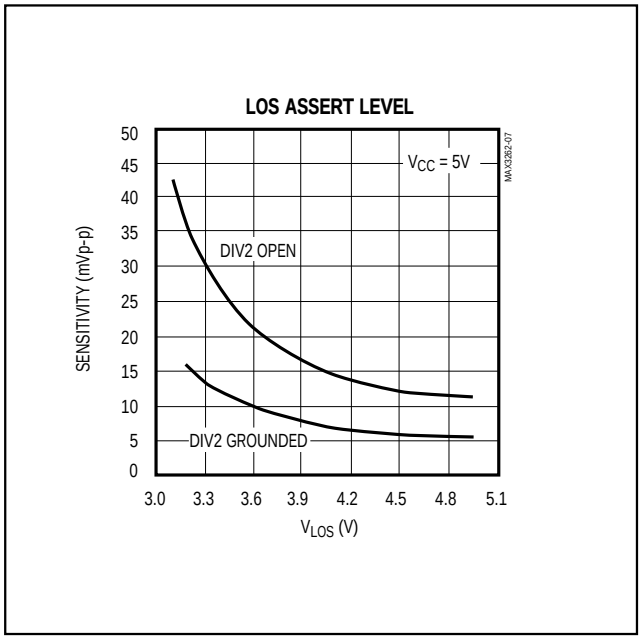


Figure 2. MAX3262 Sensitivity vs. V_{LOS} Setting

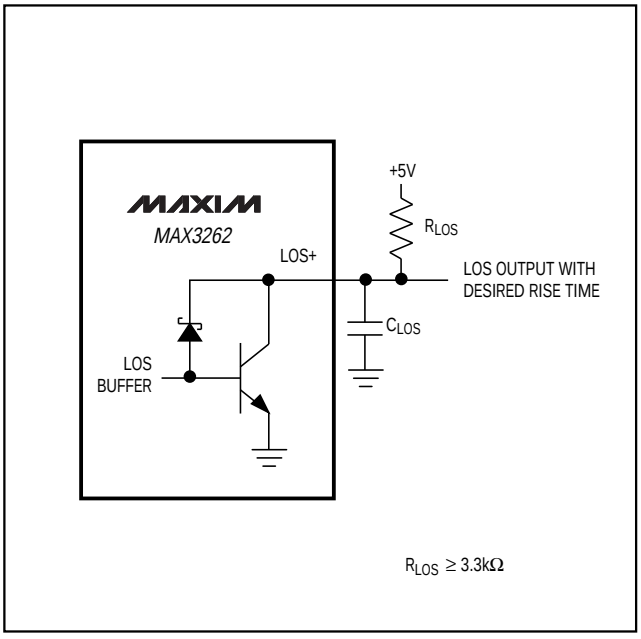


Figure 3. Setting the LOS Time Constant

Level-detect hysteresis and a 200ns internal delay ensure chatter-free LOS outputs when the input signal level is close to the LOS threshold. The hysteresis for any programmed loss-of-signal level is nominally 2.5dB.

The LOS+ and LOS- outputs are open-collector, Schottky-clamped transistors, that require pull-up resistors for proper operation (Figure 3). The loss-of-signal time constant is set externally with the appropriate pull-up resistor and shunt load capacitance.

The $\overline{ENB}$ pin allows the user to disable the output signal without removing the input signal.

Wire Bonding Die

For reliable operation, the MAX3262 has gold metalization. Connections to the die should be made with gold wire only, using ball bonding techniques. Wedge bonding is not recommended. Bond pad size is 4 mils.

Design Procedure

Determining Capacitor Values

The MAX3262 inputs must be AC coupled to allow proper operation of the offset correction function. Figure 4 shows the circuit's input stage. The circuit's lower -3dB point is determined by the input coupling capacitors. The lower -3dB frequency is $1 / [(2\pi)(1500\Omega)(C_{IN})]$ Hz.

C_{IN} should be large enough to not affect the signal quality, but small enough to not affect the LOS assert time. When an open-fiber condition occurs, the input coupling capacitors must discharge below the LOS threshold level before the LOS can assert. The worst-case discharge time would occur with the maximum input signal and the minimum LOS threshold. In this case, the input capacitor must discharge from 0.9V to 4.5mV. The time required for this to occur is:

$$t = (1500)(C_{IN})\ ln(V_{MAX} / V_{THRESH})\ seconds$$

Example: If the MAX3262 is configured for 6mV sensitivity, C_{IN} = 100pF results in a lower -3dB frequency of 1MHz, and a maximum LOS delay of about 1µs.

The offset correction capacitor (C_{AZ}) must be greater than 100nF to ensure stable operation. This capacitor is in series with an internal 40kΩ of resistance. The -3dB point of the offset zeroing circuit is:

$$1 / [(2\pi)(C_{AZ})(40k\Omega)]\ Hz$$

For C_{AZ} = 180nF, the bandwidth of the offset correction circuit is 22Hz. Maxim's proprietary offset-correction architecture decouples the input coupling time constant from the offset correction time constant. This ensures there is no interaction between these two networks, eliminating an additional source of chatter on LOS.

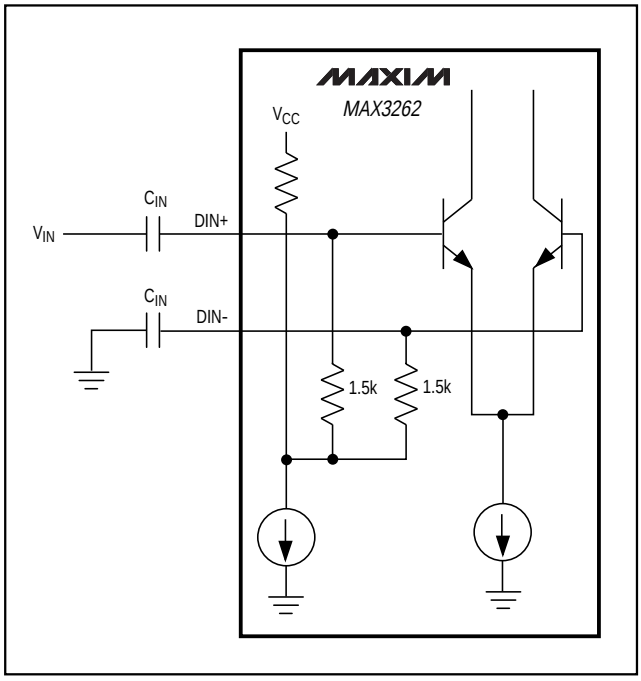


Figure 4. MAX3262 Equivalent Input Circuit

Output Termination

The MAX3262 outputs must be terminated with a 50Ω load to (V_{CC} - 2V), or a Thevenin equivalent. Figure 5 shows two possible output termination methods.

Layout and PC Board Design

Since the MAX3262 is a high-frequency component, the circuit's performance can largely be determined by board layout and design. A common problem with high-gain amplifiers is feedback from the large swing outputs to the input via the power supply. Some fiber-optic limiting amplifiers suffer from LOS "chatter." The act of switching the LOS outputs on or off generates noise on the power supply, which can cause the LOS outputs to chatter. With proper board layout, the MAX3262 ensures chatter-free LOS operation.

The MAX3262 has five ground pins and a substrate connection. All of these should be connected to the circuit board's ground. Use multiple PCB vias close to the part to connect the grounds. Avoid long, inductive runs, which can degrade MAX3262 performance. The MAX3262's six V_{CC} supply pins must all be connected. V_{CC}A–V_{CC}E can be collectively decoupled with one capacitor. V_{CC} (pin 23) should be decoupled separately (see the *Typical Operating Circuit*).

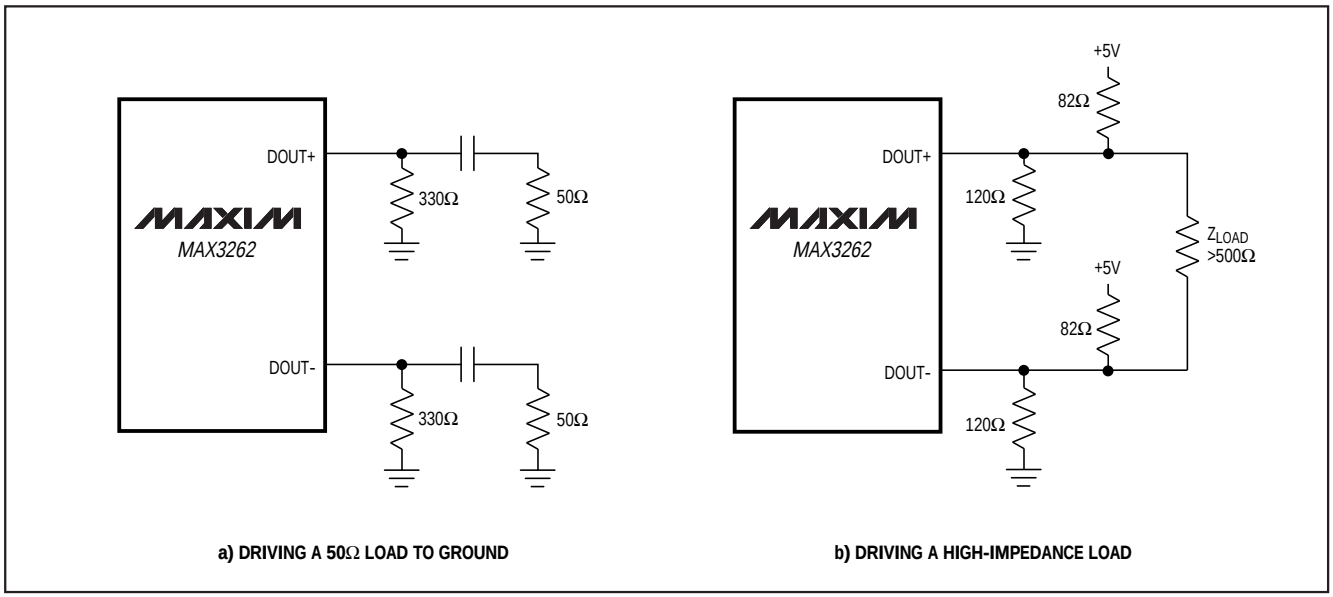


Figure 5. Output Termination Techniques

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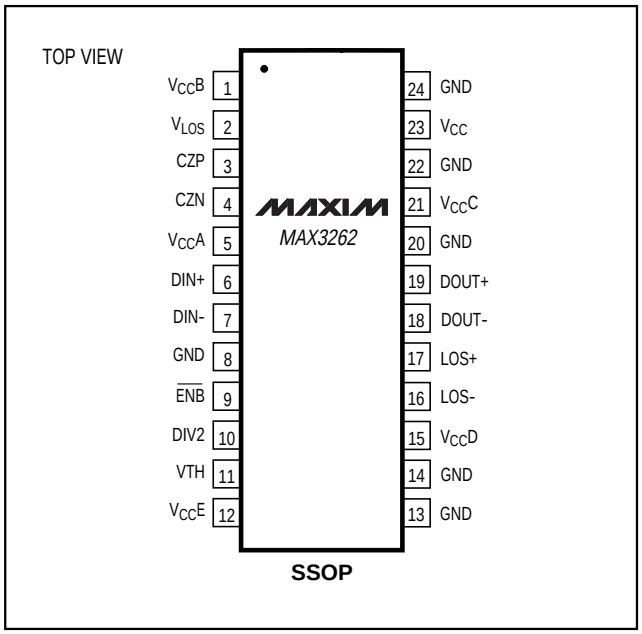
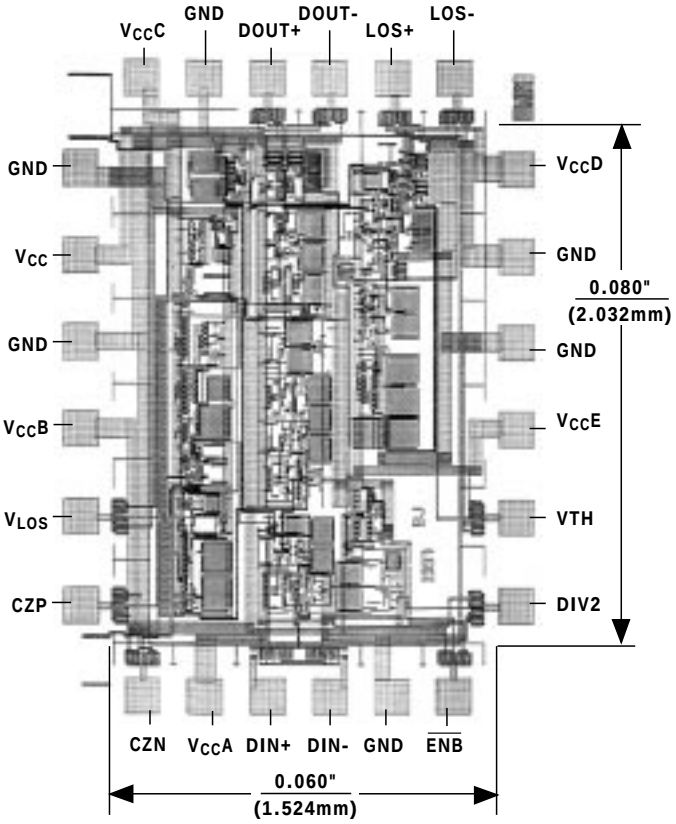
Pin Configuration



Chip Topography



TRANSISTOR COUNT: 200

SUBSTRATE CONNECTED TO GND PIN 17