

TRF3701/TRF3702 ***Quadrature Modulator*** ***Evaluation Module***

User's Guide

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Preface

Read This First

About This Manual

This user's guide describes the configuration of the of the TRF3701/2 evaluation module (EVM), modes of operation, function, and the physical characteristics.

How to Use This Manual

This document contains the following chapters:

- Chapter 1 - Overview
- Chapter 2 - Physical Description
- Chapter 3 - Circuit Description
- Chapter 4 - Circuit Board Test Points
- Chapter 5 - Schematic

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Overview

This document relates to the TRF3701/TRF3702 direct launch quadrature modulator for applications in the transmit path of base stations and communications equipment. The TRF3701 operates between 400 MHz and 1.5 GHz and the TRF3702 between 1.5 GHz and 2.5 GHz. A quadrature modulator is used for up conversion of signals from the transmit chain DAC to the RF power amplifier device. Evaluating a modulator complex performance involves careful bias voltage setup, an LO signal and at least two signals (I/Q) at the input to the modulator. This document describes the wide range of test options available with this EVM and the factors that must be considered in using the EVM.

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1.3 Power Requirements	1-2
1.4 TRF3701/2 EVM Operating Procedure	1-3

1.1 Purpose

The TRF3701/TRF3702 evaluation module (EVM) is intended for the evaluation of the TRF3701 and TRF3702 direct launch quadrature modulator. Unless otherwise stated, the functionality described in this manual applies to both the TRF3701 and TRF3702 devices.

1.2 EVM Circuit Overview

The EVM comes configured for differential I/Q input signals via four SMA connectors as shown in the schematic and Table 1-1.

The EVM has an option for differential I/Q input signals via the two THS4503 op amps as shown in the schematic and Table 1-1. The THS4503 (U2, U3) provides single-ended/differential inputs and outputs in an 8-pin package. The device has a unity gain bandwidth of 370 MHz, a slew rate of 2800 V/ μ s, and a IMD3 –95 dBc at 30 MHz. The outputs from U2 and U3 are applied to the TRF3701/TRF3702 quadrature modulator IC.

The I signals are connected to J4 (I+) and J8 (I-), respectively. The Q signals are connected to J5 (Q+) and J11 (Q-), respectively. The LO signal is fed to J2 and the SMA connector J3 is used to monitor the output signal from the quadrature modulator (U1).

The quadrature modulator requires a supply voltage of 5 V / 145 mA from a regulated power supply. Both the amplifiers (U2, U3) and the TRF3701/TRF3702 are powered from external power supplies connected to connector J1. The op amp supply voltage must not exceed ± 7.5 V.

The TRF3701/TRF3702 quadrature modulator requires a dc common mode bias voltage (3.7 Vdc) on all four input pins. Power supply connectors J6 and J13 accept these voltages from an external power supply.

1.3 Power Requirements

The EVM has three dc-power supply connectors: J1 accepts ± 7 V for op amp supply and a V_{CC} of 5 V for the TRF3701/TRF3702. J6 accepts the VCM (3.7 V) common-mode bias voltage for the TRF3701/TRF3702. J13 accepts the VCM (3.7 V) input signal common-mode bias when using op amps U2 and U3.

Voltage Limits

Exceeding the ± 7.5 V maximum may damage the THS4503 op amp.

Exceeding 5.6 V may damage the TRF3701/2

1.4 TRF3701/02 EVM Operating Procedure

Set up the EVM as follows:

- 1) Verify all settings against Table 1-1.

Table 1-1. EVM Configuration

Configuration Table	
Op-Amp	No Op-Amp
Single-Ended Inputs Available – TRF370x Driven Single-Endedly	DC-Coupled Differential Inputs Available – TRF370x Driven Differentially (Default Configuration)
W5 pins 1-2, W1, W3, W7, W8, W9, W10, R6, R7, R13, R15, R12 [†] , R14 [†] , R17 [†] , R18 [†] , C53-C56 [†] , W2 [†] , W4 [†] Apply dc offset (VCM = 3.7 Vdc) to J13. Adjust VCOM1 and VCOM2 externally to optimize. Apply I signal to J4, Q to J5.	W5 pins 1-2, W1 [†] , W3 [†] , W7 [†] , W8, W9 [†] , W10, W2, W4, R12-R15 [†] , (C53 -C56)⇒ replace with 0 Ω , (R29-R32)⇒ if 50- Ω termination required. All dc offsets adjusted externally. Apply I signal to J9, $\bar{I}$ to J7, Q to J12, $\bar{Q}$ to J10.
Differential Inputs Available – TRF370x Driven Differentially	DC-Coupled Single-Ended Inputs Available – TRF370x Driven Single-Endedly
W5 pins 1-2, W2, W4, W8, W10, R12-R15, R6 [†] , R7 [†] , R17, R18, C53-C56 [†] , W1 [†] , W3 [†] , W7 [†] , W9 [†] Apply dc offset (VCM = 3.7 Vdc) to J13. Adjust VCOM1 and VCOM2 externally to optimize. Residual dc can be applied to op-amp inputs for adjusting the complementary inputs if desired. Apply I signal to J4, /I to J8, Q to J5 and /Q to J11.	W5 pins 1-2, W1, W3, W7 [†] , W8, W9 [†] , W10, W2 [†] , W4 [†] , R12-R15 [†] , (C54, C56)⇒ replace with 0 Ω , C53 [†] , C55 [†] , (R30, R32)⇒ if 50- Ω termination required. Apply dc offset (VCM = 3.7 Vdc) to J6 and adjust R33 and R34 to optimize the dc offset level of the complementary I, Q inputs. Apply I signal to J9, Q to J12.
Single-Ended Inputs Available – TRF370x Driven Differentially	AC-Coupled Single-Ended Inputs Available – TRF370x Driven Single-Endedly
W5 pins 1-2, W2, W4, W8, W10, R12-R15, R6, R7, R17 [†] , R18 [†] , C53-C56 [†] , W1 [†] , W3 [†] , W7 [†] , W9 [†] Apply dc offset (VCM = 3.7 Vdc) to J13. Adjust VCOM1 and VCOM2 externally to optimize. Residual dc can be applied to op-amp inputs for adjusting the complementary inputs if desired. In this case, follow the connections of the section above (differential drive). Apply I signal to J4, Q to J5.	W5 pins 1-2, W1, W3, W7, W8, W9, W10, W2 [†] , W4 [†] , R12-R15 [†] , C54, C56, C53 [†] , C55 [†] , (R30, R32)⇒ if 50- Ω termination required. Apply dc offset (VCM = 3.7 Vdc) to J6 and adjust R33 and R34 to optimize. Apply I signal to J9, Q to J12.
	AC-Coupled Differential Inputs Available – TRF370x Driven Differentially
	W5 pins 1-2, W1, W3, W7, W8, W9, W10, W2, W4, R12-R15 [†] , C54, C56, C53, C55, (R29-R32)⇒ if 50- Ω termination required. Apply dc offset (VCM = 3.7 Vdc) to J6 and adjust R33 and R34 to optimize. Apply I signal to J9, $\bar{I}$ to J7, Q to J12, $\bar{Q}$ to J10.

[†] Remove from circuit

- 2) Connect the regulated power supplies to the EVM as follows:
 - a) Switch on the V_{CC} (5 V) supply and verify that the current drawn is approximately 130 - 140 mA.
 - b) Switch on the VCM (3.7 Vdc) precision regulated bias voltage supply connected to J6 (if needed).

- c) Switch on the ± 7 -V op amp supply, then turn on the precision regulated power supply connected to J13, set to VCM, and used to provide the VCOM1 and VCOM2 voltages (if needed).
- 3) Use a suitable 50- Ω output signal generator to supply the LO signal: 0 dBm.
- 4) Use an arbitrary waveform generator to provide the I/Q input signals. A typical setup is as follows: a 1-Vp-p sine wave, a frequency of 900 KHz, a dc-offset of 0 V, and an output impedance 50- Ω .
- 5) Connect a spectrum analyzer to the SMA connector marked RFOUT (J3) and monitor the TRF3701/TRF3702 output.
- 6) To optimize the carrier suppression, this modulator performs the following (if using on-board dc offset through J3):
 - a) Connect a spectrum analyzer to output port J3, rotate R33 to decrease the LO feed through as required.
 - b) Then rotate R34 to further decrease the LO feed through.
 - c) Repeat this procedure until you obtain the minimum LO feed through. A typical optimized sideband suppression value is 60 dBc.
- 7) Use an arbitrary waveform generator to suppress the sideband. Adjust the I/Q amplitude and phase of the CW signal coming from the arbitrary waveform generator. A typical optimized side band suppression value is 60 dBc.

Physical Description

This chapter discusses the four layer PCB layout, component placement, and list of components used on the evaluation module.

Topic	Page
2.1 PCB Layout	2-2
2.2 Parts Llists	2-5

2.1 PCB Layout

The EVM is constructed on a four layer, 76 mm x 76 mm x 1,575 mm thick PCB using FR-4 material. Figure 2-1 through Figure 2-4 show the individual layers.

Figure 2-1. Top Layer

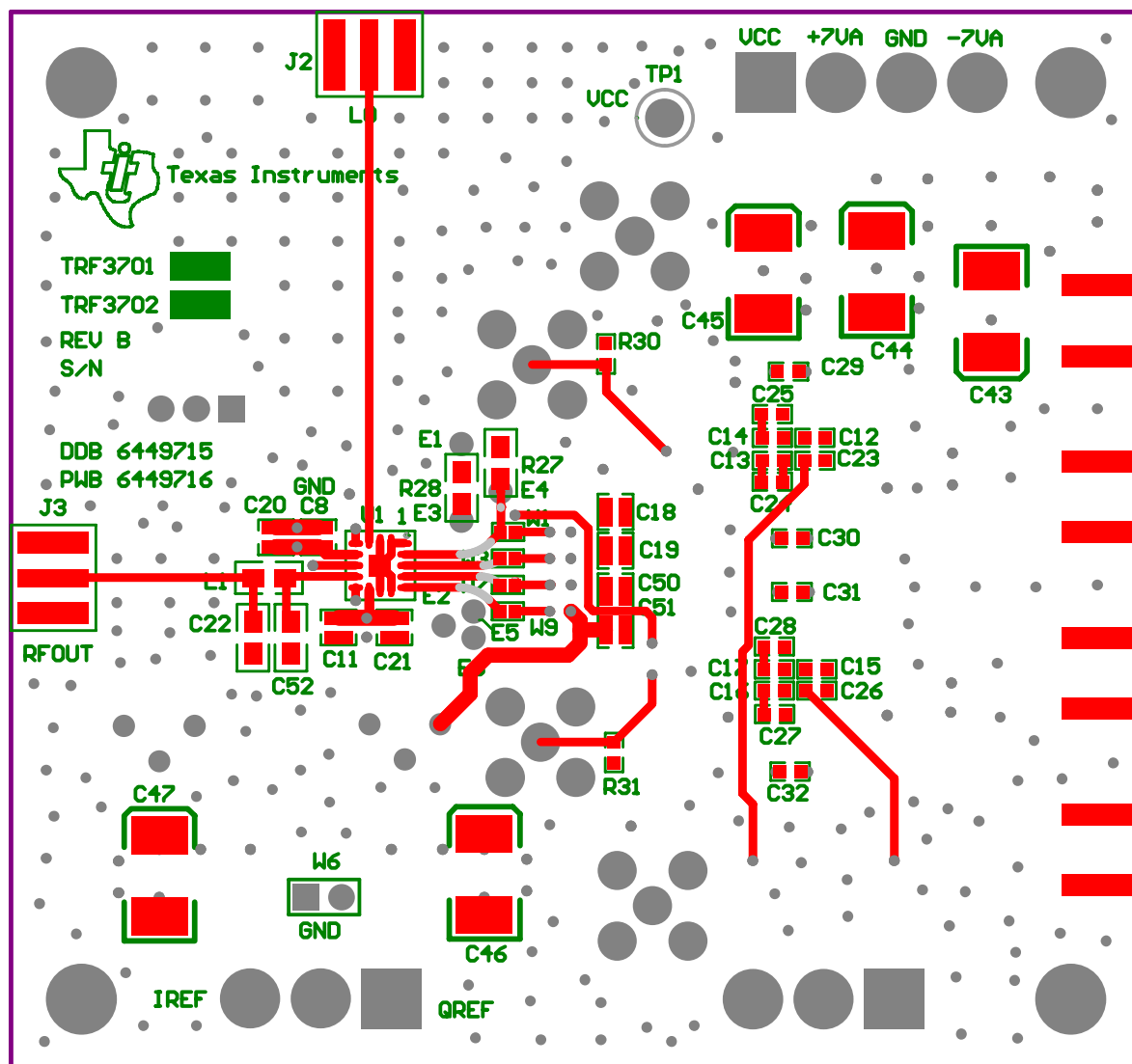


Figure 2-2. Layer 2—Ground Plane

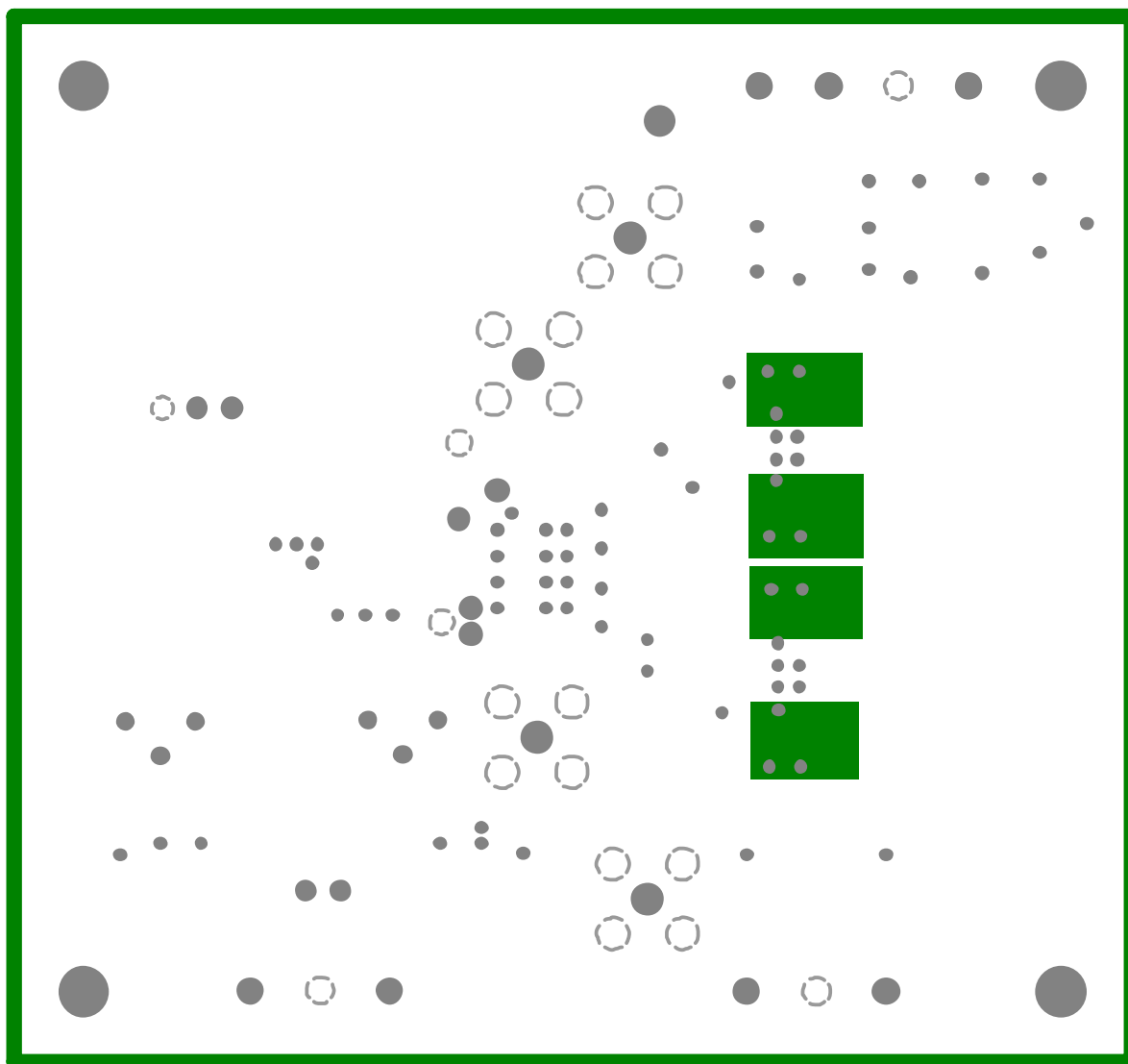


Figure 2-3. Layer 3—Power Plane

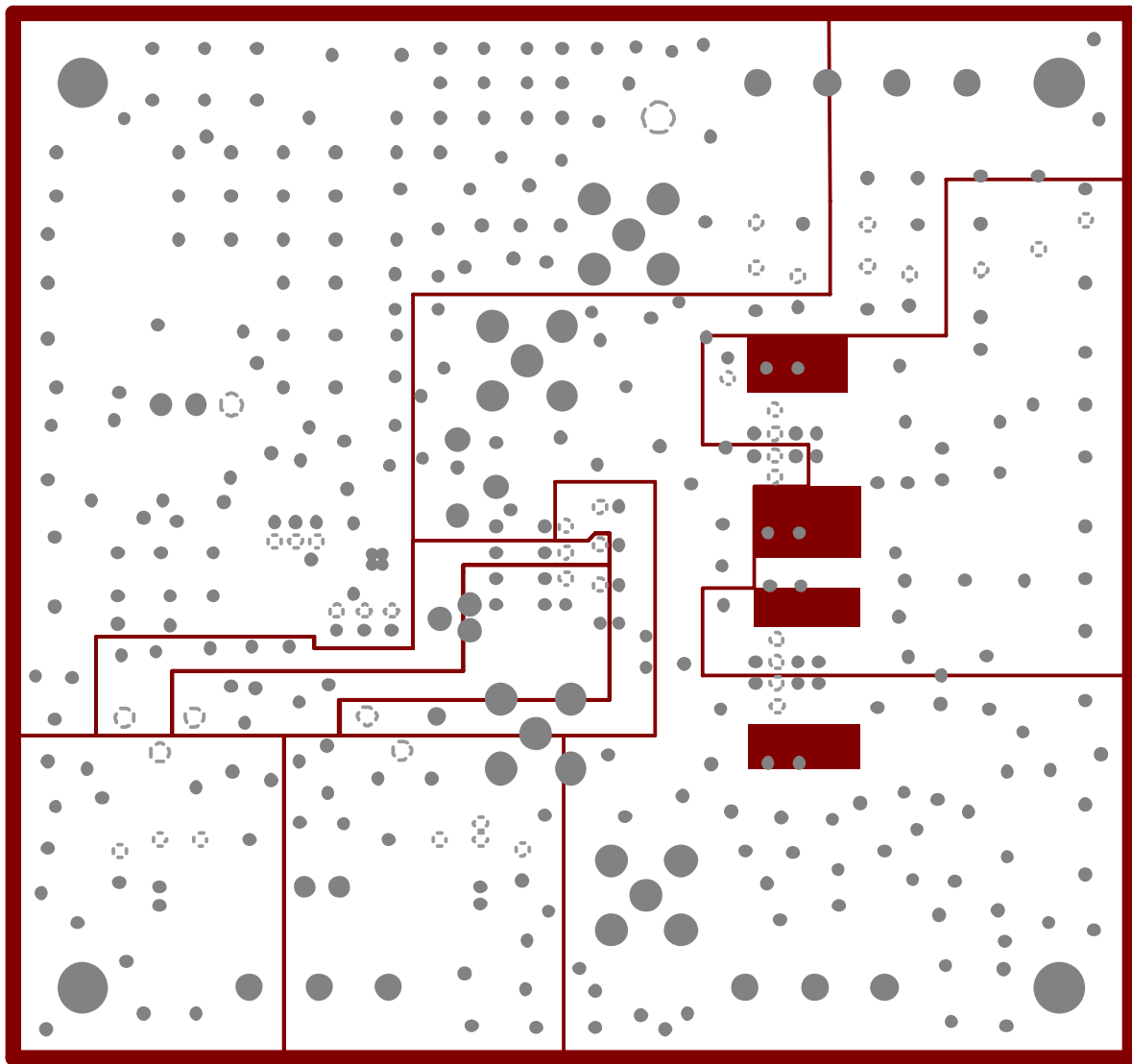
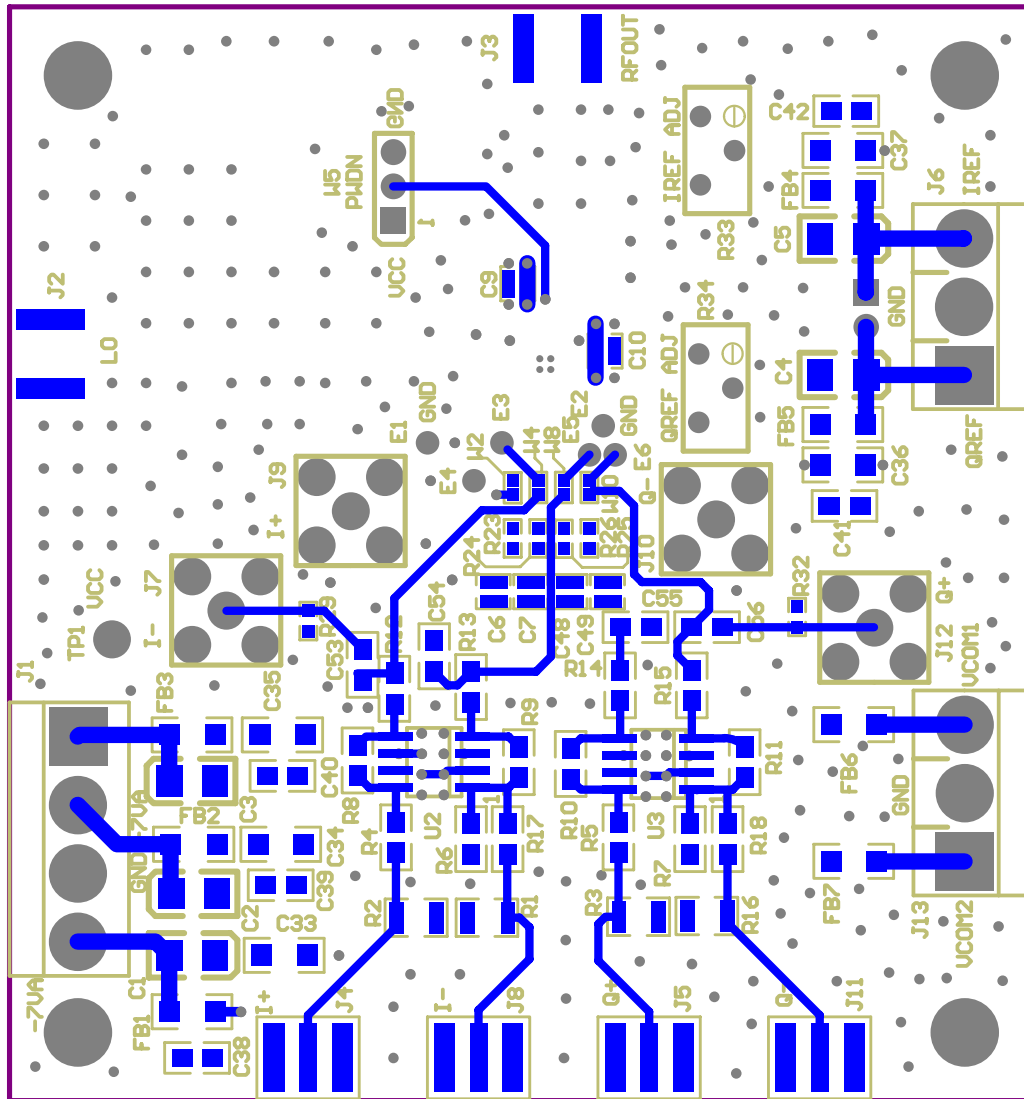


Figure 2-4. Bottom Layer



2.2 Parts List

Table 2-1. Parts List

Description	Footprint	Qty	Part Number	MFR	Reference Description	Not Installed
47 μ F, tantalum, 10%, 10 V	7343	5	10TPA47M	Sanyo	C43-C47	
0.1 μ F, 16 V, 10% capacitor	508	8			C6-C11, C48, C49	
0.1 μ F, 16 V, 10% capacitor	603	6	ECJ-1VB1C104K	Panasonic	C12-C17	
10 μ F, 10 V, 10% capacitor	3528	5	GRM42X5R106K10	Murata	C1-C5	
0.01 μ F, 50 V, 10% capacitor	603	6		AVX	C23-C28	
1 pF, 50 V, 10% capacitor	603	6		AVX	C18-C21, C50, C51	
1 μ F, 16 V, 10% capacitor	1206	5			C33-C37	
1800 pF, 50 V, 10% capacitor	805	0				C22, C52
10 pF, 50 V, 10% capacitor	603	4	PCC120ACVCT	AVX	C29-C32	
0.01 μ F, 16 V, 10% capacitor	805	5			C38-C42	
Ferrite bead	1206	7			FB1-FB7	
392- Ω resistor, 1/10 W, 1%	805	4	ERJ-6ENF392R0V	Panasonic	R8-R11	
374- Ω resistor, 1/10 W, 1%	805	4	ERJ-6ENF374R0V	Panasonic	R4, R5, R17, R18	
402- Ω resistor, 1/10 W, 1%	805	0	ERJ-6ENF402R0V	Panasonic		R6, R7
56.2- Ω resistor, 1/16 W, 1%	1210	4	ERJ-13NF56R2	Panasonic	R1-R3, R16	
1-k Ω resistor, 1/16 W, 1%	603	4	ERJ-3EKF1.00K	Panasonic	R23-R26	
49.9- Ω resistor, 1/16 W, 1%	603	0	ERJ-3EKF49R9V	Panasonic		R29-R32
22.1- Ω resistor, 1/10 W, 1%	805	0		Panasonic		R12-R15
0- Ω resistor, 1/10 W, 1%	603	0	ERJ-3EKF0R00V	Panasonic		R27, R28
0- Ω resistor, 1/10 W, 1%	805	5	ERJ-6ENF0R00V	Panasonic	L1, C53-C56	
10 k Ω Pot	BOURNS_3296Y	2	3296Y-103	Bourns	R33, R34	
SMA connectors	SMA_Jack	4	2262-0000-09	Macom	J7, J9, J10, J12	
3POS_header	3pow_jumper	1	TSW-150-07-L-S	Samtec	W5	
2POS_header	2pos_jumper	1	TSW-150-07-L-S	Samtec	W6	
2POS solder jumpers		8			W1-W4, W7 - W10	
SMA connectors	SMA_END_SMA	6	90F2624	Newark	J2-J5, J8, J11	
3-pin power connector		2	93F7124	Newark	J6, J13	
3-pin power mate		2	95F5347	Newark		P6, P13
4-pin power connector		2	93F7125	Newark	J1	
4-pin power mate		1	95F5348	Newark		P1
THS4503	8-SOP (D)	2	THS4502ID	Texas Instruments	U2, U3	
TRF3701 or TRF3702	16-RHC (QFN)	1	TRF3701 or TRF3702	Texas Instruments	U1	
Screws	4-40 screw	4				

Circuit Description

This chapter discusses the various functions of the EVM.

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3.1 Circuit Function	3-2

3.1 Circuit Function

Two quad sets of SMA connectors are provided on the EVM for inputting differential I/Q signals via the op amp or directly to the input pins of TRF3701/TRF3702. Connectors J4, J8, J5, and J11 are for connecting the I/Q signals via the op amp, while connectors J7, J9, J10, and J12 are used to directly connect the signal source I/Q signals to the TRF3701/TRF3702.

3.1.1 Differential/Single-Ended Inputs via Buffer Amplifiers

Connectors J4, J8, J5, and J11 are used to dc-couple differential signal pairs I+, I- and Q+, Q- to the unity gain differential buffer amplifier U2 and U3. For a gain of two, change the value of R8, R9, R10, and R11 to 825 Ω .

For single-ended input, the I-channel input signal can be applied to either J4 or J8. However, the EVM is configured to accept the single ended I-channel signal on J4.

The Q-channel input is via J5.

3.1.2 Differential/Singled-Ended Inputs Without Buffer Amplifier

Direct I/Q inputs, without the op amp, are routed to the TRF3701/TRF3702 through another set of SMA connectors, namely: J7, J9, J10, and J12.

3.1.3 Power Down

The EVM has a 3-position jumper (W5) for controlling the operation of the device. For normal operation W5 pins 1-2 are shorted. In power-down mode, W5 pins 2-3 are shorted.

3.1.4 Input Pins Bias

The TRF3701/TRF3702 I/Q input pins common-mode bias voltage is provided either through J6 and adjusted by potentiometers R33 and R34 or via the op amp VCOM1 and VCOM2 inputs through J13.

3.1.5 Power

Power is supplied to the EVM via header J1. Header J1 is a Molex 861904 4-pin male connector, and allows easy connection to a standard bench power supply through a Molex 860504 4-pin female connector. The connector pin outs are listed in Table 3-1.

Table 3-1. Power Supply J1

J1 Pin	Description
1	5 V (V_{CC}), U1 analog supply
2	7 V, op amp supply
3	AGND
4	-7 V, op amp supply

Connectors J6 and J13 are used to supply the dc bias voltage to U1 I/Q input channels. Both connectors are a 3-position male Molex header (part number 8610903).

Table 3-2. CM Bias Voltage

J6 Pin	Description
1	QREF1, QREF2 ($V_{CM} = 3.7$ Vdc)
2	AGND
3	IREF1, IREF2 ($V_{CM} = 3.7$ Vdc)

Table 3-3. CM Bias Voltages via Op Amp

J13 Pin	Description
1	VCOM2 ($V_{CM} = 3.7$ Vdc)
2	AGND
3	VCOM1 ($V_{CM} = 3.7$ Vdc)



Circuit Board Test Points

This chapter shows the circuit board test points.

Topic	Page
4.1 Circuit Board Test Point Locations	4-2

Figure 4-1. Silkscreen Top Layer—Test Points Location

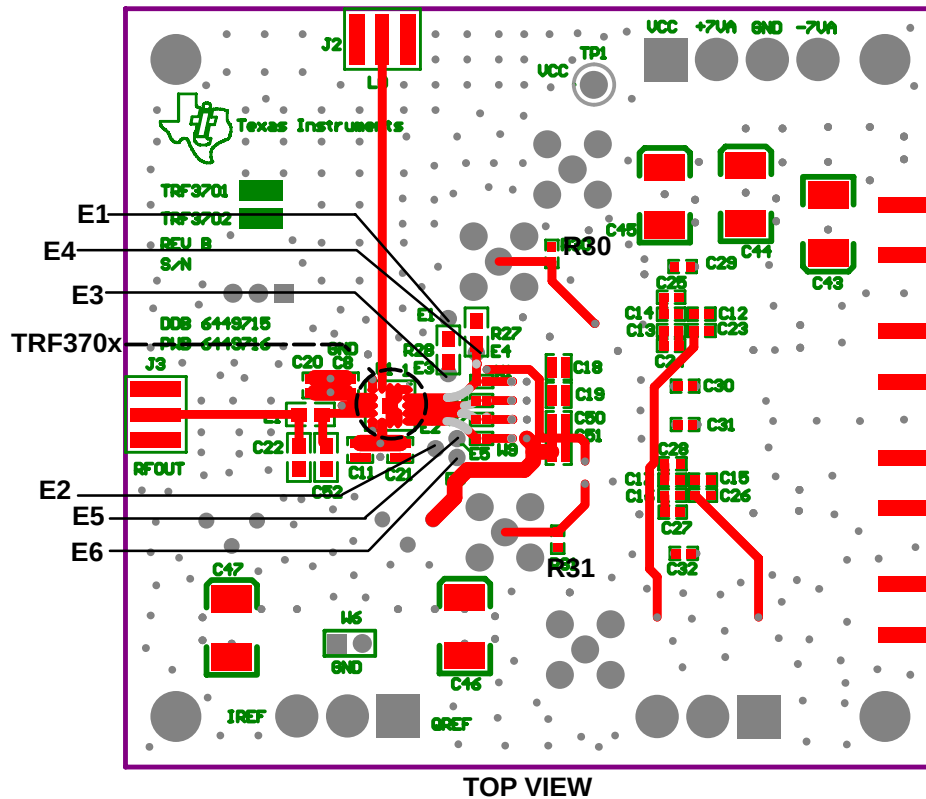
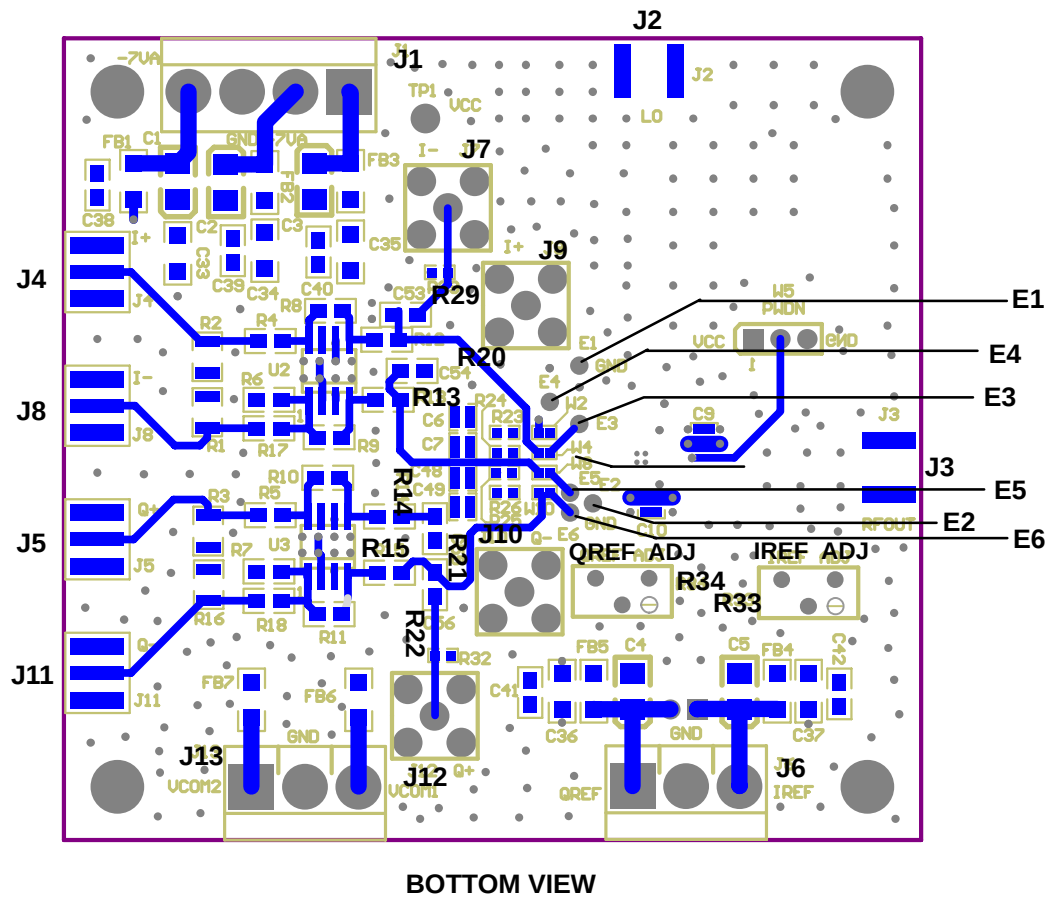


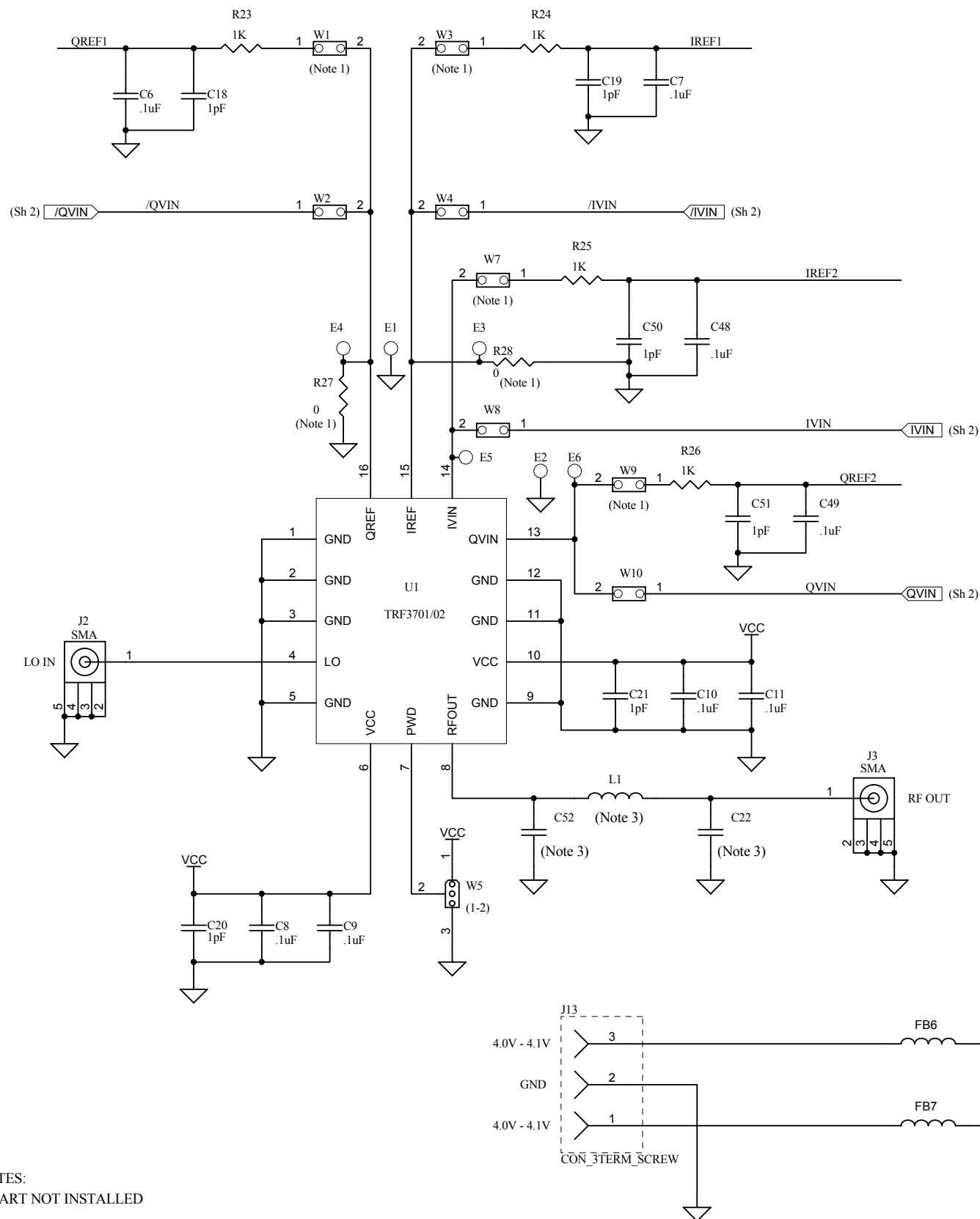
Figure 4-2. Bottom Layer—Test Points Location



Schematics

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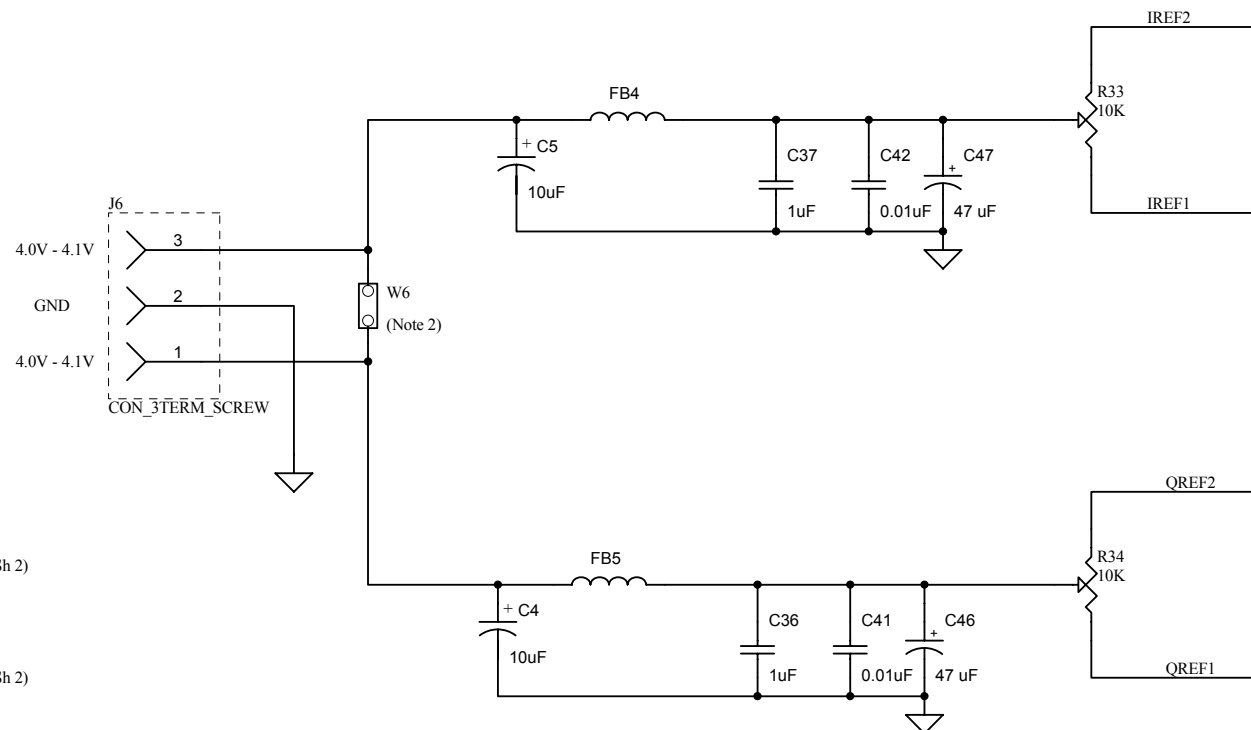
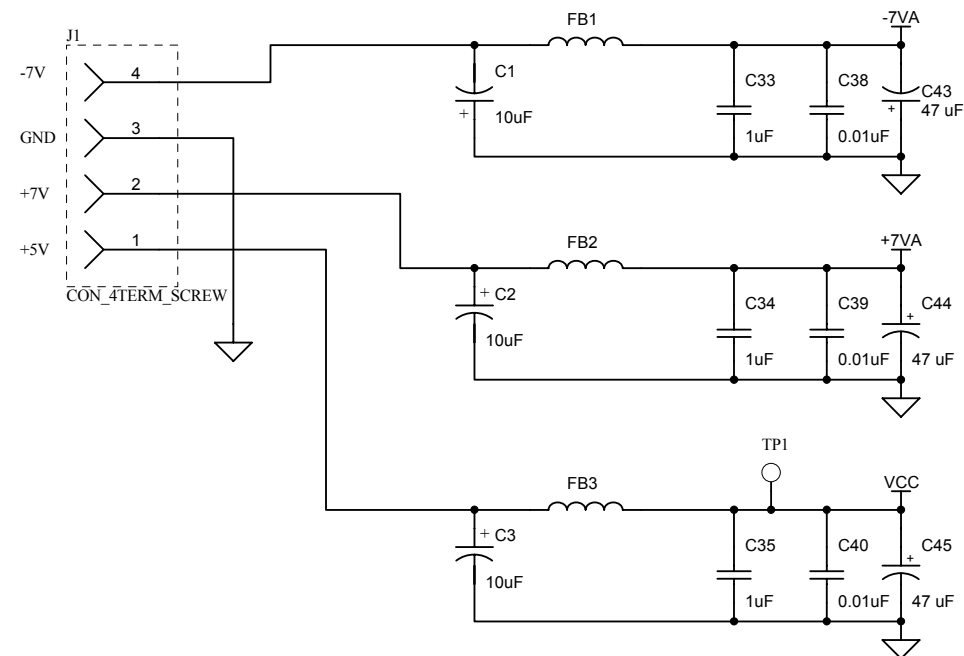
This chapter shows the EVM schematic.



NOTES:

1. PART NOT INSTALLED
2. OPTIONAL, USED TO TIE IREF, QREF TOGETHER
3. VALUE UNKNOWN, TO BE DETERMINED BY MATCHING. IF NOT USING MATCHING, MAKE L1 A 0 OHM RESISTOR, LEAVE C22 AND C52 UNPOPULATED.

Revision History		
REV	ECN Number	Approved



12500 TI Boulevard. Dallas, Texas 75243

Title: TRF3701/02

DOCUMENTCONTROL #

REV: A

Engineer: D. MILLER

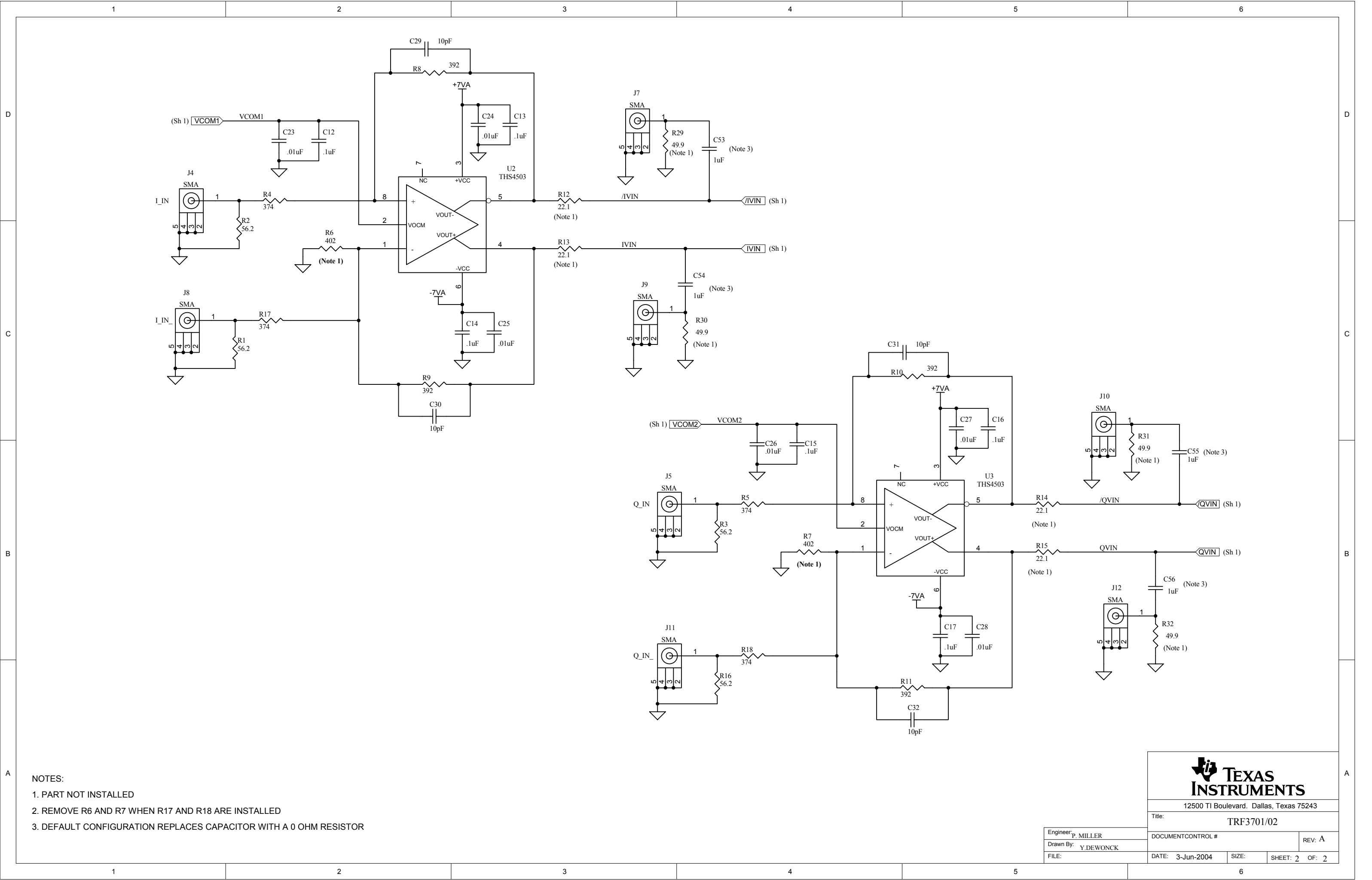
Drawn By: Y DEWONCK

FILE: Sheet1 Sch

DATE:	3-Jun-2004
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SIZE:

SHEET: 1 OF: 2



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Title: TRF3701/02

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