



CYPRESS

CY7C1327A/GVT71256G18

256K x 18 Synchronous Pipelined Burst SRAM

Features

- Fast access times: 3.5, 3.8, and 4.0 ns
- Fast clock speed: 166, 150, 133, and 117 MHz
- Provide high-performance 3-1-1 access rate
- Fast OE access times: 3.5 ns and 3.8 ns
- Optimal for depth expansion (one cycle chip deselect to eliminate bus contention)
- 3.3V –5% and +10% power supply
- 2.5V or 3.3V I/O supply
- 5V tolerant inputs except I/Os
- Clamp diodes to V_{SSQ} at all inputs and outputs
- Common data inputs and data outputs
- Byte Write Enable and Global Write control
- Three chip enables for depth expansion and address pipeline
- Address, data and control registers
- Internally self-timed Write Cycle
- Burst control pins (interleaved or linear burst sequence)
- Automatic power-down for portable applications
- Low profile 119-lead, 14-mm x 22-mm BGA (Ball Grid Array) and 100-pin TQFP packages

Functional Description

The Cypress Synchronous Burst SRAM family employs high-speed, low-power CMOS designs using advanced triple-layer polysilicon, double-layer metal technology. Each memory cell consists of four transistors and two high-valued resistors.

The CY7C1327A/GVT71256G18 SRAM integrates 262,144x18 SRAM cells with advanced synchronous peripheral

circuitry and a 2-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive-edge-triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining Chip Enable ($\overline{CE}$), depth-expansion Chip Enables ($\overline{CE2}$ and $\overline{CE2}$), Burst Control inputs ($\overline{ADSC}$, $\overline{ADSP}$, and $\overline{ADV}$), Write Enables ($\overline{WEL}$, $\overline{WEH}$, and $\overline{BWE}$), and Global Write ($\overline{GW}$).

Asynchronous inputs include the Output Enable ($\overline{OE}$) and Burst Mode Control ($\overline{MODE}$). The data outputs (Q), enabled by $\overline{OE}$, are also asynchronous.

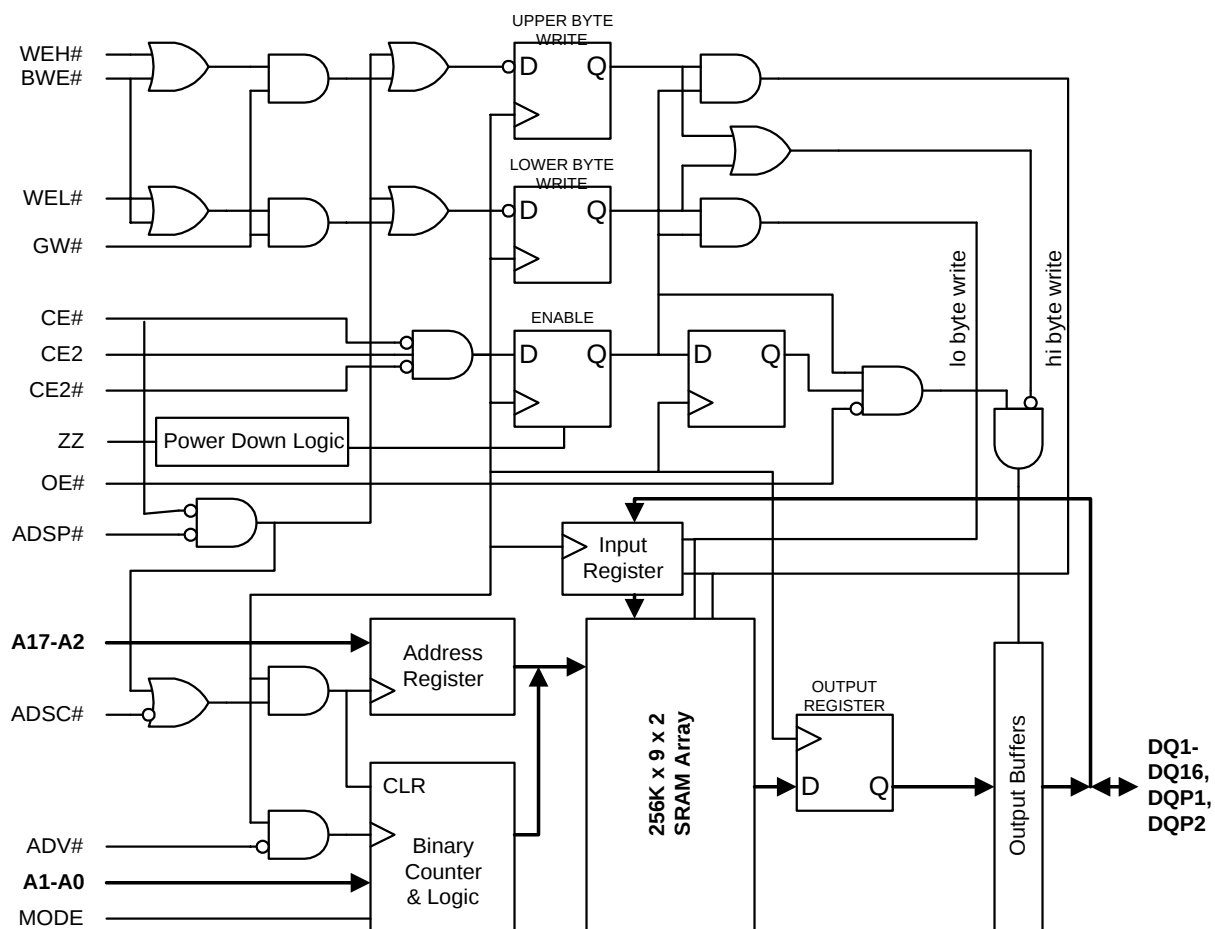
Addresses and chip enables are registered with either Address Status Processor ($\overline{ADSP}$) or Address Status Controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be internally generated as controlled by the Burst Advance pin ($\overline{ADV}$).

Address, data inputs, and write controls are registered on-chip to initiate a self-timed Write cycle. Write cycles can be one to four bytes wide as controlled by the write control inputs. Individual byte write allows individual byte to be written. $\overline{WEL}$ controls $\overline{DQ1-DQ8}$ and $\overline{DQP1}$. $\overline{WEH}$ controls $\overline{DQ9-DQ16}$ and $\overline{DQP2}$. $\overline{WEL}$ and $\overline{WEH}$ can be active only with $\overline{BWE}$ being LOW. $\overline{GW}$ being LOW causes all bytes to be written. Write pass-through capability allows written data available at the output for the immediately next Read cycle. This device also incorporates pipelined enable circuit for easy depth expansion without penalizing system performance.

The CY7C1327A/GVT71256G18 operates from a +3.3V power supply and all outputs operate on a +2.5V supply. All inputs and outputs are JEDEC standard JESD8-5 compatible. The device is ideally suited for 486, Pentium®, 680x0, and PowerPC™ systems and for systems that benefit from a wide synchronous data bus.

Selection Guide

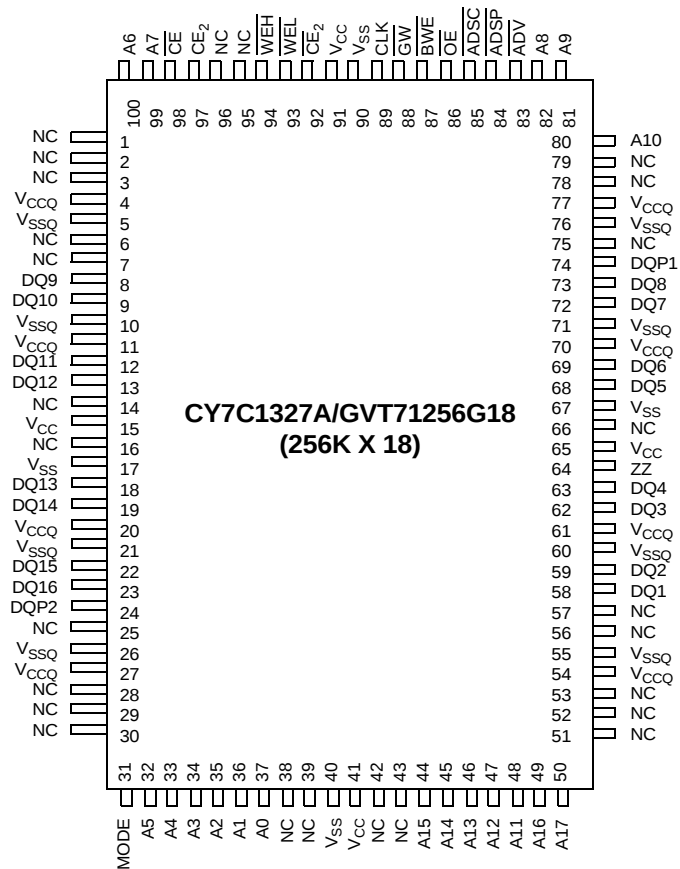
	7C1327A-166 71256G18-3	7C1327A-150 71256G18-4	7C1327A-133 71256G18-5	7C1327A-117 71256G18-6
Maximum Access Time (ns)	3.5	3.8	4.0	4.0
Maximum Operating Current (mA)	425	400	375	350
Maximum CMOS Standby Current (mA)	10	10	10	10

256K x 18 (CY7C1327A/GVT71256G18) Functional Block Diagram^[1]

Note:

1. The Functional Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions, and timing diagrams for detailed information.

Pin Configurations

100-Pin TQFP Top View



Pin Configurations (continued)

119-Ball Bump BGA
256Kx18—CY7C1327A/GVT71256G18
Top View

	1	2	3	4	5	6	7
A	V _{CCQ}	A6	A4	$\overline{\text{ADSP}}$	A8	A16	V _{CCQ}
B	NC	CE2	A3	$\overline{\text{ADSC}}$	A9	$\overline{\text{CE2}}$	NC
C	NC	A7	A2	V _{CC}	A12	A15	NC
D	DQ9	NC	V _{SS}	NC	V _{SS}	DQ ¹ P1	NC
E	NC	DQ10	V _{SS}	$\overline{\text{CE}}$	V _{SS}	NC	DQ8
F	V _{CCQ}	NC	V _{SS}	$\overline{\text{OE}}$	V _{SS}	DQ7	V _{CCQ}
G	NC	DQ11	$\overline{\text{BWH}}$	$\overline{\text{ADV}}$	V _{SS}	NC	DQ6
H	DQ12	NC	V _{SS}	$\overline{\text{GW}}$	V _{SS}	DQ5	NC
J	V _{CCQ}	V _{CC}	NC	V _{CC}	NC	V _{CC}	V _{CCQ}
K	NC	DQ13	V _{SS}	CLK	V _{SS}	NC	DQ4
L	DQ14	NC	V _{SS}	NC	$\overline{\text{BWL}}$	DQ3	NC
M	V _{CCQ}	DQ15	V _{SS}	$\overline{\text{BWE}}$	V _{SS}	NC	V _{CCQ}
N	DQ18	NC	V _{SS}	A1	V _{SS}	DQ2	NC
P	NC	DQP2	V _{SS}	A0	V _{SS}	NC	DQ1
R	NC	A5	MODE	V _{CC}	NC	A13	NC
T	NC	A10	A11	NC	A14	A17	ZZ
U	V _{CCQ}	NC	NC	NC	NC	NC	V _{CCQ}

Pin Descriptions

BGA Pins	QFP Pins	Pin Name	Type	Description
4P, 4N, 2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 2R, 6R, 2T, 3T, 5T, 6T	37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 80, 48, 47, 46, 45, 44, 49, 50	A0–A17	Input-Synchronous	Addresses: These inputs are registered and must meet the set-up and hold times around the rising edge of CLK. The burst counter generates internal addresses associated with A0 and A1, during burst cycle and wait cycle.
5L, 3G	93, 94	$\overline{\text{WEL}}$, WEH	Input-Synchronous	Byte Write Enables: A byte write enable is LOW for a Write cycle and HIGH for a Read cycle. $\overline{\text{WEL}}$ controls DQ1–DQ8 and DQP1. WEH controls DQ9–DQ16 and DQP2. Data I/O are high-impedance if either of these inputs are LOW, conditioned by BWE being LOW.
4M	87	$\overline{\text{BWE}}$	Input-Synchronous	Write Enable: This active LOW input gates byte write operations and must meet the set-up and hold times around the rising edge of CLK.
4H	88	$\overline{\text{GW}}$	Input-Synchronous	Global Write: This active LOW input allows a full 18-bit Write to occur independent of the BWE and WEn lines and must meet the set-up and hold times around the rising edge of CLK.
4K	89	CLK	Input-Synchronous	Clock: This signal registers the addresses, data, chip enables, write control and burst control inputs on its rising edge. All synchronous inputs must meet set-up and hold times around the clock's rising edge.

Pin Descriptions (continued)

BGA Pins	QFP Pins	Pin Name	Type	Description
4E	98	$\overline{CE}$	Input-Synchronous	Chip Enable: This active LOW input is used to enable the device and to gate ADSP.
6B	92	$\overline{CE2}$	Input-Synchronous	Chip Enable: This active LOW input is used to enable the device.
2B	97	CE2	input-Synchronous	Chip Enable: This active HIGH input is used to enable the device.
4F	86	$\overline{OE}$	Input	Output Enable: This active LOW asynchronous input enables the data output drivers.
4G	83	$\overline{ADV}$	Input-Synchronous	Address Advance: This active LOW input is used to control the internal burst counter. A HIGH on this pin generates wait cycle (no address advance).
4A	84	$\overline{ADSP}$	Input-Synchronous	Address Status Processor: This active LOW input, along with $\overline{CE}$ being LOW, causes a new external address to be registered and a Read cycle is initiated using the new address.
4B	85	$\overline{ADSC}$	Input-Synchronous	Address Status Controller: This active LOW input causes device to be deselected or selected along with new external address to be registered. A Read or Write cycle is initiated depending upon write control inputs.
3R	31	MODE	Input-Static	Mode: This input selects the burst sequence. A LOW on this pin selects Linear Burst. A NC or HIGH on this pin selects Interleaved Burst.
7T	64	ZZ	Input-Asynchronous	Snooze: This active HIGH input puts the device in low power consumption standby mode. For normal operation, this input has to be either LOW or NC (No Connect).
7P, 6N, 6L, 7K, 6H, 7G, 6F, 7E, 1D, 2E, 2G, 1H, 2K, 1L, 2M, 1N	58, 59, 62, 63, 68, 69, 72, 73, 8, 9, 12, 13, 18, 19, 22, 23	DQ1–DQ16	Input/Output	Data Inputs/Outputs: Low Byte is DQ1–DQ8. High Byte is DQ9–DQ16. Input data must meet set-up and hold times around the rising edge of CLK.
6D, 2P	74, 24	DQP1, DQP2	Input/Output	Parity Inputs/Outputs: DQP1 is parity bit for DQ1–DQ8 and DQP2 is parity bit for DQ9–DQ16.
4C, 2J, 4J, 6J, 4R	15, 41, 65, 91	V _{CC}	Supply	Power Supply: +3.3V –5% and +10%
3D, 5D, 3E, 5E, 3F, 5F, 5G, 3H, 5H, 3K, 5K, 3L, 3M, 5M, 3N, 5N, 3P, 5P	17, 40, 67, 90	V _{SS}	Ground	Ground: GND
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	4, 11, 20, 27, 54, 61, 70, 77	V _{CCQ}	I/O Supply	Output Buffer Supply: +2.5V (from 2.375V to V _{CC})
	5, 10, 21, 26, 55, 60, 71, 76	V _{SSQ}	I/O Ground	Output Buffer Ground: GND
1B, 7B, 1C, 7C, 2D, 4D, 7D, 1E, 6E, 2F, 1G, 6G, 2H, 7H, 3J, 5J, 1K, 6K, 2L, 4L, 7L, 6M, 2N, 7N, 1P, 6P, 1R, 5R, 7R, 1T, 4T, 2U, 3U, 4U, 5U, 6U	1-3, 6, 7, 14, 16, 25, 28-30, 38, 39, 42, 43, 51-53, 56, 57, 66, 75, 78, 79, 80, 95, 96	NC	-	No Connect: These signals are not internally connected.

Burst Address Table (MODE = NC/V_{CC})

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
A...A00	A...A01	A...A10	A...A11
A...A01	A...A00	A...A11	A...A10
A...A10	A...A11	A...A00	A...A01
A...A11	A...A10	A...A01	A...A00

Burst Address Table (MODE = GND)

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
A...A00	A...A01	A...A10	A...A11
A...A01	A...A10	A...A11	A...A00
A...A10	A...A11	A...A00	A...A01
A...A11	A...A00	A...A01	A...A10

Truth Table^[2, 3, 4, 5, 6, 7, 8]

Operation	Address Used	$\overline{\text{CE}}$	$\overline{\text{CE2}}$	CE2	$\overline{\text{ADSP}}$	$\overline{\text{ADSC}}$	$\overline{\text{ADV}}$	$\overline{\text{WRITE}}$	$\overline{\text{OE}}$	CLK	DQ
Deselected Cycle, Power Down	None	H	X	X	X	L	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	X	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	H	X	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	X	L	H	L	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	H	X	H	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	L-H	D

Notes:

2. **X** means "Don't Care." H means logic HIGH. L means logic LOW. $\overline{\text{WRITE}} = \text{L}$ means $[\overline{\text{BWE}} + \overline{\text{WEL}} * \overline{\text{WEH}}] * \overline{\text{GW}}$ equals LOW. $\overline{\text{WRITE}} = \text{H}$ means $[\overline{\text{BWE}} + \overline{\text{WEL}} * \overline{\text{WEH}}] * \overline{\text{GW}}$ equals HIGH.
3. $\overline{\text{WEL}}$ enables write to DQ1–DQ8 and DQP1. $\overline{\text{WEH}}$ enables write to DQ9–DQ16 and DQP2.
4. All inputs except OE must meet set-up and hold times around the rising edge (LOW to HIGH) of CLK.
5. Suspending burst generates wait cycle.
6. For a write operation following a read operation, $\overline{\text{OE}}$ must be HIGH before the input data required set-up time plus High-Z time for $\overline{\text{OE}}$ and staying HIGH throughout the input data hold time.
7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
8. ADSP LOW along with chip being selected always initiates a READ cycle at the L-H edge of CLK. A WRITE cycle can be performed by setting $\overline{\text{WRITE}}$ LOW for the CLK L-H edge of the subsequent wait cycle. Refer to WRITE timing diagram for clarification.

Partial Truth Table for Read/Write

FUNCTION	GW	BWE	WEH	WEL
READ	H	H	X	X
READ	H	L	H	H
WRITE one byte	H	L	L	H
WRITE all bytes	H	L	L	L
WRITE all bytes	L	X	X	X

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines only, not tested.)

Voltage on V_{CC} Supply Relative to V_{SS}-0.5V to +4.6V

V_{IN} -0.5V to $+V_{CC}+0.5V$

Storage Temperature (plastic) -55°C to +150°C

Junction Temperature +150°C

Power Dissipation..... 1.0W

Short Circuit Output Current 50 mA

Operating Range

Range	Ambient Temperature ^[9]	V_{CC}
Com'l	0°C to +70°C	3.3V -5%/+10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{IHD}	Input High (Logic 1) Voltage ^[10, 11]	Data Inputs (DQxx)	1.7	$V_{CC}+0.3$	
V_{IH}		All other	1.7	4.6	V
V_{IL}	Input Low (Logic 0) Voltage ^[10, 11]		-0.3	0.7	V
I_{L1}	Input Leakage Current ^[12]	$0V \leq V_{IN} \leq V_{CC}$	-2	2	μA
I_{LO}	Output Leakage Current	Output(s) disabled, $0V \leq V_{OUT} \leq V_{CC}$	-2	2	μA
V_{OH}	Output High Voltage ^[10, 13]	$I_{OH} = -2.0$ mA	1.7		V
V_{OL}	Output Low Voltage ^[10, 13]	$I_{OL} = 2.0$ mA		0.7	V
V_{CC}	Supply Voltage ^[10]		3.135	3.6	V
V_{CCQ}	I/O Supply		2.375	V_{CC}	V

Parameter	Description	Conditions	Typ.	-3 166 MHz	-4 150 MHz	-5 133 MHz	-6 117 MHz	Unit
I_{CC}	Power Supply Current: Operating ^[14, 15, 16]	Device selected; all inputs $\leq V_{IL}$ or $\geq V_{IH}$; cycle time $\geq t_{KC}$ Min.; $V_{CC} = \text{Max.}$; outputs open	150	425	400	375	350	mA
I_{SB2}	CMOS Standby ^[15, 16]	Device deselected; $V_{CC} = \text{Max.}$; all inputs $\leq V_{SS} + 0.2$ or $\geq V_{CC} - 0.2$; all inputs static; CLK frequency = 0	5	10	10	10	10	mA
I_{SB3}	TTL Standby ^[15, 16]	Device deselected; all inputs $\leq V_{IL}$ or $\geq V_{IH}$; all inputs static; $V_{CC} = \text{Max.}$; CLK frequency = 0	10	20	20	20	20	mA
I_{SB4}	Clock Running ^[15, 16]	Device deselected; all inputs $\leq V_{IL}$ or $\geq V_{IH}$; $V_{CC} = \text{Max.}$; CLK cycle time $\geq t_{KC}$ Min.	40	90	80	70	60	mA

Notes:

9. T_A is the case temperature.
10. All voltages referenced to V_{SS} (GND).
11. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq t_{KC}/2$.
Undershoot: $V_{IL} \leq -2.0V$ for $t \leq t_{KC}/2$.
12. MODE pin has an internal pull-up and ZZ pin has an internal pull-down. These two pins exhibit an input leakage current of $\pm 30 \mu A$.
13. AC I/O curves are available upon request.
14. I_{CC} is given with no output current. I_{CC} increases with greater output loading and faster cycle times.
15. "Device Deselected" means the device is in Power-Down mode as defined in the truth table. "Device Selected" means the device is active.
16. Typical values are measured at 3.3V, 25°C and 20-ns cycle time.

Thermal Consideration

Parameter	Description	Conditions	TQFP Typ.	Unit
Θ_{JA}	Thermal Resistance - Junction to Ambient	Still air, soldered on 4.25 x 1.125 inch 4-layer PCB	25	°C/W
Θ_{JC}	Thermal Resistance - Junction to Case		9	°C/W

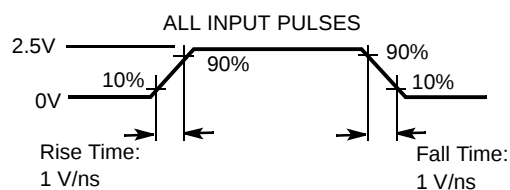
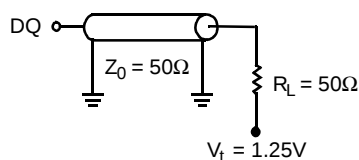
Capacitance

Parameter	Description	Test Conditions	Typ.	Max.	Unit
C_I	Input Capacitance ^[17]	$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = 3.3\text{V}$	4	5	pF
C_O	Input/Output Capacitance (DQ) ^[17]		7	8	pF

Typical Output Buffer Characteristics

Output High Voltage	Pull-up Current		Output Low Voltage	Pull-down Current	
V_{OH} (V)	I_{OH} (mA) Min.	I_{OH} (mA) Max.	V_{OL} (V)	I_{OL} (mA) Min.	I_{OL} (mA) Max.
-0.5	-38	-105	-0.5	0	0
0	-38	-105	0	0	0
0.8	-38	-105	0.4	10	20
1.25	-26	-83	0.8	20	40
1.5	-20	-70	1.25	31	63
2.3	0	-30	1.6	40	80
2.7	0	-10	2.8	40	80
2.9	0	0	3.2	40	80
3.4	0	0	3.4	40	80

AC Test Loads and Waveforms



Note:

17. This parameter is sampled.

Switching Characteristics Over the Operating Range^[18]

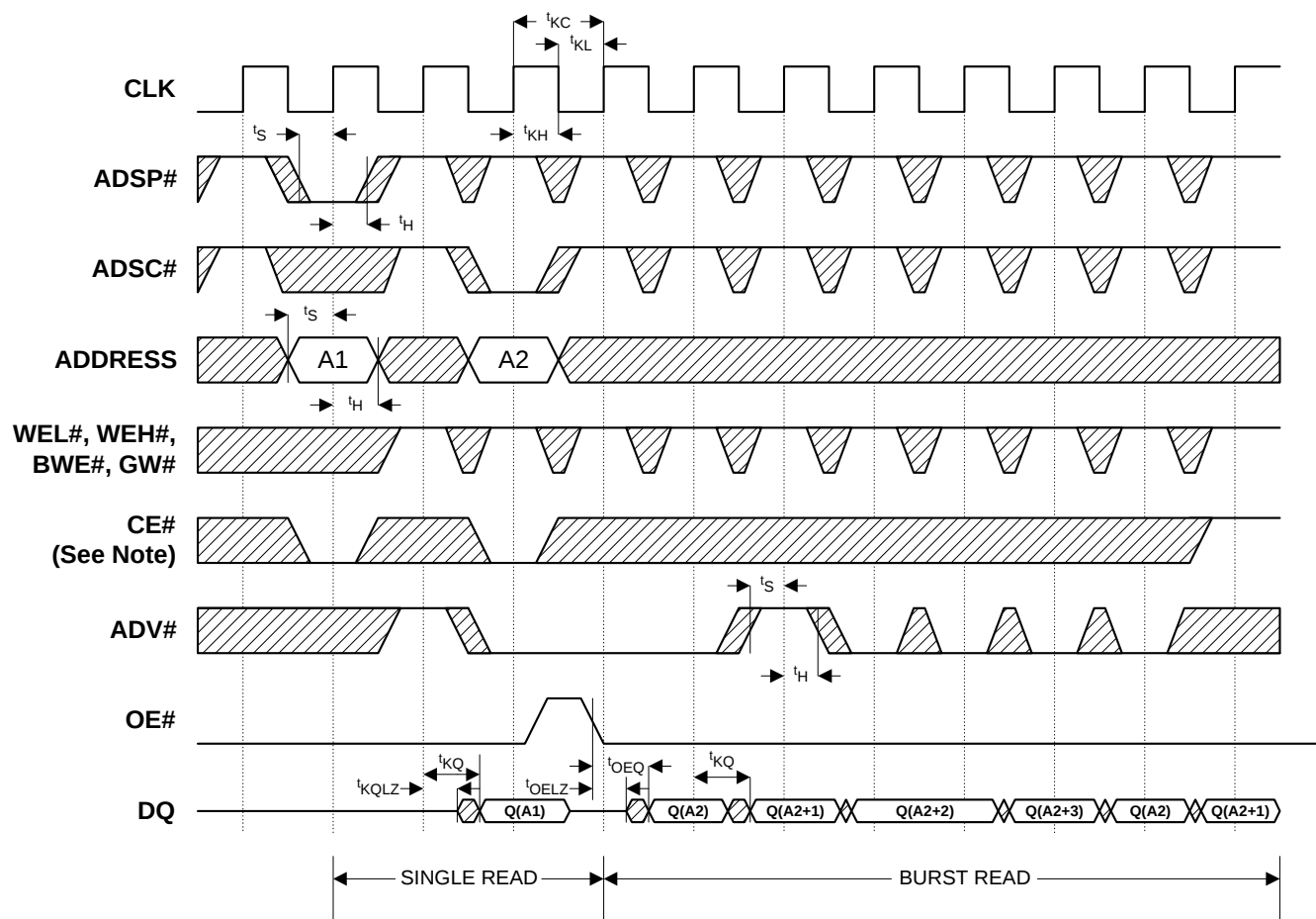
Parameter	Description	-3 166 MHz		-4 150 MHz		-5 133 MHz		-6 117 MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Clock										
t _{KC}	Clock Cycle Time	6.0		6.7		7.5		8.5		ns
t _{KH}	Clock HIGH Time	2.4		2.6		2.8		3.4		ns
t _{KL}	Clock LOW Time	2.4		2.6		2.8		3.4		ns
Output Times										
t _{KQ}	Clock to Output Valid		3.5		3.8		4.0		4.0	ns
t _{KQX}	Clock to Output Invalid	1.5		1.5		1.5		1.5		ns
t _{KQLZ}	Clock to Output in Low-Z ^[17, 19, 20]	0		0		0		0		ns
t _{KQHZ}	Clock to Output in High-Z ^[17, 19, 20]	1.5	6.0	1.5	6.7	1.5	7.5	1.5	8.5	ns
t _{OEQ}	OE to Output Valid ^[21]		3.5		3.5		3.8		3.8	ns
t _{OELZ}	OE to Output in Low-Z ^[17, 19, 20]	0		0		0		0		ns
t _{OEHZ}	OE to Output in High-Z ^[17, 19, 20]		3.5		3.5		3.8		3.8	ns
Set-Up Times										
t _S	Address, Controls and Data In ^[22]	1.5		1.5		1.5		2.0		ns
Hold Times										
t _H	Address, Controls and Data In ^[22]	0.5		0.5		0.5		0.5		ns

Notes:

18. Test conditions as specified with the output loading as shown in AC Test Loads unless otherwise noted.
19. Output loading is specified with $C_L=5$ pF as in AC Test Loads.
20. At any given temperature and voltage condition, t_{KQHZ} is less than t_{KQLZ} and t_{OEHZ} is less than t_{OELZ} .
21. OE is a "Don't Care" when a byte write enable is sampled LOW.
22. This is a synchronous device. All synchronous inputs must meet specified set-up and hold time, except for "Don't Care" as defined in the truth table.

Timing Diagrams

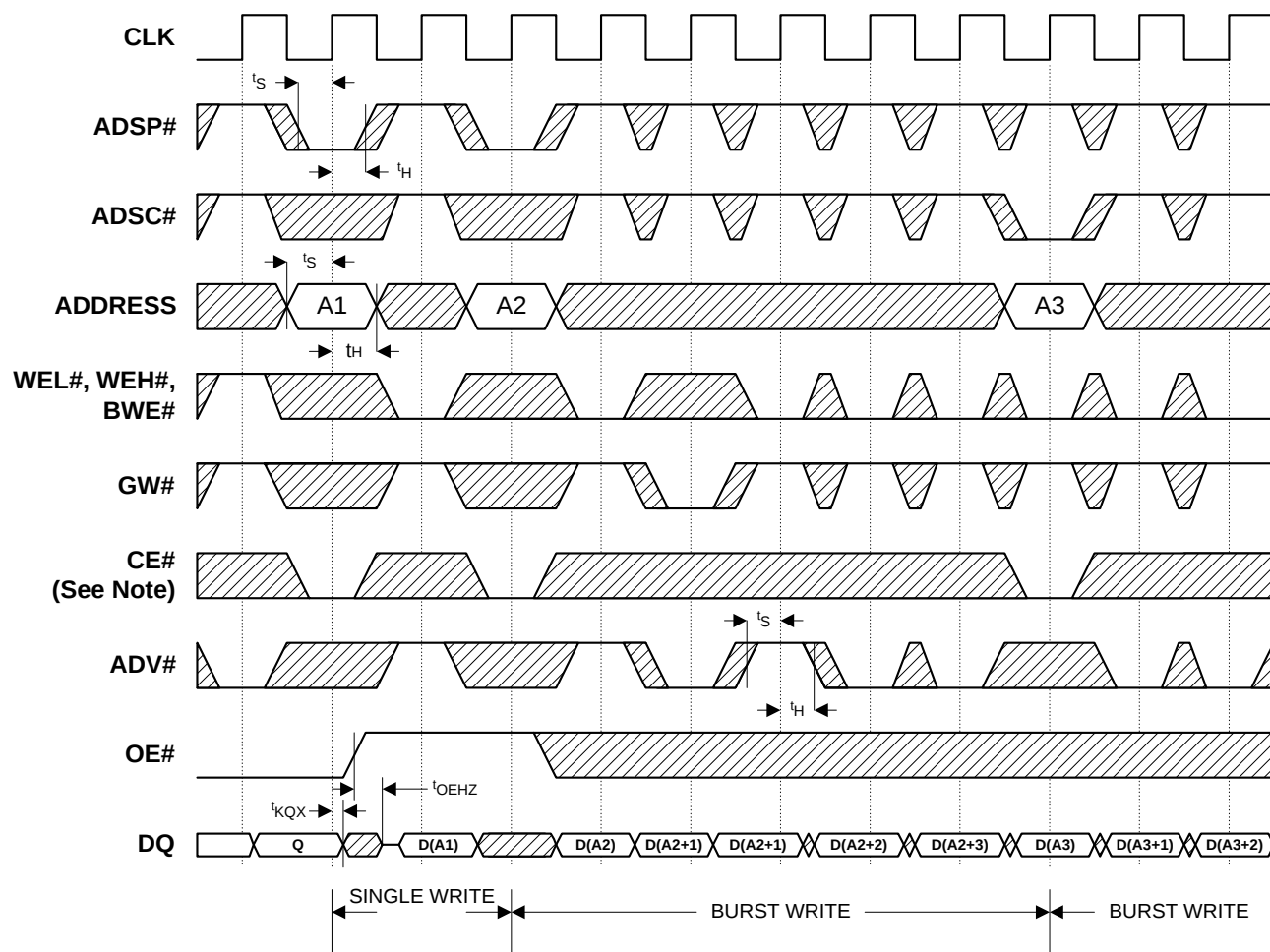
Read Timing^[23]



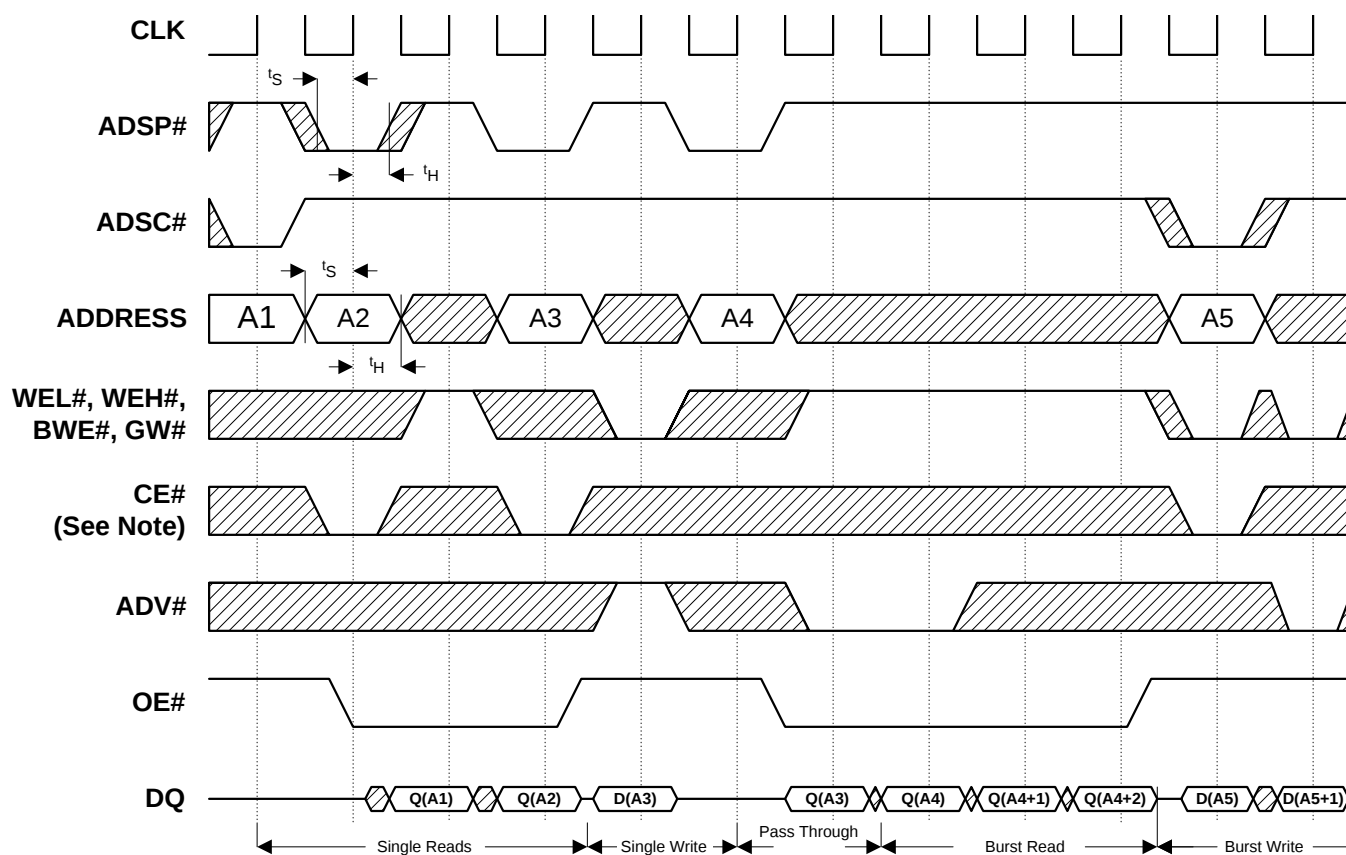
Note:

23. $\overline{CE}$ active in this timing diagram means that all Chip Enables $\overline{CE}$, $\overline{CE2}$, and CE2 are active.

Timing Diagrams (continued)

Write Timing^[23]


Timing Diagrams (continued)

Read/Write Timing^[23]


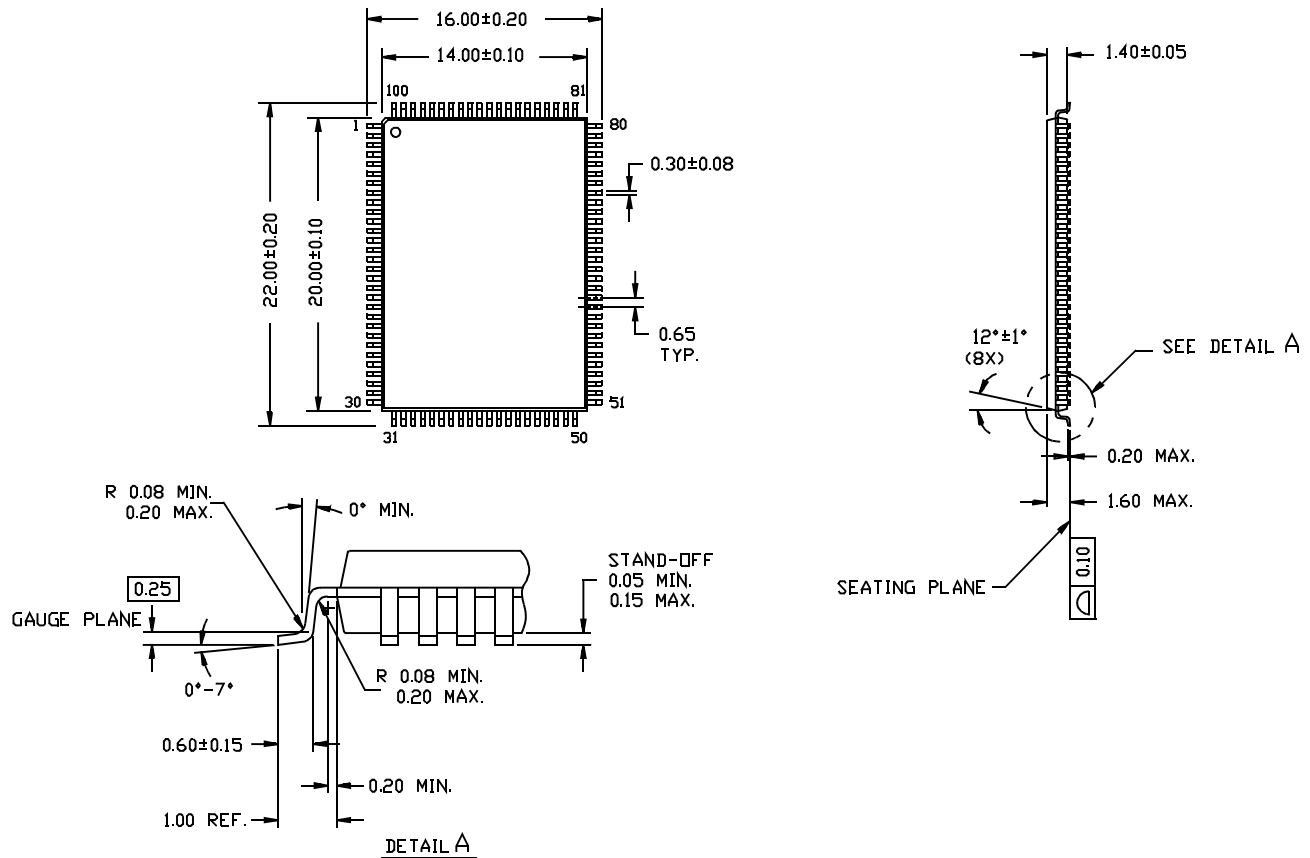
Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
166	CY7C1327A-166AC	A101	100-Lead Thin Quad Flat Pack	Commercial
	GVT71256G18T-3			
	CY7C1327A-166BGC	BG119	119-Lead FBGA (14 x 22 x 2.4 mm)	
	GVT71256G18B-3			
150	CY7C1327A-150AC	A101	100-Lead Thin Quad Flat Pack	Commercial
	GVT71256G18T-4			
	CY7C1327A-150BGC	BG119	119-Lead FBGA (14 x 22 x 2.4 mm)	
	GVT71256G18B-4			
133	CY7C1327A-133AC	A101	100-Lead Thin Quad Flat Pack	Commercial
	GVT71256G18T-5			
	CY7C1327A-133BGC	BG119	119-Lead FBGA (14 x 22 x 2.4 mm)	
	GVT71256G18B-5			
117	CY7C1327A-117AC	A101	100-Lead Thin Quad Flat Pack	Commercial
	GVT71256G18T-6			
	CY7C1327A-117BGC	BG119	119-Lead FBGA (14 x 22 x 2.4 mm)	
	GVT71256G18B-6			

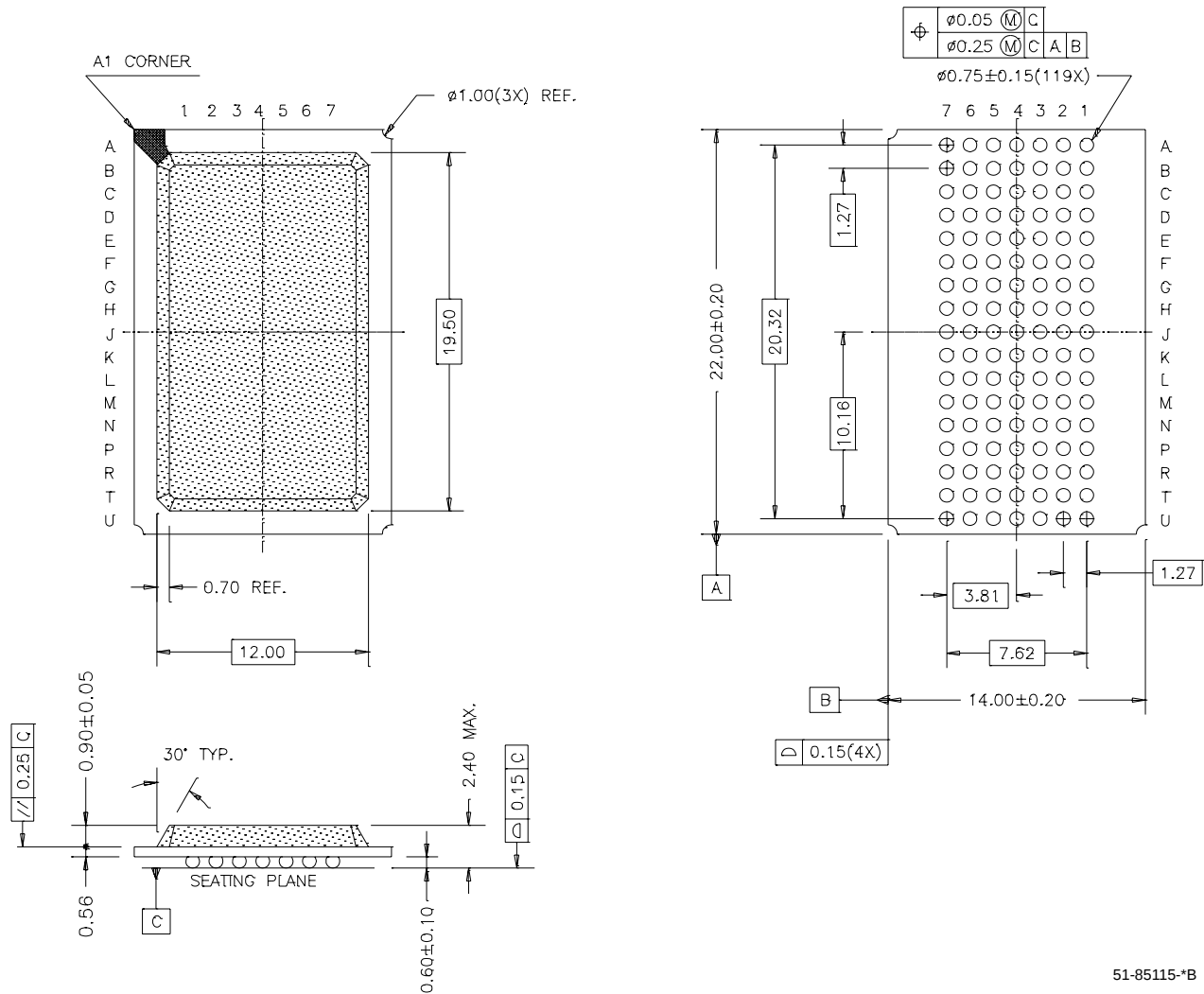
Package Diagrams

100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101

DIMENSIONS ARE IN MILLIMETERS.



51-85050-A

Package Diagrams (continued)
119-Lead PBGA (14 x 22 x 2.4 mm) BG119


51-85115-B

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REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	108984	09/25/01	BRI	New Cypress spec—converted from Galvantech format
*A	121072	11/13/02	DSG	Updated package diagram 51-85115 (BG119) to rev. *B