

SN74CBT162292  
12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER  
WITH INTERNAL PULLDOWN RESISTORS

SCDS052E – MARCH 1998 – REVISED OCTOBER 2000

- Member of Texas Instruments' Widebus™ Family
- TTL-Compatible Control Input Levels
- Isolation Under Power-Off Conditions
- Make-Before-Break Feature
- Internal 500- $\Omega$  Pulldown Resistors to Ground
- A-Port Inputs/Outputs Have Equivalent 25- $\Omega$  Series Resistors, So No External Resistors Are Required
- Latch-Up Performance Exceeds 250 mA Per JESD 17

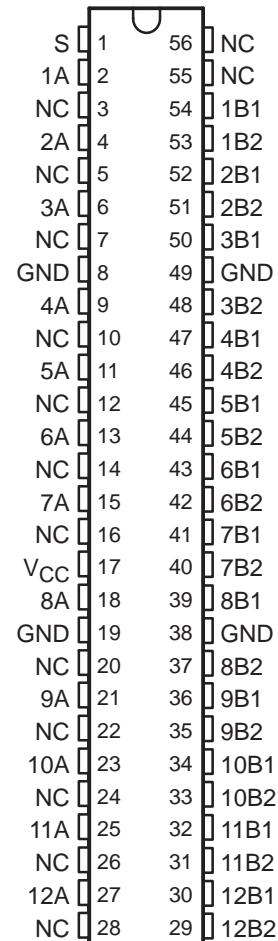
#### description

The SN74CBT162292 is a 12-bit 1-of-2 high-speed TTL-compatible FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

When the select (S) input is low, port A is connected to port B1, and  $R_{INT}$  is connected to port B2. When S is high, port A is connected to port B2, and  $R_{INT}$  is connected to port B1.

The A-port inputs/outputs include equivalent 25- $\Omega$  series resistors to reduce overshoot and undershoot.

DGG, DGV, OR DL PACKAGE  
(TOP VIEW)



NC – No internal connection

#### ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP – DL	Tube	SN74CBT162292DL	CBT162292
		Tape and reel	SN74CBT162292DLR	
	TSSOP – DGG	Tape and reel	SN74CBT162292DGGR	CBT162292
	TVSOP – DGV	Tape and reel	SN74CBT162292DGVR	CY2292

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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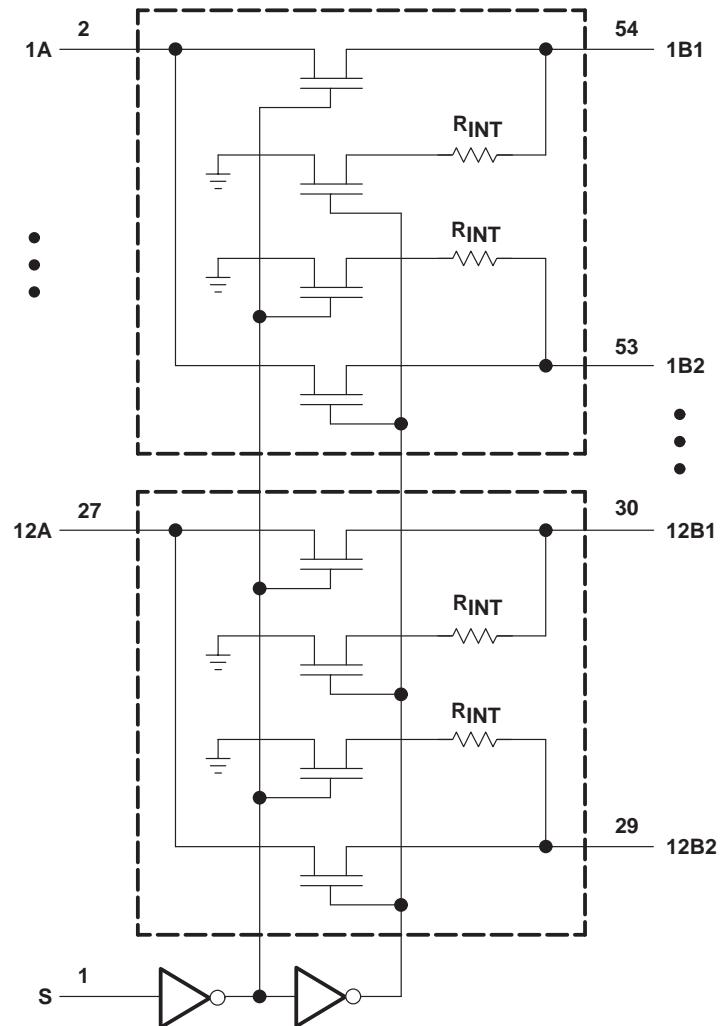
**SN74CBT162292****12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER****WITH INTERNAL PULLDOWN RESISTORS**

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FUNCTION TABLE

INPUT S	FUNCTION
L	A port = B1 port $R_{INT}$ = B2 port
H	A port = B2 port $R_{INT}$ = B1 port

logic diagram (positive logic)



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Continuous channel current .....	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
DGG package .....	64°C/W
DGV package .....	48°C/W
DL package .....	56°C/W
Storage temperature range, $T_{STG}$ .....	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

### **recommended operating conditions (see Note 3)**

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4	5.5	V
$V_{IH}$	High-level control input voltage	2		V
$V_{IL}$	Low-level control input voltage		0.8	V
$T_A$	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT	
$V_{IK}$	$V_{CC} = 4.5 \text{ V}$ ,	$I_I = -18 \text{ mA}$				-1.2	V	
$I_I$	$V_{CC} = 5.5 \text{ V}$ ,	$V_I = V_{CC}$ or GND				$\pm 5$	$\mu\text{A}$	
$I_{off}$	$V_{CC} = 0$ ,	$V_I$ or $V_O = 0$ to $7 \text{ V}$				10	$\mu\text{A}$	
$I_{CC}$	$V_{CC} = 5.5 \text{ V}$ ,	$I_O = 0$ ,	$V_I = V_{CC}$ or GND			3	$\mu\text{A}$	
$\Delta I_{CC}^{\$}$	Control input	$V_{CC} = 5.5 \text{ V}$ ,	One input at $3.4 \text{ V}$ ,	Other inputs at $V_{CC}$ or GND		2.5	mA	
$C_i$	Control input	$V_I = 3 \text{ V}$ or 0				3.5	pF	
$C_{io}$	$V_{CC} = 0$ ,	$V_O = 3 \text{ V}$ or 0				8	pF	
$r_{on}^{\parallel}$	$V_{CC} = 4 \text{ V}$ , TYP at $V_{CC} = 4 \text{ V}$	$V_I = 2.4 \text{ V}$ ,	$I_I = 15 \text{ mA}$			38	55	$\Omega$
	$V_{CC} = 4.5 \text{ V}$	$V_I = 0$	$I_I = 45 \text{ mA}$			39	63	
			$I_I = 30 \text{ mA}$			37	55	
		$V_I = 2.4 \text{ V}$ ,	$I_I = 15 \text{ mA}$			37	55	

† All typical values are at  $V_{CC} = 5$  V (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

SN74CBT162292

12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

WITH INTERNAL PULLDOWN RESISTORS

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switching characteristics over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$ , (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4 \text{ V}$		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd}^{\dagger}$	A or B	B or A	1.9		1.85		ns
$t_{en}$	S	A or B	1	10.7	1	9.5	ns
$t_{dis}$	S	A or B	1	10.9	1	9.7	ns

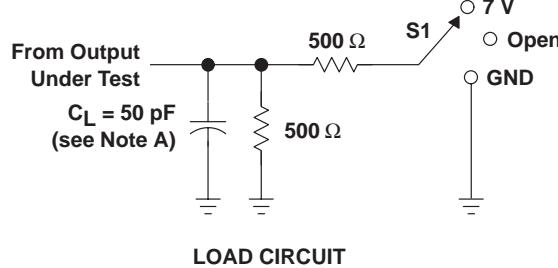
<sup>†</sup> The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

switching characteristics over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$ , (unless otherwise noted) (see Figure 1)

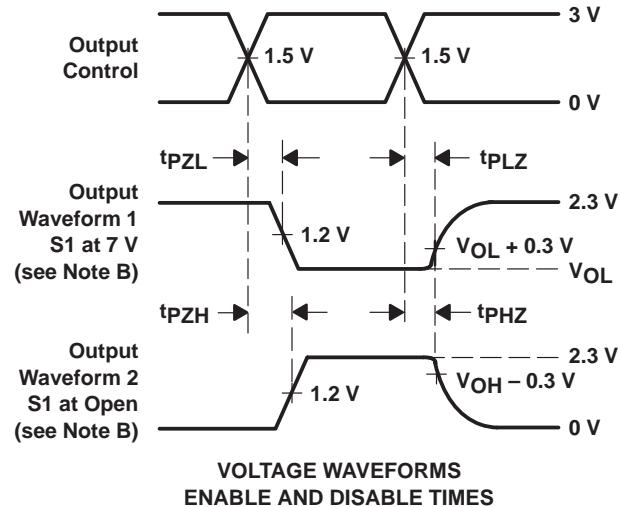
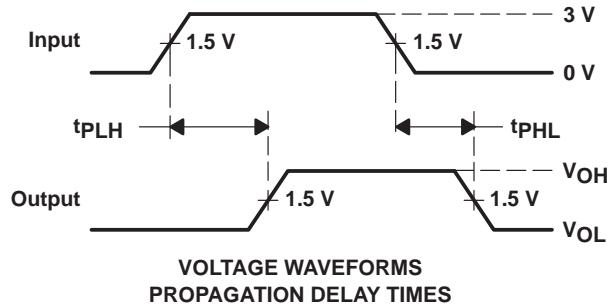
PARAMETER	DESCRIPTION	$V_{CC} = 4 \text{ V}$		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		UNIT
		MIN	MAX	MIN	MAX	
$t_{mbb}^{\ddagger}$	Make-before-break time	0	2	0	2	ns

<sup>‡</sup> The make-before-break time is the time interval between make and break, during the transition from one selected port to the other.

PARAMETER MEASUREMENT INFORMATION



TEST	S1
tpd	Open
tPZL/tPLZ	7 V
tPZH/tPHZ	Open



NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when connected to the internal 500- $\Omega$  pulldown resistor. Waveform 2 is for an output with internal conditions such that the output is high except when connected to the internal 500- $\Omega$  pulldown resistor.  
 C. All pulse inputs and DC inputs are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O$  = 50  $\Omega$ ,  $t_r \leq$  2.5 ns,  $t_f \leq$  2.5 ns.  
 D. The outputs are measured one at a time with one transition per measurement.  
 E. tPZL and tPHZ are the same as tdis.  $Z = R_{INT} = 500 \Omega$ .  
 F. tPZL and tPZH are the same as t<sub>en</sub>.  $Z = R_{INT} = 500 \Omega$ .  
 G. tPLH and tPHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74CBT162292DGGRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBT162292DGGRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBT162292DGVRE4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBT162292DGVRG4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT162292DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT162292DGVR	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT162292DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT162292DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

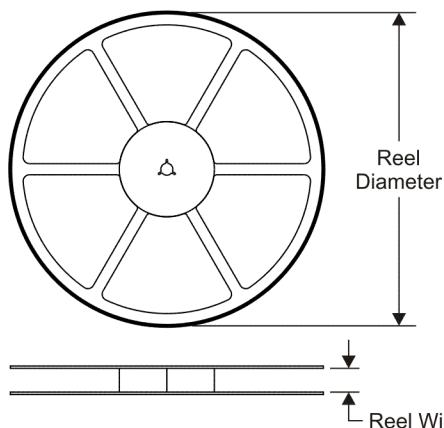
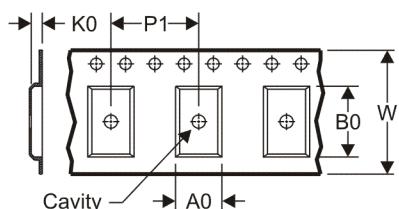
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

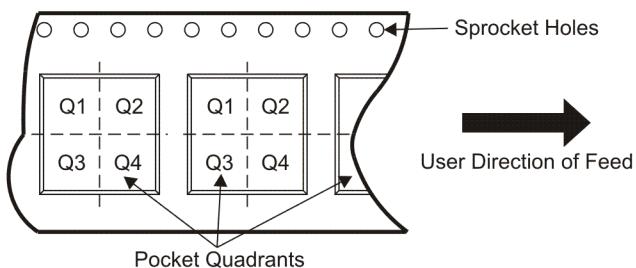
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT162292DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74CBT162292DGVR	TVSOP	DGV	56	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

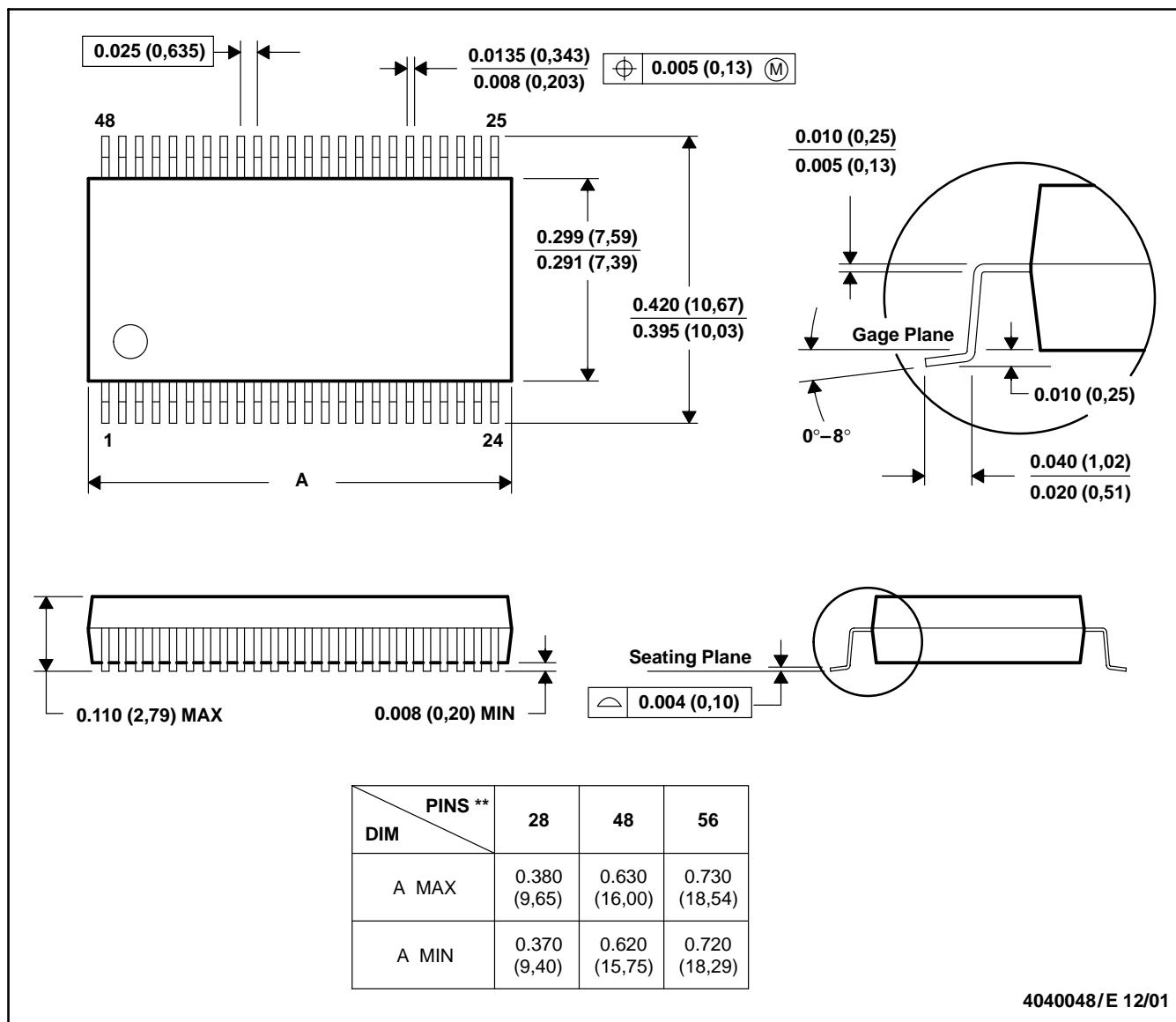
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBT162292DGGR	TSSOP	DGG	56	2000	346.0	346.0	41.0
SN74CBT162292DGVR	TVSOP	DGV	56	2000	346.0	346.0	41.0

## DL (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

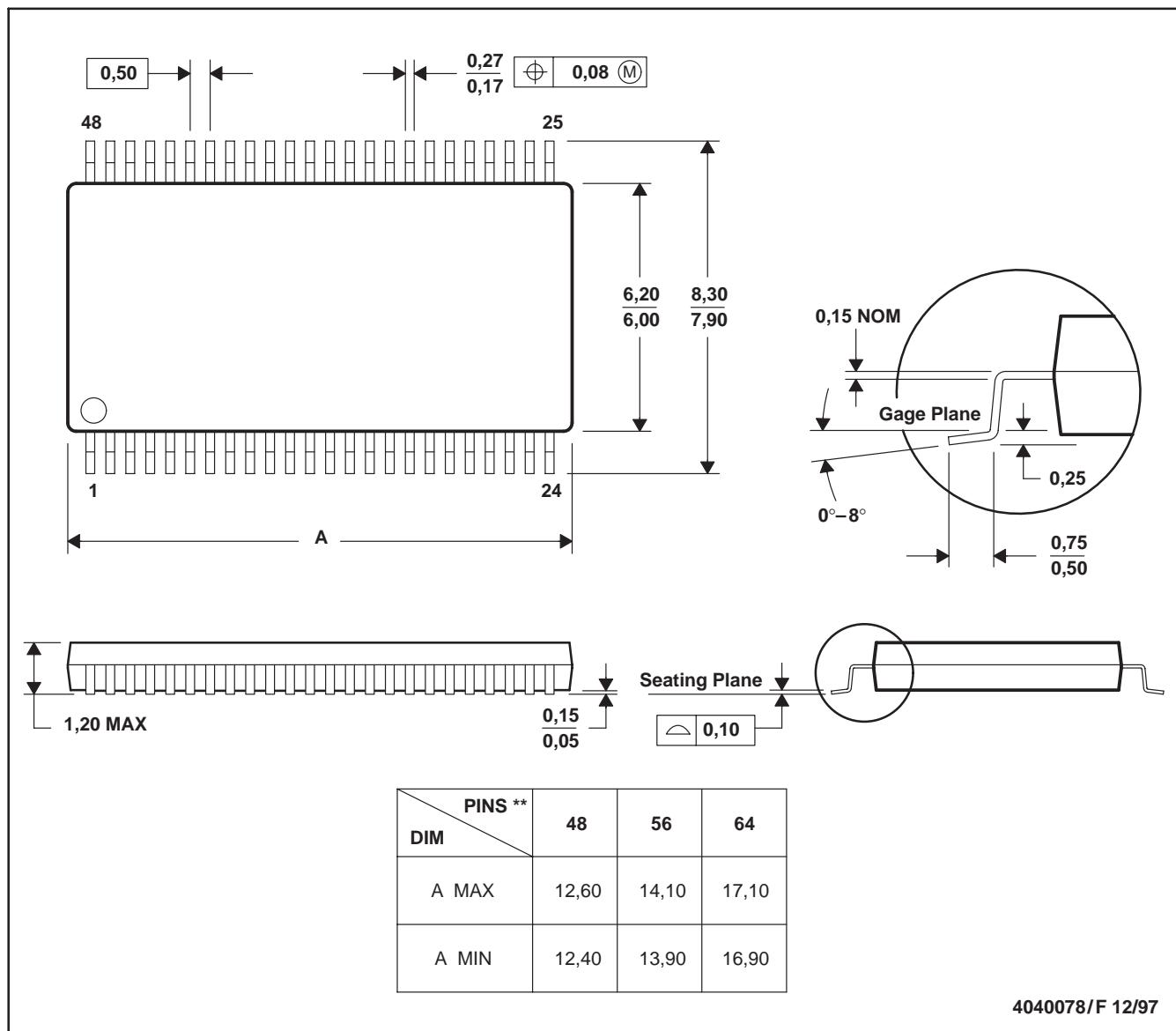


NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-118

## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

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