

Features

- Supports 133 MHz bus operations
- 2M × 36 common I/O
- 3.3 V core power supply (V_{DD})
- 2.5 V or 3.3 V I/O supply (V_{DDQ})
- Fast clock to output time
 - 6.5 ns (133 MHz version)
- Provide high performance 2-1-1-1 access rate
- User selectable burst counter supporting Intel® Pentium® interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self timed write
- Asynchronous output enable
- CY7C1481BV33 available in JEDEC standard Pb-free 100-pin TQFP, Pb-free and non Pb-free 165-ball FBGA package.
- IEEE 1149.1 JTAG compatible boundary scan
- ZZ sleep mode option

Functional Description

The CY7C1481BV33 is a 3.3 V, 2M × 36 synchronous flow through SRAM designed to interface with high speed microprocessors with minimum glue logic. Maximum access delay from clock rise is 6.5 ns (133 MHz version). A 2-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access. All synchronous inputs are gated by registers controlled by a positive edge triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, address pipelining Chip Enable (CE_1), depth expansion Chip Enables (CE_2 and CE_3), Burst Control inputs (ADSC, ADSP, and ADV), Write Enables (BW_x and BWE), and Global Write (GW). Asynchronous inputs include the Output Enable (OE) and the ZZ pin.

The CY7C1481BV33 enables either interleaved or linear burst sequences, selected by the MODE input pin. A HIGH selects an interleaved burst sequence, while a LOW selects a linear burst sequence. Burst accesses are initiated with the Processor Address Strobe (ADSP) or the cache Controller Address Strobe (ADSC) inputs. Address advancement is controlled by the Address Advancement (ADV) input.

Addresses and chip enables are registered at rising edge of clock when either Address Strobe Processor (ADSP) or Address Strobe Controller (ADSC) are active. Subsequent burst addresses can be internally generated as controlled by the Advance pin (ADV).

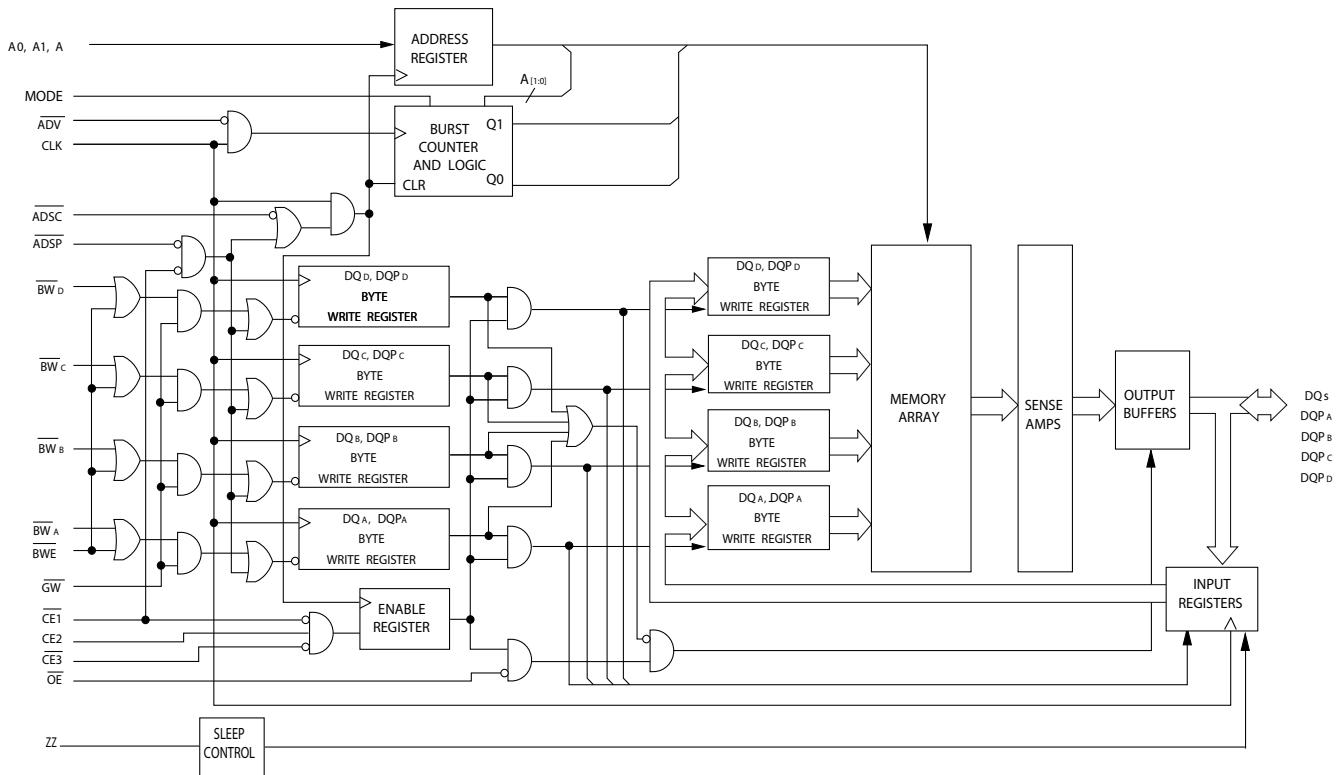
The CY7C1481BV33 operates from a +3.3 V core power supply while all outputs may operate with either a +2.5 or +3.3 V supply. All inputs and outputs are JEDEC standard JESD8-5 compatible.

For a complete list of related documentation, click [here](#).

Selection Guide

| Description | 133 MHz | Unit |
|------------------------------|---------|------|
| Maximum Access Time | 6.5 | ns |
| Maximum Operating Current | 335 | mA |
| Maximum CMOS Standby Current | 150 | mA |

Logic Block Diagram – CY7C1481BV33

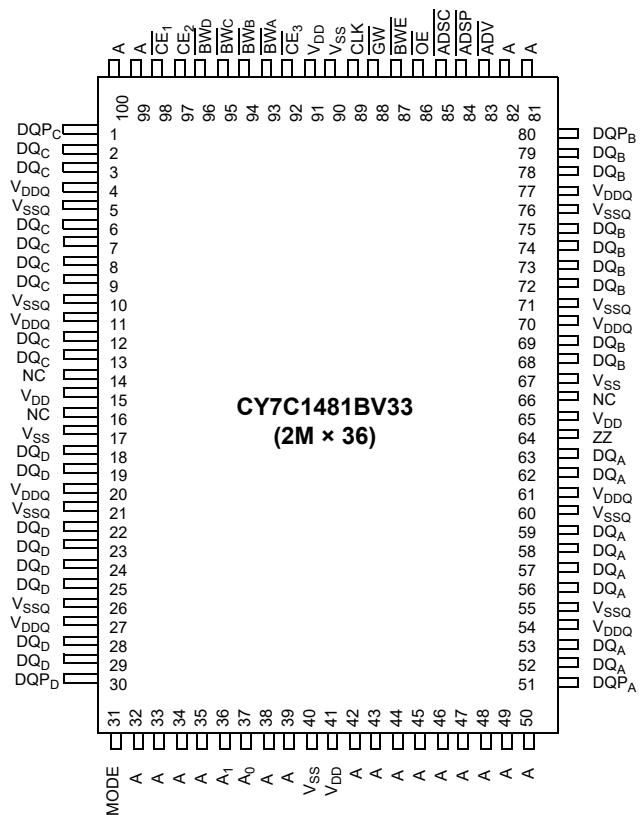


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Pin Configurations

Figure 1. 100-pin TQFP (14 × 20 × 1.4 mm) pinout



Pin Configurations (continued)

Figure 2. 165-ball FBGA (15 × 17 × 1.4 mm) pinout
CY7C1481BV33 (2M × 36)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|----------|----------|----------|-------------------|-------------------|-------------------|-------------------|------------------|-------------------|-------------------|-----------|-----------|
| A | NC/288M | A | \overline{CE}_1 | \overline{BW}_C | \overline{BW}_B | \overline{CE}_3 | \overline{BWE} | \overline{ADSC} | \overline{ADV} | A | NC |
| B | NC/144M | A | CE_2 | \overline{BW}_D | \overline{BW}_A | CLK | \overline{GW} | \overline{OE} | \overline{ADSP} | A | NC/576M |
| C | DQP_C | NC | V_{DDQ} | V_{SS} | V_{SS} | V_{SS} | V_{SS} | V_{SS} | V_{DDQ} | NC/1G | DQP_B |
| D | DQ_C | DQ_C | V_{DDQ} | V_{DD} | V_{SS} | V_{SS} | V_{SS} | V_{DD} | V_{DDQ} | DQ_B | DQ_B |
| E | DQ_C | DQ_C | V_{DDQ} | V_{DD} | V_{SS} | V_{SS} | V_{SS} | V_{DD} | V_{DDQ} | DQ_B | DQ_B |
| F | DQ_C | DQ_C | V_{DDQ} | V_{DD} | V_{SS} | V_{SS} | V_{SS} | V_{DD} | V_{DDQ} | DQ_B | DQ_B |
| G | DQ_C | DQ_C | V_{DDQ} | V_{DD} | V_{SS} | V_{SS} | V_{SS} | V_{DD} | V_{DDQ} | DQ_B | DQ_B |
| H | NC | NC | NC | V_{DD} | V_{SS} | V_{SS} | V_{SS} | V_{DD} | NC | NC | ZZ |
| J | DQ_D | DQ_D | V_{DDQ} | V_{DD} | V_{SS} | V_{SS} | V_{SS} | V_{DD} | V_{DDQ} | DQ_A | DQ_A |
| K | DQ_D | DQ_D | V_{DDQ} | V_{DD} | V_{SS} | V_{SS} | V_{SS} | V_{DD} | V_{DDQ} | DQ_A | DQ_A |
| L | DQ_D | DQ_D | V_{DDQ} | V_{DD} | V_{SS} | V_{SS} | V_{SS} | V_{DD} | V_{DDQ} | DQ_A | DQ_A |
| M | DQ_D | DQ_D | V_{DDQ} | V_{DD} | V_{SS} | V_{SS} | V_{SS} | V_{DD} | V_{DDQ} | DQ_A | DQ_A |
| N | DQP_D | NC | V_{DDQ} | V_{SS} | NC | A | NC | V_{SS} | V_{DDQ} | NC | DQP_A |
| P | NC | A | A | A | TDI | A1 | TDO | A | A | A | A |
| R | MODE | A | A | A | TMS | A0 | TCK | A | A | A | A |

Pin Definitions

| Pin Name | I/O | Description |
|---|--------------------|--|
| A ₀ , A ₁ , A | Input-Synchronous | Address Inputs Used to Select One of the Address Locations. Sampled at the rising edge of the CLK if ADSP or ADSC is active LOW, and CE ₁ , CE ₂ , and CE ₃ are sampled active. A _[1:0] feed the 2-bit counter. |
| BW _A , BW _B , BW _C , BW _D | Input-Synchronous | Byte Write Select Inputs, Active LOW. Qualified with BWE to conduct byte writes to the SRAM. Sampled on the rising edge of CLK. |
| GW | Input-Synchronous | Global Write Enable Input, Active LOW. When asserted LOW on the rising edge of CLK, a global write is conducted (ALL bytes are written, regardless of the values on BW _X and BWE). |
| CLK | Input-Clock | Clock Input. Captures all synchronous inputs to the device. Also used to increment the burst counter when ADV is asserted LOW during a burst operation. |
| CE ₁ | Input-Synchronous | Chip Enable 1 Input, Active LOW. Sampled on the rising edge of CLK. Used in conjunction with CE ₂ and CE ₃ to select or deselect the device. ADSP is ignored if CE ₁ is HIGH. CE ₁ is sampled only when a new external address is loaded. |
| CE ₂ | Input-Synchronous | Chip Enable 2 Input, Active HIGH. Sampled on the rising edge of CLK. Used in conjunction with CE ₁ and CE ₃ to select or deselect the device. CE ₂ is sampled only when a new external address is loaded. |
| CE ₃ | Input-Synchronous | Chip Enable 3 Input, Active LOW. Sampled on the rising edge of CLK. Used in conjunction with CE ₁ and CE ₂ to select or deselect the device. CE ₃ is sampled only when a new external address is loaded. |
| OE | Input-Asynchronous | Output Enable, Asynchronous Input, Active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins. OE is masked during the first clock of a read cycle when emerging from a deselected state. |
| ADV | Input-Synchronous | Advance Input Signal, Sampled on the Rising Edge of CLK. When asserted, it automatically increments the address in a burst cycle. |
| ADSP | Input-Synchronous | Address Strobe from Processor, Sampled on the Rising Edge of CLK, Active LOW. When asserted LOW, addresses presented to the device are captured in the address registers. A _[1:0] are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized. ADSP is ignored when CE ₁ is deasserted HIGH. |
| ADSC | Input-Synchronous | Address Strobe from Controller, Sampled on the Rising Edge of CLK, Active LOW. When asserted LOW, addresses presented to the device are captured in the address registers. A _[1:0] are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized. |
| BWE | Input-Synchronous | Byte Write Enable Input, Active LOW. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write. |
| ZZ | Input-Asynchronous | ZZ “Sleep” Input, Active HIGH. When asserted HIGH, places the device in a non time-critical “sleep” condition with data integrity preserved. For normal operation, this pin must be LOW or left floating. ZZ pin has an internal pull down. |
| DQ _S | I/O-Synchronous | Bidirectional Data I/O Lines. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by OE. When OE is asserted LOW, the pins behave as outputs. When HIGH, DQ _S and DQP _X are placed in a tri-state condition. The outputs are automatically tri-stated during the data portion of a write sequence, the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of OE. |
| DQP _X | I/O-Synchronous | Bidirectional Data Parity I/O Lines. Functionally, these signals are identical to DQ _S . During write sequences, DQP _X is controlled by BW _X correspondingly. |
| MODE | Input-Static | Selects Burst Order. When tied to GND, selects linear burst sequence. When tied to V _{DD} or left floating, selects interleaved burst sequence. This is a strap pin and must remain static during device operation. Mode Pin has an internal pull up. |

Pin Definitions (continued)

| Pin Name | I/O | Description |
|-----------------|--------------------------------|---|
| V_{DD} | Power Supply | Power Supply Inputs to the Core of the Device. |
| V_{DDQ} | I/O Power Supply | Power Supply for the I/O Circuitry. |
| V_{SS} | Ground | Ground for the Core of the Device. |
| $V_{SSQ}^{[1]}$ | I/O Ground | Ground for the I/O Circuitry. |
| TDO | JTAG Serial Output Synchronous | Serial Data-Out to the JTAG Circuit. Delivers data on the negative edge of TCK. If the JTAG feature is not used, this pin must be left unconnected. This pin is not available on TQFP packages. |
| TDI | JTAG Serial Input Synchronous | Serial Data-In to the JTAG Circuit. Sampled on the rising edge of TCK. If the JTAG feature is not used, this pin can be left floating or connected to V_{DD} through a pull up resistor. This pin is not available on TQFP packages. |
| TMS | JTAG Serial Input Synchronous | Serial Data-In to the JTAG Circuit. Sampled on the rising edge of TCK. If the JTAG feature is not used, this pin can be disconnected or connected to V_{DD} . This pin is not available on TQFP packages. |
| TCK | JTAG Clock | Clock Input to the JTAG Circuit. If the JTAG feature is not used, this pin must be connected to V_{SS} . This pin is not available on TQFP packages. |
| NC | – | No Connects. Not internally connected to the die. 144M, 288M, 576M, and 1G are address expansion pins and are not internally connected to the die. |

Note

1. Applicable for TQFP package. For BGA package V_{SS} serves as ground for the core and the I/O circuitry.

Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CDV}) is 6.5 ns (133 MHz device).

The CY7C1481BV33 supports secondary cache in systems using either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486™ processors. The linear burst sequence is suited for processors that use a linear burst sequence. The burst order is user selectable and is determined by sampling the MODE input. Accesses are initiated with either the Processor Address Strobe (ADSP) or the Controller Address Strobe (ADSC). Address advancement through the burst sequence is controlled by the ADV input. A 2-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the Byte Write Enable (BWE) and Byte Write Select (BW_X) inputs. A Global Write Enable (GW) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self timed write circuitry.

Three synchronous Chip Selects (\overline{CE}_1 , \overline{CE}_2 , \overline{CE}_3) and an asynchronous Output Enable (OE) provide easy bank selection and output tri-state control. ADSP is ignored if \overline{CE}_1 is HIGH.

Single Read Accesses

A single read access is initiated when the following conditions are satisfied at clock rise: (1) \overline{CE}_1 , \overline{CE}_2 , and \overline{CE}_3 are all asserted active, and (2) ADSC or ADSP is asserted LOW (if the access is initiated by ADSC, the write inputs must be deasserted during this first cycle). The address presented to the address inputs is latched into the address register and the burst counter/control logic. It is then presented to the memory core. If the OE input is asserted LOW, the requested data is available at the data outputs a maximum to t_{CDV} after clock rise. ADSP is ignored if \overline{CE}_1 is HIGH.

Single Write Accesses Initiated by ADSP

This access is initiated when the following conditions are satisfied at clock rise: (1) \overline{CE}_1 , \overline{CE}_2 , \overline{CE}_3 are all asserted active, and (2) ADSP is asserted LOW. The addresses presented are loaded into the address register and the burst inputs (GW, BWE, and BW_X) are ignored during this first clock cycle. If the write inputs are asserted active (see [Truth Table for Read/Write on page 10](#) for appropriate states that indicate a write) on the next clock rise, the appropriate data is latched and written into the device. The device allows byte writes. All I/Os are tri-stated during a byte write. Because this is a common I/O device, the asynchronous OE input signal must be deasserted and the I/Os must be tri-stated prior to the presentation of data to DQ_S. As a safety precaution, the data lines are tri-stated after a write cycle is detected, regardless of the state of OE.

Single Write Accesses Initiated by ADSC

This write access is initiated when the following conditions are satisfied at clock rise: (1) \overline{CE}_1 , \overline{CE}_2 , and \overline{CE}_3 are all asserted active, (2) ADSC is asserted LOW, (3) ADSP is deasserted

HIGH, and (4) the write input signals (\overline{GW} , \overline{BWE} , and \overline{BW}_X) indicate a write access. ADSP is ignored if ADSP is active LOW.

The addresses presented are loaded into the address register and the burst counter/control logic and delivered to the memory core. The information presented to DQ_S is written into the specified address location. The device allows byte writes. All I/Os are tri-stated when a write is detected, even a byte write. Because this is a common I/O device, the asynchronous OE input signal must be deasserted and the I/Os must be tri-stated before the data is presented to DQ_S. As a safety precaution, the data lines are tri-stated after a write cycle is detected, regardless of the state of OE.

Burst Sequences

The CY7C1481BV33 provides an on-chip 2-bit wraparound burst counter inside the SRAM. The burst counter is fed by A[1:0], and can follow either a linear or interleaved burst order. The burst order is determined by the state of the MODE input. A LOW on MODE selects a linear burst sequence. A HIGH on MODE selects an interleaved burst order. Leaving MODE unconnected causes the device to default to an interleaved burst sequence.

Sleep Mode

The ZZ input pin is asynchronous. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed.

Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed.

The device must be deselected before entering the “sleep” mode. \overline{CE}_1 , \overline{CE}_2 , \overline{CE}_3 , ADSP, and ADSC must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Interleaved Burst Address Table

(MODE = Floating or V_{DD})

| First Address A1:A0 | Second Address A1:A0 | Third Address A1:A0 | Fourth Address A1:A0 |
|---------------------|----------------------|---------------------|----------------------|
| 00 | 01 | 10 | 11 |
| 01 | 00 | 11 | 10 |
| 10 | 11 | 00 | 01 |
| 11 | 10 | 01 | 00 |

Linear Burst Address Table

(MODE = GND)

| First Address A1:A0 | Second Address A1:A0 | Third Address A1:A0 | Fourth Address A1:A0 |
|---------------------|----------------------|---------------------|----------------------|
| 00 | 01 | 10 | 11 |
| 01 | 10 | 11 | 00 |
| 10 | 11 | 00 | 01 |
| 11 | 00 | 01 | 10 |

ZZ Mode Electrical Characteristics

| Parameter | Description | Test Conditions | Min | Max | Unit |
|-------------|-----------------------------------|----------------------------------|------------|------------|------|
| I_{DDZZ} | Sleep mode standby current | $ZZ \geq V_{DD} - 0.2 \text{ V}$ | – | 150 | mA |
| t_{ZZS} | Device operation to ZZ | $ZZ \geq V_{DD} - 0.2 \text{ V}$ | – | $2t_{CYC}$ | ns |
| t_{ZZREC} | ZZ recovery time | $ZZ \leq 0.2 \text{ V}$ | $2t_{CYC}$ | – | ns |
| t_{ZZI} | ZZ active to sleep current | This parameter is sampled | – | $2t_{CYC}$ | ns |
| t_{RZZI} | ZZ inactive to exit sleep current | This parameter is sampled | 0 | – | ns |

Truth Table

The truth table for CY7C1481BV33 follows. [2, 3, 4, 5, 6]

| Cycle Description | Address Used | CE ₁ | CE ₂ | CE ₃ | ZZ | ADSP | ADSC | ADV | WRITE | OE | CLK | DQ |
|------------------------------|--------------|-----------------|-----------------|-----------------|----|------|------|-----|-------|----|-----|-----------|
| Deselected Cycle, Power Down | None | H | X | X | L | X | L | X | X | X | L-H | Tri-State |
| Deselected Cycle, Power Down | None | L | L | X | L | L | X | X | X | X | L-H | Tri-State |
| Deselected Cycle, Power Down | None | L | X | H | L | L | X | X | X | X | L-H | Tri-State |
| Deselected Cycle, Power Down | None | L | L | X | L | H | L | X | X | X | L-H | Tri-State |
| Deselected Cycle, Power Down | None | X | X | H | L | H | L | X | X | X | L-H | Tri-State |
| Sleep Mode, Power Down | None | X | X | X | H | X | X | X | X | X | X | Tri-State |
| Read Cycle, Begin Burst | External | L | H | L | L | L | X | X | X | L | L-H | Q |
| Read Cycle, Begin Burst | External | L | H | L | L | L | X | X | X | H | L-H | Tri-State |
| Write Cycle, Begin Burst | External | L | H | L | L | H | L | X | L | X | L-H | D |
| Read Cycle, Begin Burst | External | L | H | L | L | H | L | X | H | L | L-H | Q |
| Read Cycle, Begin Burst | External | L | H | L | L | H | L | X | H | H | L-H | Tri-State |
| Read Cycle, Continue Burst | Next | X | X | X | L | H | H | L | H | L | L-H | Q |
| Read Cycle, Continue Burst | Next | X | X | X | L | H | H | L | H | H | L-H | Tri-State |
| Read Cycle, Continue Burst | Next | H | X | X | L | X | H | L | H | L | L-H | Q |
| Read Cycle, Continue Burst | Next | H | X | X | L | X | H | L | H | H | L-H | Tri-State |
| Write Cycle, Continue Burst | Next | X | X | X | L | H | H | L | L | X | L-H | D |
| Write Cycle, Continue Burst | Next | H | X | X | L | X | H | L | L | X | L-H | D |
| Read Cycle, Suspend Burst | Current | X | X | X | L | H | H | H | H | L | L-H | Q |
| Read Cycle, Suspend Burst | Current | X | X | X | L | H | H | H | H | H | L-H | Tri-State |
| Read Cycle, Suspend Burst | Current | H | X | X | L | X | H | H | H | L | L-H | Q |
| Read Cycle, Suspend Burst | Current | H | X | X | L | X | H | H | H | H | L-H | Tri-State |
| Write Cycle, Suspend Burst | Current | X | X | X | L | H | H | H | L | X | L-H | D |
| Write Cycle, Suspend Burst | Current | H | X | X | L | X | H | H | L | X | L-H | D |

Notes

2. X = Do Not Care, H = Logic HIGH, L = Logic LOW.
3. WRITE = L when any one or more byte write enable signals and $\overline{BWE} = L$ or $\overline{GW} = L$. WRITE = H when all byte write enable signals, \overline{BWE} , $\overline{GW} = H$.
4. The DQ pins are controlled by the current cycle and the OE signal. OE is asynchronous and is not sampled with the clock.
5. The SRAM always initiates a read cycle when ADSP is asserted, regardless of the state of GW, BWE, or BW_X. Writes may occur only on subsequent clocks after the ADSP or with the assertion of ADSC. As a result, OE must be driven HIGH prior to the start of the write cycle to enable the outputs to tri-state. OE is a do not care for the remainder of the write cycle.
6. OE is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are tri-state when OE is inactive or when the device is deselected, and all data bits behave as outputs when OE is active (LOW).

Truth Table for Read/Write

The read-write truth table for CY7C1481BV33 follows. [7, 8]

| Function (CY7C1481BV33) | \overline{GW} | \overline{BWE} | $\overline{BW_D}$ | $\overline{BW_C}$ | $\overline{BW_B}$ | $\overline{BW_A}$ |
|---|-----------------|------------------|-------------------|-------------------|-------------------|-------------------|
| Read | H | H | X | X | X | X |
| Read | H | L | H | H | H | H |
| Write Byte A (DQ _A , DQP _A) | H | L | H | H | H | L |
| Write Byte B (DQ _B , DQP _B) | H | L | H | H | L | H |
| Write Bytes A, B (DQ _A , DQ _B , DQP _A , DQP _B) | H | L | H | H | L | L |
| Write Byte C (DQ _C , DQP _C) | H | L | H | L | H | H |
| Write Bytes C, A (DQ _C , DQ _A , DQP _C , DQP _A) | H | L | H | L | H | L |
| Write Bytes C, B (DQ _C , DQ _B , DQP _C , DQP _B) | H | L | H | L | L | H |
| Write Bytes C, B, A (DQ _C , DQ _B , DQ _A , DQP _C , DQP _B , DQP _A) | H | L | H | L | L | L |
| Write Byte D (DQ _D , DQP _D) | H | L | L | H | H | H |
| Write Bytes D, A (DQ _D , DQ _A , DQP _D , DQP _A) | H | L | L | H | H | L |
| Write Bytes D, B (DQ _D , DQ _B , DQP _D , DQP _A) | H | L | L | H | L | H |
| Write Bytes D, B, A (DQ _D , DQ _B , DQ _A , DQP _D , DQP _B , DQP _A) | H | L | L | H | L | L |
| Write Bytes D, B (DQ _D , DQ _B , DQP _D , DQP _B) | H | L | L | L | H | H |
| Write Bytes D, B, A (DQ _D , DQ _C , DQ _A , DQP _D , DQP _C , DQP _A) | H | L | L | L | H | L |
| Write Bytes D, C, A (DQ _D , DQ _B , DQ _A , DQP _D , DQP _B , DQP _A) | H | L | L | L | L | H |
| Write All Bytes | H | L | L | L | L | L |
| Write All Bytes | L | X | X | X | X | X |

Notes

7. X = Do Not Care, H = Logic HIGH, L = Logic LOW.

8. Table only includes a partial listing of the byte write combinations. Any combination of $\overline{BW_X}$ is valid. An appropriate write is performed based on which byte write is active.

IEEE 1149.1 Serial Boundary Scan (JTAG)

The CY7C1481BV33 incorporates a serial boundary scan test access port (TAP). This port operates in accordance with IEEE Standard 1149.1-1990 but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC standard 3.3 V or 2.5 V I/O logic levels.

The CY7C1481BV33 contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, tie TCK LOW (V_{SS}) to prevent device clocking. TDI and TMS are internally pulled up and may be unconnected. They may alternatively be connected to V_{DD} through a pull up resistor. TDO must be left unconnected. At power up, the device comes up in a reset state, which does not interfere with the operation of the device.

Test Access Port (TAP)

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input gives commands to the TAP controller and is sampled on the rising edge of TCK. You can leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI ball serially inputs information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the [TAP Controller State Diagram on page 13](#). TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register.

Test Data-Out (TDO)

The TDO output ball serially clocks data-out from the registers. Whether the output is active depends on the current state of the TAP state machine (see [Identification Codes on page 17](#)). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

Performing a TAP Reset

To perform a RESET, force TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power up, the TAP is reset internally to ensure that TDO comes up in a High Z state.

TAP Registers

Registers are connected between the TDI and TDO balls to scan the data in and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls, as shown in the [TAP Controller Block Diagram on page 14](#). At power up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state, as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary "01" pattern to enable fault isolation of the board level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that is placed between the TDI and TDO balls. This shifts the data through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM. The $\times 36$ configuration has a 73-bit long register.

The boundary scan register is loaded with the contents of the RAM IO ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions are used to capture the contents of the I/O ring.

The [Boundary Scan Exit Order on page 18](#) show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in [Identification Register Definitions on page 17](#).

TAP Instruction Set

Overview

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in [Identification Codes on page 17](#). Three of these instructions are listed as RESERVED and must not be used. The other five instructions are described in this section in detail.

The TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented.

The TAP controller cannot be used to load address data or control signals into the SRAM and cannot preload the I/O buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather, it performs a capture of the I/O ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction after it is shifted in, the TAP controller must be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction that is executed whenever the instruction register is loaded with all zeros. EXTEST is not implemented in this SRAM TAP controller, and therefore this device is not compliant to 1149.1. The TAP controller does recognize an all-zero instruction.

When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction is loaded. There is one difference between the two instructions. Unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a High Z state.

IDCODE

The IDCODE instruction loads a vendor specific, 32-bit code into the instruction register. It also places the instruction register between the TDI and TDO balls and shifts the IDCODE out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register at power up or whenever the TAP controller is in a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction connects the boundary scan register between the TDI and TDO balls when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the device TAP controller is not fully 1149.1 compliant.

When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and bidirectional balls is captured in the boundary scan register.

Be aware that the TAP controller clock only operates at a frequency up to 10 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output may undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This does not harm the device, but there is no guarantee as to the value that may be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time (t_{CS} plus t_{CH}).

The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CLK captured in the boundary scan register.

After the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO balls.

Note that because the PRELOAD part of the command is not implemented, putting the TAP to the Update-DR state while performing a SAMPLE/PRELOAD instruction has the same effect as the Pause-DR command.

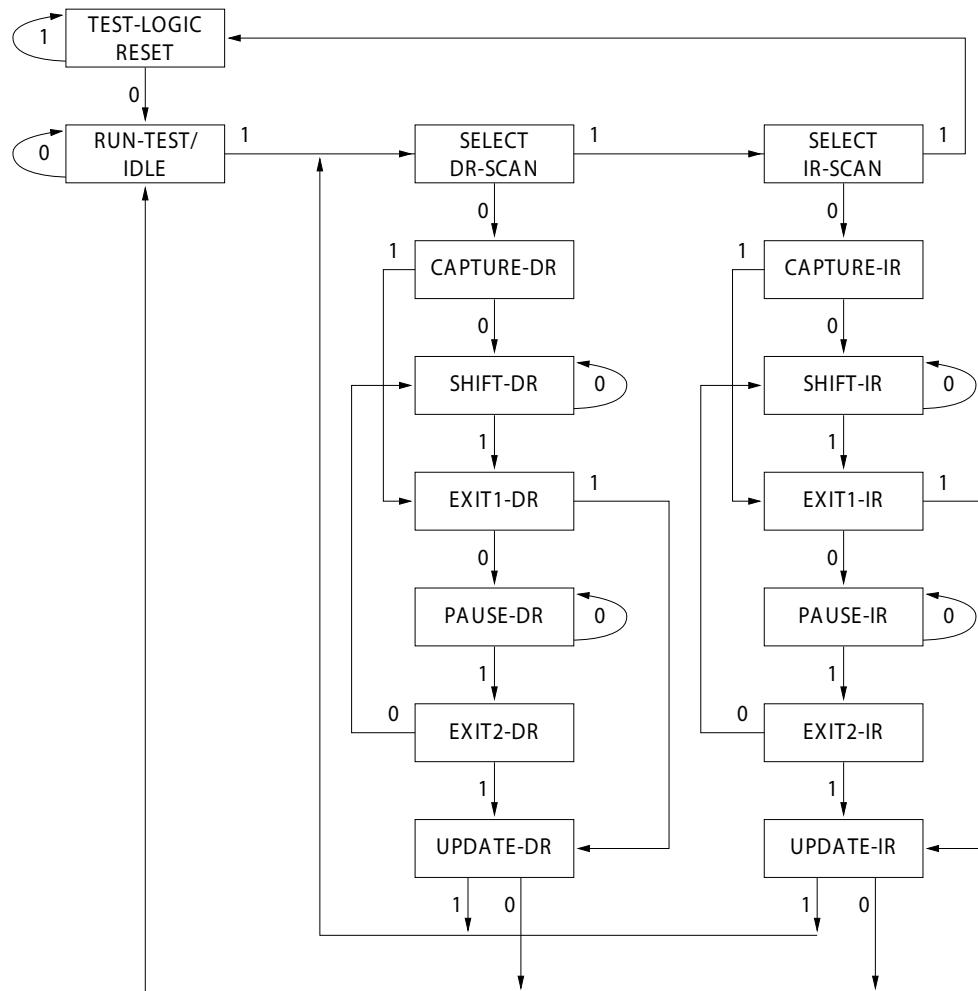
BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO balls. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

Reserved

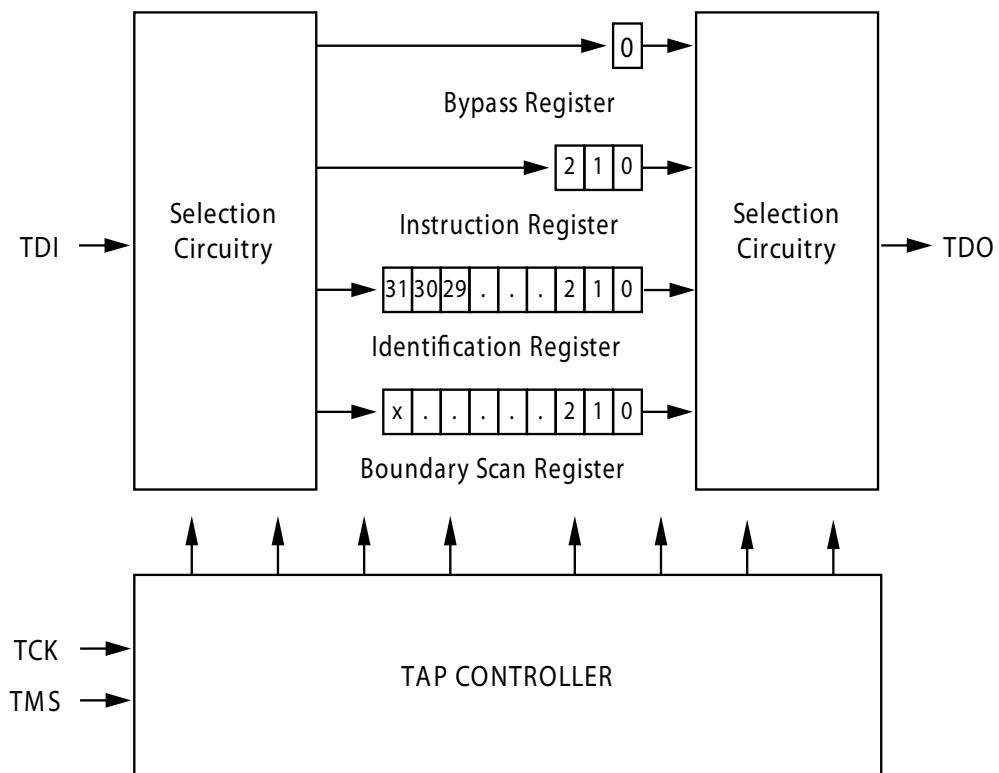
These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Controller State Diagram



The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

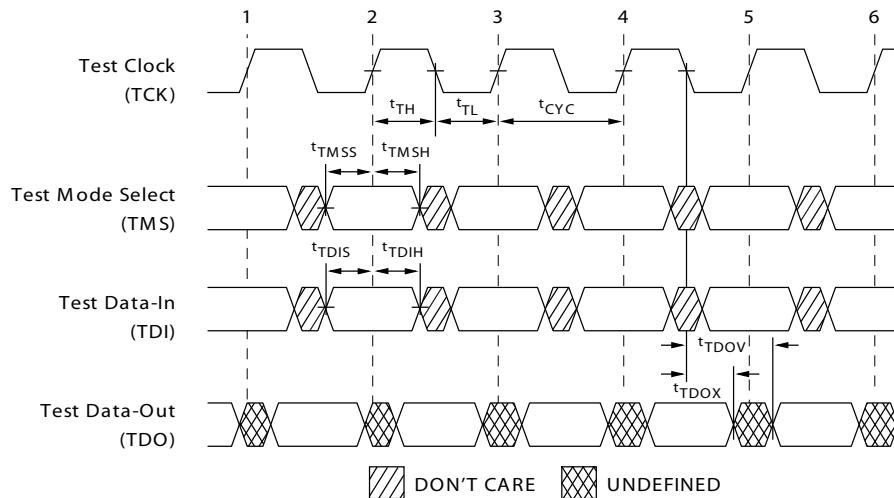
TAP Controller Block Diagram



TAP Timing

Figure 3 shows the TAP timing diagram.

Figure 3. TAP Timing



TAP AC Switching Characteristics

Over the Operating Range

| Parameter ^[9, 10] | Description | Min | Max | Unit |
|------------------------------|-------------------------------|-----|-----|------|
| Clock | | | | |
| t_{TCYC} | TCK Clock Cycle Time | 50 | — | ns |
| t_{TF} | TCK Clock Frequency | — | 20 | MHz |
| t_{TH} | TCK Clock HIGH Time | 20 | — | ns |
| t_{TL} | TCK Clock LOW Time | 20 | — | ns |
| Output Times | | | | |
| t_{TDOV} | TCK Clock LOW to TDO Valid | — | 10 | ns |
| t_{TDOX} | TCK Clock LOW to TDO Invalid | 0 | — | ns |
| Setup Times | | | | |
| t_{TMSS} | TMS Setup to TCK Clock Rise | 5 | — | ns |
| t_{TDIS} | TDI Setup to TCK Clock Rise | 5 | — | ns |
| t_{CS} | Capture Setup to TCK Rise | 5 | — | ns |
| Hold Times | | | | |
| t_{TMSH} | TMS hold after TCK Clock Rise | 5 | — | ns |
| t_{TDIH} | TDI Hold after Clock Rise | 5 | — | ns |
| t_{CH} | Capture Hold after Clock Rise | 5 | — | ns |

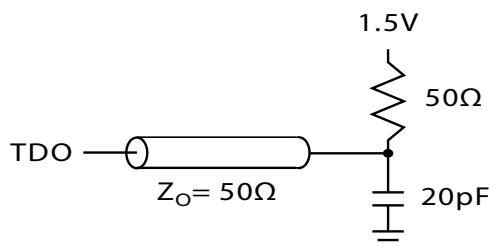
Notes

9. t_{CS} and t_{CH} refer to the setup and hold time requirements of latching data from the boundary scan register.
 10. Test conditions are specified using the load in TAP AC test Conditions. $t_R/t_F = 1$ ns.

3.3 V TAP AC Test Conditions

Input pulse levels V_{SS} to 3.3 V
 Input rise and fall times 1 ns
 Input timing reference levels 1.5 V
 Output reference levels 1.5 V
 Test load termination supply voltage 1.5 V

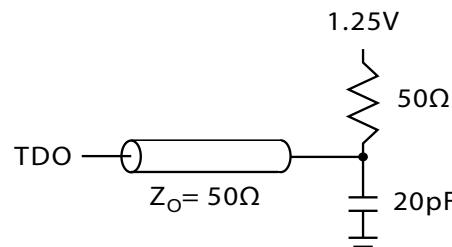
3.3 V TAP AC Output Load Equivalent



2.5 V TAP AC Test Conditions

Input pulse levels V_{SS} to 2.5 V
 Input rise and fall time 1 ns
 Input timing reference levels 1.25 V
 Output reference levels 1.25 V
 Test load termination supply voltage 1.25 V

2.5 V TAP AC Output Load Equivalent



TAP DC Electrical Characteristics and Operating Conditions

($0^\circ\text{C} < T_A < +70^\circ\text{C}$; $V_{DD} = 3.135\text{ V}$ to 3.6 V unless otherwise noted)

| Parameter ^[11] | Description | | Conditions | Min | Max | Unit |
|---------------------------|---------------------|------------------------------------|--------------------------|------|----------------|---------------|
| V_{OH1} | Output HIGH Voltage | $I_{OH} = -4.0\text{ mA}$ | $V_{DDQ} = 3.3\text{ V}$ | 2.4 | — | V |
| | | $I_{OH} = -1.0\text{ mA}$ | $V_{DDQ} = 2.5\text{ V}$ | 2.0 | — | V |
| V_{OH2} | Output HIGH Voltage | $I_{OH} = -100\text{ }\mu\text{A}$ | $V_{DDQ} = 3.3\text{ V}$ | 2.9 | — | V |
| | | | $V_{DDQ} = 2.5\text{ V}$ | 2.1 | — | V |
| V_{OL1} | Output LOW Voltage | $I_{OL} = 8.0\text{ mA}$ | $V_{DDQ} = 3.3\text{ V}$ | — | 0.4 | V |
| | | $I_{OL} = 1.0\text{ mA}$ | $V_{DDQ} = 2.5\text{ V}$ | — | 0.4 | V |
| V_{OL2} | Output LOW Voltage | $I_{OL} = 100\text{ }\mu\text{A}$ | $V_{DDQ} = 3.3\text{ V}$ | — | 0.2 | V |
| | | | $V_{DDQ} = 2.5\text{ V}$ | — | 0.2 | V |
| V_{IH} | Input HIGH Voltage | | $V_{DDQ} = 3.3\text{ V}$ | 2.0 | $V_{DD} + 0.3$ | V |
| | | | $V_{DDQ} = 2.5\text{ V}$ | 1.7 | $V_{DD} + 0.3$ | V |
| V_{IL} | Input LOW Voltage | | $V_{DDQ} = 3.3\text{ V}$ | -0.3 | 0.8 | V |
| | | | $V_{DDQ} = 2.5\text{ V}$ | -0.3 | 0.7 | V |
| I_x | Input Load Current | $GND \leq V_{IN} \leq V_{DDQ}$ | | -5 | 5 | μA |

Note

11. All voltages refer to V_{SS} (GND).

Identification Register Definitions

Bit# 24 is "1" in the ID Register definitions for both 2.5 V and 3.3 V versions of the device.

| Instruction Field | CY7C1481BV33 (2M × 36) | Description |
|------------------------------------|---------------------------|--|
| Revision Number (31:29) | 000 | Describes the version number |
| Device Depth (28:24) | 01011 | Reserved for internal use |
| Architecture/Memory Type (23:18) | 000001 | Defines memory type and architecture |
| Bus Width/Density (17:12) | 100100 | Defines width and density |
| Cypress JEDEC ID Code (11:1) | 00000110100 | Enables unique identification of SRAM vendor |
| ID Register Presence Indicator (0) | 1 | Indicates the presence of an ID register |

Scan Register Sizes

| Register Name | Bit Size (× 36) |
|-------------------------------------|-----------------|
| Instruction Bypass | 3 |
| Bypass | 1 |
| ID | 32 |
| Boundary Scan Order – 165-ball FBGA | 73 |

Identification Codes

| Instruction | Code | Description |
|----------------|------|--|
| EXTTEST | 000 | Captures I/O ring contents. |
| IDCODE | 001 | Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations. |
| SAMPLE Z | 010 | Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High Z state. |
| RESERVED | 011 | Do Not Use: This instruction is reserved for future use. |
| SAMPLE/PRELOAD | 100 | Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation. |
| RESERVED | 101 | Do Not Use: This instruction is reserved for future use. |
| RESERVED | 110 | Do Not Use: This instruction is reserved for future use. |
| BYPASS | 111 | Places the bypass register between TDI and TDO. This operation does not affect SRAM operations. |

Boundary Scan Exit Order

(2M × 36)

| Bit # | 165-ball ID |
|-------|-------------|
| 1 | C1 |
| 2 | D1 |
| 3 | E1 |
| 4 | D2 |
| 5 | E2 |
| 6 | F1 |
| 7 | G1 |
| 8 | F2 |
| 9 | G2 |
| 10 | J1 |
| 11 | K1 |
| 12 | L1 |
| 13 | J2 |
| 14 | M1 |
| 15 | N1 |
| 16 | K2 |
| 17 | L2 |
| 18 | M2 |
| 19 | R1 |
| 20 | R2 |

| Bit # | 165-ball ID |
|-------|-------------|
| 21 | R3 |
| 22 | P2 |
| 23 | R4 |
| 24 | P6 |
| 25 | R6 |
| 26 | N6 |
| 27 | P11 |
| 28 | R8 |
| 29 | P3 |
| 30 | P4 |
| 31 | P8 |
| 32 | P9 |
| 33 | P10 |
| 34 | R9 |
| 35 | R10 |
| 36 | R11 |
| 37 | N11 |
| 38 | M11 |
| 39 | L11 |
| 40 | M10 |

| Bit # | 165-ball ID |
|-------|-------------|
| 41 | L10 |
| 42 | K11 |
| 43 | J11 |
| 44 | K10 |
| 45 | J10 |
| 46 | H11 |
| 47 | G11 |
| 48 | F11 |
| 49 | E11 |
| 50 | D10 |
| 51 | D11 |
| 52 | C11 |
| 53 | G10 |
| 54 | F10 |
| 55 | E10 |
| 56 | A10 |
| 57 | B10 |
| 58 | A9 |
| 59 | B9 |
| 60 | A8 |

| Bit # | 165-ball ID |
|-------|-------------|
| 61 | B8 |
| 62 | A7 |
| 63 | B7 |
| 64 | B6 |
| 65 | A6 |
| 66 | B5 |
| 67 | A5 |
| 68 | A4 |
| 69 | B4 |
| 70 | B3 |
| 71 | A3 |
| 72 | A2 |
| 73 | B2 |

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Ambient Temperature

with Power Applied -55°C to $+125^{\circ}\text{C}$

Supply Voltage on V_{DD} Relative to GND -0.3 V to $+4.6\text{ V}$

Supply Voltage on V_{DDQ} Relative to GND -0.3 V to $+V_{DD}$

DC Voltage Applied to Outputs

in Tri-State -0.5 V to $V_{DDQ} + 0.5\text{ V}$

DC Input Voltage -0.5 V to $V_{DD} + 0.5\text{ V}$

Current into Outputs (LOW) 20 mA

Static Discharge Voltage

(MIL-STD-883, Method 3015) $>2001\text{ V}$

Latch Up Current $>200\text{ mA}$

Operating Range

| Range | Ambient Temperature | V_{DD} | V_{DDQ} |
|------------|--|------------------------------------|-------------------------------------|
| Commercial | 0°C to $+70^{\circ}\text{C}$ | $3.3\text{ V} - 5\%$ / $+ 10\%$ | $2.5\text{ V} - 5\%$ to V_{DD} |
| Industrial | -40°C to $+85^{\circ}\text{C}$ | | |

Electrical Characteristics

Over the Operating Range

| Parameter ^[12, 13] | Description | Test Conditions | | Min | Max | Unit |
|-------------------------------|---|---|--------------------------|-------|-------------------------|---------------|
| V_{DD} | Power Supply Voltage | | | 3.135 | 3.6 | V |
| V_{DDQ} | IO Supply Voltage | For 3.3 V I/O | | 3.135 | V_{DD} | V |
| | | For 2.5 V I/O | | 2.375 | 2.625 | V |
| V_{OH} | Output HIGH Voltage | For 3.3 V I/O, $I_{OH} = -4.0\text{ mA}$ | | 2.4 | — | V |
| | | For 2.5 V I/O, $I_{OH} = -1.0\text{ mA}$ | | 2.0 | — | V |
| V_{OL} | Output LOW Voltage | For 3.3 V I/O, $I_{OL} = 8.0\text{ mA}$ | | — | 0.4 | V |
| | | For 2.5 V I/O, $I_{OL} = 1.0\text{ mA}$ | | — | 0.4 | V |
| V_{IH} | Input HIGH Voltage ^[12] | For 3.3 V I/O | | 2.0 | $V_{DD} + 0.3\text{ V}$ | V |
| | | For 2.5 V I/O | | 1.7 | $V_{DD} + 0.3\text{ V}$ | V |
| V_{IL} | Input LOW Voltage ^[12] | For 3.3 V I/O | | -0.3 | 0.8 | V |
| | | For 2.5 V I/O | | -0.3 | 0.7 | V |
| I_x | Input Leakage Current Except ZZ and MODE | $GND \leq V_I \leq V_{DDQ}$ | | -5 | 5 | μA |
| | Input Current of MODE | Input = V_{SS} | | -30 | — | μA |
| | | Input = V_{DD} | | — | 5 | μA |
| | Input Current of ZZ | Input = V_{SS} | | -5 | — | μA |
| | | Input = V_{DD} | | — | 30 | μA |
| I_{OZ} | Output Leakage Current | $GND \leq V_I \leq V_{DD}$, Output Disabled | | -5 | 5 | μA |
| I_{DD} ^[14] | V_{DD} Operating Supply Current | $V_{DD} = \text{Max}$, $I_{OUT} = 0\text{ mA}$, $f = f_{MAX} = 1/t_{CYC}$ | 7.5 ns cycle, 133 MHz | — | 335 | mA |
| I_{SB1} | Automatic CE Power Down Current – TTL Inputs | Max V_{DD} , Device Deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$, inputs switching | 7.5 ns cycle, 133 MHz | — | 200 | mA |
| I_{SB2} | Automatic CE Power Down Current – CMOS Inputs | Max V_{DD} , Device Deselected, $V_{IN} \geq V_{DD} - 0.3\text{ V}$ or $V_{IN} \leq 0.3\text{ V}$, $f = 0$, inputs static | 7.5 ns cycle, 133 MHz | — | 150 | mA |
| I_{SB3} | Automatic CE Power Down Current – CMOS Inputs | Max V_{DD} , Device Deselected, $V_{IN} \geq V_{DDQ} - 0.3\text{ V}$ or $V_{IN} \leq 0.3\text{ V}$, $f = f_{MAX}$, inputs switching | 7.5 ns cycle, 133 MHz | — | 200 | mA |
| I_{SB4} | Automatic CE Power Down Current – TTL Inputs | Max V_{DD} , Device Deselected, $V_{IN} \geq V_{DD} - 0.3\text{ V}$ or $V_{IN} \leq 0.3\text{ V}$, $f = 0$, inputs static | 7.5 ns cycle, 133 MHz | — | 165 | mA |

Notes

12. Overshoot: $V_{IH(AC)} < V_{DD} + 1.5\text{ V}$ (pulse width less than $t_{CYC}/2$). Undershoot: $V_{IL(AC)} > -2\text{ V}$ (pulse width less than $t_{CYC}/2$).

13. $T_{Power-up}$: assumes a linear ramp from 0 V to $V_{DD(\text{minimum})}$ within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \leq V_{DD}$.

14. The operation current is calculated with 50% read cycle and 50% write cycle.

Capacitance

| Parameter ^[15] | Description | Test Conditions | 100-pin TQFP Max | 165-ball FBGA Max | Unit |
|---------------------------|---------------------------|---|------------------|-------------------|------|
| $C_{ADDRESS}$ | Address Input Capacitance | $T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{DD} = 3.3\text{ V}$, $V_{DDQ} = 2.5\text{ V}$ | 6 | 6 | pF |
| C_{DATA} | Data Input Capacitance | | 5 | 5 | pF |
| C_{CTRL} | Control Input Capacitance | | 8 | 8 | pF |
| C_{CLK} | Clock Input Capacitance | | 6 | 6 | pF |
| C_{IO} | Input/Output Capacitance | | 5 | 5 | pF |

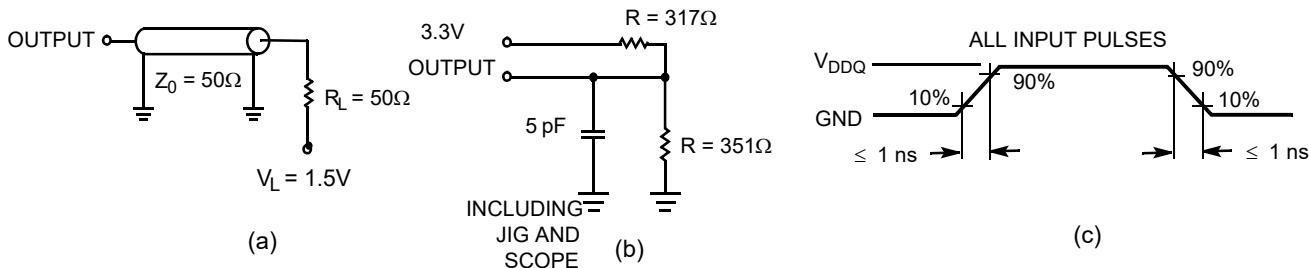
Thermal Resistance

| Parameter ^[15] | Description | Test Conditions | 100-pin TQFP Package | 165-ball FBGA Package | Unit |
|---------------------------|--|--|----------------------|-----------------------|--------------------|
| Θ_{JA} | Thermal Resistance (Junction to Ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51. | 24.63 | 16.3 | $^\circ\text{C/W}$ |
| Θ_{JC} | Thermal Resistance (Junction to Case) | | 2.28 | 2.1 | $^\circ\text{C/W}$ |

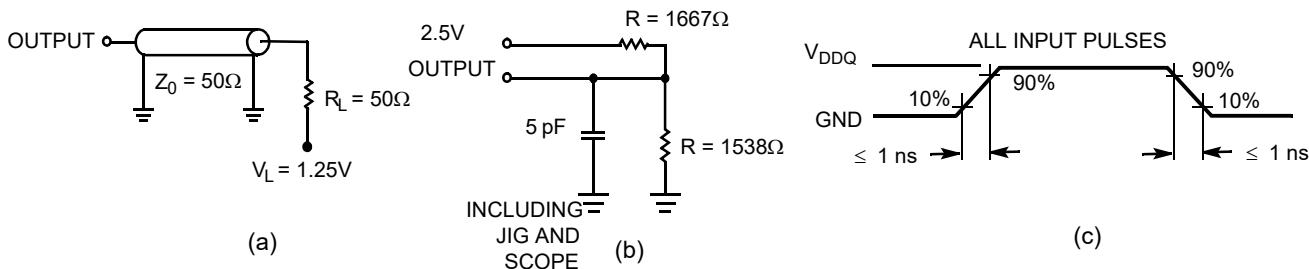
AC Test Loads and Waveforms

Figure 4. AC Test Loads and Waveforms

3.3V IO Test Load



2.5V IO Test Load



Note

15. Tested initially and after any design or process change that may affect these parameters.

Switching Characteristics

Over the Operating Range

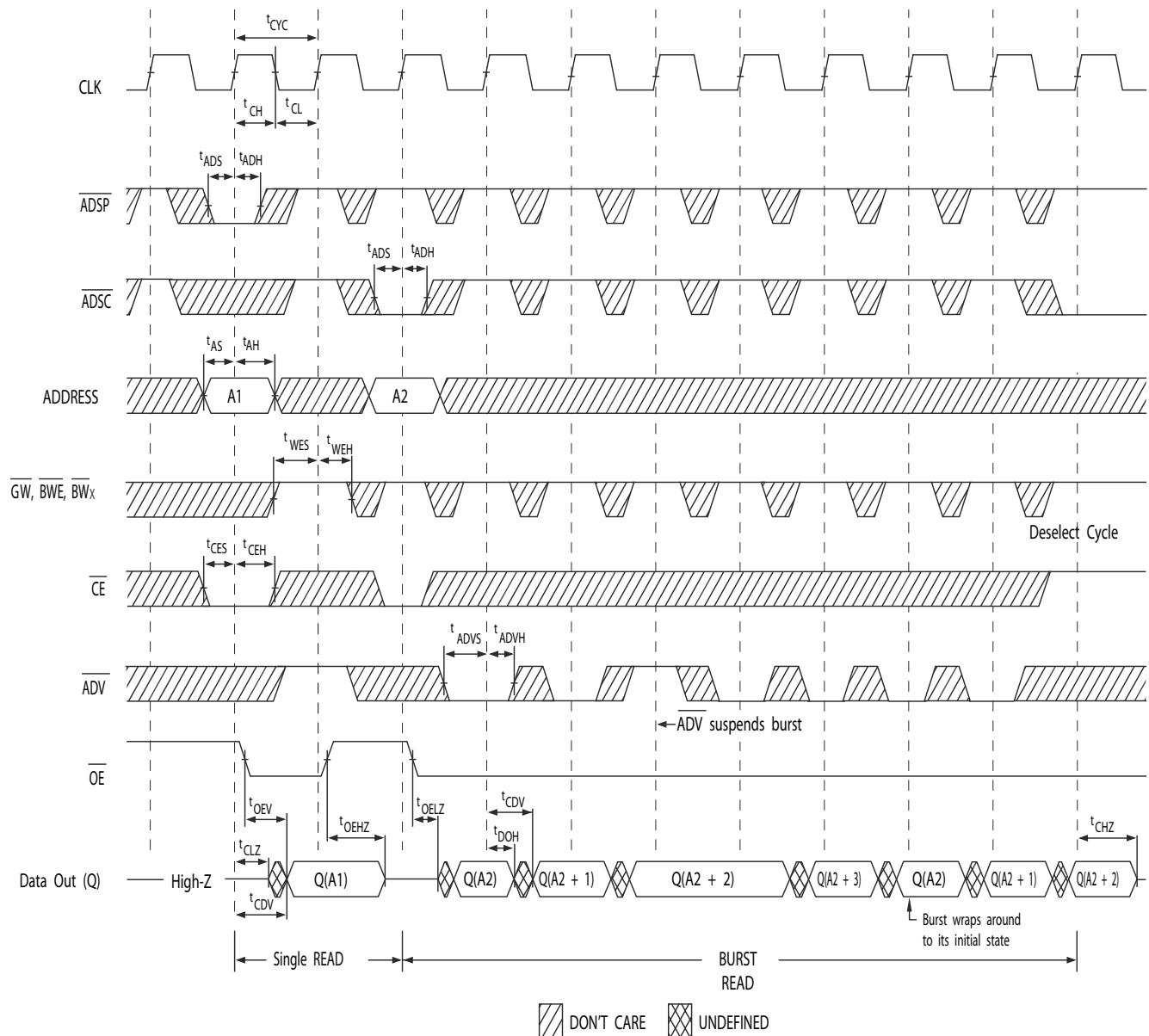
| Parameter [16, 17] | Description | 133 MHz | | Unit |
|---------------------|--|---------|-----|------|
| | | Min | Max | |
| t_{POWER} | V_{DD} (typical) to the First Access [18] | 1 | — | ms |
| Clock | | | | |
| t_{CYC} | Clock Cycle Time | 7.5 | — | ns |
| t_{CH} | Clock HIGH | 2.5 | — | ns |
| t_{CL} | Clock LOW | 2.5 | — | ns |
| Output Times | | | | |
| t_{CDV} | Data Output Valid After CLK Rise | — | 6.5 | ns |
| t_{DOH} | Data Output Hold After CLK Rise | 2.5 | — | ns |
| t_{CLZ} | Clock to Low Z [19, 20, 21] | 3.0 | — | ns |
| t_{CHZ} | Clock to High Z [19, 20, 21] | — | 3.8 | ns |
| t_{OEV} | \overline{OE} LOW to Output Valid | — | 3.0 | ns |
| t_{OELZ} | \overline{OE} LOW to Output Low Z [19, 20, 21] | 0 | — | ns |
| t_{OEHZ} | \overline{OE} HIGH to Output High Z [19, 20, 21] | — | 3.0 | ns |
| Setup Times | | | | |
| t_{AS} | Address Setup Before CLK Rise | 1.5 | — | ns |
| t_{ADS} | ADSP, ADSC Setup Before CLK Rise | 1.5 | — | ns |
| t_{ADVS} | ADV Setup Before CLK Rise | 1.5 | — | ns |
| t_{WES} | GW, BWE, \overline{BW}_X Setup Before CLK Rise | 1.5 | — | ns |
| t_{DS} | Data Input Setup Before CLK Rise | 1.5 | — | ns |
| t_{CES} | Chip Enable Setup | 1.5 | — | ns |
| Hold Times | | | | |
| t_{AH} | Address Hold After CLK Rise | 0.5 | — | ns |
| t_{ADH} | ADSP, ADSC Hold After CLK Rise | 0.5 | — | ns |
| t_{WEH} | GW, BWE, \overline{BW}_X Hold After CLK Rise | 0.5 | — | ns |
| t_{ADVH} | ADV Hold After CLK Rise | 0.5 | — | ns |
| t_{DH} | Data Input Hold After CLK Rise | 0.5 | — | ns |
| t_{CEH} | Chip Enable Hold After CLK Rise | 0.5 | — | ns |

Notes

16. Timing reference level is 1.5 V when $V_{DDQ} = 3.3$ V and is 1.25 V when $V_{DDQ} = 2.5$ V.
17. Test conditions shown in (a) of [Figure 4 on page 20](#) unless otherwise noted.
18. This part has an internal voltage regulator; t_{POWER} is the time that the power is supplied above $V_{DD(\text{minimum})}$ initially, before a read or write operation can be initiated.
19. t_{CHZ} , t_{CLZ} , t_{OELZ} , and t_{OEHZ} are specified with AC test conditions shown in part (b) of [Figure 4 on page 20](#). Transition is measured ± 200 mV from steady-state voltage.
20. At any supplied voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. The device is designed to achieve High Z before Low Z under the same system conditions.
21. This parameter is sampled and not 100% tested.

Timing Diagrams

Figure 5. Read Cycle Timing [22]

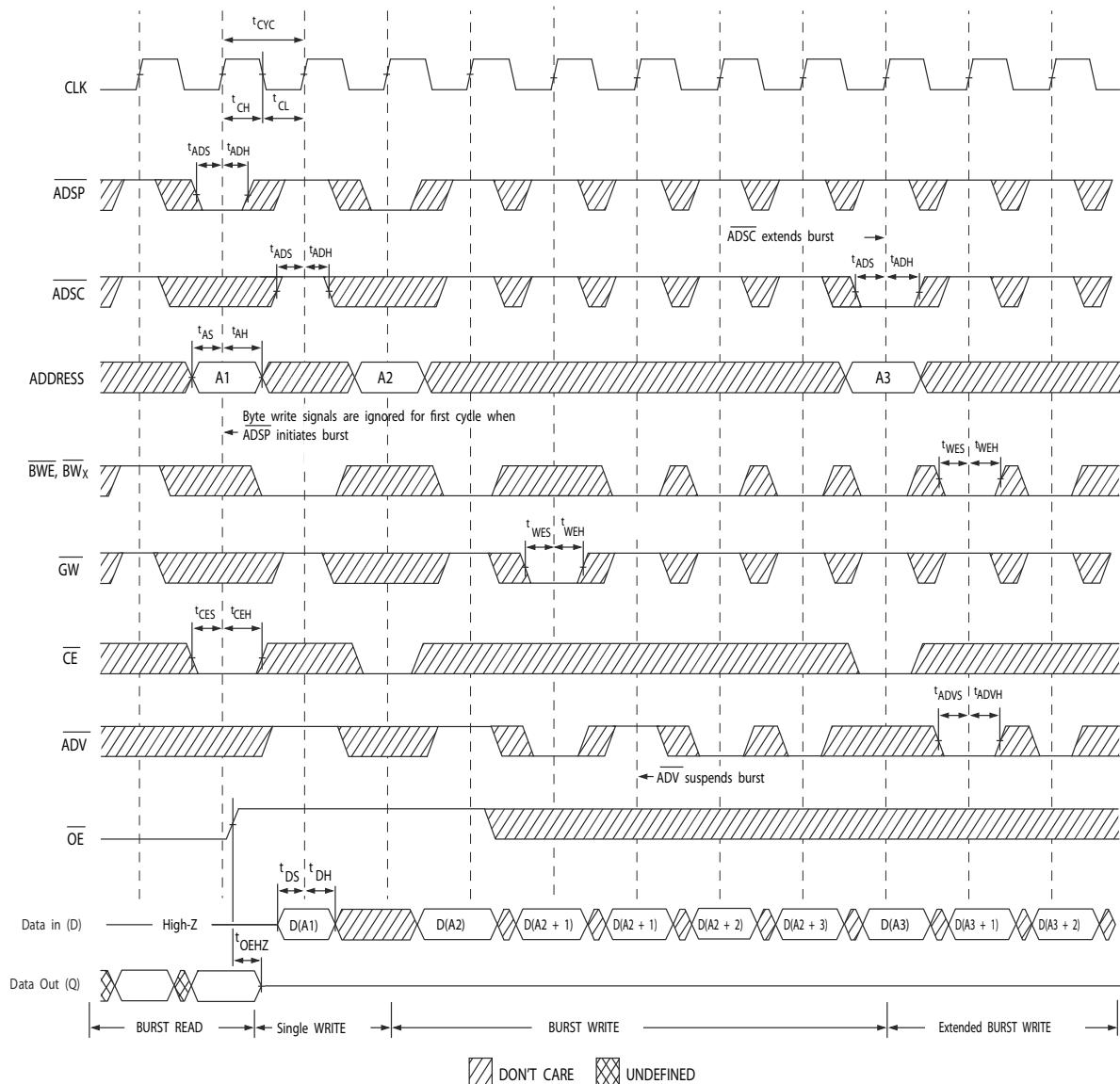


Note

22. On this diagram, when \overline{CE} is LOW: \overline{CE}_1 is LOW, CE_2 is HIGH, and \overline{CE}_3 is LOW. When \overline{CE} is HIGH: \overline{CE}_1 is HIGH, CE_2 is LOW, or \overline{CE}_3 is HIGH.

Timing Diagrams (continued)

Figure 6. Write Cycle Timing [23, 24]

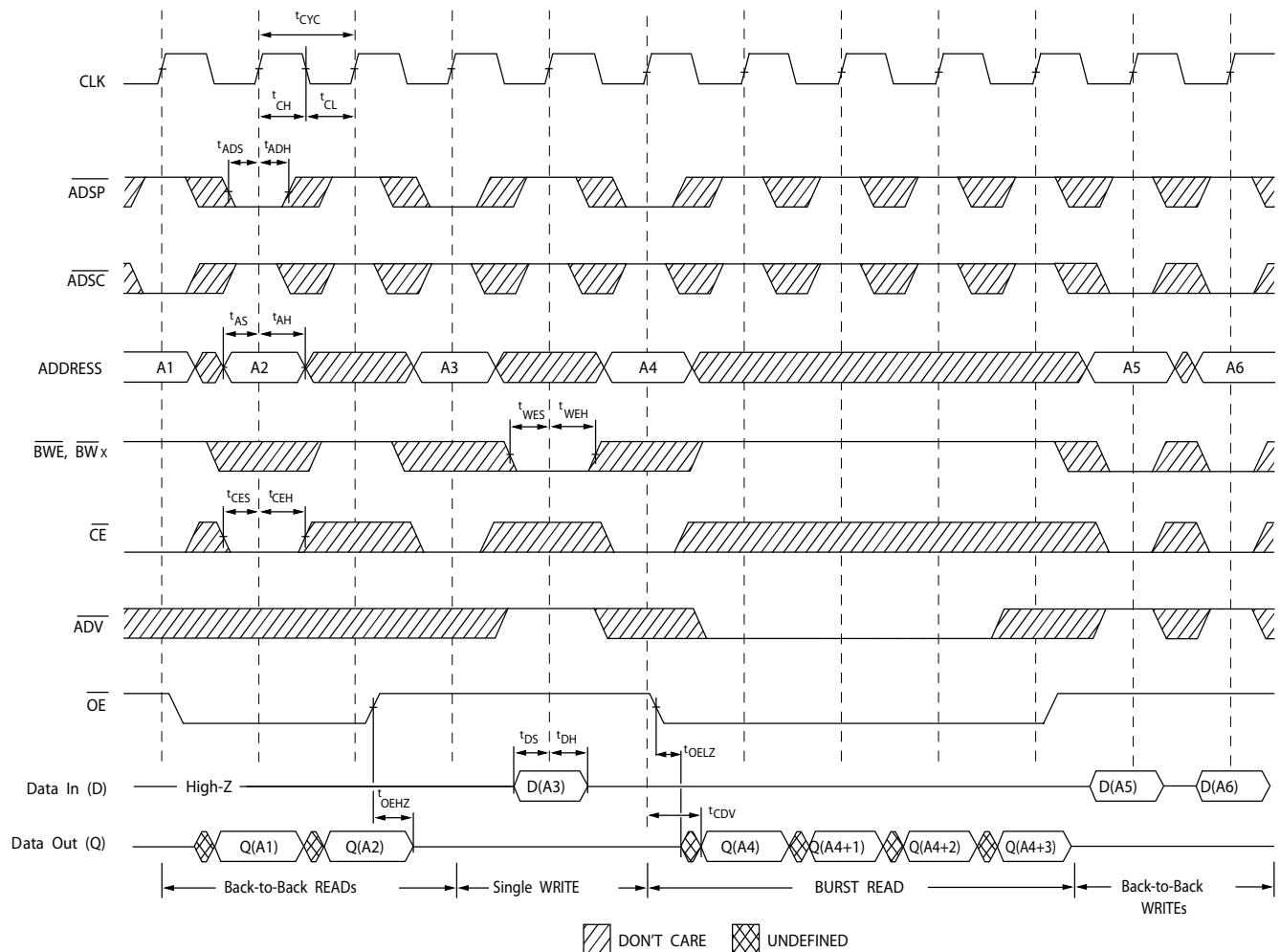


Notes

23. On this diagram, when \overline{CE} is LOW: \overline{CE}_1 is LOW, CE_2 is HIGH, and \overline{CE}_3 is LOW. When \overline{CE} is HIGH: \overline{CE}_1 is HIGH, CE_2 is LOW, or \overline{CE}_3 is HIGH.
24. Full width write can be initiated by either GW LOW; or by GW HIGH, BWE LOW, and BWx LOW.

Timing Diagrams (continued)

Figure 7. Read/Write Cycle Timing [25, 26, 27]

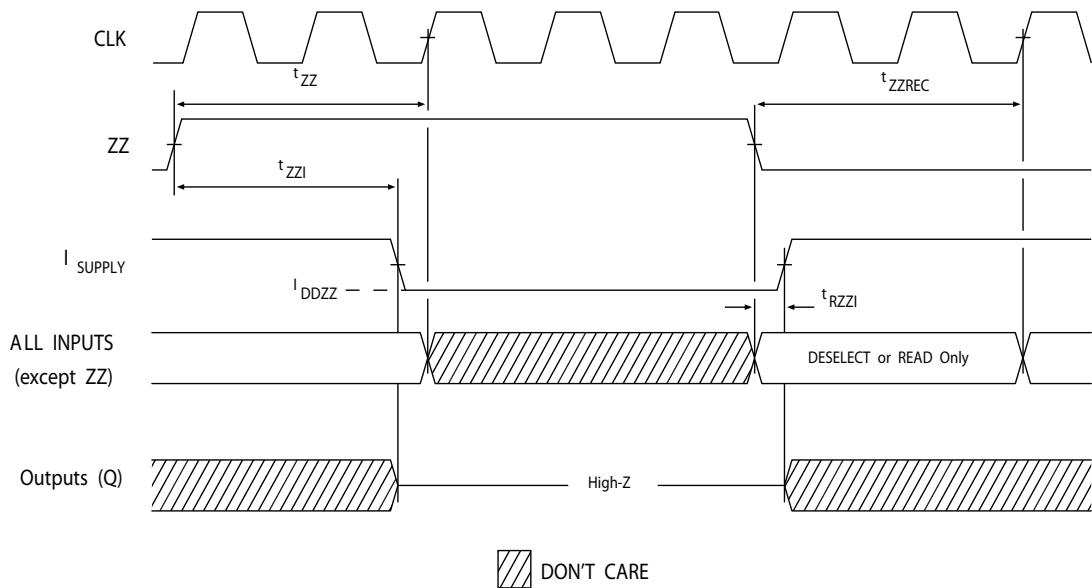


Notes

25. On this diagram, when \overline{CE} is LOW: \overline{CE}_1 is LOW, CE_2 is HIGH, and \overline{CE}_3 is LOW. When \overline{CE} is HIGH: \overline{CE}_1 is HIGH, CE_2 is LOW, or \overline{CE}_3 is HIGH.
26. The data bus (Q) remains in High Z following a write cycle, unless a new read access is initiated by ADSP or ADSC.
27. GW is HIGH.

Timing Diagrams (continued)

Figure 8. ZZ Mode Timing [28, 29]



Notes

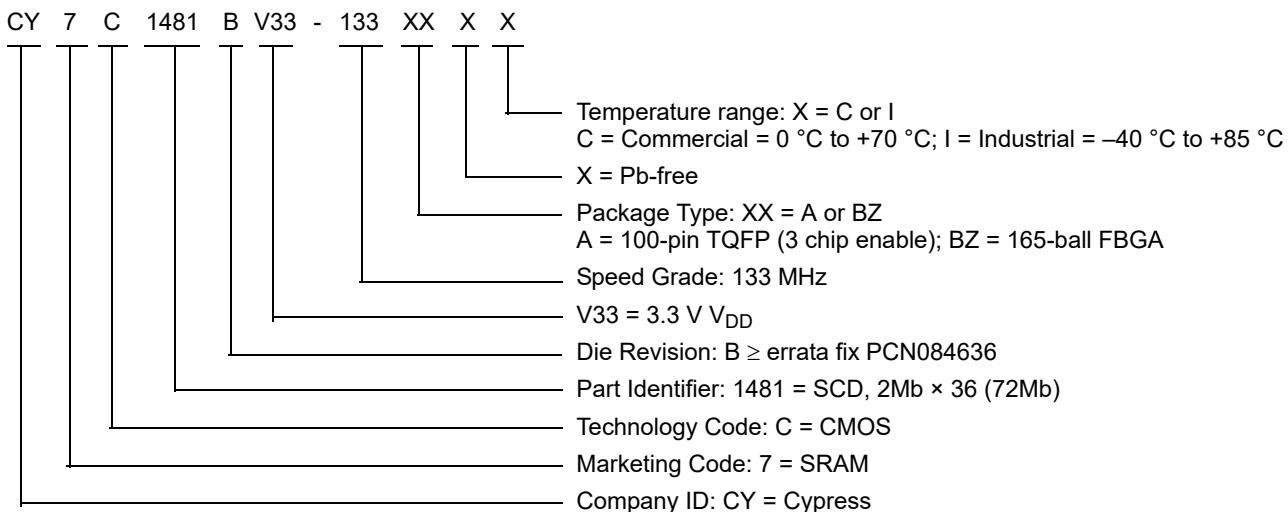
28. Device must be deselected when entering ZZ mode. See [Truth Table on page 9](#) for all possible signal conditions to deselect the device.
 29. DQs are in High Z when exiting ZZ sleep mode.

Ordering Information

Not all of the speed, package, and temperature ranges are available. Please contact your local sales representative or visit www.cypress.com for actual products offered.

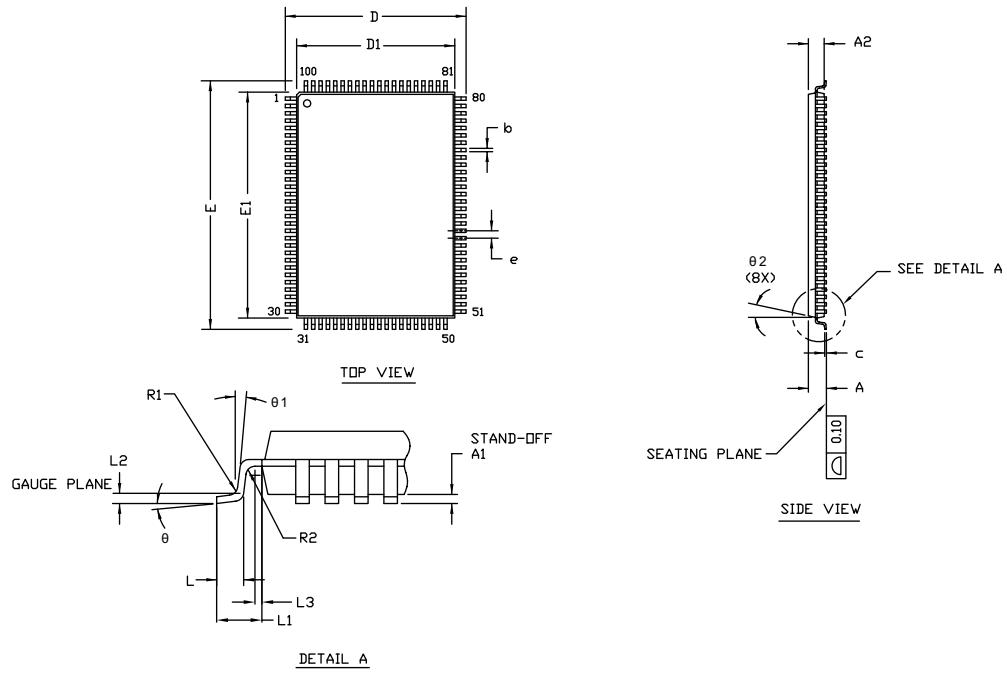
| Speed (MHz) | Ordering Code | Package Diagram | Part and Package Type | Operating Range |
|-------------|---------------------|-----------------|---|-----------------|
| 133 | CY7C1481BV33-133AXI | 51-85050 | 100-pin TQFP (14 × 20 × 1.4 mm) Pb-free | Industrial |

Ordering Code Definitions



Package Diagrams

Figure 9. 100-pin TQFP (14 x 20 x 1.4 mm) A100RA Package Outline, 51-85050



| SYMBOL | DIMENSIONS | | |
|------------|------------|-------|-------|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.60 |
| A1 | 0.05 | — | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| D | 15.80 | 16.00 | 16.20 |
| D1 | 13.90 | 14.00 | 14.10 |
| E | 21.80 | 22.00 | 22.20 |
| E1 | 19.90 | 20.00 | 20.10 |
| R1 | 0.08 | — | 0.20 |
| R2 | 0.08 | — | 0.20 |
| θ | 0° | — | 7° |
| $\theta 1$ | 0° | — | — |
| $\theta 2$ | 11° | 12° | 13° |
| c | — | — | 0.20 |
| b | 0.22 | 0.30 | 0.38 |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00 | REF | |
| L2 | 0.25 | BSC | |
| L3 | 0.20 | — | — |
| e | — | 0.65 | TYP |

NOTE:

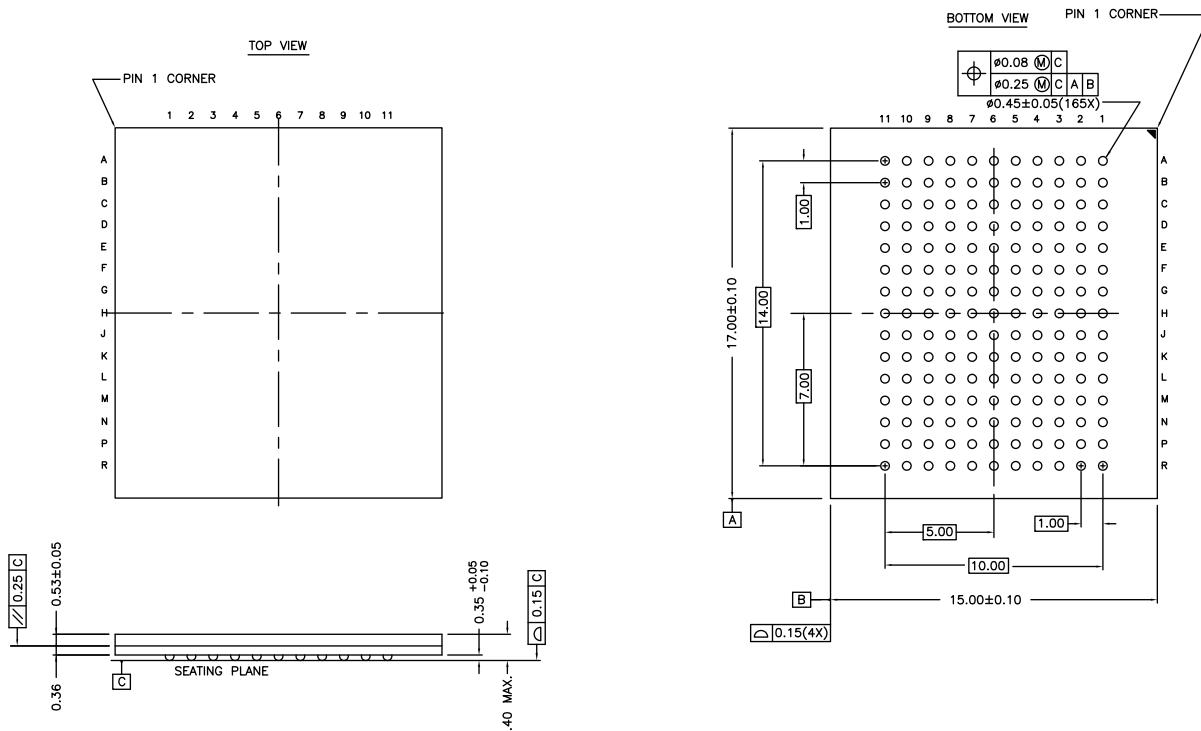
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH. MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE. BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH.
3. JEDEC SPECIFICATION NO. REF: MS-026.

51-85050 *G

Package Diagrams (continued)

Figure 10. 165-ball FBGA (15 × 17 × 1.4 mm (0.45 Ball Diameter)) Package Outline, 51-85165

NOTES:
SOLDER PAD TYPE: SOLDER MASK DEFINED (SMD)
PACKAGE WEIGHT: 0.60g
JEDEC REFERENCE: MO-216 / ISSUE E
PACKAGE CODES: BB0AA / BW0AG



51-85165 *E

Acronyms

| Acronym | Description |
|---------|--|
| CE | Chip Enable |
| CMOS | Complementary Metal Oxide Semiconductor |
| EIA | Electronic Industries Alliance |
| FBGA | Fine-Pitch Ball Grid Array |
| I/O | Input/Output |
| JEDEC | Joint Electron Devices Engineering Council |
| OE | Output Enable |
| SRAM | Static Random Access Memory |
| TQFP | Thin Quad Flat Pack |
| TTL | Transistor-Transistor Logic |

Document Conventions

Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C | degree Celsius |
| MHz | megahertz |
| µA | microampere |
| mA | milliampere |
| mm | millimeter |
| ms | millisecond |
| mV | millivolt |
| ns | nanosecond |
| Ω | ohm |
| % | percent |
| pF | picofarad |
| V | volt |
| W | watt |

Document History Page

Document Title: CY7C1481BV33, 72-Mbit (2M × 36) Flow-Through SRAM
 Document Number: 001-74857

| Rev. | ECN No. | Orig. of Change | Submission Date | Description of Change |
|------|---------|-----------------|-----------------|---|
| ** | 3466988 | GOPA | 01/17/2012 | New data sheet. |
| *A | 3508574 | GOPA | 01/25/2012 | Changed status from Preliminary to Final. |
| *B | 3862706 | PRIT | 01/09/2013 | No technical updates. Completing Sunset Review. |
| *C | 4575228 | PRIT | 11/20/2014 | Updated Functional Description : Added "For a complete list of related documentation, click here ." at the end. Updated Package Diagrams : spec 51-85050 – Changed revision from *D to *E. |
| *D | 5071457 | PRIT | 01/04/2016 | Updated Package Diagrams : spec 51-85165 – Changed revision from *D to *E. Updated to new template. Completing Sunset Review. |
| *E | 5309766 | PRIT | 06/15/2016 | Updated Truth Table . Updated to new template. |
| *F | 6010395 | CNX | 01/02/2018 | Updated Ordering Information : Updated part numbers. Updated Package Diagrams : spec 51-85050 – Changed revision from *E to *G. Updated to new template. Completing Sunset Review. |

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