Switched-Capacitor Voltage Converter with Regulator

FEATURES

- **Available in Space Saving SO-8 Package**
- **Output Current: 100mA**
- Low Loss: 1.1V at 100mA
- Operating Range: 3.5V to 15V
- **Reference and Error Amplifier for Regulation**
- External Shutdown
- External Oscillator Synchronization
- Can Be Paralleled
- Pin Compatible with the LTC®1044/LTC7660

APPLICATIONS

- Voltage Inverter
- Voltage Regulator
- Negative Voltage Doubler
- Positive Voltage Doubler

DESCRIPTION

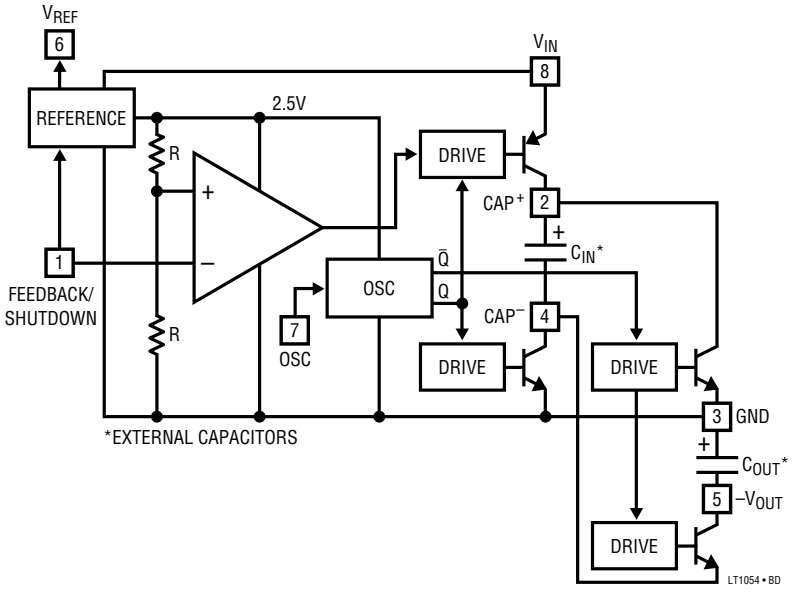
The LT®1054 is a monolithic, bipolar, switched-capacitor voltage converter and regulator. The LT1054 provides higher output current than previously available converters with significantly lower voltage losses. An adaptive switch driver scheme optimizes efficiency over a wide range of output currents. Total voltage loss at 100mA output current is typically 1.1V. This holds true over the full supply voltage range of 3.5V to 15V. Quiescent current is typically 2.5mA.

The LT1054 also provides regulation, a feature not previously available in switched-capacitor voltage converters. By adding an external resistive divider a regulated output can be obtained. This output will be regulated against changes in both input voltage and output current. The LT1054 can also be shut down by grounding the feedback pin. Supply current in shutdown is less than 100µA.

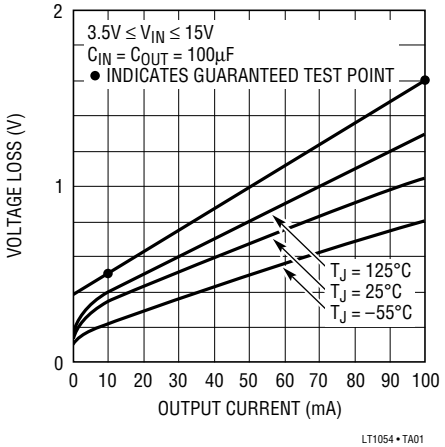
The internal oscillator of the LT1054 runs at a nominal frequency of 25kHz. The oscillator pin can be used to adjust the switching frequency or to externally synchronize the LT1054.

The LT1054 is pin compatible with previous converters such the LTC1044/LTC7660.

BLOCK DIAGRAM



Voltage Loss



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 1) 16V
Input Voltage
- Pin 1 ..... $0V \le V_{PIN1} \le V^+$
- Pin 3 (S Package) ..... $0V \le V_{PIN3} \le V^+$
- Pin 7 ..... $0V \le V_{PIN7} \le V_{REF}$
- Pin 13 (S Package) ..... $0V \le V_{PIN13} \le V_{REF}$

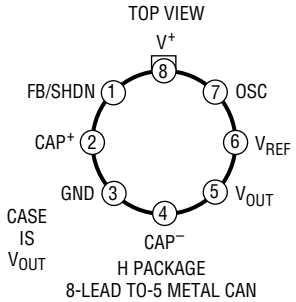
Operating Temperature Range
- LT1054C ..... 0°C to 70°C
- LT1054I ..... –40°C to 85°C
- LT1054M ..... –55°C to 125°C

Junction Temperature Range (Note 2)
- LT1054C ..... 125°C
- LT1054I ..... 125°C
- LT1054M ..... 150°C

Storage Temperature Range
- H, J8, N8 and S8 Packages ..... –55°C to 150°C
- S Package ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

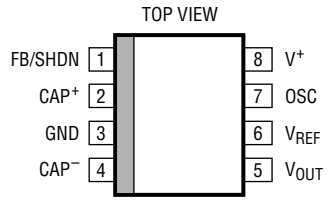
PACKAGE/ORDER INFORMATION (Note 6)



H PACKAGE
8-LEAD TO-5 METAL CAN

T_{JMAX} = 150°C, θ_{JA} = 150°C, θ_{JC} = 45°C/W

ORDER PART NUMBER
LT1054CH
LT1054MH

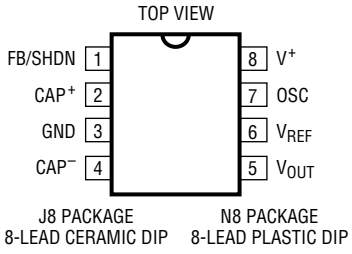


S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = XXX°C, θ_{JA} = XXX°C/W

SEE REGULATION AND CAPACITOR SELECTION SECTIONS IN THE APPLICATIONS INFORMATION FOR IMPORTANT INFORMATION ON THE S8 DEVICE

ORDER PART NUMBER
LT1054CS8
S8 PART MARKING
1054

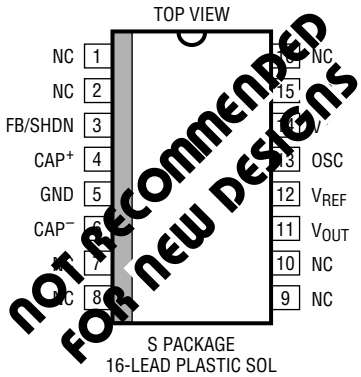


J8 PACKAGE
8-LEAD CERAMIC DIP

N8 PACKAGE
8-LEAD PLASTIC DIP

T_{JMAX} = 150°C, θ_{JA} = 100°C/W (J8)
T_{JMAX} = 125°C, θ_{JA} = 130°C/W (N8)

ORDER PART NUMBER
LT1054CJ8
LT1054CN8
LT1054IN8
LT1054MJ8



NOT RECOMMENDED FOR NEW DESIGNS

S PACKAGE
16-LEAD PLASTIC SOL

T_{JMAX} = 125°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LT1054CS
LT1054IS

ELECTRICAL CHARACTERISTICS (Note 6)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current	I_{LOAD} = 0mA					
	V_{IN} = 3.5V	●		2.5	4.0	mA
	V_{IN} = 15V	●		3.0	5.0	mA
Supply Voltage Range		●	3.5		15	V
Voltage Loss ($V_{IN} - \|V_{OUT}\|$)	$C_{IN} = C_{OUT}$ = 100µF Tantalum (Note 3)					
	I_{OUT} = 10mA	●		0.35	0.55	V
	I_{OUT} = 100mA	●		1.10	1.60	V
Output Resistance	ΔI_{OUT} = 10mA to 100mA (Note 4)	●		10	15	Ω
Oscillator Frequency	3.5V ≤ V_{IN} ≤ 15V	●	15	25	35	kHz
Reference Voltage	I_{REF} = 60µA, T_J = 25°C		2.35	2.50	2.65	V
		●	2.25		2.75	V
Regulated Voltage	V_{IN} = 7V, T_J = 25°C, R_L = 500Ω (Note 5)		–4.70	–5.00	–5.20	V
Line Regulation	7V ≤ V_{IN} ≤ 12V, R_L = 500Ω (Note 5)	●		5	25	mV
Load Regulation	V_{IN} = 7V, 100Ω ≤ R_L ≤ 500Ω (Note 5)	●		10	50	mV
Maximum Switch Current				300		mA
Supply Current in Shutdown	V_{PIN1} = 0V	●		100	200	µA

The ● denotes specifications which apply over the full operating temperature range. For C grade parts these specifications also apply up to a junction temperature of 100°C.

Note 1: The absolute maximum supply voltage rating of 16V is for unregulated circuits. For regulation mode circuits with V_{OUT} ≤ 15V at pin 5, (pin 11 S package) this rating may be increased to 20V.

Note 2: The devices are guaranteed by design to be functional up to the absolute maximum junction temperature.

Note 3: For voltage loss tests, the device is connected as a voltage inverter, with pins 1, 6, and 7 (3, 12, and 13 S package) unconnected. The voltage losses may be higher in other configurations.

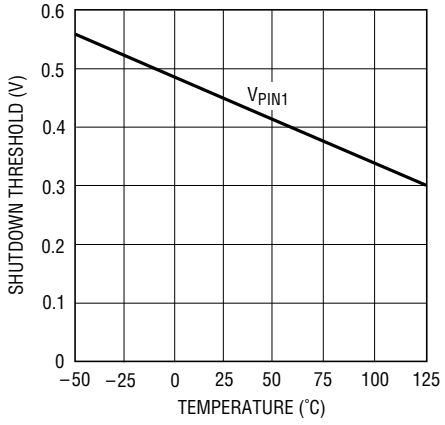
Note 4: Output resistance is defined as the slope of the curve, (ΔV_{OUT} vs ΔI_{OUT}), for output currents of 10mA to 100mA. This represents the linear portion of the curve. The incremental slope of the curve will be higher at currents <10mA due to the characteristics of the switch transistors.

Note 5: All regulation specifications are for a device connected as a positive-to-negative converter/regulator with R1 = 20k, R2 = 102.5k, C1 = 0.002µF, (C1 = 0.05µF S package) C_{IN} = 10µF tantalum, C_{OUT} = 100µF tantalum.

Note 6: The S8 package uses a different die than the H, J8, N8 and S packages. The S8 device will meet all the existing data sheet parameters. See Regulation and Capacitor Selection in the Applications Information section for differences in application requirements.

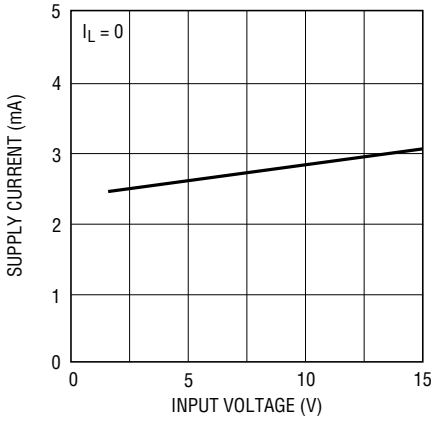
TYPICAL PERFORMANCE CHARACTERISTICS

Shutdown Threshold



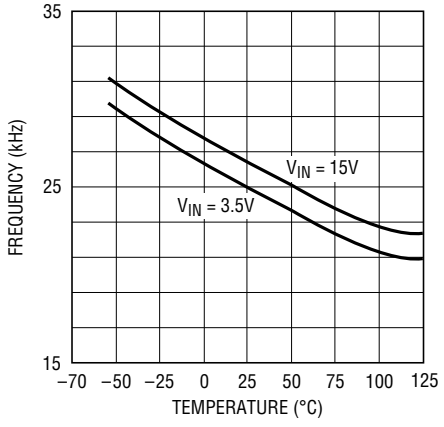
LT1054 • TPC01

Supply Current



LT1054 • TPC02

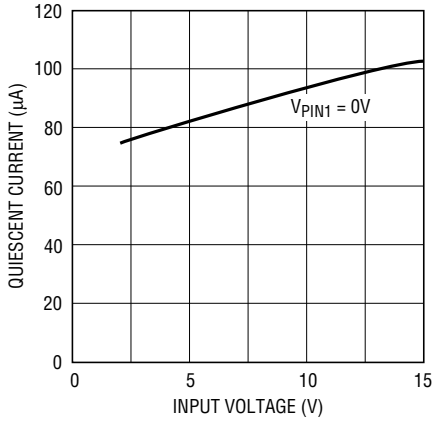
Oscillator Frequency



LT1054 • TPC03

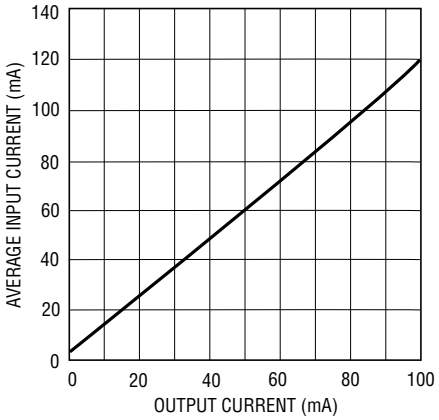
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current in Shutdown



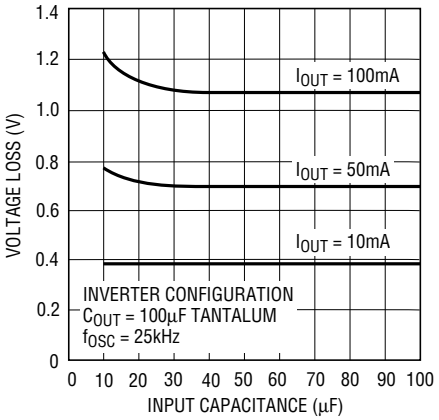
LT1054 • TPC04

Average Input Current



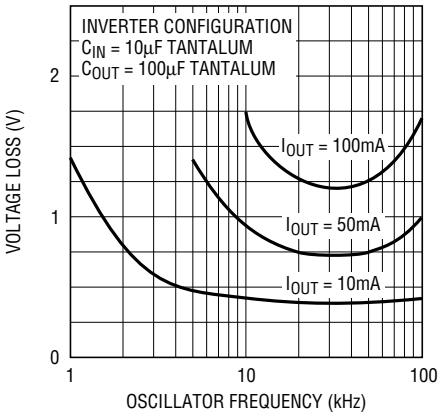
LT1050 • TPC05

Output Voltage Loss



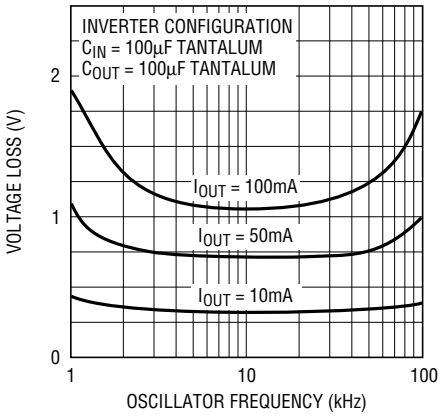
LT1054 • TPC06

Output Voltage Loss



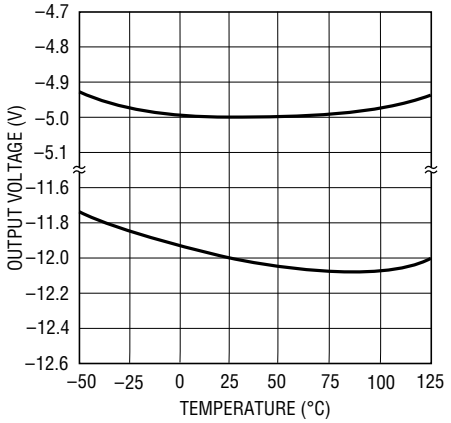
LT1054 • TPC07

Output Voltage Loss



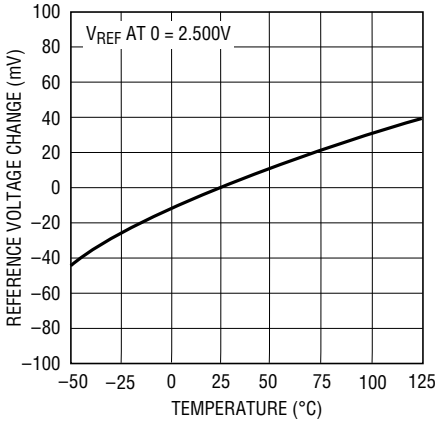
LT1054 • TPC08

Regulated Output Voltage



LT1054 • TPC09

Reference Voltage Temperature Coefficient



LT1054 • TPC10

PIN FUNCTIONS

V^+ (Pin 8): Input Supply. The LT1054 alternately charges C_{IN} to the input voltage when C_{IN} is switched in parallel with the input supply and then transfers charge to C_{OUT} when C_{IN} is switched in parallel with C_{OUT}. Switching occurs at the oscillator frequency. During the time that C_{IN} is charging, the peak supply current will be approximately equal to 2.2 times the output current. During the time that C_{IN} is delivering charge to C_{OUT} the supply current drops to approximately 0.2 times the output current. An input supply bypass capacitor will supply part of the peak input current drawn by the LT1054 and average out the current drawn from the supply. A minimum input supply bypass capacitor of 2µF, preferably tantalum or some other low ESR type is recommended. A larger capacitor may be desirable in some cases, for example, when the actual input supply is connected to the LT1054 through long leads, or when the pulse current drawn by the LT1054 might affect other circuitry through supply coupling.

V_{OUT} (Pin 5): In addition to being the output pin the pin is also tied to the substrate of the device. **Special care must be taken in LT1054 circuits to avoid pulling this pin positive with respect to any of the other pins**. Pulling pin 5 positive with respect to pin 3 (GND) will forward bias the substrate diode which will prevent the device from starting. This condition can occur when the output load driven by the LT1054 is referred to its positive supply (or to some other positive voltage). Note that most op amps present just such a load since their supply currents flow from their V^+ terminals to their V^- terminals. To prevent start-up problems with this type of load an external transistor must be added as shown in Figure 1. This will prevent V_{OUT} (pin 5) from being pulled above the ground pin (pin 3) during start-up. Any small, general purpose transistor such as 2N2222 or 2N2219 can be used. R_X should be chosen to provide enough base drive to the external transistor so that it is saturated under nominal output voltage and maximum output current conditions. In some cases an N-channel enhancement mode MOSFET can be used in place of the transistor.

$$R_X \leq \frac{(|V_{OUT}|)\beta}{I_{OUT}}$$

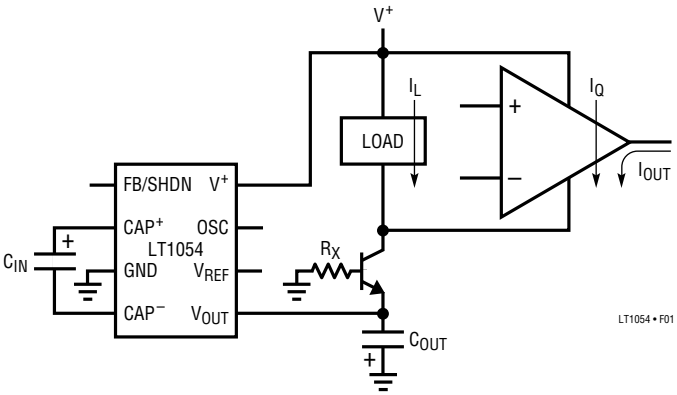


Figure 1

V_{REF} (Pin 6): Reference Output. This pin provides a 2.5V reference point for use in LT1054-based regulator circuits. The temperature coefficient of the reference voltage has been adjusted so that the temperature coefficient of the regulated output voltage is close to zero. This requires the reference output to have a positive temperature coefficient as can be seen in the typical performance curves. This nonzero drift is necessary to offset a drift term inherent in the internal reference divider and comparator network tied to the feedback pin. The overall result of these drift terms is a regulated output which has a slight positive temperature coefficient at output voltages below 5V and a slight negative TC at output voltages above 5V. Reference output current should be limited, for regulator feedback networks, to approximately 60µA. The reference pin will draw ≈100µA when shorted to ground and will not affect the internal reference/regulator, so that this pin can also be used as a pull-up for LT1054 circuits that require synchronization.

CAP^+/CAP^- (Pin 2/Pin 4): Pin 2, the positive side of the input capacitor (C_{IN}), is alternately driven between V^+ and ground. When driven to V^+, pin 2 sources current from V^+. When driven to ground pin 2 sinks current to ground. Pin 4, the negative side of the input capacitor, is driven alternately between ground the V_{OUT}. When driven to ground, pin 4 sinks current to ground. When driven to V_{OUT} pin 4 sources current from C_{OUT}. In all cases current flow in the switches is unidirectional as should be expected using bipolar switches.

PIN FUNCTIONS

OSC (Pin 7): Oscillator Pin. This pin can be used to raise or lower the oscillator frequency or to synchronize the device to an external clock. Internally pin 7 is connected to the oscillator timing capacitor ($C_t \approx 150pF$) which is alternately charged and discharged by current sources of $\pm 7\mu A$ so that the duty cycle is $\approx 50\%$. The LT1054 oscillator is designed to run in the frequency band where switching losses are minimized. However the frequency can be raised, lowered, or synchronized to an external system clock if necessary.

The frequency can be lowered by adding an external capacitor (C1, Figure 2) from pin 7 to ground. This will increase the charge and discharge times which lowers the oscillator frequency. The frequency can be increased by adding an external capacitor (C2, Figure 2, in the range of 5pF to 20pF) from pin 2 to pin 7. This capacitor will couple charge into C_t at the switch transitions, which will shorten the charge and discharge time, raising the oscillator frequency. Synchronization can be accomplished by adding an external resistive pull-up from pin 7 to the reference pin (pin 6). A 20k pull-up is recommended. An open collector gate or an NPN transistor can then be used to drive the oscillator pin at the external clock frequency as shown in Figure 2. Pulling up pin 7 to an external voltage is **not recommended**. For circuits that require both frequency synchronization and regulation, an external reference can be used as the reference point for the top of the R1/R2 divider allowing pin 6 to be used as a pull-up point for pin 7.

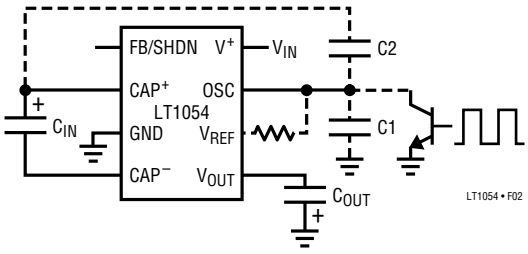


Figure 2

FB/SHDN (Pin 1): Feedback/Shutdown Pin. This pin has two functions. Pulling pin 1 below the shutdown threshold ($\approx 0.45V$) puts the device into shutdown. In shutdown the reference/regulator is turned off and switching stops. The switches are set such that both C_{IN} and C_{OUT} are discharged through the output load. Quiescent current in shutdown drops to approximately 100μA (see Typical Performance Characteristics). Any open-collector gate can be used to put the LT1054 into shutdown. For normal (unregulated) operation the device will start back up when the external gate is shut off. In LT1054 circuits that use the regulation feature, the external resistor divider can provide enough pull-down to keep the device in shutdown until the output capacitor (C_{OUT}) has fully discharged. For most applications where the LT1054 would be run intermittently, this does not present a problem because the discharge time of the output capacitor will be short compared to the off-time of the device. In applications where the device has to start up before the output capacitor (C_{OUT}) has fully discharged, a restart pulse must be applied to pin 1 of the LT1054. Using the circuit of Figure 5, the restart signal can be either a pulse ($t_p > 100\mu s$) or a logic high. Diode coupling the restart signal into pin 1 will allow the output voltage to come up and regulate without overshoot. The resistor divider R3/R4 in Figure 5 should be chosen to provide a signal level at pin 1 of 0.7V to 1.1V.

Pin 1 is also the inverting input of the LT1054's error amplifier and as such can be used to obtain a regulated output voltage.

APPLICATIONS INFORMATION

Theory of Operation

To understand the theory of operation of the LT1054, a review of a basic switched-capacitor building block is helpful.

In Figure 3 when the switch is in the left position, capacitor C1 will charge to voltage V1. The total charge on C1 will be q1 = C1V1. The switch then moves to the right, discharging C1 to voltage V2. After this discharge time the charge on C1 is q2 = C1V2. Note that charge has been transferred from the source V1 to the output V2. The amount of charge transferred is:

$$\Delta q = q1 - q2 = C1(V1 - V2)$$

If the switch is cycled f times per second, the charge transfer per unit time (i.e., current) is:

$$I = f \times \Delta q = f \times C1(V1 - V2)$$

To obtain an equivalent resistance for the switched-capacitor network we can rewrite this equation in terms of voltage and impedance equivalence:

$$I = \frac{V1 - V2}{(1/fC1)} = \frac{V1 - V2}{R_{EQUIV}}$$

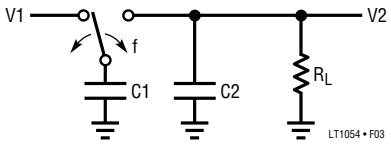


Figure 3. Switched-Capacitor Building Block

A new variable R_{EQUIV} is defined such that $R_{EQUIV} = 1/fC1$. Thus the equivalent circuit for the switched-capacitor network is as shown in Figure 4. The LT1054 has the same switching action as the basic switched-capacitor building block. Even though this simplification doesn't include finite switch on-resistance and output voltage ripple, it provides an intuitive feel for how the device works.

These simplified circuits explain voltage loss as a function of frequency (see Typical Performance Characteristics). As frequency is decreased, the output impedance will eventually be dominated by the 1/fC1 term and voltage losses will rise.

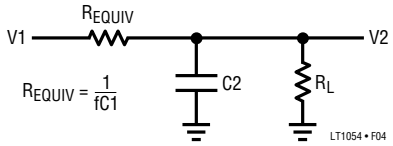


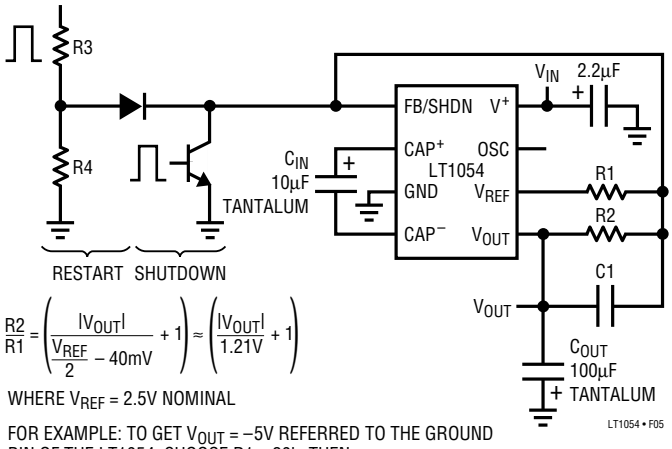
Figure 4. Switched-Capacitor Equivalent Circuit

Note that losses also rise as frequency increases. This is caused by internal switching losses which occur due to some finite charge being lost on each switching cycle. This charge loss per-unit-cycle, when multiplied by the switching frequency, becomes a current loss. At high frequency this loss becomes significant and voltage losses again rise.

The oscillator of the LT1054 is designed to run in the frequency band where voltage losses are at a minimum.

Regulation

The error amplifier of the LT1054 servos the drive to the PNP switch to control the voltage across the input capacitor (C_{IN}) which in turn will determine the output voltage. Using the reference and error amplifier of the LT1054, an external resistive divider is all that is needed to set the regulated output voltage. Figure 5 shows the basic regulator configuration and the formula for calculating the appropriate resistor values. R1 should be chosen to be



$$\frac{R2}{R1} = \left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40mV} + 1\right) \approx \left(\frac{|V_{OUT}|}{1.21V} + 1\right)$$

WHERE V_{REF} = 2.5V NOMINAL

FOR EXAMPLE: TO GET V_{OUT} = –5V REFERRED TO THE GROUND PIN OF THE LT1054, CHOOSE R1 = 20k, THEN

$$R2 = 20k\left(\frac{|-5V|}{\frac{2.5V}{2} - 40mV} + 1\right) = 102.6k^*$$

*CHOOSE THE CLOSEST 1% VALUE

Figure 5

APPLICATIONS INFORMATION

20k or greater because the reference output current is limited to ≈100μA. R2 should be chosen to be in the range of 100k to 300k. For optimum results the ratio of C_{IN}/C_{OUT} is recommended to be 1/10. C1, required for good load regulation at light load currents, should be 0.002μF for all output voltages.

A new die layout was required to fit into the physical dimensions of the S8 package. Although the new die of the LT1054CS8 will meet all the specifications of the existing LT1054 data sheet, subtle differences in the layout of the new die require consideration in some application circuits. In regulating mode circuits using the 1054CS8 the nominal values of the capacitors, C_{IN} and C_{OUT}, must be approximately equal for proper operation at elevated junction temperatures. This is different from the earlier part. Mismatches within normal production tolerances for the capacitors are acceptable. Making the nominal capacitor values equal will ensure proper operation at elevated junction temperatures at the cost of a small degradation in the transient response of regulator circuits. For unregulated circuits the values of C_{IN} and C_{OUT} are normally equal for all packages. For S8 applications assistance in unusual applications circuits, please consult the factory.

It can be seen from the circuit block diagram that the maximum regulated output voltage is limited by the supply voltage. For the basic configuration, $|V_{OUT}|$ referred to the ground pin of the LT1054 must be less than the total of the supply voltage minus the voltage loss due to the switches. The voltage loss versus output current due to the switches can be found in Typical Performance Characteristics. Other configurations such as the negative doubler can provide higher output voltages at reduced output currents (see Typical Applications).

Capacitor Selection

For unregulated circuits the nominal values of C_{IN} and C_{OUT} should be equal. For regulated circuits see the section on Regulation. While the exact values of C_{IN} and C_{OUT} are noncritical, good quality, low ESR capacitors such as solid tantalum are necessary to minimize voltage losses at high currents. For C_{IN} the effect of the ESR of the capacitor will be multiplied by four due to the fact that switch currents are approximately two times higher than output current and losses will occur on both the charge and discharge cycle. This means that using a capacitor with 1Ω of ESR for C_{IN} will have the same effect as increasing the output impedance of the LT1054 by 4Ω. This represents a significant increase in the voltage losses. For C_{OUT} the affect of ESR is less dramatic. C_{OUT} is alternately charged and discharged at a current approximately equal to the output current and the ESR of the capacitor will cause a step function to occur in the output ripple at the switch transitions. This step function will degrade the output regulation for changes in output load current and should be avoided. Realizing that large value tantalum capacitors can be expensive, a technique that can be used is to parallel a smaller tantalum capacitor with a large aluminum electrolytic capacitor to gain both low ESR and reasonable cost. Where physical size is a concern some of the newer chip type surface mount tantalum capacitors can be used. These capacitors are normally rated at working voltages in the 10V to 20V range and exhibit very low ESR (in the range of 0.1Ω).

Output Ripple

The peak-to-peak output ripple is determined by the value of the output capacitor and the output current. Peak-to-peak output ripple may be approximated by the formula:

$$dV = \frac{I_{OUT}}{2fC_{OUT}}$$

where dV = peak-to-peak ripple and f = oscillator frequency.

For output capacitors with significant ESR a second term must be added to account for the voltage step at the switch transitions. This step is approximately equal to:

$(2I_{OUT})$(ESR of C_{OUT})

Power Dissipation

The power dissipation of any LT1054 circuit must be limited such that the junction temperature of the device does not exceed the maximum junction temperature ratings. The total power dissipation must be calculated from two components, the power loss due to voltage drops in the switches and the power loss due to drive current losses. The total power dissipated by the LT1054 can be calculated from:

APPLICATIONS INFORMATION

$$P \approx (V_{IN} - |V_{OUT}|)(I_{OUT}) + (V_{IN})(I_{OUT})(0.2)$$

where both V_{IN} and V_{OUT} are referred to the ground pin (pin 3) of the LT1054. For LT1054 regulator circuits, the power dissipation will be equivalent to that of a linear regulator. Due to the limited power handling capability of the LT1054 packages, the user will have to limit output current requirements or take steps to dissipate some power external to the LT1054 for large input/output differentials. This can be accomplished by placing a resistor in series with C_{IN} as shown in Figure 6. A portion of the input voltage will then be dropped across this resistor without affecting the output regulation. Because switch current is approximately 2.2

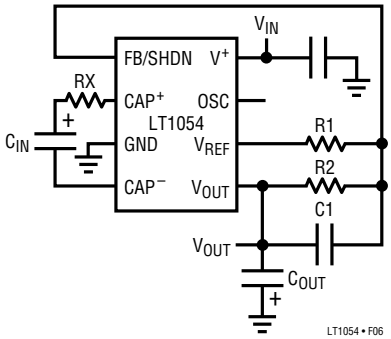


Figure 6

times the output current and the resistor will cause a voltage drop when C_{IN} is both charging and discharging, the resistor should be chosen as:

$$R_X = V_X/(4.4\ I_{OUT})$$

where

$$V_X \approx V_{IN} - [(\text{LT1054 Voltage Loss})(1.3) + |V_{OUT}|]$$

and I_{OUT} = maximum required output current. The factor of 1.3 will allow some operating margin for the LT1054.

For example: assume a 12V to –5V converter at 100mA output current. First calculate the power dissipation without an external resistor:

$$P = (12V - |-5V|)(100mA) + (12V)(100mA)(0.2)$$
$$P = 700mW + 240mW = 940mW$$

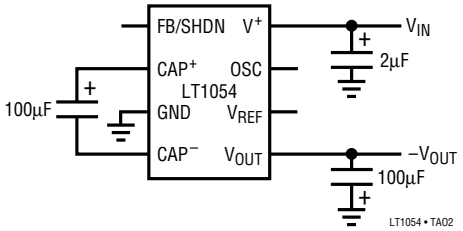
At θ_{JA} of 130°C/W for a commercial plastic device this would cause a junction temperature rise of 122°C so that the device would exceed the maximum junction temperature at an ambient temperature of 25°C. Now calculate the power dissipation with an external resistor (R_X). First find how much voltage can be dropped across R_X. The maximum voltage loss of the LT1054 in the standard regulator configuration at 100mA output current is 1.6V, so

$$V_X = 12V - [(1.6V)(1.3) + |-5V|] = 4.9V \text{ and}$$
$$R_X = 4.9V/(4.4)(100mA) = 11\Omega$$

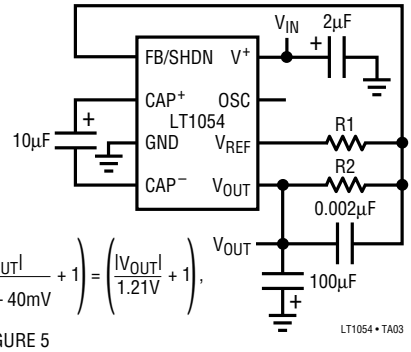
This resistor will reduce the power dissipated by the LT1054 by (4.9V)(100mA) = 490mW. The total power dissipated by the LT1054 would then be = (940mW – 490mW) = 450mW. The junction temperature rise would now be only 58°C. Although commercial devices are guaranteed to be functional up to a junction temperature of 125°C, the specifications are only guaranteed up to a junction temperature of 100°C, so ideally you should limit the junction temperature to 100°C. For the above example this would mean limiting the ambient temperature to 42°C. Other steps can be taken to allow higher ambient temperatures. The thermal resistance numbers for the LT1054 packages represent worst case numbers with no heat sinking and still air. Small clip-on type heat sinks can be used to lower the thermal resistance of the LT1054 package. In some systems there may be some available airflow which will help to lower the thermal resistance. Wide PC board traces from the LT1054 leads can also help to remove heat from the device. This is especially true for plastic packages.

TYPICAL APPLICATIONS

Basic Voltage Inverter



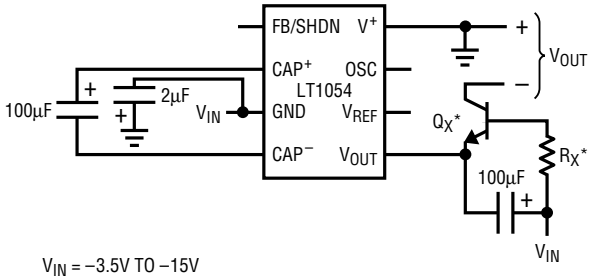
Basic Voltage Inverter/Regulator



$$\frac{R2}{R1} = \left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40mV} + 1\right) = \left(\frac{|V_{OUT}|}{1.21V} + 1\right),$$

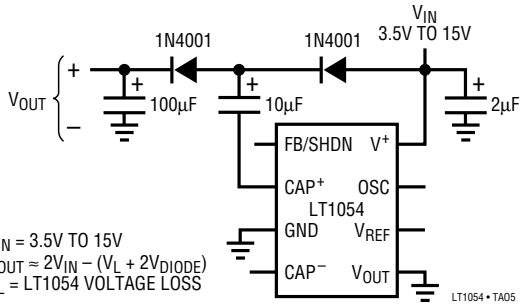
REFER TO FIGURE 5

Negative Voltage Doubler



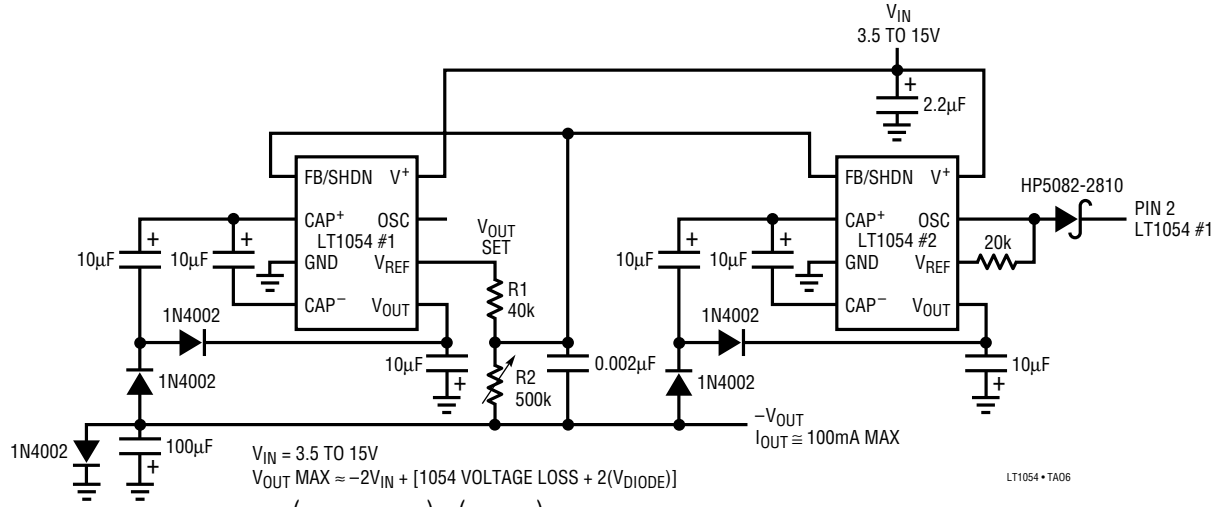
V_{IN} = –3.5V TO –15V
$V_{OUT} = 2V_{IN}$ + (LT1054 VOLTAGE LOSS) + (Q_X SATURATION VOLTAGE)
*SEE FIGURE 3

Positive Doubler



V_{IN} = 3.5V TO 15V
$V_{OUT} \approx 2V_{IN} - (V_L + 2V_{DIODE})$
V_L = LT1054 VOLTAGE LOSS

100mA Regulating Negative Doubler

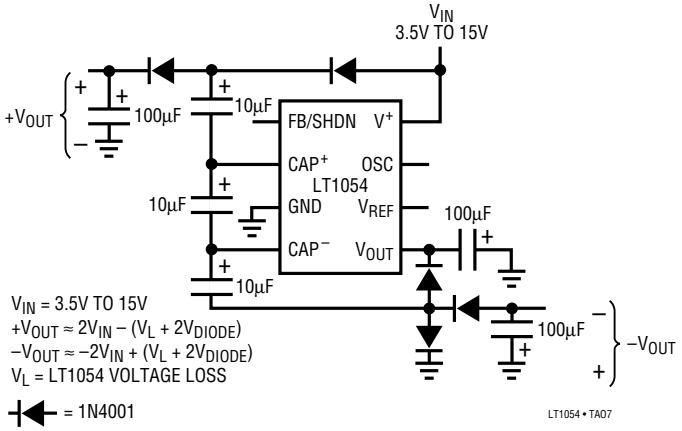


V_{IN} = 3.5 TO 15V
V_{OUT} MAX ≈ –2V_{IN} + [1054 VOLTAGE LOSS + 2(V_{DIODE})]

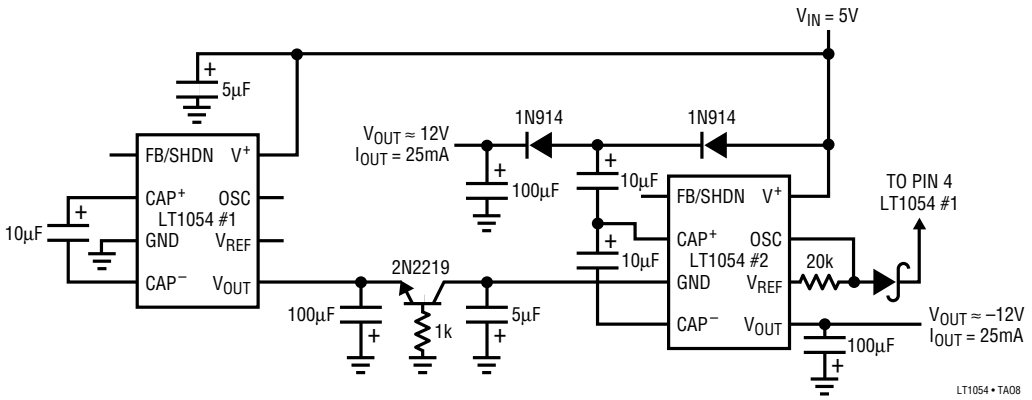
$$\frac{R2}{R1} = \left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40mV} + 1\right) = \left(\frac{|V_{OUT}|}{1.21V} + 1\right), \text{ REFER TO FIGURE 5}$$

TYPICAL APPLICATIONS

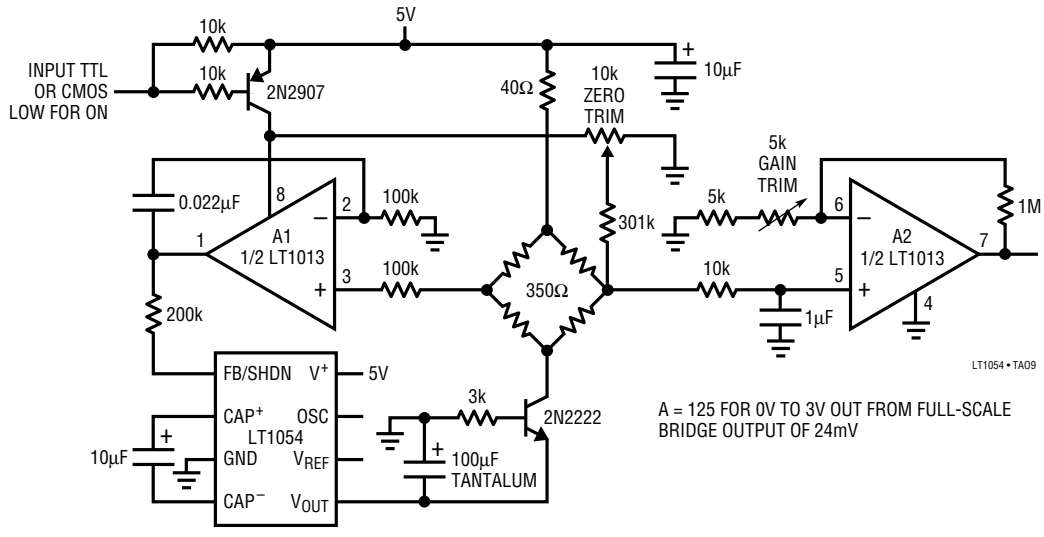
Strain Gauge Bridge Signal Conditioner



5V to ±12V Converter

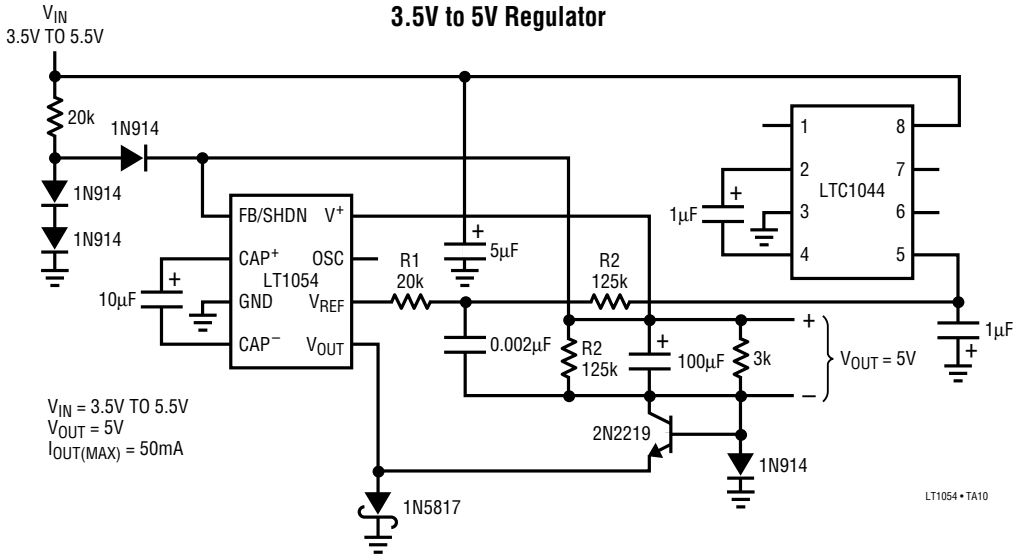


5V to ±12V Converter

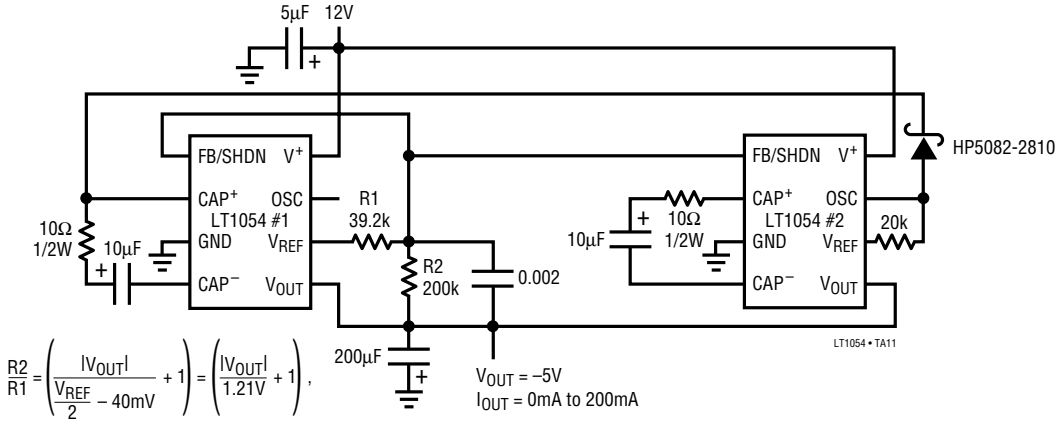


TYPICAL APPLICATIONS

3.5V to 5V Regulator



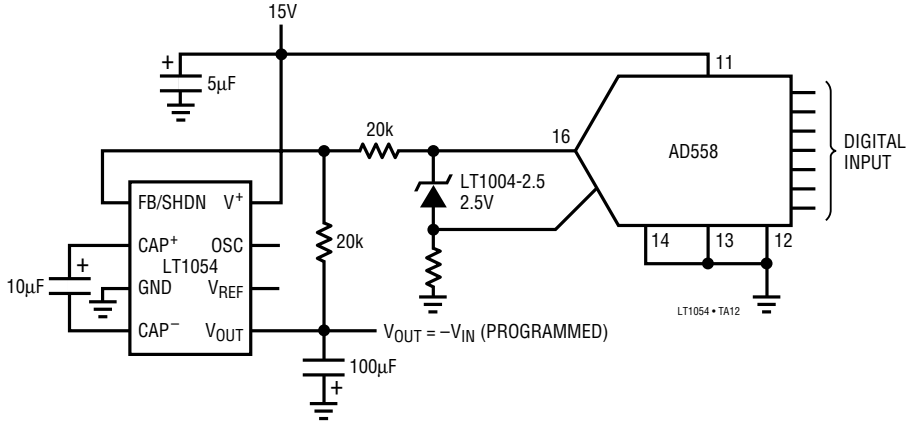
Regulating 200mA, 12V to –5V Converter



$$\frac{R2}{R1} = \left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40mV} + 1\right) = \left(\frac{|V_{OUT}|}{1.21V} + 1\right),$$

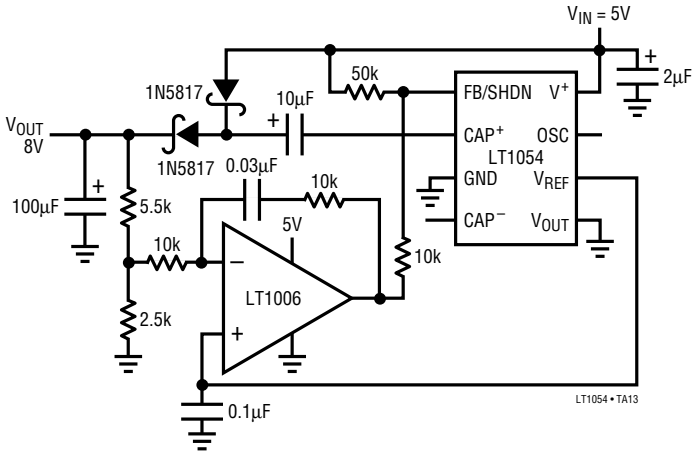
REFER TO FIGURE 5

Digitally Programmable Negative Supply

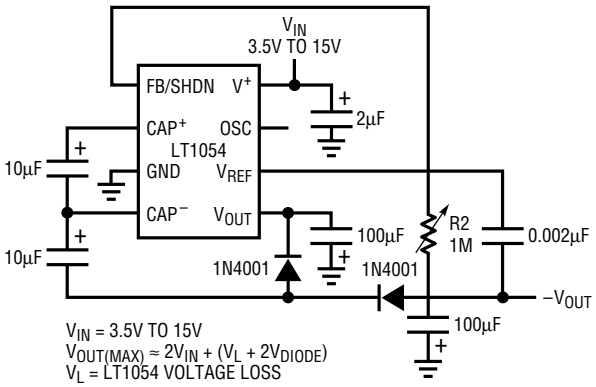


TYPICAL APPLICATIONS

Positive Doubler with Regulation (5V to 8V Converter)



Negative Doubler with Regulator

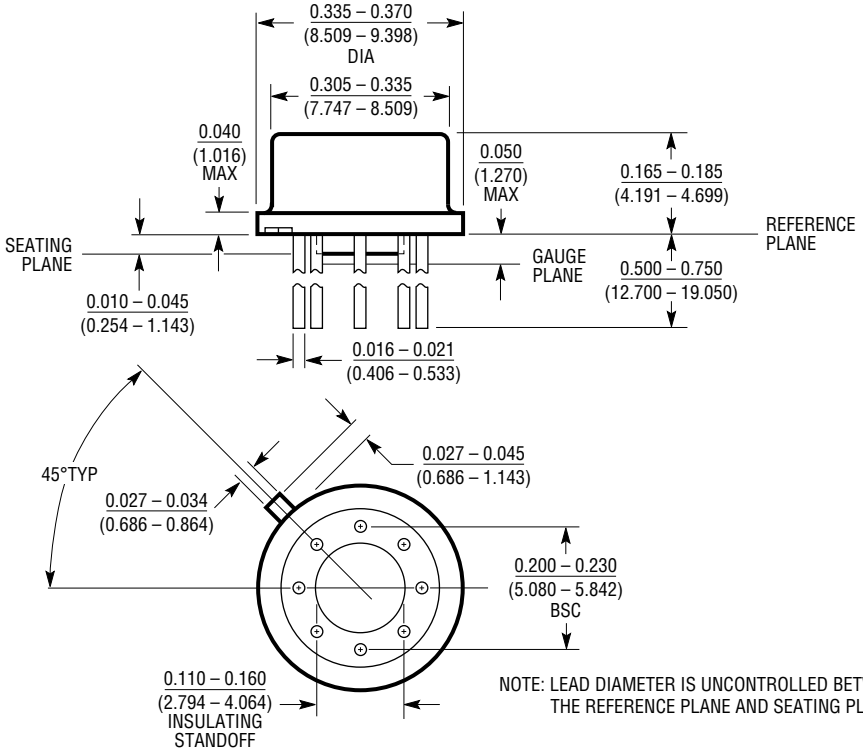


THE TYPICAL APPLICATIONS CIRCUITS WERE VERIFIED USING THE STANDARD LT1054. FOR S8 APPLICATIONS ASSISTANCE IN ANY OF THE UNUSUAL APPLICATIONS CIRCUITS PLEASE CONSULT THE FACTORY

PACKAGE DESCRIPTION

Dimension in inches (millimeters) unless otherwise noted.

H Package
8-Lead TO-5 Metal Can



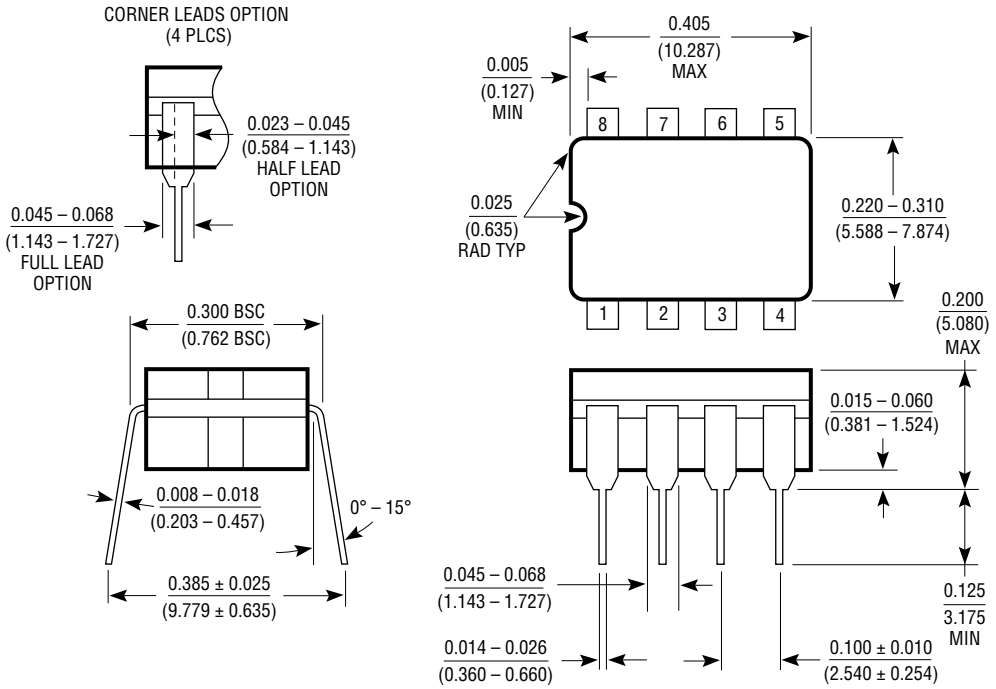
NOTE: LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE.

H8(5) 0592

PACKAGE DESCRIPTION

Dimension in inches (millimeters) unless otherwise noted.

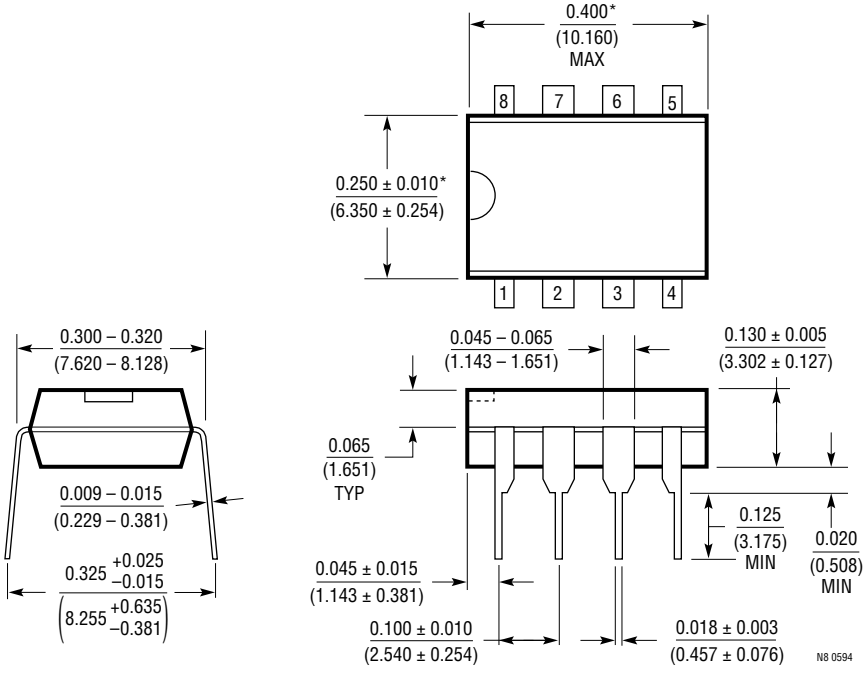
J8 Package
8-Lead Ceramic DIP



NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP OR TIN PLATE LEADS.

J8 0694

N8 Package
8-Lead Plastic DIP



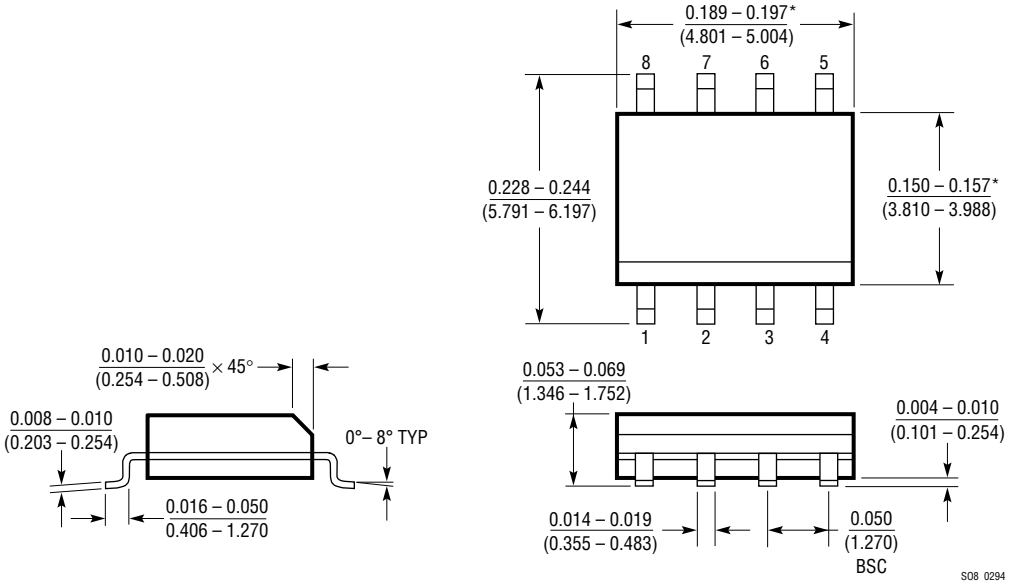
N8 0594

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTURSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm).

PACKAGE DESCRIPTION

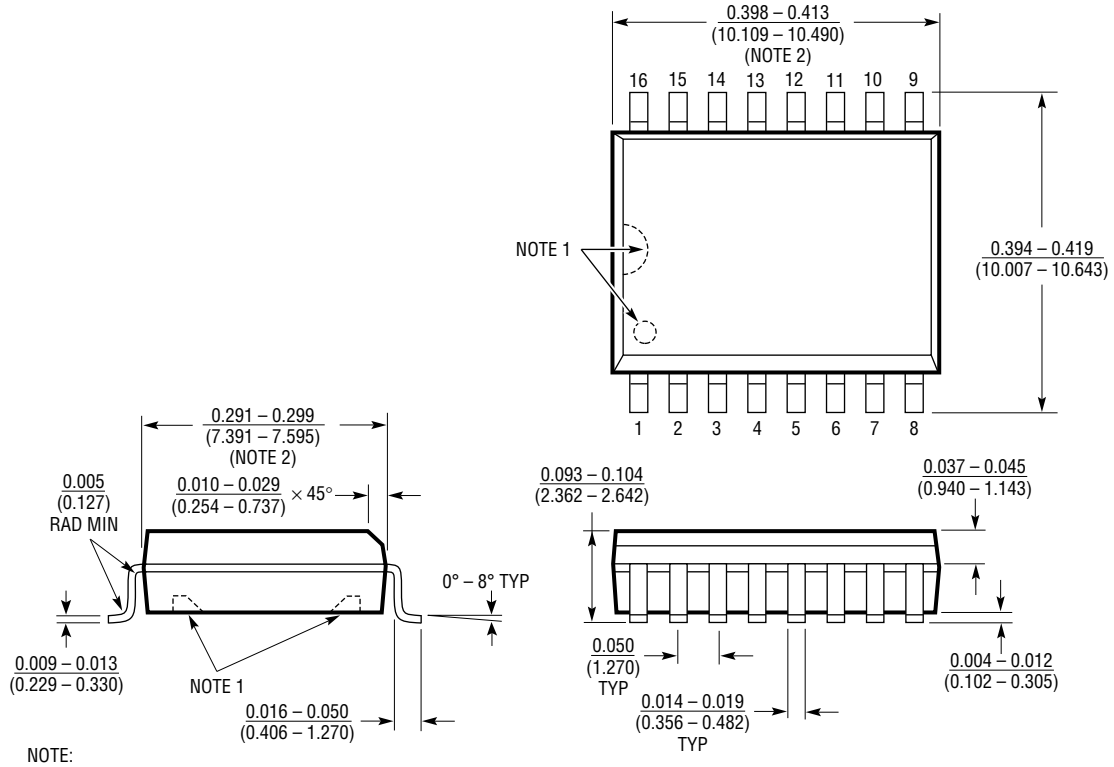
Dimension in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Ceramic DIP



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).

S Package
16-Lead Plastic SOL



NOTE:
1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.
2. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).

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0295

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5A and 2.5A High Efficiency Switching Regulators

FEATURES

- Wide Input Voltage Range 3V-60V
- Low Quiescent Current—6mA
- Internal 5A Switch (2.5A for LT1071)
- Very Few External Parts Required
- Self-Protected Against Overloads
- Operates in Nearly All Switching Topologies
- Shutdown Mode Draws Only 50μA Supply Current
- Flyback-Regulated Mode has Fully Floating Outputs
- Comes in Standard 5-Pin Packages
- Can be Externally Synchronized (Consult Factory)

APPLICATIONS

- Logic Supply 5V @ 10A
- 5V Logic to ±15V Op Amp Supply
- Offline Converter up to 200W
- Battery Upconverter
- Power Inverter (+ to −) or (− to +)
- Fully Floating Multiple Outputs
- For Lower Current Applications see LT1072

USER NOTE:

This data sheet is only intended to provide specifications, graphs, and a general functional description of the LT1070/LT1071. Application circuits are included to show the capability of the LT1070/LT1071. A complete design manual (AN-19) should be obtained to assist in developing new designs. This manual contains a comprehensive discussion of both the LT1070 and the external components used with it, as well as complete formulas for calculating the values of these components. The manual can also be used for the LT1071 by factoring in the lower switch current rating. A second application note, AN-25, which details off-line applications is available.

DESCRIPTION

The LT1070 and LT1071 are monolithic high power switching regulators. They can be operated in all standard switching configurations including buck, boost, flyback, forward, inverting and "Cuk". A high current, high efficiency switch is included on the die along with all oscillator, control, and protection circuitry. Integration of all functions allows the LT1070/LT1071 to be built in a standard 5-pin TO-3 or TO-220 power package. This makes it extremely easy to use and provides "bust proof" operation similar to that obtained with 3-pin linear regulators.

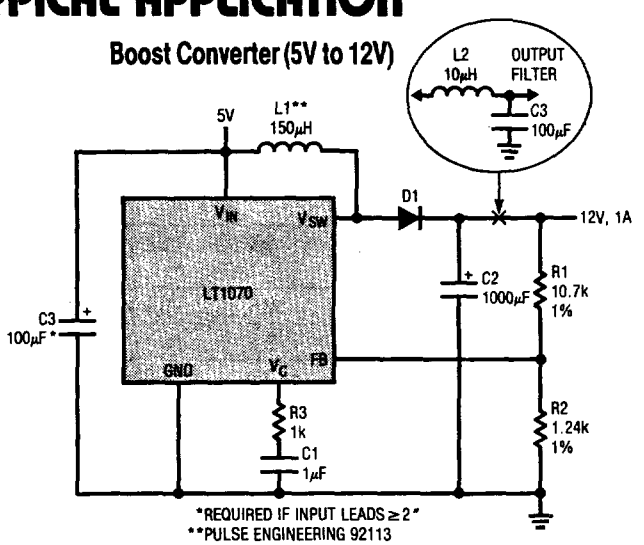
The LT1070/LT1071 operates with supply voltages from 3V to 60V, and draws only 6mA quiescent current. It can deliver load power up to 100 watts with no external power devices. By utilizing current-mode switching techniques, it provides excellent AC and DC load and line regulation.

The LT1070/LT1071 has many unique features not found even on the vastly more difficult to use low power control chips presently available. It uses adaptive anti-sat switch drive to allow very wide ranging load currents with no loss in efficiency. An externally activated shutdown mode reduces total supply current to 50μA typical for standby operation. Totally isolated and regulated outputs can be generated by using the optional "flyback regulation mode" built into the LT1070/LT1071, without the need for opto-couplers or extra transformer windings.

5

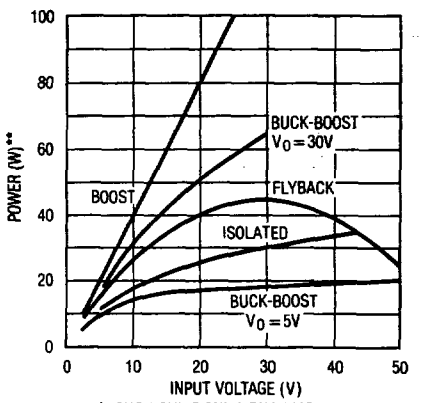
TYPICAL APPLICATION

Boost Converter (5V to 12V)



*REQUIRED IF INPUT LEADS ≥ 2"
**PULSE ENGINEERING 92113

Maximum Output Power*



*ROUGH GUIDE ONLY. BUCK MODE
$P_{OUT} = 5A \times V_{OUT}$. SPECIAL TOPOLOGIES DELIVER MORE POWER.
**DIVIDE VERTICAL POWER SCALE BY 2 FOR LT1071

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- LT1070/71HV (See Note 1) 60V
- LT1070/71 (See Note 1) 40V

Switch Output Voltage
- LT1070/71HV 75V
- LT1070/71 ..... 65V

Feedback Pin Voltage (Transient, 1ms) ..... ±15V

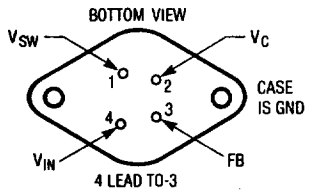
Operating Junction Temperature Range
- LT1070/71HVM, LT1070/71M ..... −55°C to +150°C
- LT1070/71HVC, LT1070/71C (Oper.) ..... 0°C to +100°C
- LT1070/71HVC, LT1070/71C (Sh. Ckt.) ... 0°C to +125°C

Storage Temperature Range ..... −65°C to +150°C

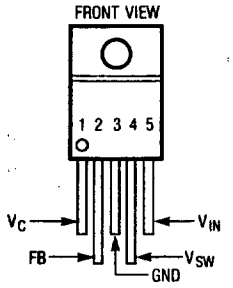
Lead Temperature (Soldering, 10sec) ..... 300°C

Note 1: Minimum switch "on" time for the LT1070/LT1071 in current limit is ≈1.0μsec. This limits the maximum input voltage during short circuit conditions, *in the buck and inverting modes only,* to ≈35V. Normal (unshorted) conditions are not affected. Mask changes are being implemented which will reduce minimum "on" time to ≤1μsec, increasing maximum short circuit input voltage above 40V. If the present LT1070/LT1071 (contact factory for package date code) is being operated in the buck or inverting mode at high input voltages and short circuit conditions are expected, a resistor must be placed in series with the inductor, as follows:

PACKAGE/ORDER INFORMATION



4 LEAD TO-3



5 LEAD TO-220

ORDER PART NUMBER
LT1070/LT1071HVMK LT1070/LT1071MK LT1070/LT1071HVCK LT1070/LT1071CK
LT1070/LT1071HVCT LT1070/LT1071CT

The value of the resistor is given by:

$$R = \frac{t \bullet f \bullet V_{IN} - Vf}{I_{(LIMIT)}} - R_L$$

t = Minimum "on" time of LT1070/LT1071 in current limit, ≈1μs

f = Operating frequency (40kHz)

Vf = Forward voltage of external catch diode at $I_{(LIMIT)}$

$I_{(LIMIT)}$ = Current limit of LT1070 (≈8A), LT1071 (≈4A)

R_L = Internal series resistance of inductor

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN} = 15V, V_C = 0.5V, V_{FB} = V_{REF}, output pin open.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF}	Reference Voltage	Measured at Feedback Pin		1.224	1.244	1.264	V
			●	1.214	1.244	1.274	
I_B	Feedback Input Current	$V_{FB} = V_{REF}$			350	750	nA
			●			1100	
gm	Error Amplifier Transconductance	$\Delta I_C = \pm 25\mu A$		3000	4400	6000	μmho
			●	2400		7000	
	Error Amplifier Source or Sink Current	V_C = 1.5V		150	200	350	μA
			●	120		400	μA
	Error Amplifier Clamp Voltage	Hi Clamp, V_{FB} = 1V		1.8		2.3	V
		Lo Clamp, V_{FB} = 1.5V		0.25	0.38	0.52	V
	Reference Voltage Line Regulation	$3V \le V_{IN} \le V_{MAX}$	●			0.03	%/V
A_V	Error Amplifier Voltage Gain	$0.7V \le V_C \le 1.4V$		500	800	2000	V/V
	Minimum Input Voltage		●		2.6	3.0	V
I_Q	Supply Current	$3V \le V_{IN} \le V_{MAX}$, V_C = 0.6V			6	9	mA
	Control Pin Threshold	Duty Cycle = 0		0.8	0.9	1.08	V
			●	0.6		1.25	
	Normal/Flyback Threshold on Feedback Pin			0.4	0.45	0.54	V
V_{FB}	Flyback Reference Voltage	$I_{FB} = 50\mu A$		15	16.3	17.6	V
			●	14		18	

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN} = 15V, V_C = 0.5V, V_{FB} = V_{REF}, output pin open.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{FB}	Change in Flyback Reference Voltage	$0.05 \le I_{FB} \le 1mA$		4.5	6.8	8.5	V
	Flyback Reference Voltage Line Regulation	$I_{FB} = 50\mu A$ $3V \le V_{IN} \le V_{MAX}$			0.01	0.03	%/V
	Flyback Amplifier Transconductance (gm)	$\Delta I_C = \pm 10\mu A$		150	300	500	μmho
	Flyback Amplifier Source and Sink Current	V_C = 1.5V Source $I_{FB} = 50\mu A$ Sink	● ●	15 25	32 40	70 70	μA μA
BV	Output Switch Breakdown Voltage	$3V \le V_{IN} \le V_{MAX}$ LT1070/LT1071 I_{SW} = 5mA LT1070HV/LT1071HV	● ●	65 75	90 90		V V
V_{SAT}	Output Switch (Note 1) "On" Resistance	LT1070 LT1071	● ●		0.15 0.3	0.24 0.5	Ω Ω
	Control Voltage to Switch Current Transconductance	LT1070 LT1071			8 4		A/V A/V
I_{LIM}	Switch Current Limit (LT1070)	Duty Cycle ≤ 50% Tj ≥ 25°C Duty Cycle ≤ 50% Tj < 25°C Duty Cycle = 80% (Note 2)	● ● ●	5 5 4		10 11 10	A A A
I_{LIM}	Switch Current Limit (LT1071)	Duty Cycle ≤ 50% Tj ≥ 25°C Duty Cycle ≤ 50% Tj < 25°C Duty Cycle = 80% (Note 2)	● ● ●	2.5 2.5 2		5 5.5 5	A A A
$\frac{\Delta I_{IN}}{\Delta I_{SW}}$	Supply Current Increase During Switch On-Time				25	35	mA/A
f	Switching Frequency		 ●	35 33	40	45 47	kHz
DC (max)	Maximum Switch Duty Cycle			90	92	97	%
	Flyback Sense Delay Time				1.5		μs
	Shutdown Mode Supply Current	$3V \le V_{IN} \le V_{MAX}$ V_C = 0.05V			100	250	μA
	Shutdown Mode Threshold Voltage	$3V \le V_{IN} \le V_{MAX}$	 ●	100 50	150	250 300	mV mV

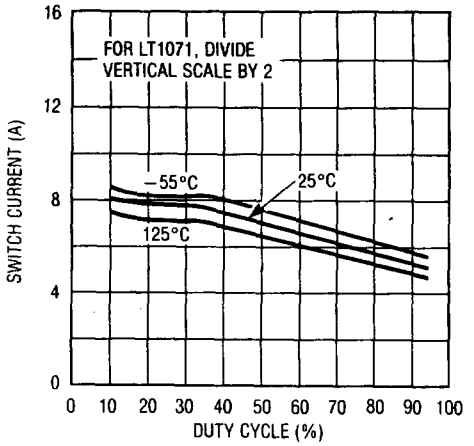
The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Measured with V_C in hi clamp, V_{FB} = 0.8V. I_{SW} = 4A for LT1070 and 2A for LT1071.

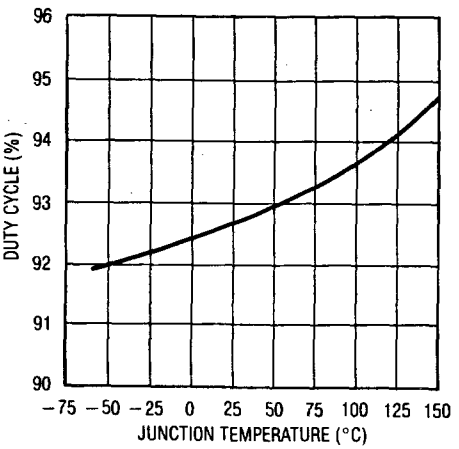
Note 2: For duty cycles (DC) between 50% and 80%, minimum guaranteed switch current is given by $I_{LIM} = 3.33 (2 - DC)$ for the LT1070 and $I_{LIM} = 1.67 (2 - DC)$ for the LT1071.

TYPICAL PERFORMANCE CHARACTERISTICS

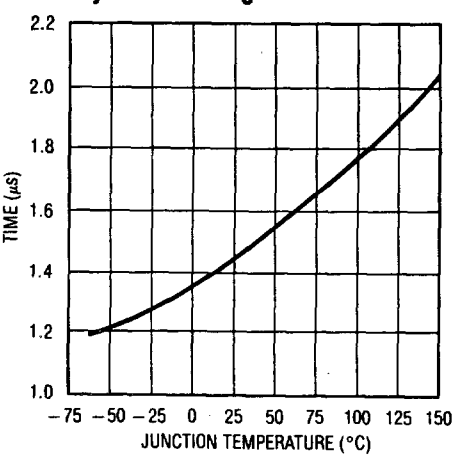
Switch Current Limit vs Duty Cycle



Maximum Duty Cycle

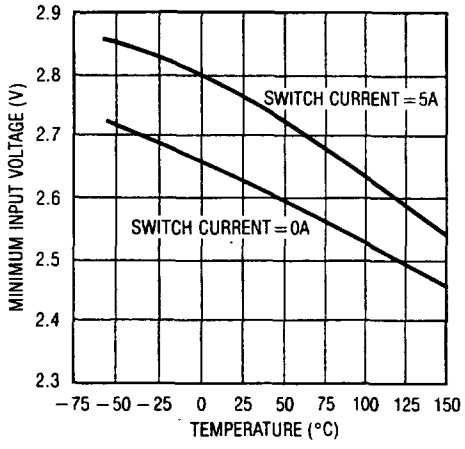


Flyback Blanking Time

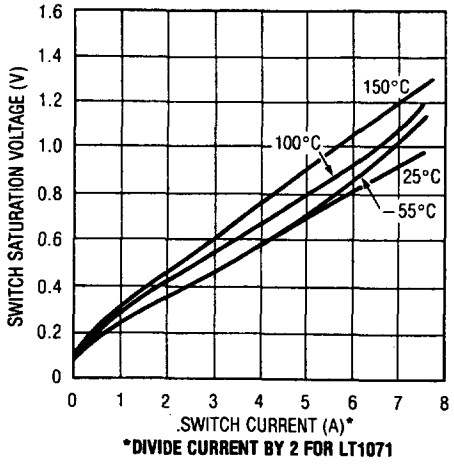


TYPICAL PERFORMANCE CHARACTERISTICS

Minimum Input Voltage

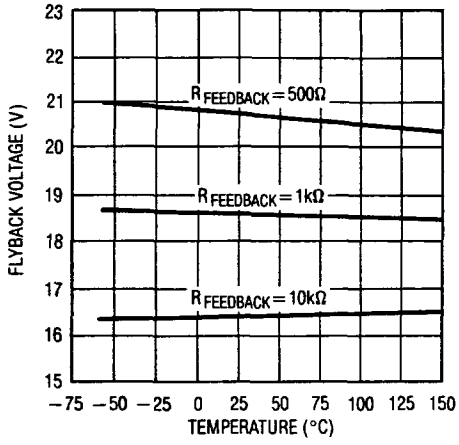


Switch Saturation Voltage

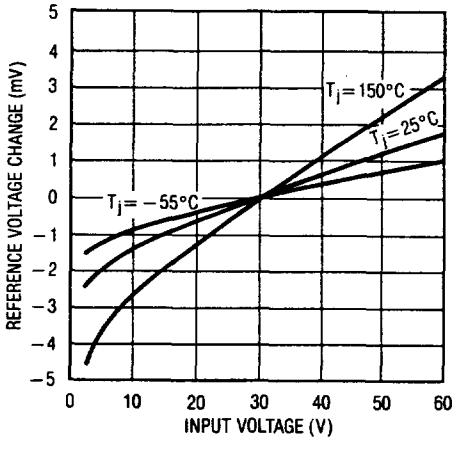


*DIVIDE CURRENT BY 2 FOR LT1071

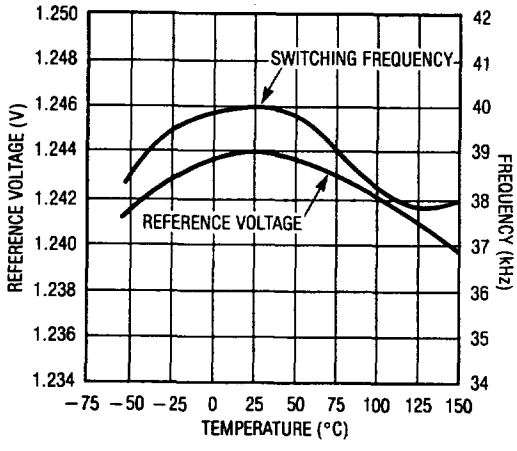
Isolated Mode Flyback Reference Voltage



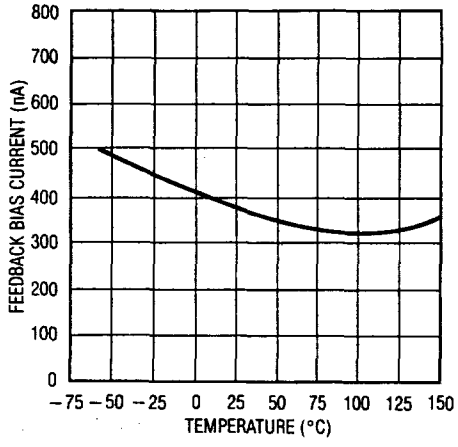
Line Regulation



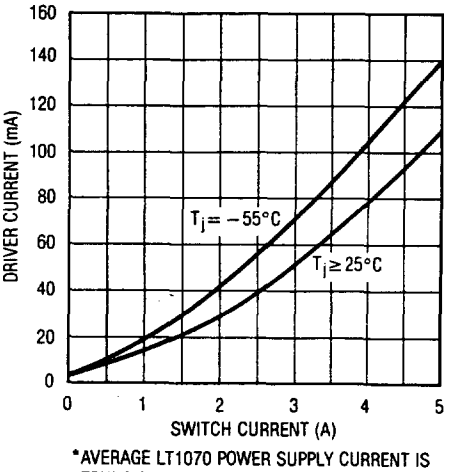
Reference Voltage vs Temperature



Feedback Bias Current vs Temperature

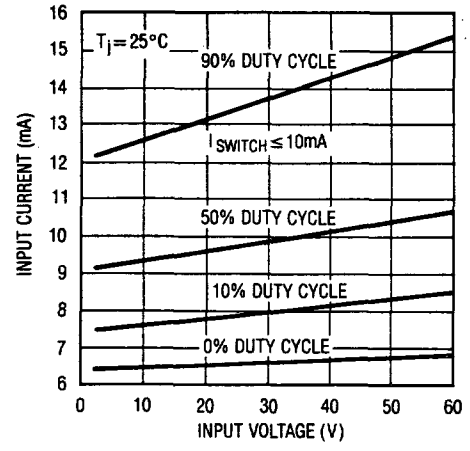


Driver Current* vs Switch Current



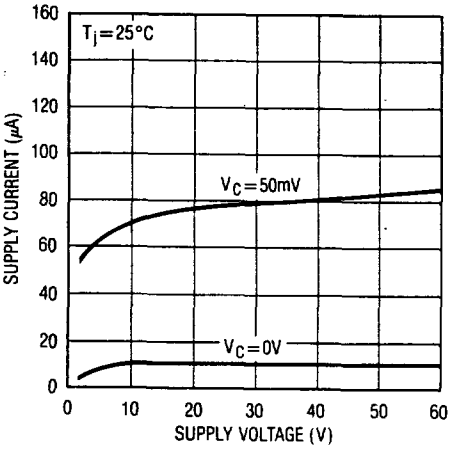
*AVERAGE LT1070 POWER SUPPLY CURRENT IS FOUND BY MULTIPLYING DRIVER CURRENT BY DUTY CYCLE, THEN ADDING QUIESCENT CURRENT.

Supply Current vs Input Voltage*



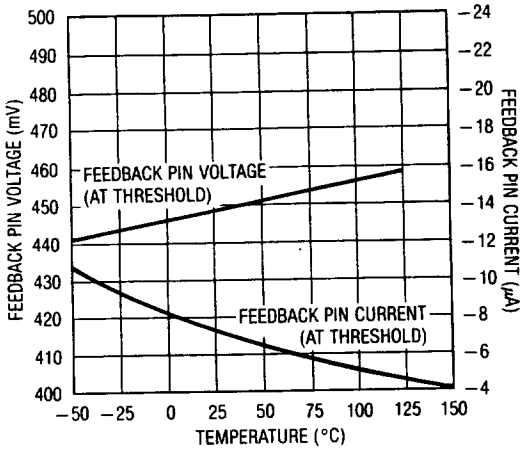
*UNDER VERY LOW OUTPUT CURRENT CONDITIONS, DUTY CYCLE FOR MOST CIRCUITS WILL APPROACH 10% OR LESS.

Supply Current vs Supply Voltage (Shutdown Mode)

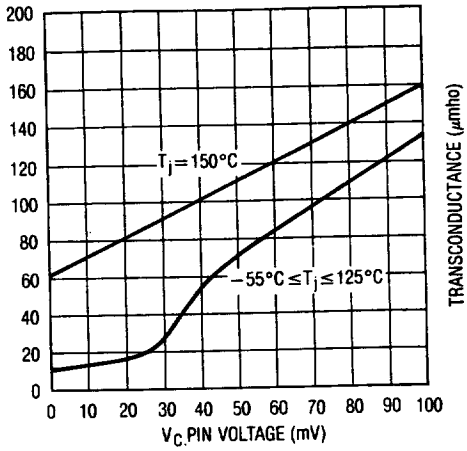


TYPICAL PERFORMANCE CHARACTERISTICS

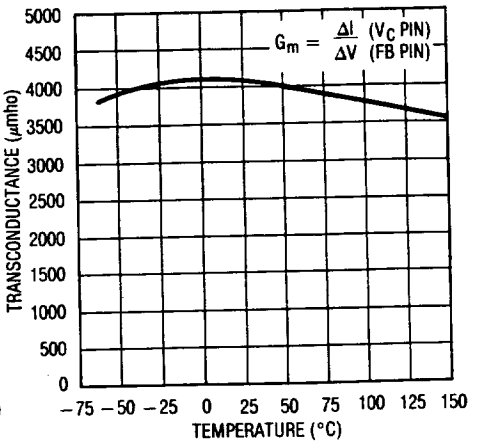
Normal/Flyback Mode Threshold on Feedback Pin



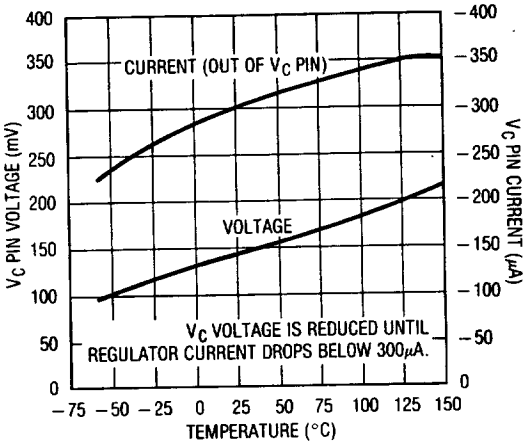
Shutdown Mode Supply Current



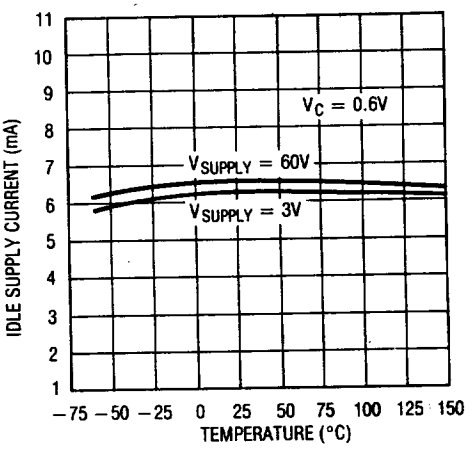
Error Amplifier Transconductance



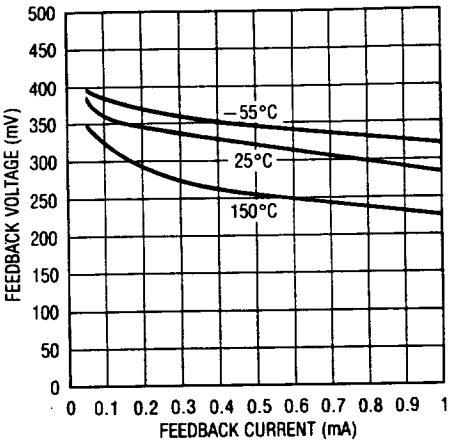
Shutdown Thresholds



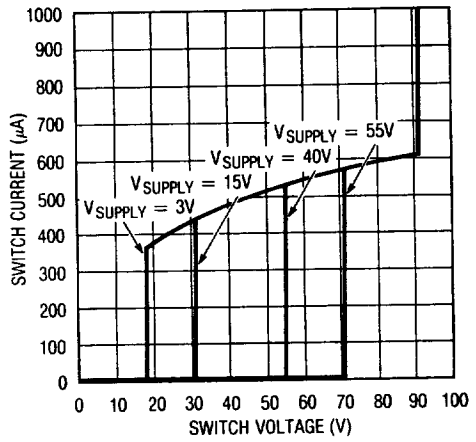
Idle Supply Current vs Temperature



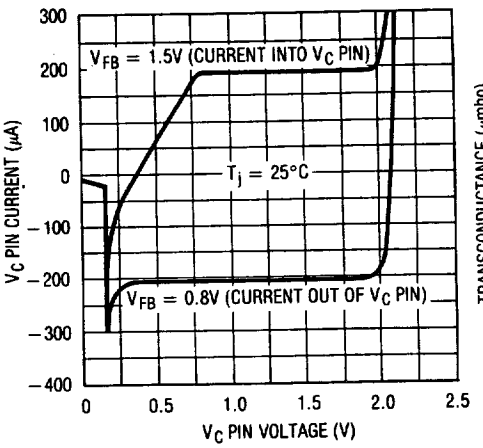
Feedback Pin Clamp Voltage



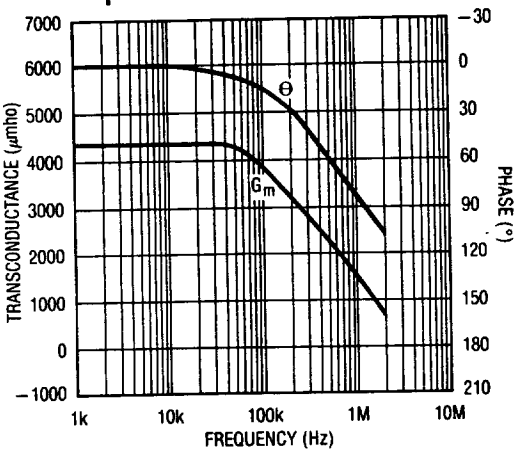
Switch "Off" Characteristics



V_C Pin Characteristics



Transconductance of Error Amplifier



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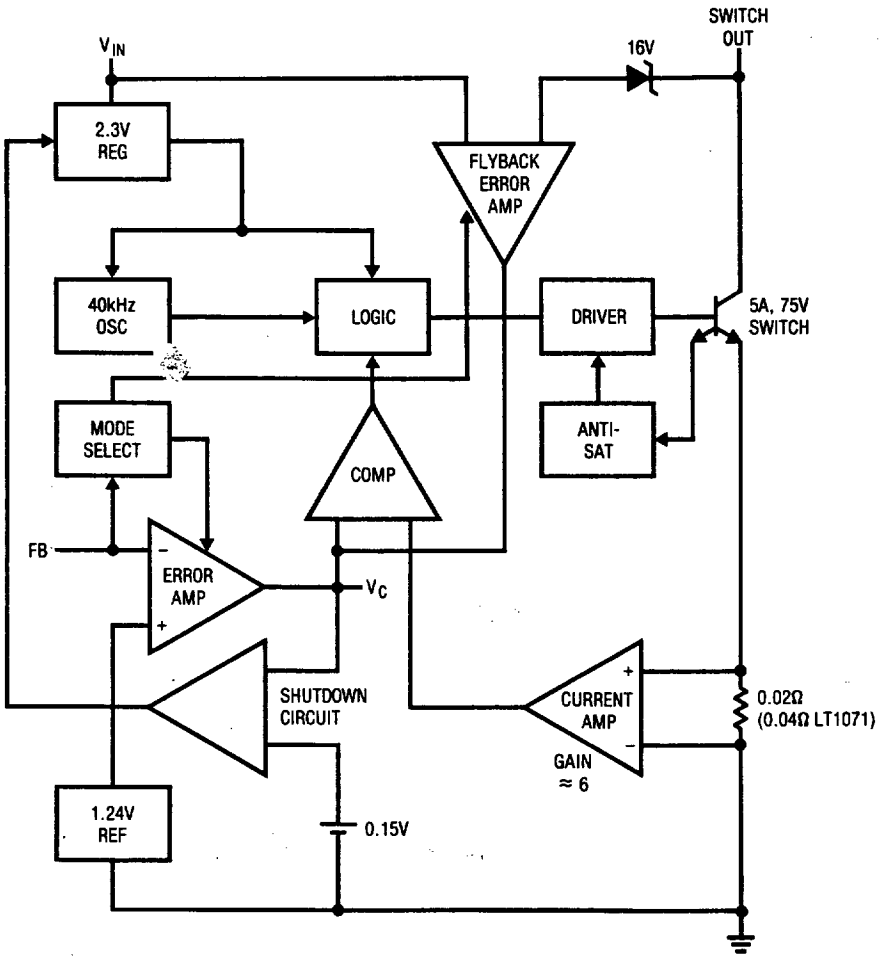
BLOCK DIAGRAM



LT1070/LT1071 OPERATION

The LT1070/LT1071 is a current mode switcher. This means that switch duty cycle is directly controlled by switch current rather than by output voltage. Referring to the block diagram, the switch is turned "on" at the start of each oscillator cycle. It is turned "off" when switch current reaches a predetermined level. Control of output voltage is obtained by using the output of a voltage sensing error amplifier to set current trip level. This technique has several advantages. First, it has immediate response to input voltage variations, unlike ordinary switchers which have notoriously poor line transient response. Second, it reduces the 90° phase shift at midfrequencies in the energy storage inductor. This greatly simplifies closed loop frequency compensation under widely varying input voltage or output load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short conditions. A low-dropout internal regulator provides a 2.3V supply for all internal circuitry on the LT1070/LT1071. This low-dropout design allows input voltage to vary from 3V to 60V with virtually no change in device performance. A 40kHz oscillator is the basic clock for all internal timing. It turns "on" the output switch via the logic and driver circuitry. Special adaptive anti-sat circuitry detects onset of saturation in the power switch and adjusts driver current instantaneously to limit switch saturation. This minimizes driver dissipation and provides very rapid turn-off of the switch.

A 1.2V bandgap reference biases the positive input of the error amplifier. The negative input is brought out for output voltage sensing. This feedback pin has a second function; when pulled low with an external resistor, it programs the LT1070/LT1071 to disconnect the main error amplifier output

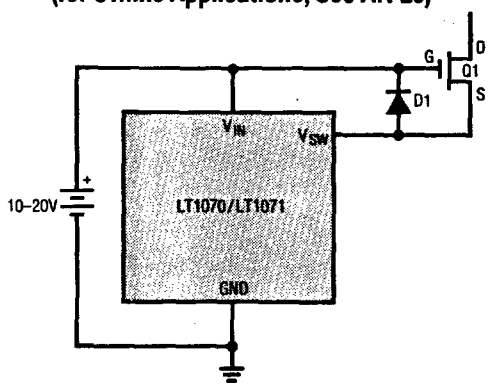
LT1070/LT1071 OPERATION

and connects the output of the flyback amplifier to the comparator input. The LT1070/LT1071 will then regulate the value of the flyback pulse with respect to the supply voltage. This flyback pulse is directly proportional to output voltage in the traditional transformer coupled flyback topology regulator. By regulating the amplitude of the flyback pulse, the output voltage can be regulated with no direct connection between input and output. The output is fully floating up to the breakdown voltage of the transformer windings. Multiple floating outputs are easily obtained with additional windings. A special delay network inside the LT1070/LT1071 ignores the leakage inductance spike at the leading edge of the flyback pulse to improve output regulation.

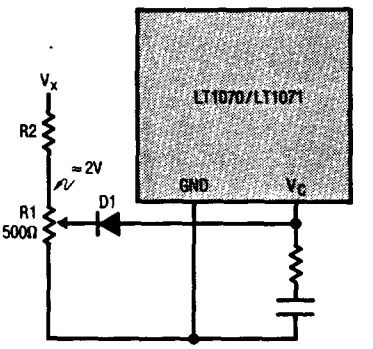
The error signal developed at the comparator input is brought out externally. This pin (V_C) has four different functions. It is used for frequency compensation, current limit adjustment, soft starting, and total regulator shutdown. During normal regulator operation this pin sits at a voltage between 0.9V (low output current) and 2.0V (high output current). The error amplifiers are current output (gm) types, so this voltage can be externally clamped for adjusting current limit. Likewise, a capacitor coupled external clamp will provide soft start. Switch duty cycle goes to zero if the V_C pin is pulled to ground through a diode, placing the LT1070/LT1071 in an idle mode. Pulling the V_C pin below 0.15V causes total regulator shutdown, with only 50μA supply current for shutdown circuitry biasing. See AN-19 for full application details.

TYPICAL APPLICATIONS (Note that maximum output currents are divided by 2 for LT1071.)

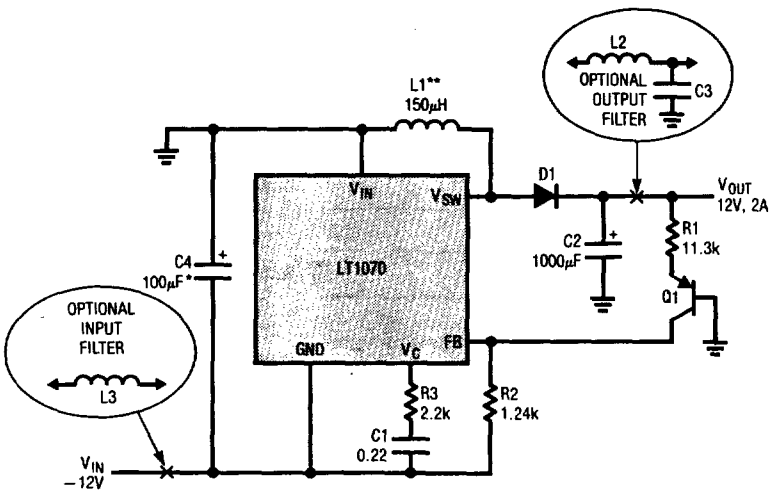
Driving High Voltage FET
(for Offline Applications, See AN-25)



External Current Limit

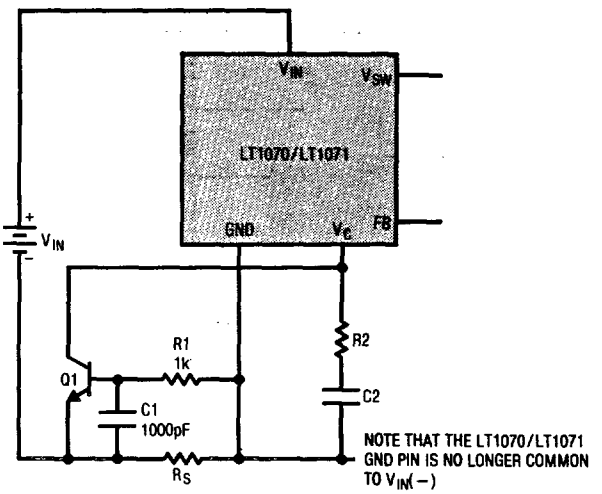


Negative to Positive Buck-Boost Converter



*REQUIRED IF INPUT LEADS ≥ 2"
**PULSE ENGINEERING 92113

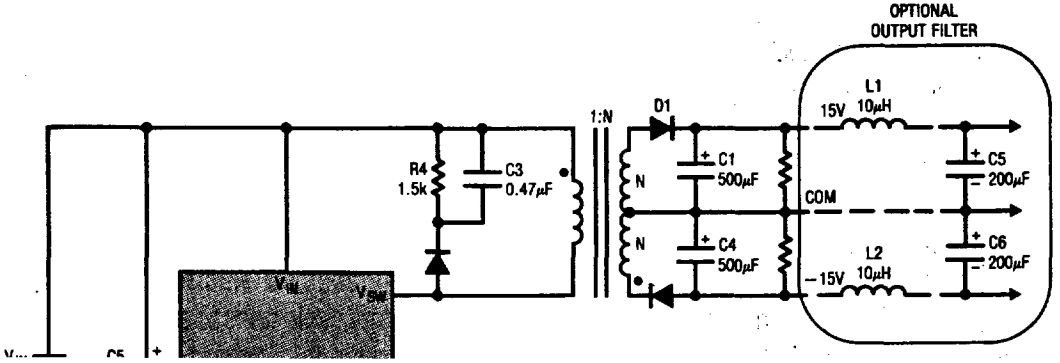
External Current Limit



NOTE THAT THE LT1070/LT1071 GND PIN IS NO LONGER COMMON TO $V_{IN}(-)$

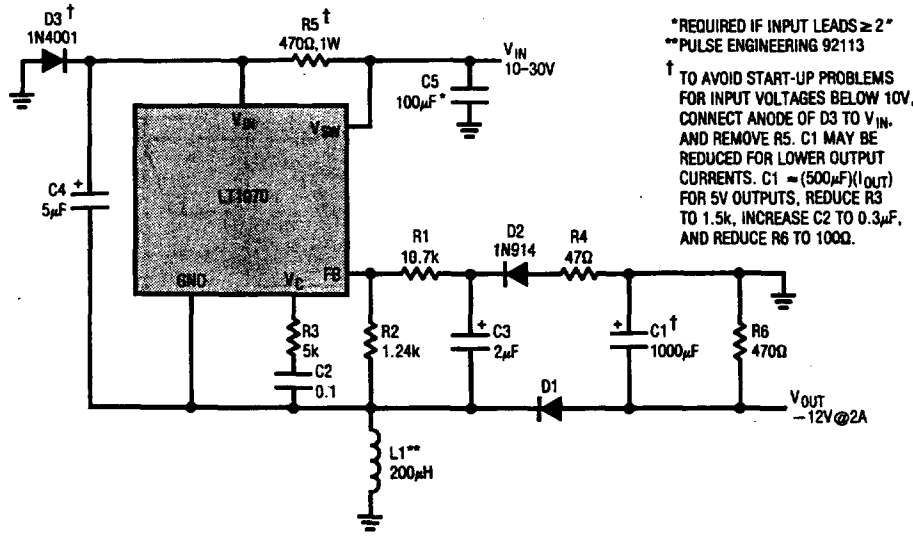
TYPICAL APPLICATIONS

Totally Isolated Converter

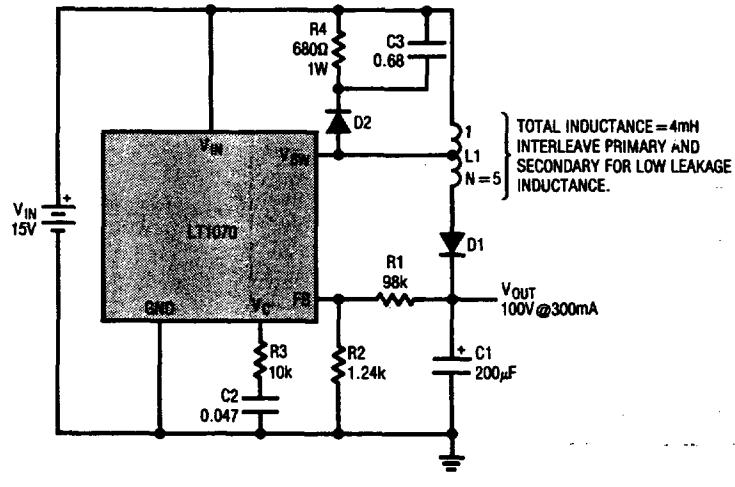


TYPICAL APPLICATIONS

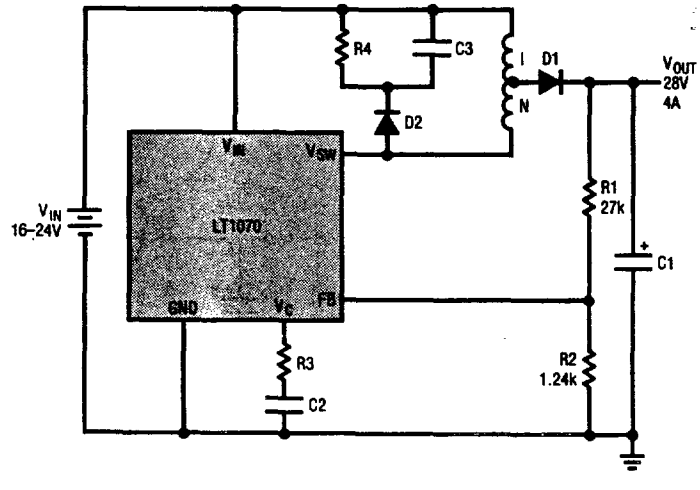
Positive to Negative Buck-Boost Converter



Voltage Boosted Boost Converter



Current Boosted Boost Converter



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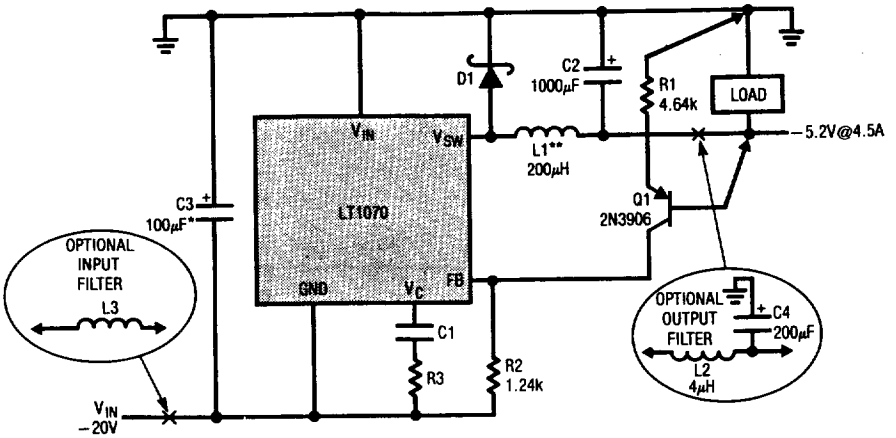
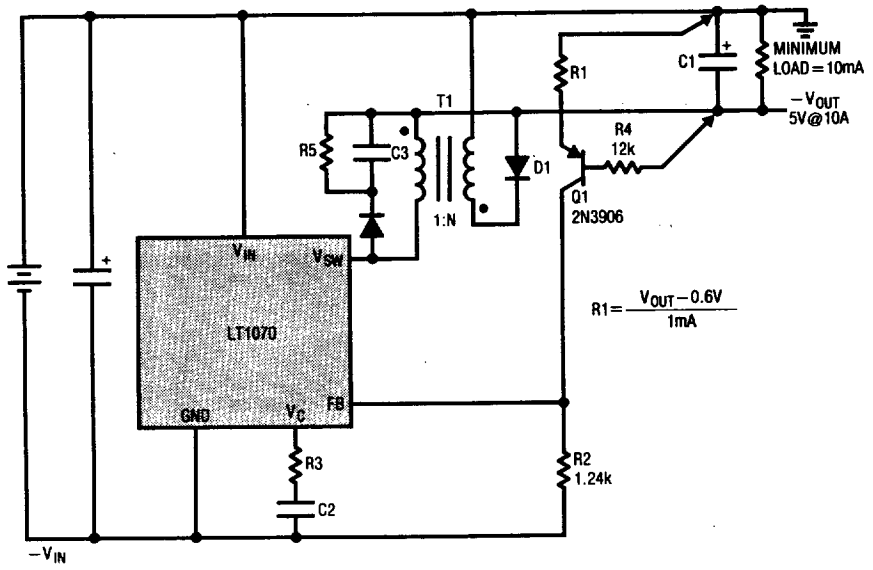
TYPICAL APPLICATIONS

Negative Buck Converter

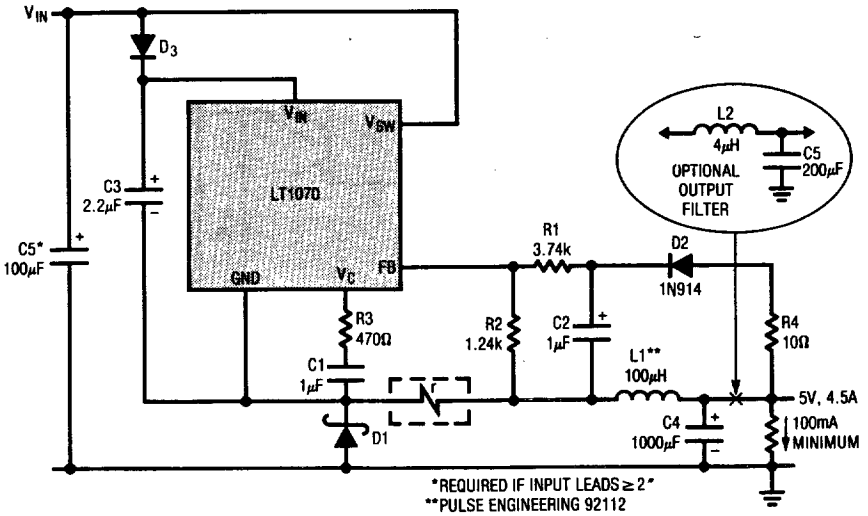


*REQUIRED IF INPUT LEADS ≥ 2"
**PULSE ENGINEERING 92113

Negative Current Boosted Buck Converter



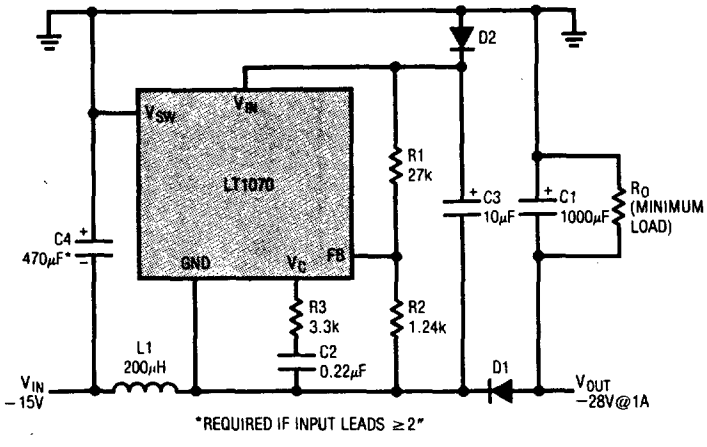
Positive Buck Converter



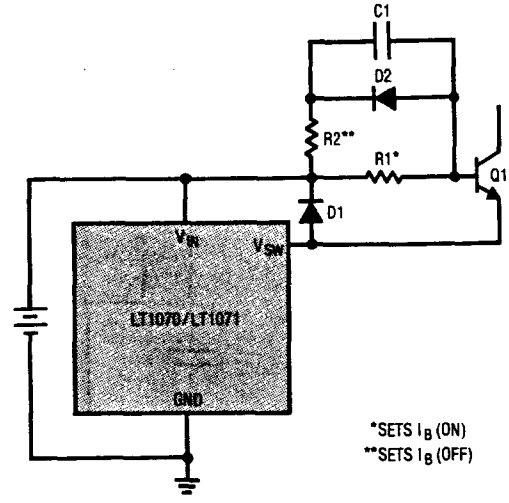
*REQUIRED IF INPUT LEADS ≥ 2"
**PULSE ENGINEERING 92112

TYPICAL APPLICATIONS

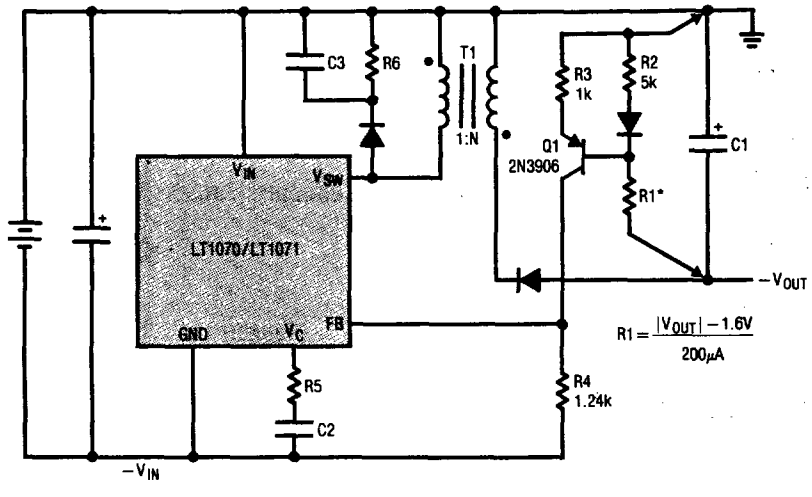
Negative Boost Regulator



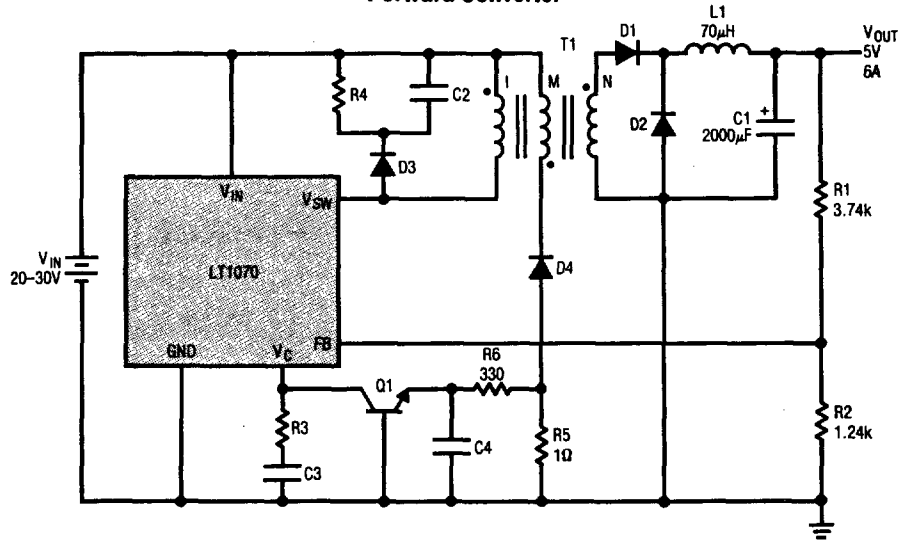
Driving High Voltage NPN



Negative Input-Negative Output Flyback Converter

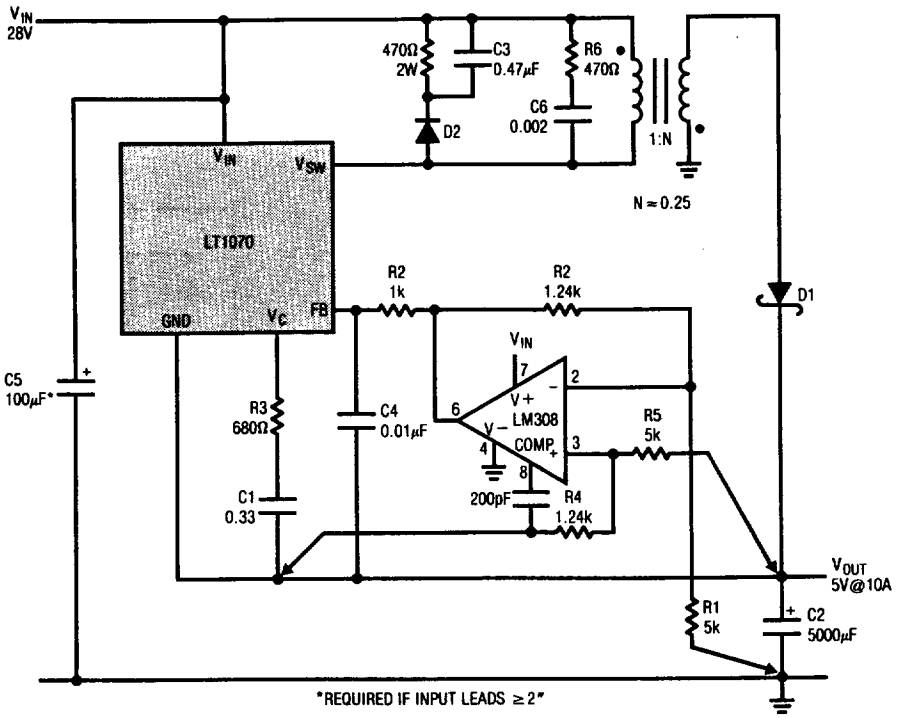


Forward Converter



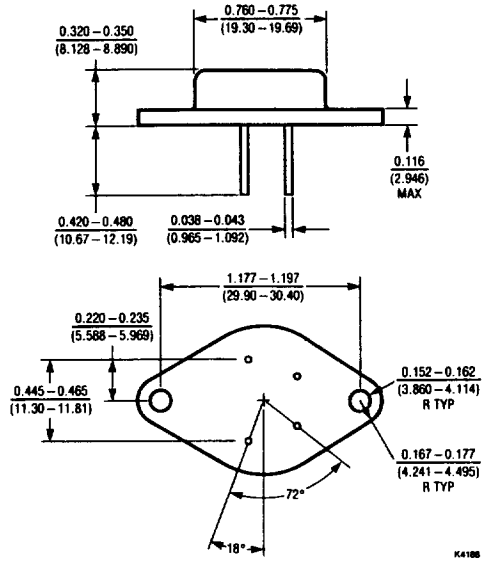
TYPICAL APPLICATIONS

Positive Current Boosted Buck Converter

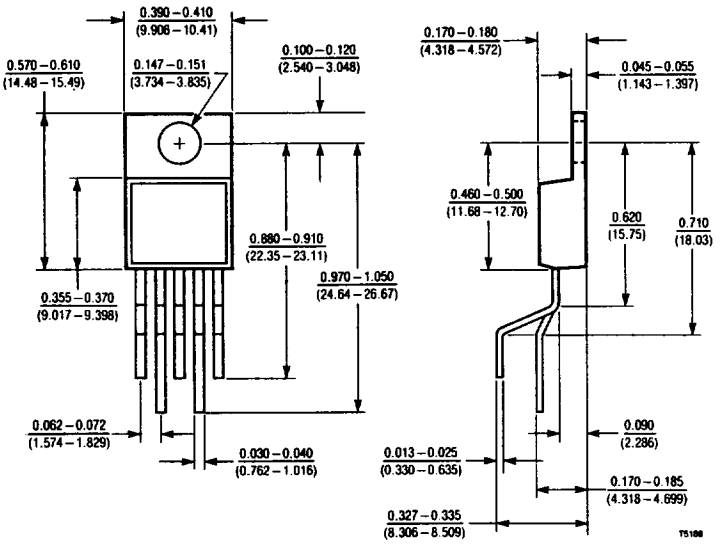


PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

TO-3 Type Metal Can (Steel) K Package



TO-220 Type Plastic T Package



	T_{JMAX}	θ_{JC}	θ_{JA}
LT1070MK, LT1070HVMK	150°C	2°C/W	35°C/W
LT1070CK, LT1070HVCK	100°C	2°C/W	35°C/W
LT1071MK, LT1071HVMK	150°C	4°C/W	35°C/W
LT1071CK, LT1071HVCK	100°C	4°C/W	35°C/W

	T_{JMAX}	θ_{JC}	θ_{JA}
LT1070CT, LT1070HVCT	100°C	2°C/W	75°C/W
LT1071CT, LT1071HVCT	100°C	4°C/W	75°C/W

5V Step-Down Switching Regulator

FEATURES

- Fixed 5V Output
- 2A On-Board Switch
- 100kHz Switching Frequency
- 2% Output Voltage Tolerance Over Temperature
- Greatly Improved Dynamic Behavior
- Available in Low Cost 5-Lead Package
- Only 9.5mA Quiescent Current
- Operates Up to 60V Input

APPLICATIONS

- 5V Output Buck Converter
- Tapped Inductor Buck Converter with 4A Output at 5V
- Positive-to-Negative Converter

DESCRIPTION

The LT1076-5 is a 2A fixed 5V output monolithic bipolar switching regulator which requires only a few external parts for normal operation. The power switch, all oscillator and control circuitry, all current limit components, and an output monitor are included on the chip. The topology is a classic positive "buck" configuration but several design innovations allow this device to be used as a positive-to-negative converter, a negative boost converter, and as a flyback converter. The switch output is specified to swing 40V below ground, allowing the LT1076-5 to drive a tapped inductor in the buck mode with output currents up to 4A.

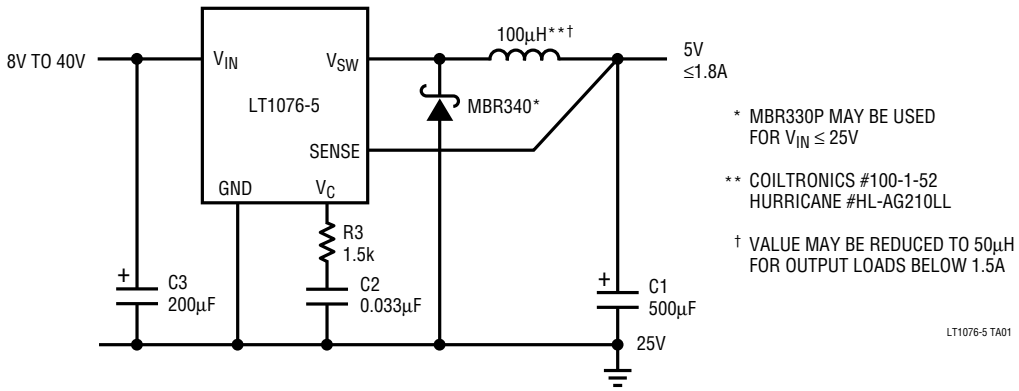
The LT1076-5 uses a true analog multiplier in the feedback loop. This makes the device respond nearly instantaneously to input voltage fluctuations and makes loop gain independent of input voltage. As a result, dynamic behavior of the regulator is significantly improved over previous designs.

On-chip pulse by pulse current limiting makes the LT1076-5 nearly bust-proof for output overloads or shorts. The input voltage range as a buck converter is 8V to 60V, but a self-boot feature allows input voltages as low as 5V in the inverting and boost configurations.

The LT1076-5 is available in a low cost 5-lead TO-220 package with frequency pre-set at 100kHz and current limit at 2.6A. See Application Note 44 for design details.

TYPICAL APPLICATION

Basic Positive Buck Converter



ABSOLUTE MAXIMUM RATINGS

Input Voltage
- LT1076-5 ..... 45V
- LT1076HV-5 ..... 64V

Switch Voltage with Respect to Input Voltage
- LT1076-5 ..... 64V
- LT1076HV-5 ..... 75V

Switch Voltage with Respect to Ground Pin (V_{SW} **Negative**)
- LT1076-5 (Note 5) 35V
- LT1076HV-5 (Note 5) 45V

Sense Pin Voltage ..... –2V, 10V

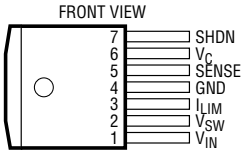
Maximum Operating Ambient Temperature Range
- LT1076C-5, LT1076HVC-5 ..... 0°C to 70°C
- LT1076I-5, LT1076HVI-5 ..... –40°C to 85°C

Maximum Operating Junction Temperature Range
- LT1076C-5, LT1076HVC-5 ..... 0°C to 125°C
- LT1076I-5, LT1076HVI-5 ..... –40°C to 125°C

Maximum Storage Temperature ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION

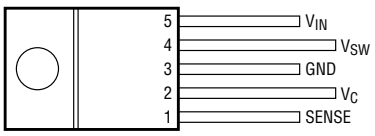


R PACKAGE
7-LEAD PLASTIC DD

T_{JMAX} = 110°C

θ WILL VARY FROM APPROXIMATELY 30°C/W WITH 2.8IN^2 OF 1 OZ COPPER TO 70°C/W WITH 0.20IN^2 OF 1 OZ COPPER.

ORDER PART NUMBER: LT1076CR-5

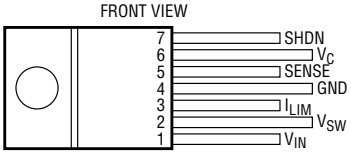


T PACKAGE
5-LEAD TO-220

FOR STRAIGHT LEADS, ORDER FLOW 06

T_{JMAX} = 110°C, θ_{JA} = 130°C/W

ORDER PART NUMBER: LT1076CT-5, LT1076HVCT-5, LT1076IT-5, LT1076HVIT-5



Y PACKAGE
7-LEAD TO-220

T_{JMAX} = 110°C, θ_{JA} = 130°C/W

ORDER PART NUMBER: LT1076CY-5

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

T_J = 25°C, V_{IN} = 25V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switch "On" Voltage (Note 1)	I_{SW} = 0.5A I_{SW} = 2A	● ●			1.2 1.7	V V
Switch "Off" Leakage	V_{IN} = 25V, V_{SW} = 0 V_{IN} = V_{MAX}, V_{SW} = 0 (Note 6)				150 250	µA µA
Supply Current (Note 2)	V_{OUT} = 5.5V, V_{IN} ≤ 40V 40V < V_{IN} < 60V V_{SHDN} = 0.1V (Device Shutdown) (Note 8)	● ●		8.5 9.0 140	11 12 300	mA mA µA
Minimum Supply Voltage	Normal Mode Start-Up Mode (Note 3)	● ●		7.3 3.5	8.0 4.8	V V
Switch Current Limit (Note 4)	I_{LIM} = Open R_{LIM} = 10k (Note 9) R_{LIM} = 7k (Note 9)	●	2	2.6 1.8 1.2	3.2	A A A
Maximum Duty Cycle		●	85	90		%

ELECTRICAL CHARACTERISTICS $T_J = 25°C$, $V_{IN} = 25V$, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switching Frequency			90	100	110	kHz
	$T_J \le 125°C$	●	85		120	kHz
	$V_{OUT} = V_{SENSE} = 0V$ (Note 4)			20		kHz
Switching Frequency Line Regulation	$8V \le V_{IN} \le V_{MAX}$ (Note 7)	●		0.03	0.1	%/V
Error Amplifier Voltage Gain (Note 7)	$1V \le V_C \le 4V$			2000		V/V
Error Amplifier Transconductance (Note 7)			3700	5000	8000	μmho
Error Amplifier Source and Sink Current	Source ($V_{SENSE} = 4.5V$)		100	140	225	μA
	Sink ($V_{SENSE} = 5.5V$)		0.7	1.0	1.6	mA
Sense Pin Divider Resistance			3	5	8	kΩ
Sense Voltage	$V_C = 2V$	●	4.85	5	5.15	V
Output Voltage Tolerance	V_{OUT} (Nominal) = 5V			±0.5	±2	%
	All Conditions of Input Voltage, Output Voltage, Temperature and Load Current	●		±1.0	±3	%
Output Voltage Line Regulation	$8V \le V_{IN} \le V_{MAX}$ (Note 6)	●		0.005	0.02	%/V
V_C Voltage at 0% Duty Cycle				1.5		V
	Over Temperature	●		–4.0		mV/°C
Multiplier Reference Voltage				24		V
Shutdown Pin Current	$V_{SHDN} = 5V$		5	10	20	μA
	$V_{SHDN} \le V_{THRESHOLD}$ (≅ 2.5V)				50	μA
Shutdown Thresholds	Switch Duty Cycle = 0		2.2	2.45	2.7	V
	Fully Shut Down		0.1	0.30	0.5	V
Thermal Resistance Junction to Case					4	°C/W

The ● denotes specifications which apply over the full operating temperature range.

Note 1: To calculate maximum switch "on" voltage at currents between low and high conditions, a linear interpolation may be used.

Note 2: A sense pin voltage (V_{SENSE}) of 5.5V forces the V_C pin to its low clamp level and the switch duty cycle to zero. This approximates the zero load condition where duty cycle approaches zero.

Note 3: Total voltage from V_{IN} pin to ground pin must be ≥ 8V after start-up for proper regulation. For $T_A < 25°C$, limit = 5V.

Note 4: Switch frequency is internally scaled down when the sense pin voltage is less than 2.6V to avoid extremely short switch on times. During current limit testing, V_{SENSE} is adjusted to give a minimum switch on time of 1μs.

Note 5: Switch to input voltage limitation must also be observed.

Note 6: V_{MAX} = 40V for the LT1076-5 and 60V for the LT1076HV-5.

Note 7: Error amplifier voltage gain and transconductance are specified relative to the internal feedback node. To calculate gain and transconductance from the Sense pin (Output) to the V_C pin, multiply by 0.44.

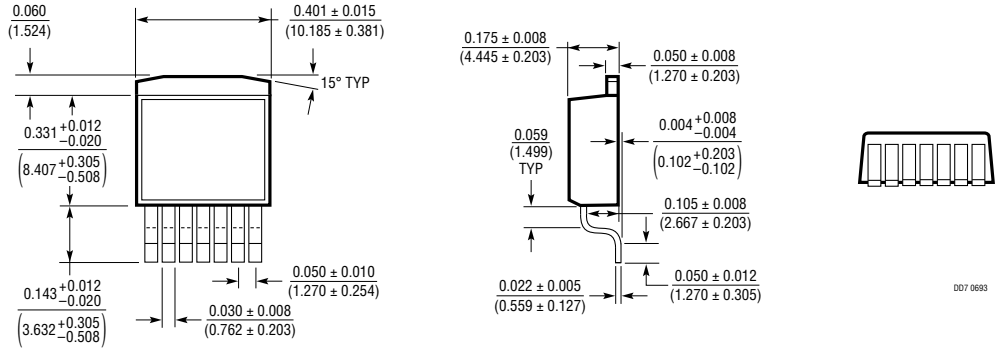
Note 8: Does not include switch leakage.

Note 9: $I_{LIM} \approx \frac{R_{LIM} - 1k}{5k}$

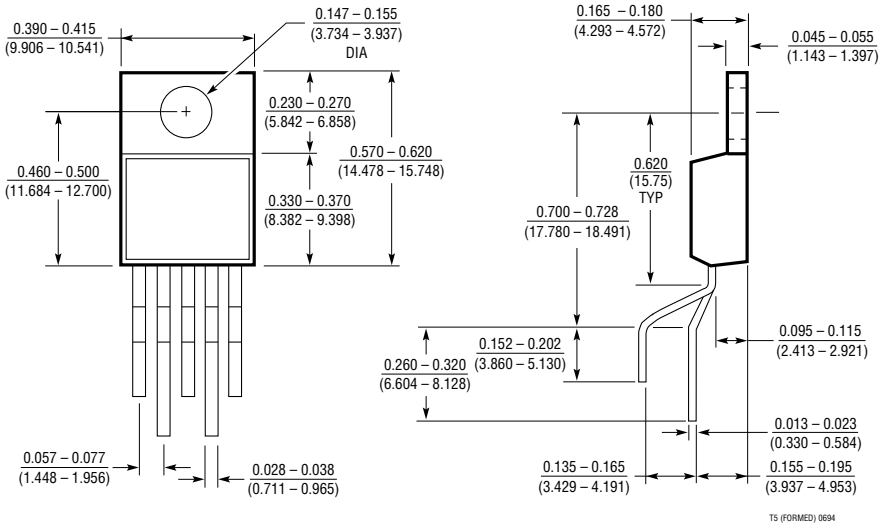
PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

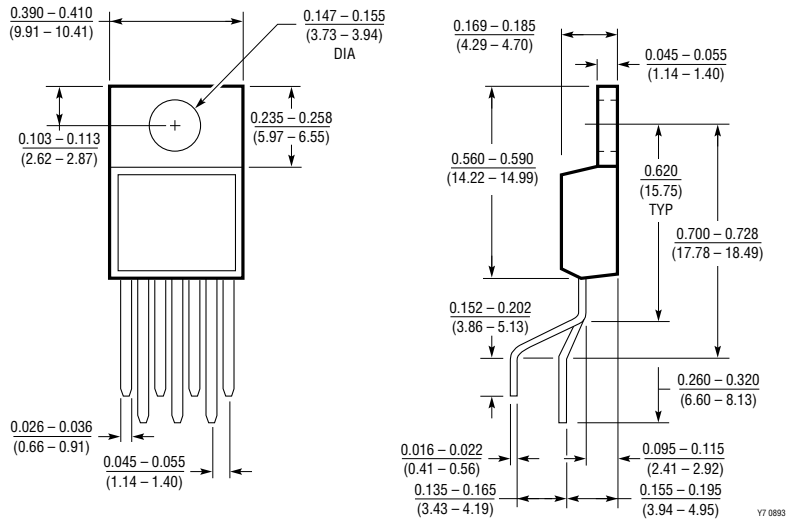
R Package, 7-Lead Plastic DD



T Package, 5-Lead TO-220



Y Package, 7-Lead TO-220



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LT/GP 0794 5K REV A • PRINTE IN USA

12V CMOS Voltage Converter

FEATURES

- **1.5V to 12V Operating Supply Voltage Range**
- **13V Absolute Maximum Rating**
- 200μA Maximum No Load Supply Current at 5V
- Boost Pin (Pin 1) for Higher Switching Frequency
- 97% Minimum Open Circuit Voltage Conversion Efficiency
- 95% Minimum Power Conversion Efficiency
- I_S = 1.5μA with 5V Supply When OSC Pin = 0V or V^+
- High Voltage Upgrade to ICL7660/LTC1044

APPLICATIONS

- Conversion of 10V to ±10V Supplies
- Conversion of 5V to ±5V Supplies
- Precise Voltage Division: $V_{OUT} = V_{IN}/2 \pm 20ppm$
- Voltage Multiplication: $V_{OUT} = \pm nV_{IN}$
- Supply Splitter: $V_{OUT} = \pm V_S/2$
- Automotive Applications
- Battery Systems with 9V Wall Adapters/Chargers

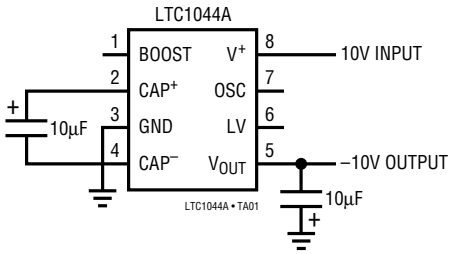
DESCRIPTION

The LTC1044A is a monolithic CMOS switched-capacitor voltage converter. It plugs in for ICL7660/LTC1044 in applications where higher input voltage (up to 12V) is needed. The LTC1044A provides several conversion functions without using inductors. The input voltage can be inverted ($V_{OUT} = -V_{IN}$), doubled ($V_{OUT} = 2V_{IN}$), divided ($V_{OUT} = V_{IN}/2$) or multiplied ($V_{OUT} = \pm nV_{IN}$).

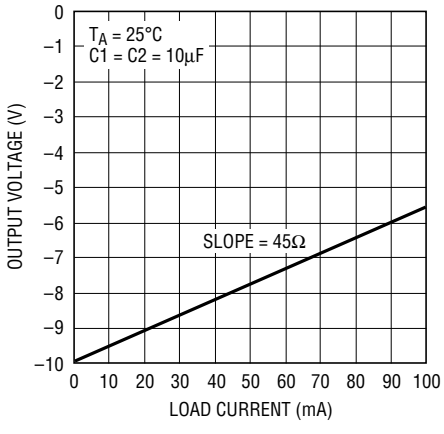
To optimize performance in specific applications, a boost function is available to raise the internal oscillator frequency by a factor of 7. Smaller external capacitors can be used in higher frequency operation to save board space. The internal oscillator can also be disabled to save power. The supply current drops to 1.5μA at 5V input when the OSC pin is tied to GND or V^+.

TYPICAL APPLICATION

Generating –10V from 10V



Output Voltage vs Load Current, V^+ = 10V

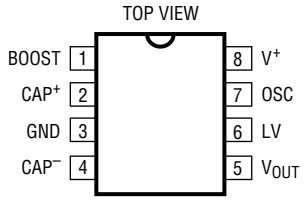


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage 13V
Input Voltage on Pins 1, 6 and 7
(Note 2) ..... $-0.3V < V_{IN} < V^+ + 0.3V$
Current into Pin 6 ..... 20μA
Output Short-Circuit Duration
$V^+ \leq 6.5V$ ..... Continuous
Operating Temperature Range
LTC1044AC ..... 0°C to 70°C
LTC1044AI ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

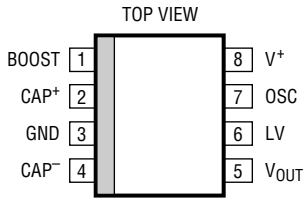
PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP

T_{JMAX} = 110°C, θ_{JA} = 100°C/W

ORDER PART NUMBER
LTC1044ACN8 LTC1044AIN8



S8 PACKAGE
8-LEAD PLASTIC SOIC

T_{JMAX} = 110°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC1044ACS8 LTC1044AIS8
S8 PART MARKING
1044A 1044AI

Consult factory for Military grade parts

ELECTRICAL CHARACTERISTICS

$V^+ = 5V$, $C_{OSC} = 0pF$, $T_A = 25°C$, See Test Circuit, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1044AC MIN	LTC1044AC TYP	LTC1044AC MAX	LTC1044AI MIN	LTC1044AI TYP	LTC1044AI MAX	UNITS
I_S	Supply Current	$R_L = \infty$, Pins 1 and 7, No Connection			60	200		60	200	μA
		$R_L = \infty$, Pins 1 and 7, No Connection, $V^+ = 3V$			15			15		μA
	Minimum Supply Voltage	$R_L = 10k$	●	1.5			1.5			V
	Maximum Supply Voltage	$R_L = 10k$	●			12			12	V
R_{OUT}	Output Resistance	$I_L = 20mA$, $f_{OSC} = 5kHz$				100			100	Ω
			●			120			130	Ω
		$V^+ = 2V$, $I_L = 3mA$, $f_{OSC} = 1kHz$	●			310			325	Ω
f_{OSC}	Oscillator Frequency	$V^+ = 5V$, (Note 3)	●	5			5			kHz
		$V^+ = 2V$	●	1			1			kHz
P_{EFF}	Power Efficiency	$R_L = 5k$, $f_{OSC} = 5kHz$		95	98		95	98		%
	Voltage Conversion Efficiency	$R_L = \infty$		97	99.9		97	99.9		%
	Oscillator Sink or Source Current	V_{OSC} = 0V or V^+								
		Pin 1 (BOOST) = 0V	●			3			3	μA
		Pin 1 (BOOST) = V^+	●			20			20	μA

The ● denotes specifications which apply over the full operating temperature range; all other limits and typicals $T_A = 25°C$.

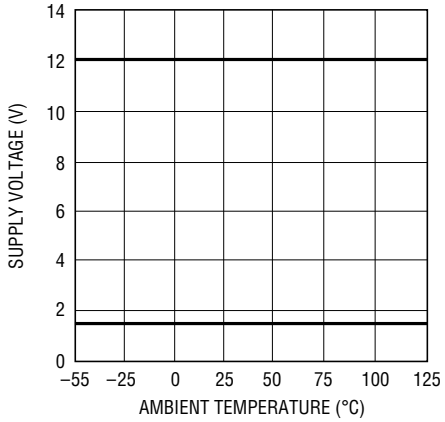
Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: Connecting any input terminal to voltages greater than V^+ or less than ground may cause destructive latch-up. It is recommended that no inputs from sources operating from external supplies be applied prior to power-up of the LTC1044A.

Note 3: f_{OSC} is tested with C_{OSC} = 100pF to minimize the effects of test fixture capacitance loading. The 0pF frequency is correlated to this 100pF test point, and is intended to simulate the capacitance at pin 7 when the device is plugged into a test socket and no external capacitor is used.

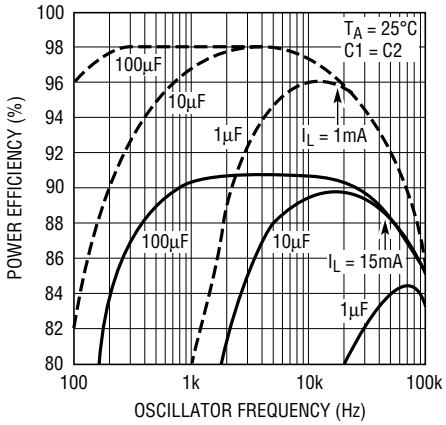
TYPICAL PERFORMANCE CHARACTERISTICS Using the Test Circuit

Operating Voltage Range vs Temperature



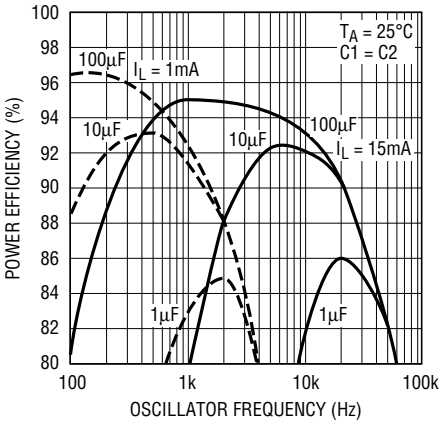
LTC1044A • TPC01

Power Efficiency vs Oscillator Frequency, V+ = 5V



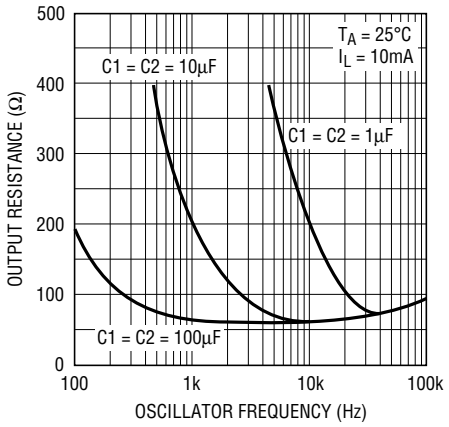
LTC1044A • G02

Power Efficiency vs Oscillator Frequency, V+ = 10V



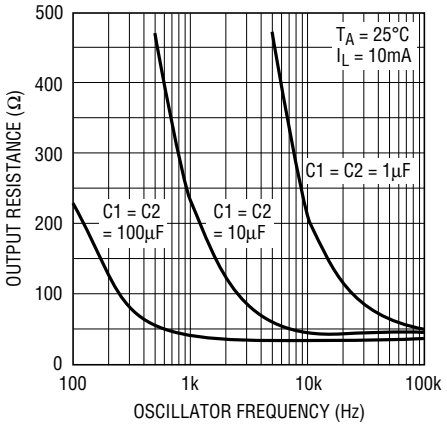
LTC1044A • TPC03

Output Resistance vs Oscillator Frequency, V+ = 5V



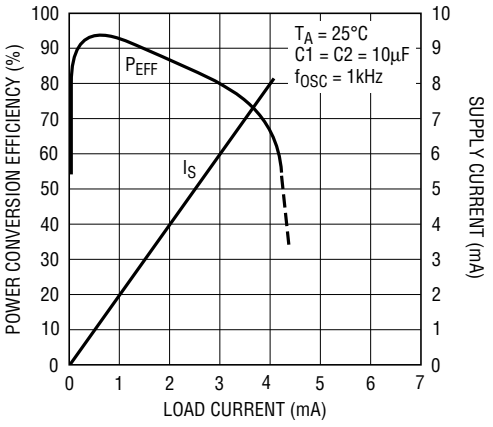
LTC1044A • TPC04

Output Resistance vs Oscillator Frequency, V+ = 10V



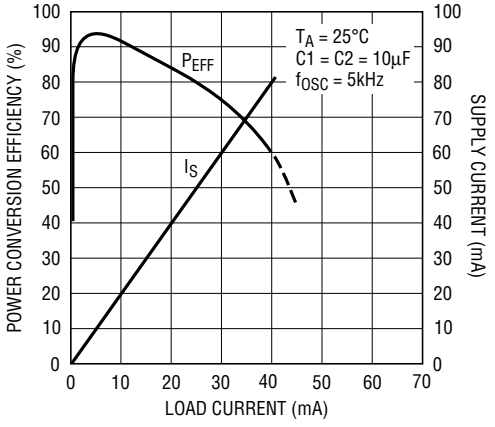
LTC1044A • TPC05

Power Conversion Efficiency vs Load Current, V+ = 2V



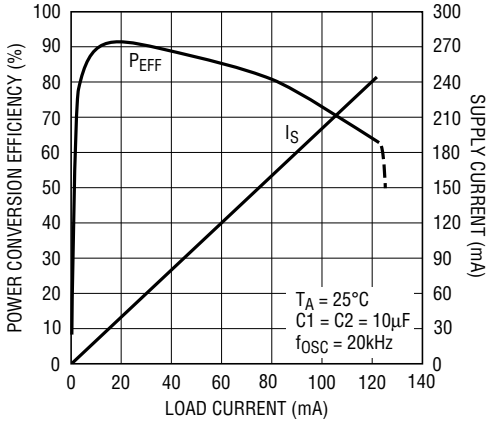
LTC1044A • TPC06

Power Conversion Efficiency vs Load Current, V+ = 5V



LTC1044A • TPC07

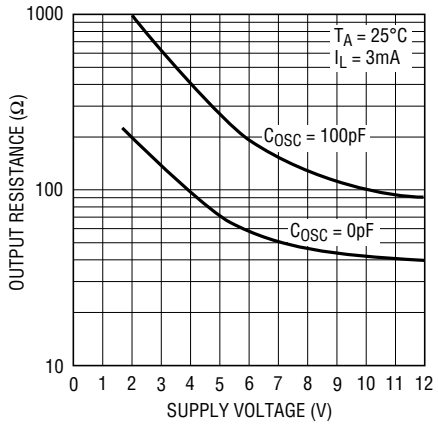
Power Conversion Efficiency vs Load Current, V+ = 10V



LTC1044A • TPC08

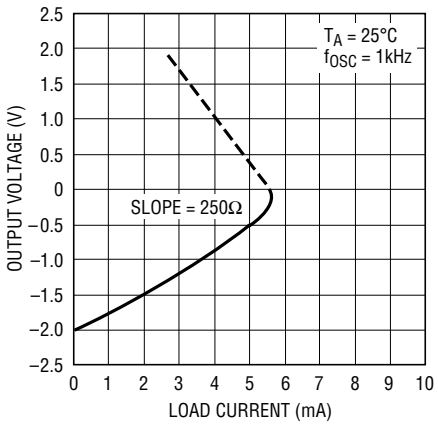
TYPICAL PERFORMANCE CHARACTERISTICS Using the Test Circuit

Output Resistance vs Supply Voltage



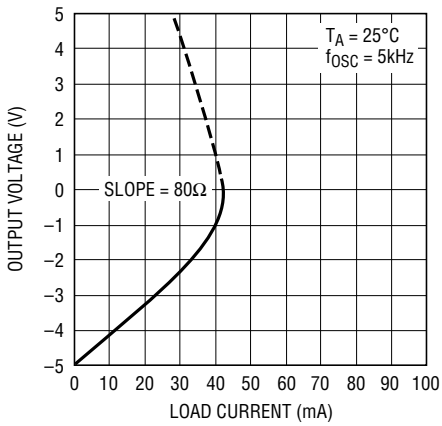
LTC1044A • TPC09

Output Voltage vs Load Current, V+ = 2V



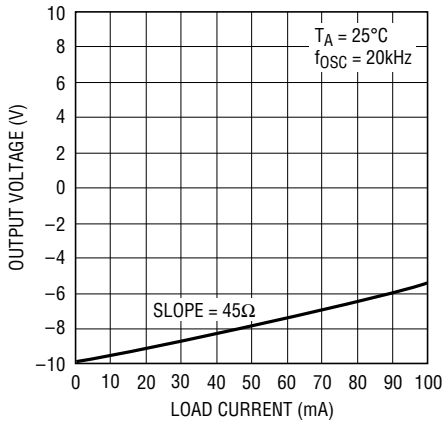
LTC1044A • TPC10

Output Voltage vs Load Current, V+ = 5V



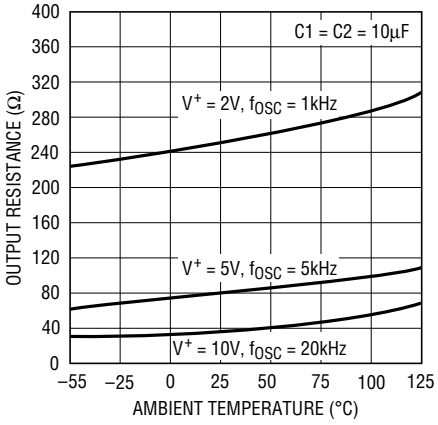
LTC1044A • TPC11

Output Voltage vs Load Current, V+ = 10V



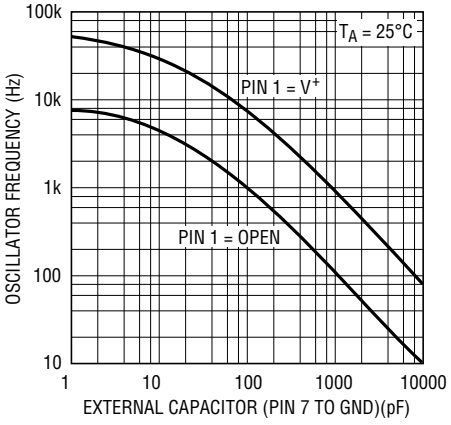
LTC1044A • TPC12

Output Resistance vs Temperature



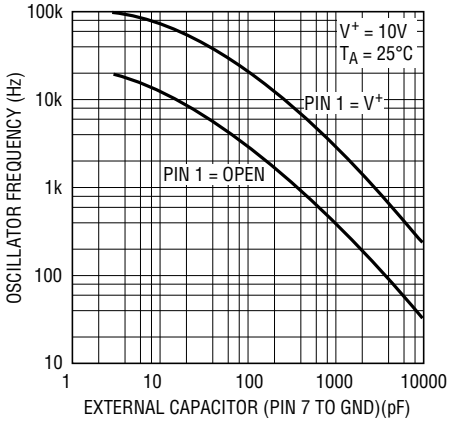
LTC1044A • TPC13

Oscillator Frequency as a Function of C_{OSC}, V+ = 5V



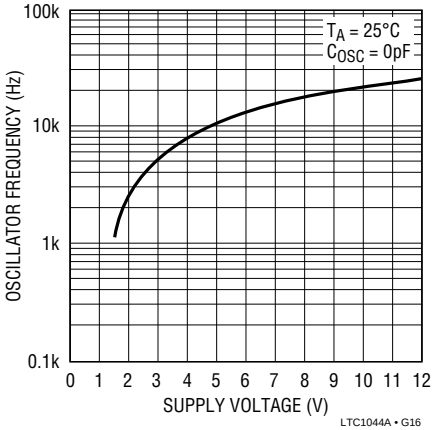
LTC1044A • TPC14

Oscillator Frequency as a Function of C_{OSC}, V+ = 10V



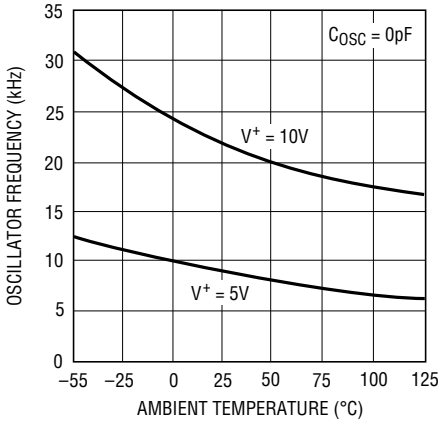
LTC1044A • TPC15

Oscillator Frequency vs Supply Voltage



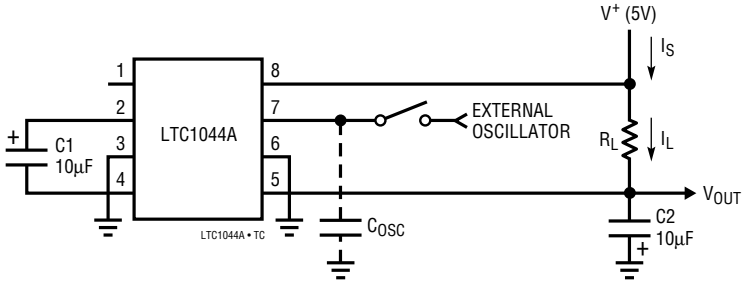
LTC1044A • G16

Oscillator Frequency vs Temperature



LTC1044A • TPC17

TEST CIRCUIT



APPLICATIONS INFORMATION

Theory of Operation

To understand the theory of operation of the LTC1044A, a review of a basic switched-capacitor building block is helpful.

In Figure 1, when the switch is in the left position, capacitor C1 will charge to voltage V1. The total charge on C1 will be q1 = C1V1. The switch then moves to the right, discharging C1 to voltage V2. After this discharge time, the charge on C1 is q2 = C1V2. Note that charge has been transferred from the source, V1, to the output, V2. The amount of charge transferred is:

$$\Delta q = q1 - q2 = C1(V1 - V2)$$

If the switch is cycled f times per second, the charge transfer per unit time (i.e., current) is:

$$I = f \times \Delta q = f \times C1(V1 - V2)$$

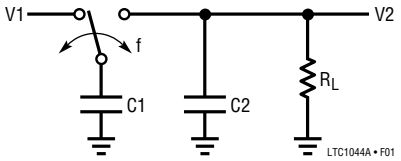


Figure 1. Switched-Capacitor Building Block

Rewriting in terms of voltage and impedance equivalence,

$$I = \frac{V1 - V2}{1/(f \times C1)} = \frac{V1 - V2}{R_{EQUIV}}$$

A new variable, R_{EQUIV}, has been defined such that $R_{EQUIV} = 1/(f \times C1)$. Thus, the equivalent circuit for the switched-capacitor network is as shown in Figure 2.

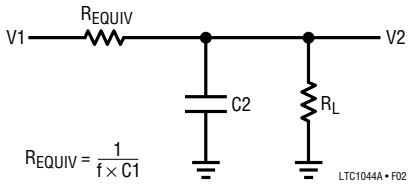


Figure 2. Switched-Capacitor Equivalent Circuit

Examination of Figure 3 shows that the LTC1044A has the same switching action as the basic switched-capacitor building block. With the addition of finite switch-on resistance and output voltage ripple, the simple theory although not exact, provides an intuitive feel for how the device works.

For example, if you examine power conversion efficiency as a function of frequency (see typical curve), this simple theory will explain how the LTC1044A behaves. The loss, and hence the efficiency, is set by the output impedance. As frequency is decreased, the output impedance will eventually be dominated by the $1/(f \times C1)$ term, and power efficiency will drop. The typical curves for Power Efficiency vs Frequency show this effect for various capacitor values.

Note also that power efficiency decreases as frequency goes up. This is caused by internal switching losses which occur due to some finite charge being lost on each switching cycle. This charge loss per unit cycle, when multiplied by the switching frequency, becomes a current loss. At high frequency this loss becomes significant and the power efficiency starts to decrease.

APPLICATIONS INFORMATION

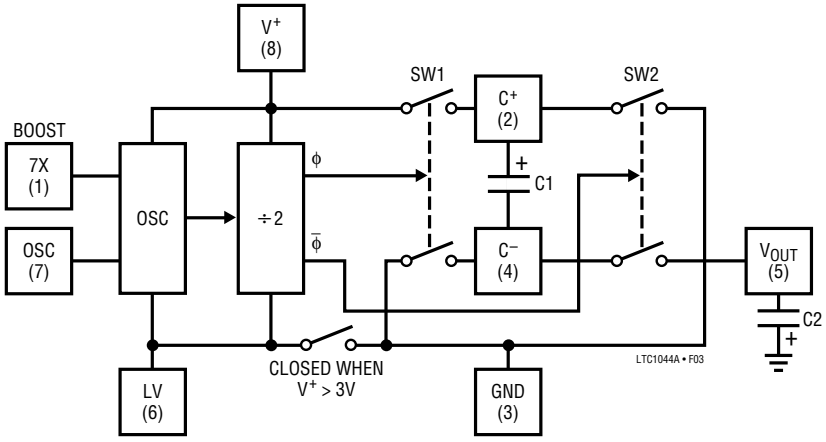


Figure 3. LTC1044A Switched-Capacitor Voltage Converter Block Diagram

LV (Pin 6)

The internal logic of the LTC1044A runs between V^+ and LV (pin 6). For V^+ greater than or equal to 3V, an internal switch shorts LV to GND (pin 3). For V^+ less than 3V, the LV pin should be tied to GND. For V^+ greater than or equal to 3V, the LV pin can be tied to GND or left floating.

OSC (Pin 7) and Boost (Pin 1)

The switching frequency can be raised, lowered, or driven from an external source. Figure 4 shows a functional diagram of the oscillator circuit.

By connecting the boost pin (pin 1) to V^+, the charge and discharge current is increased and hence, the frequency is increased by approximately 7 times. Increasing the frequency will decrease output impedance and ripple for higher load currents.

Loading pin 7 with more capacitance will lower the frequency. Using the boost (pin 1) in conjunction with external capacitance on pin 7 allows user selection of the frequency over a wide range.

Driving the LTC1044A from an external frequency source can be easily achieved by driving pin 7 and leaving the boost pin open as shown in Figure 5. The output current from pin 7 is small (typically 0.5μA) so a logic gate is capable of driving this current. The choice of using a CMOS logic gate is best because it can operate over a wide supply voltage range (3V to 15V) and has enough voltage swing to drive the internal Schmitt trigger shown in Figure 4. For 5V applications, a TTL logic gate can be used by simply adding an external pull-up resistor (see Figure 5).

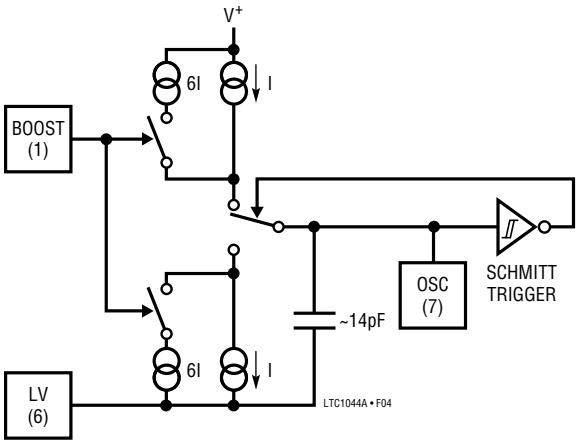


Figure 4. Oscillator

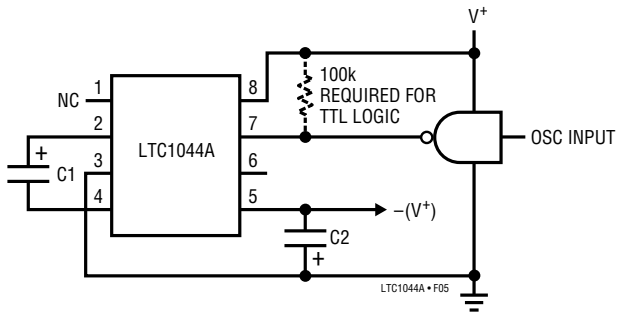


Figure 5. External Clocking

APPLICATIONS INFORMATION

Capacitor Selection

External capacitors C1 and C2 are not critical. Matching is not required, nor do they have to be high quality or tight tolerance. Aluminum or tantalum electrolytics are excellent choices with cost and size being the only consideration.

Negative Voltage Converter

Figure 6 shows a typical connection which will provide a negative supply from an available positive supply. This circuit operates over full temperature and power supply ranges *without* the need of any external diodes. The LV pin (pin 6) is shown grounded, but for $V^+ \geq 3V$ it may be "floated", since LV is internally switched to ground (pin 3) for $V^+ \geq 3V$.

The output voltage (pin 5) characteristics of the circuit are those of a nearly ideal voltage source in series with an 80Ω resistor. The 80Ω output impedance is composed of two terms:

1. The equivalent switched-capacitor resistance (see Theory of Operation).
2. A term related to the on-resistance of the MOS switches.

At an oscillator frequency of 10kHz and C1 = 10μF, the first term is:

$$R_{EQUIV} = \frac{1}{(f_{OSC}/2) \times C1}$$

$$= \frac{1}{5 \times 10^3 \times 10 \times 10^{-6}} = 20\Omega$$

Notice that the above equation for R_{EQUIV} is *not* a capacitive reactance equation ($X_C = 1/\omega C$) and does not contain a 2π term.

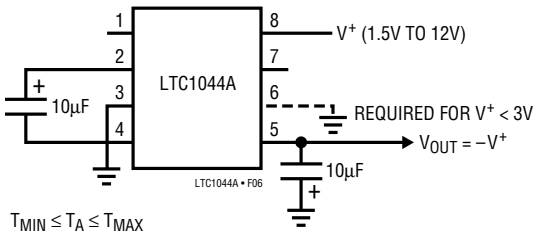


Figure 6. Negative Voltage Converter

The exact expression for output resistance is extremely complex, but the dominant effect of the capacitor is clearly shown on the typical curves of Output Resistance and Power Efficiency vs Frequency. For C1 = C2 = 10μF, the output impedance goes from 60Ω at f_{OSC} = 10kHz to 200Ω at f_{OSC} = 1kHz. As the $1/(f \times C)$ term becomes large compared to the switch-on resistance term, the output resistance is determined by $1/(f \times C)$ only.

Voltage Doubling

Figure 7 shows a two-diode capacitive voltage doubler. With a 5V input, the output is 9.93V with no load and 9.13V with a 10mA load. With a 10V input, the output is 19.93V with no load and 19.28V with a 10mA load.

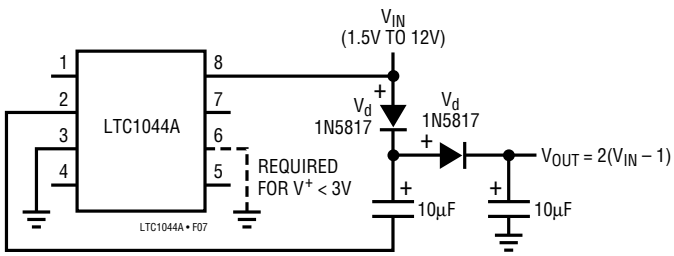


Figure 7. Voltage Doubler

Ultra-Precision Voltage Divider

An ultra-precision voltage divider is shown in Figure 8. To achieve the 0.0002% accuracy indicated, the load current should be kept below 100nA. However, with a slight loss in accuracy the load current can be increased.

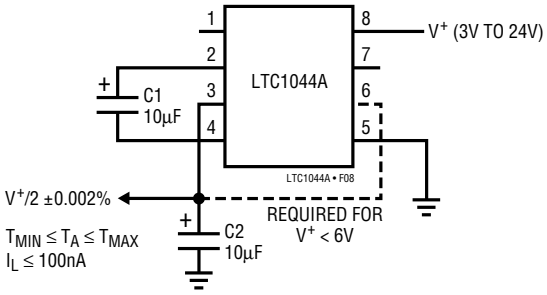


Figure 8. Ultra-Precision Voltage Divider

APPLICATIONS INFORMATION

Battery Splitter

A common need in many systems is to obtain (+) and (–) supplies from a single battery or single power supply system. Where current requirements are small, the circuit shown in Figure 9 is a simple solution. It provides symmetrical ± output voltages, both equal to one half input voltage. The output voltages are both referenced to pin 3 (output common). If the input voltage between pin 8 and pin 5 is less than 6V, pin 6 should also be connected to pin 3 as shown by the dashed line.

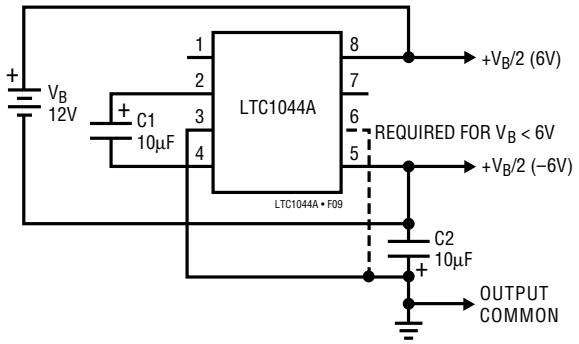


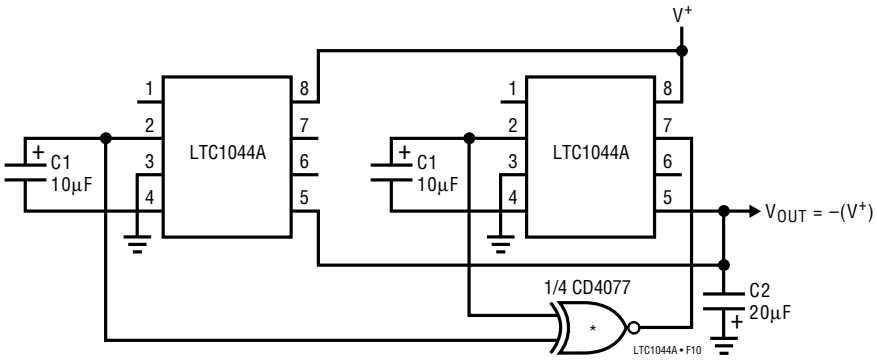
Figure 9. Battery Splitter

Paralleling for Lower Output Resistance

Additional flexibility of the LTC1044A is shown in Figures 10 and 11.

Figure 10 shows two LTC1044As connected in parallel to provide a lower effective output resistance. If, however, the output resistance is dominated by 1/(f × C1), increasing the capacitor size (C1) or increasing the frequency will be of more benefit than the paralleling circuit shown.

Figure 11 makes use of "stacking" two LTC1044As to provide even higher voltages. A negative voltage doubler or tripler can be achieved, depending upon how pin 8 of the second LTC1044A is connected, as shown schematically by the switch. The available output current will be dictated/decreased by the product of the individual power conversion efficiencies and the voltage step-up ratio.



*THE EXCLUSIVE NOR GATE SYNCHRONIZES BOTH LTC1044As TO MINIMIZE RIPPLE

Figure 10. Paralleling for Lower Output Resistance

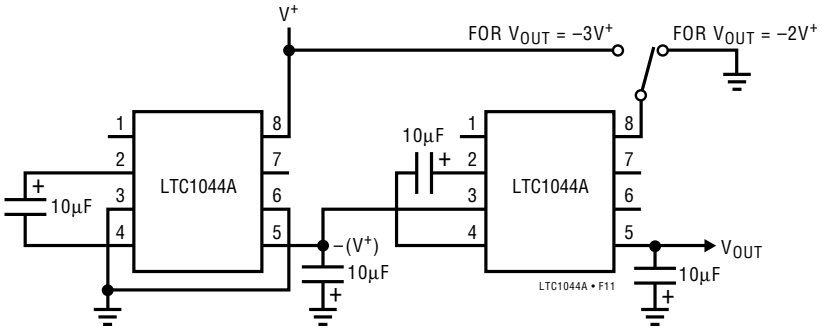
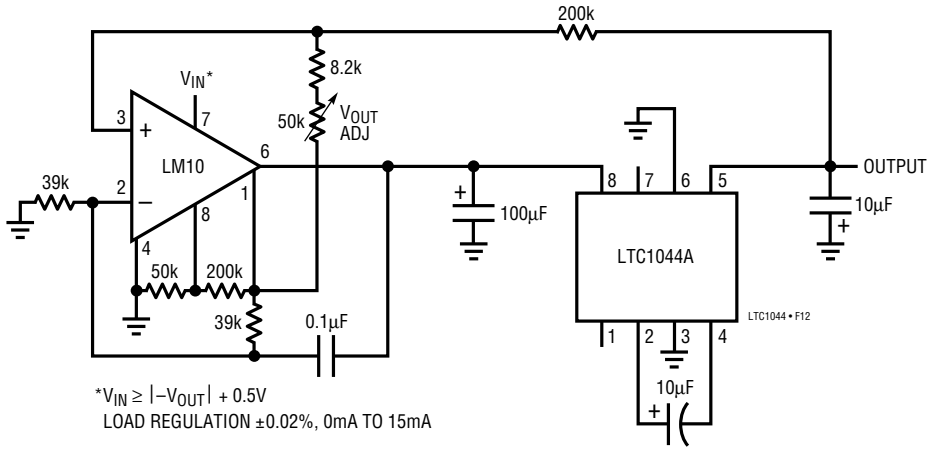


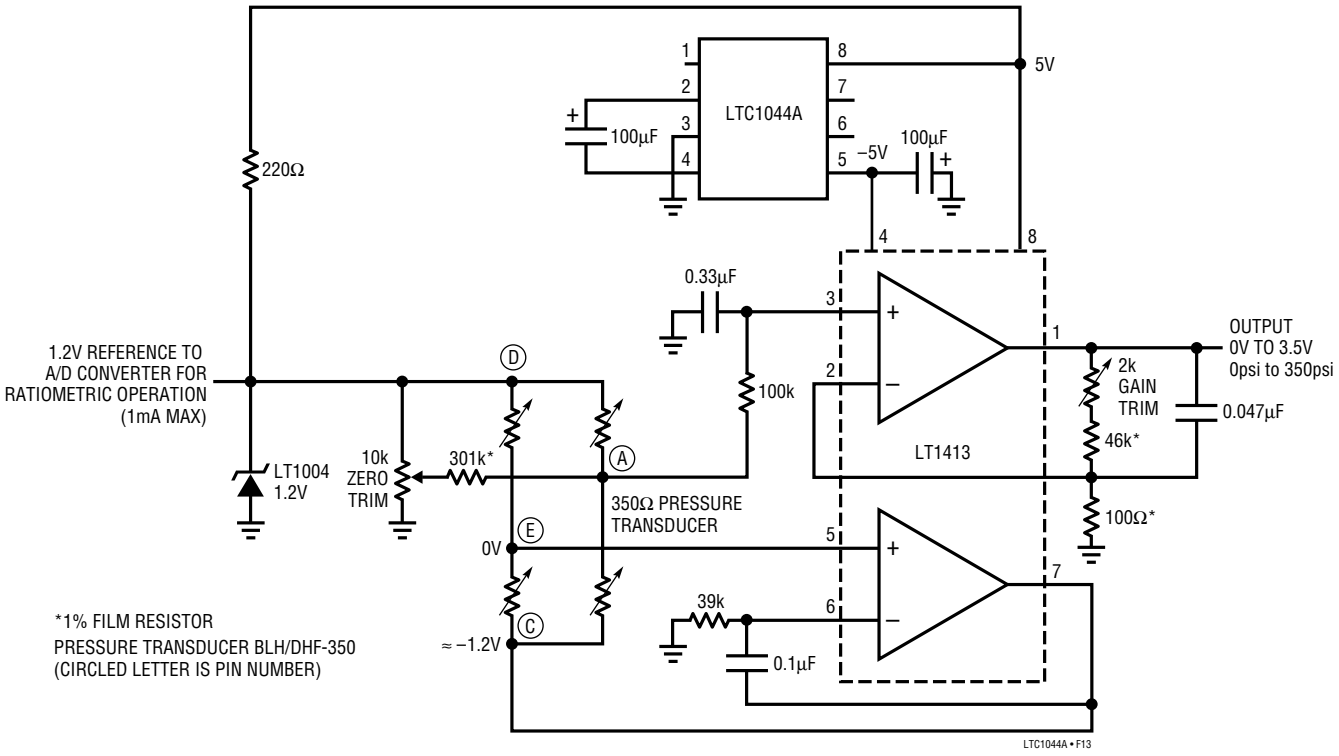
Figure 11. Stacking for Higher Voltage

TYPICAL APPLICATIONS

Low Output Impedance Voltage Converter

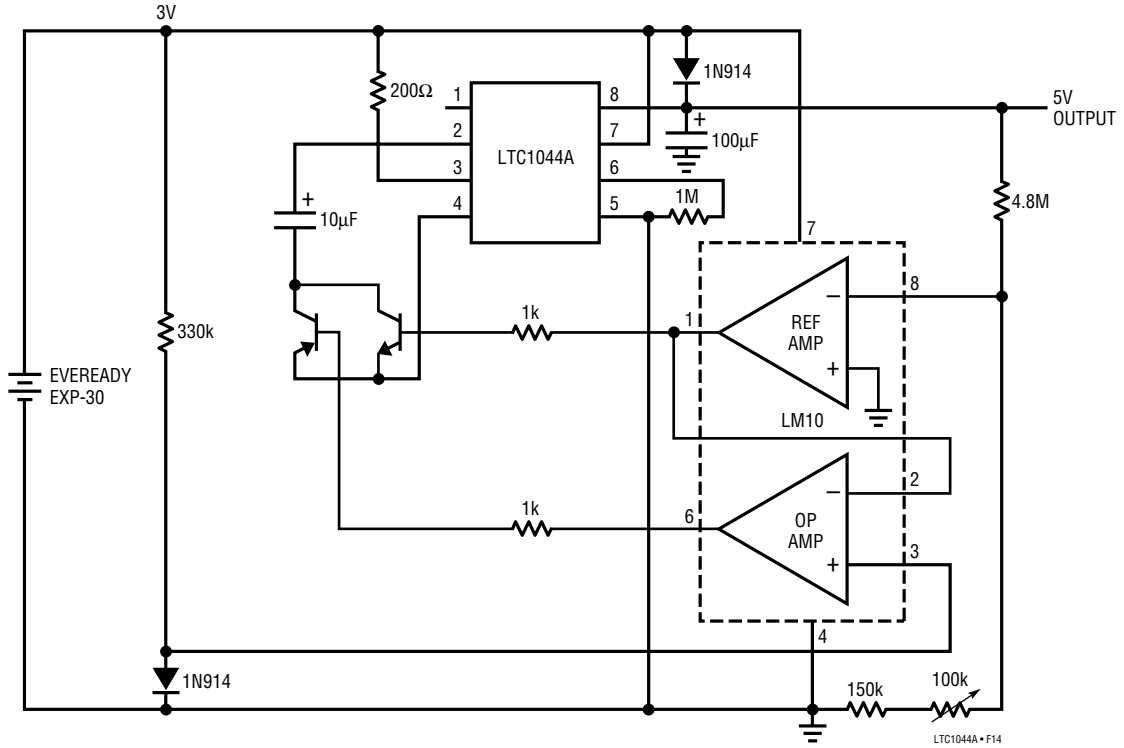


Single 5V Strain Gauge Bridge Signal Conditioner

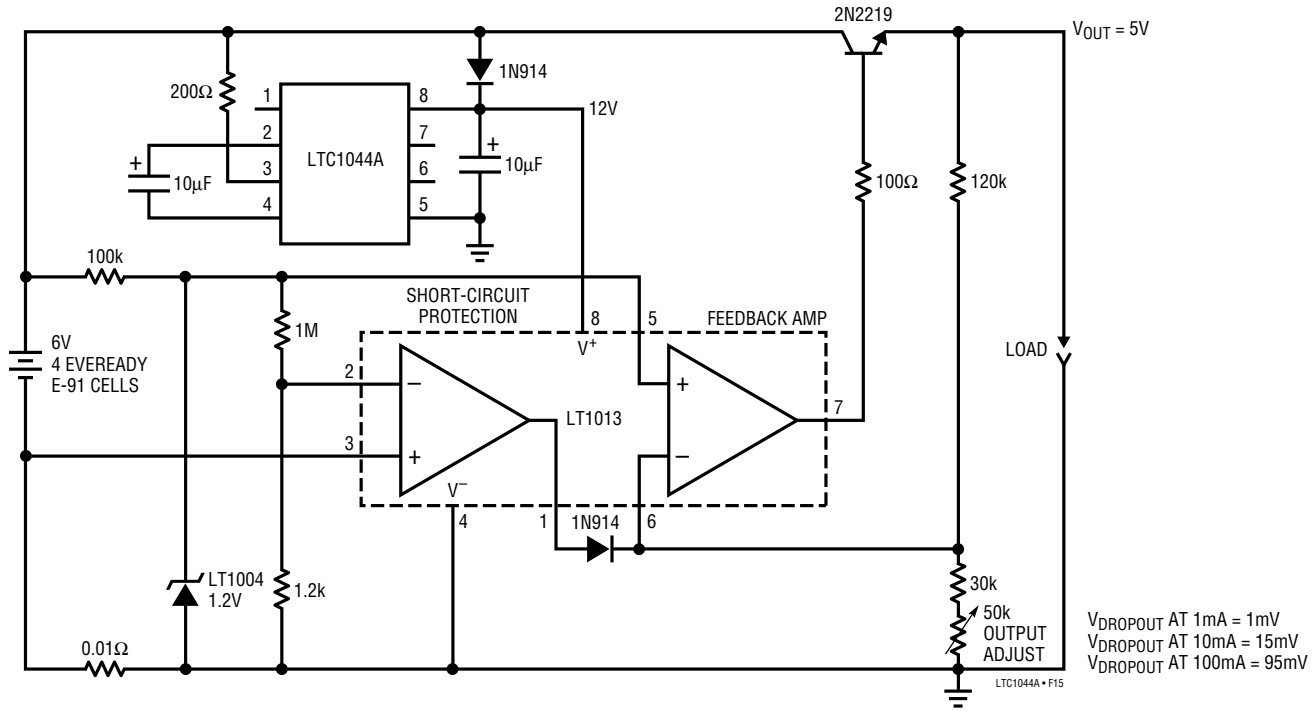


TYPICAL APPLICATIONS

Regulated Output 3V to 5V Converter



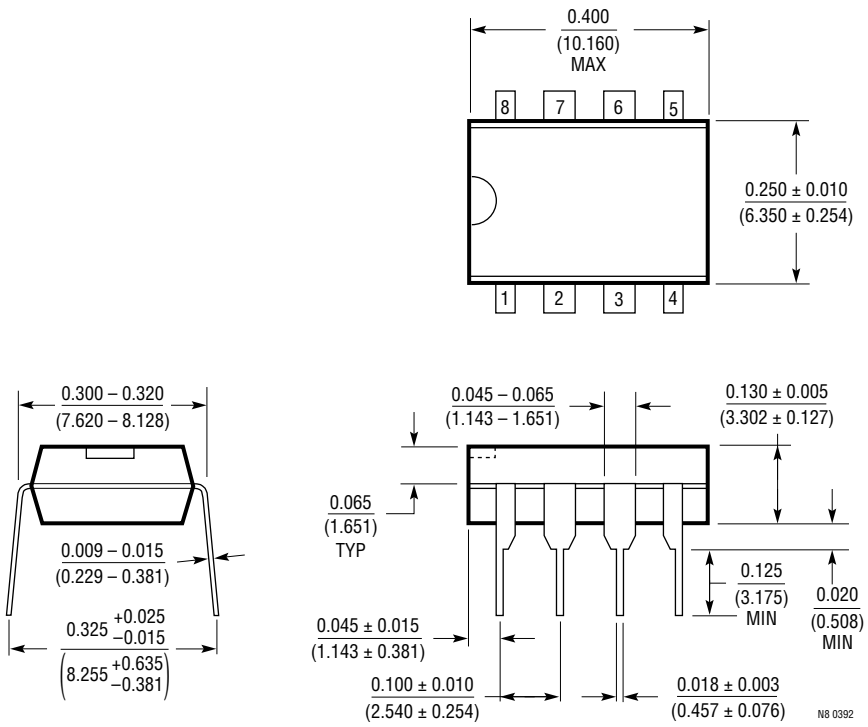
Low Dropout 5V Regulator



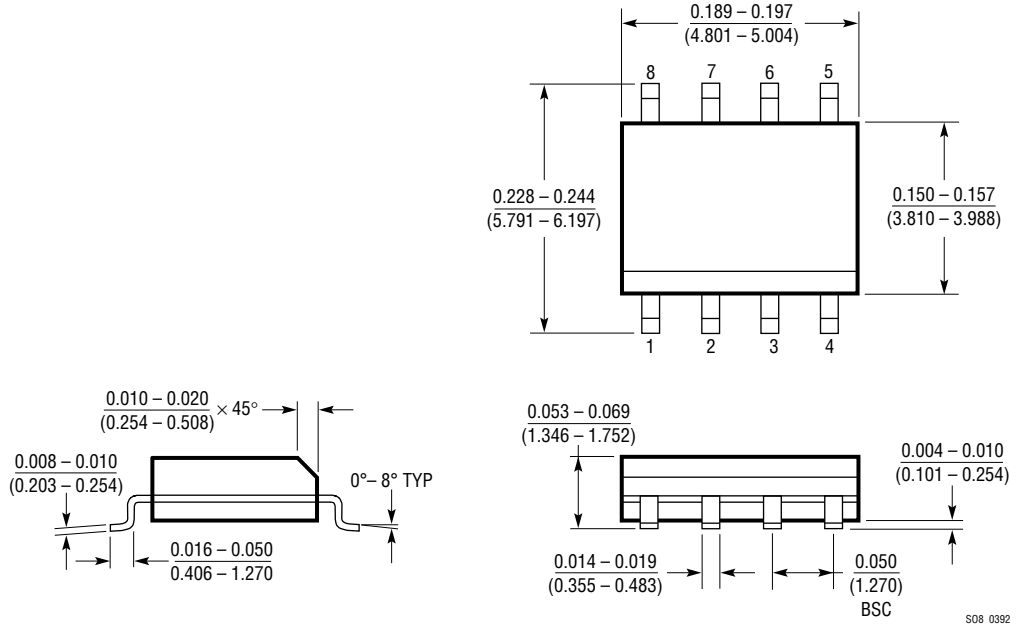
PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead Plastic DIP



S8 Package
8-Lead Plastic SOIC



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08/16/93

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High Efficiency Synchronous Step-Down Switching Regulators

FEATURES

- Operation to 48V Input Voltage
- Ultra High Efficiency: Up to 95%
- Current-Mode Operation for Excellent Line and Load Transient Response
- High Efficiency Maintained Over Wide Current Range
- Logic Controlled Micropower Shutdown
- Short-Circuit Protection
- Very Low Dropout Operation: 100% Duty Cycle
- Synchronous FET Switching for High Efficiency
- Adaptive Non-Overlap Gate Drives
- Available in 16-Pin Narrow SO Package

APPLICATIONS

- Notebook and Palmtop Computers
- Portable Instruments
- Battery-Operated Digital Devices
- Industrial Power Distribution
- Avionics Systems
- Telecom Power Supplies

DESCRIPTION

The LTC1149 series is a family of synchronous step-down switching regulator controllers featuring automatic Burst Mode™ operation to maintain high efficiencies at low output currents. These devices drive external complementary power MOSFETs at switching frequencies up to 250kHz using a constant off-time current-mode architecture.

Special on-board regulation and level-shift circuitry allow operation at input voltages from dropout to 48V (60V absolute max). The constant off-time architecture maintains constant ripple current in the inductor, easing the design of wide input range converters. Current-mode operation provides excellent line and load transient response. The operating current level is user programmable via an external current sense resistor.

The LTC1149 series incorporates automatic power saving Burst Mode™ operation when load currents drop below the level required for continuous operation. Standby power is reduced to only about 8mW at V_{IN} = 12V. In shutdown, both MOSFETs are turned off.

Burst Mode™ is a trademark of Linear Technology Corporation.

TYPICAL APPLICATION

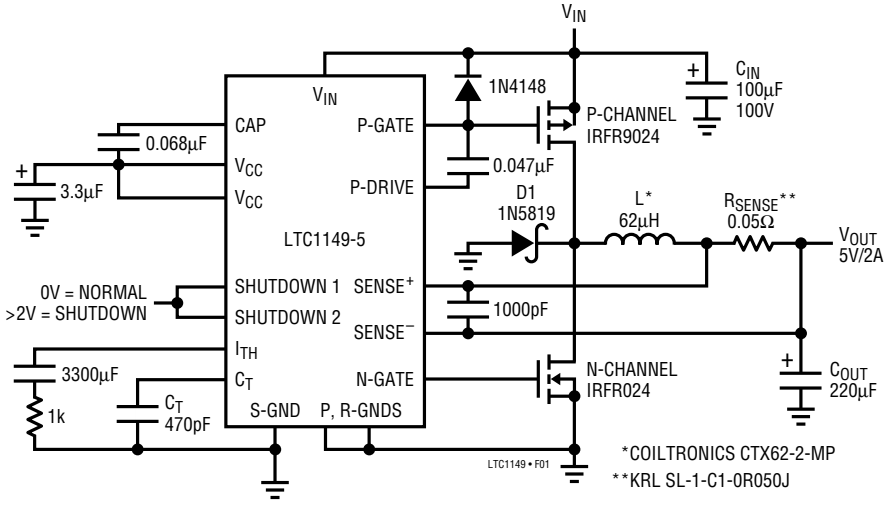
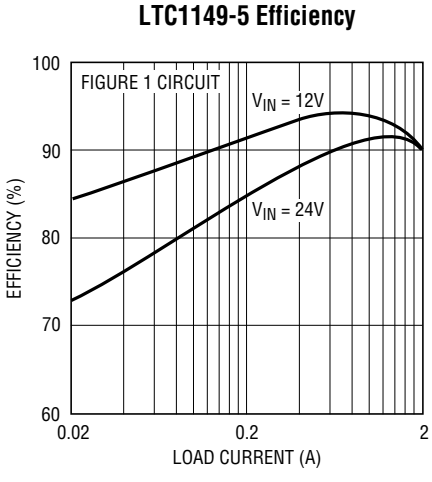


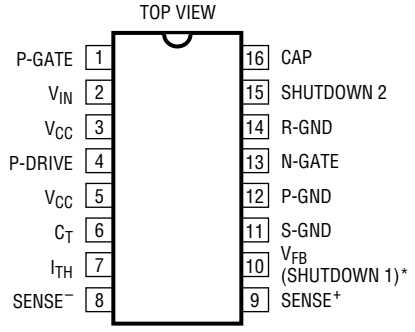
Figure 1. High Efficiency Step-Down Regulator



ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (Pin 2) ..... –15V to 60V
V_{CC} Output Current (Pin 3) 50mA
V_{CC} Input Voltage (Pin 5) 16V
Continuous Output Current (Pins 4, 13) 50mA
Sense Voltages (Pins 8, 9) ..... –0.3V to V_{CC}
Shutdown Voltages (Pins 10, 15) 7V
Operating Temperature Range ..... 0°C to 70°C
Extended Commercial
Temperature Range ..... –40°C to 85°C
Junction Temperature (Note 1) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N PACKAGE
16-LEAD PLASTIC DIP

S PACKAGE
16-LEAD PLASTIC SOIC

*FIXED OUTPUT VERSIONS

T_{JMAX} = 125°C, θ_{JA} = 70°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 110°C/W (S)

ORDER PART NUMBER
LTC1149CN
LTC1149CN-3.3
LTC1149CN-5
LTC1149CS
LTC1149CS-3.3
LTC1149CS-5

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 12V, V_{10} = 0V (Note 2), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{10}	Feedback Voltage (LTC1149 Only)	V_{IN} = 9V	●	1.21	1.25	1.29	V
I_{10}	Feedback Current (LTC1149 Only)		●		0.2	1	µA
V_{OUT}	Regulated Output Voltage LTC1149-3.3 LTC1149-5	V_{IN} = 9V I_{LOAD} = 700mA I_{LOAD} = 700mA	 ● ●	 3.23 4.9	 3.33 5.05	 3.43 5.2	 V V
ΔV_{OUT}	Output Voltage Line Regulation	V_{IN} = 9V to 48V, I_{LOAD} = 700mA		–40	0	40	mV
	Output Voltage Load Regulation LTC1149-3.3 LTC1149-5	 5mA < I_{LOAD} < 2A 5mA < I_{LOAD} < 2A	 ● ●		 40 60	 65 100	 mV mV
	Burst Mode™ Output Ripple	I_{LOAD} = 0A			50		mV_{P-P}
I_2	Input DC Supply Current (Note 3) Normal Mode	 V_{IN} = 12V V_{IN} = 48V			 2.0 2.2	 2.8 3.0	 mA mA
	Burst Mode™	V_{IN} = 12V V_{IN} = 48V			0.6 0.8	0.9 1.1	mA mA
	Shutdown	V_{IN} = 12V, V_{15} = 2V V_{IN} = 48V, V_{15} = 2V			135 300	170 390	µA µA
V_{CC}	Internal Regulator Voltage (Sets MOSFET Gate Drive Levels)	V_{IN} = 12V to 48V I_3 = 20mA	●	9.75	10.25	11	V
$V_2 – V_3$	V_{CC} Dropout Voltage	V_{IN} = 5V, I_3 = 10mA			200	250	mV
$V_{IN} – V_1$	P-Gate to Source Voltage (Off)	V_{IN} = 12V V_{IN} = 48V	● ●	–0.2 –0.2	0 0		V V

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 12V, V_{10} = 0V (Note 2), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_9 - V_8$	Current Sense Threshold Voltage						
	LTC1149	V_8 = 5V, V_{10} = 1.32V (Forced)			25		mV
		V_8 = 5V, V_{10} = 1.1V (Forced)	●	130	150	170	mV
	LTC1149-3.3	V_8 = 3.5V (Forced)			25		mV
		V_8 = 2.9V (Forced)	●	130	150	170	mV
	LTC1149-5	V_8 = 5.3V (Forced)			25		mV
		V_8 = 4.4V (Forced)	●	130	150	170	mV
V_{10}	Shutdown 1 Threshold LTC1149-3.3, LTC1149-5			0.6	0.8	2	V
V_{15}	Shutdown 2 Threshold			0.8	1.4	2	V
I_{15}	Shutdown 2 Input Current	V_{15} = 5V			18	25	µA
I_6	C_T Pin Discharge Current	V_{OUT} In Regulation, V_{SENSE}^- = V_{OUT}		50	70	90	µA
		V_{OUT} = 0V			2	10	µA
t_{OFF}	Off-Time (Note 4)	C_T = 390pF, I_{LOAD} = 700mA	●	4	5	6	µs
t_r, t_f	Driver Output Transition Times	C_L = 3000pF (Pins 4, 13), V_{IN} = 6V			100	200	ns

ELECTRICAL CHARACTERISTICS

–40°C ≤ T_A ≤ 85°C (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{10}	Feedback Voltage LTC1149 Only			1.2	1.25	1.3	V
V_{OUT}	Regulated Output Voltage	V_{IN} = 9V					
	LTC1149-3.3	I_{LOAD} = 700mA		3.17	3.33	3.4	V
	LTC1149-5	I_{LOAD} = 700mA		4.85	5.05	5.2	V
I_2	Input DC Supply Current (Note 3)						
	Normal Mode	V_{IN} = 12V			2.0	3.2	mA
		V_{IN} = 48V			2.2	3.5	mA
	Burst Mode™	V_{IN} = 12V			0.6	1.05	mA
		V_{IN} = 48V			0.8	1.30	mA
	Shutdown	V_{IN} = 12V, V_{15} = 2V			135	230	µA
		V_{IN} = 48V, V_{15} = 2V			300	520	µA
V_{CC}	Internal Regulator Voltage (Sets MOSFET Gate Drive Levels)	V_{IN} = 12V to 48V I_3 = 20mA		9.75	10.25	11	V
$V_9 - V_8$	Current Sense Threshold Voltage	Low Threshold (Forced)			25		mV
		High Threshold (Forced)		125	150	175	mV
V_{15}	Shutdown 2 Threshold			0.8	1.4	2	V
t_{OFF}	Off-Time (Note 4)	C_T = 390pF, I_{LOAD} = 700mA, V_{IN} = 10V		3.8	5	6	µs

The ● denotes specifications which apply over the full operating temperature range.

Note 1: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:
LTC1149CN, LTC1149CN-3.3, LTC1149CN-5: $T_J = T_A + (P_D \times 70°C/W)$
LTC1149CS, LTC1149CS-3.3, LTC1149CS-5: $T_J = T_A + (P_D \times 110°C/W)$

Note 2: Pin 10 is a shutdown pin on the LTC1149-3.3 and LTC1149-5 fixed output voltage versions and must be at ground potential for testing.

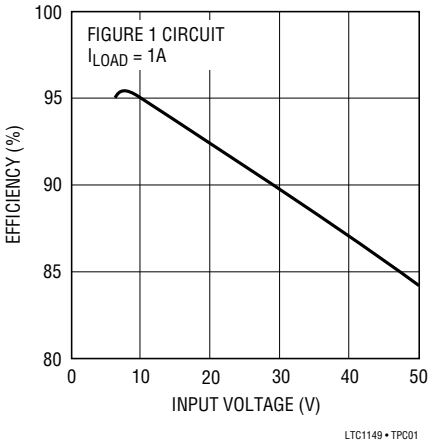
Note 3: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. The allowable operating frequency may be limited by power dissipation at high input voltages. **See Typical Performance Characteristics and Applications Information.**

Note 4: In applications where R_{SENSE} is placed at ground potential, the off-time increases approximately 40%.

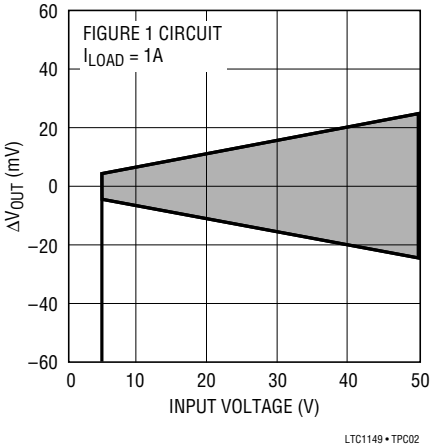
Note 5: The LTC1149, LTC1149-3.3, and LTC1149-5 are not tested and not quality assurance sampled at –40°C and 85°C. These specifications are guaranteed by design and/or correlation.

TYPICAL PERFORMANCE CHARACTERISTICS

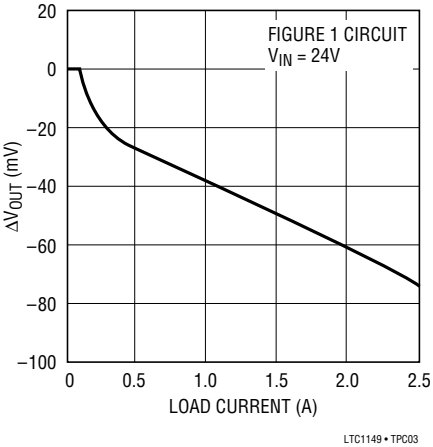
Efficiency vs Input Voltage



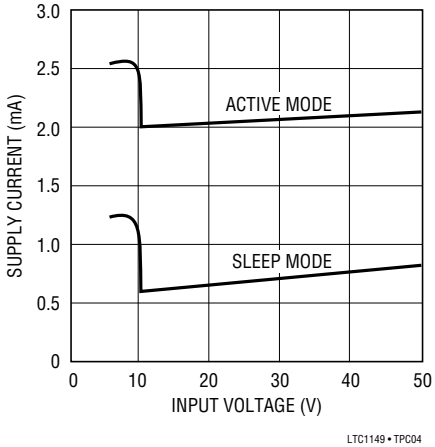
Line Regulation



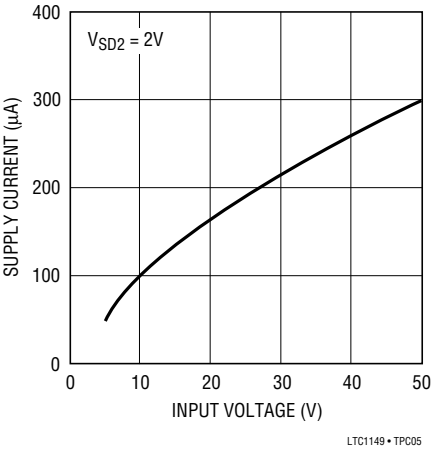
Load Regulation



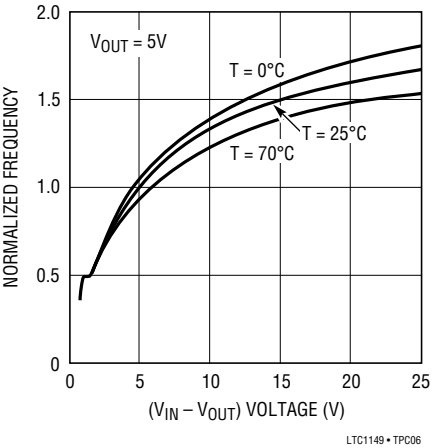
DC Supply Current



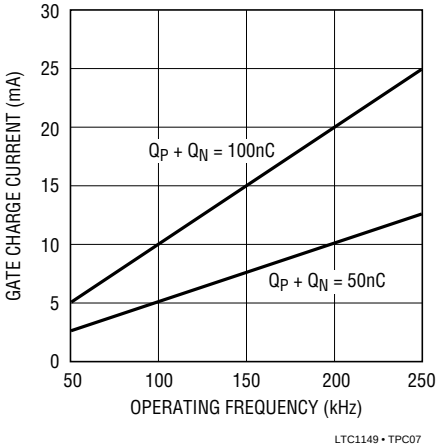
Supply Current in Shutdown



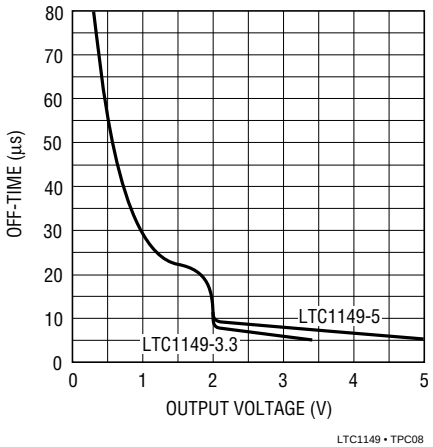
Operating Frequency vs (V_{IN} – V_{OUT})



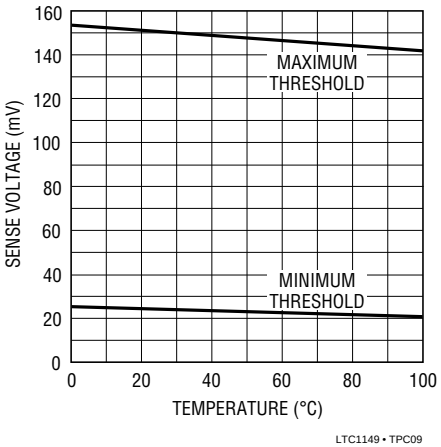
Gate Charge Supply Current



Off-Time vs V_{OUT}



Current Sense Threshold Voltage



PIN FUNCTIONS

Pin 1 (P-Gate): Level-shifted gate drive signal for top P-channel MOSFET. The voltage swing at pin 1 is from V_{IN} to $V_{IN} – V_{CC}$.

Pin 2 (V_{IN}): Main supply input pin.

Pin 3 (V_{CC}): Output pin of low dropout 10V regulator. *Pin 3 is not protected against DC short circuits.*

Pin 4 (P-Drive): High current gate drive for top P-channel MOSFET. The voltage swing at pin 4 is from V_{CC} to ground.

Pin 5 (V_{CC}): Regulated 10V input for driver and control supplies. Must be closely decoupled to power ground.

Pin 6 (C_T): External capacitor C_T from pin 6 to ground sets the operating frequency. (The frequency is also dependent on the ratio V_{OUT}/V_{IN}.)

Pin 7 (I_{TH}): Gain amplifier decoupling point. The current comparator threshold increases with the pin 7 voltage.

Pin 8 (Sense$^–$): Connects to internal resistive divider which sets the output voltage in LTC1149-3.3 and LTC1149-5 versions. Pin 8 is also the (–) input for the current comparator.

Pin 9 (Sense$^+$): The (+) input for the current comparator. A built-in offset between pins 8 and 9 in conjunction with R_{SENSE} sets the current trip threshold.

Pin 10 (Shutdown 1 or V_{FB}): In fixed output voltage versions, pin 10 serves as a shutdown pin for the control circuitry only (V_{CC} is not affected). Taking pin 10 of the LTC1149-3.3 or LTC1149-5 high holds both MOSFETs off. Must be at ground potential for normal operation.

For the LTC1149 adjustable version, pin 10 serves as the feedback pin from an external resistive divider used to set the output voltage.

Pin 11 (Signal Ground): Small signal ground. Must be routed separately from other grounds to the (–) terminal of C_{OUT}.

Pin 12 (Power Ground): Driver power ground. Connects to source of N-channel MOSFET and the (–) terminal of C_{IN}.

Pin 13 (N-Gate): High current drive for bottom N-channel MOSFET. The voltage swing at pin 13 is from ground to V_{CC}.

Pin 14 (Regulator Ground): Low dropout regulator ground. Connects to power ground.

Pin 15 (Shutdown 2): Master shutdown pin. Taking Pin 15 high shuts down V_{CC} and all control circuitry; requires a logic signal with t_r, $t_f < 1\mu s$.

Pin 16 (Cap): Charge compensation pin. A capacitor from pin 16 to V_{CC} provides the charge required by the P-drive level-shift capacitor during supply transitions. *The pin 16 capacitor must be larger than the pin 4 capacitor.*

OPERATION (Refer to Functional Diagram)

The LTC1149 series uses a current mode, constant off-time architecture to synchronously switch an external pair of complementary power MOSFETs. Operating frequency is set by an external capacitor at the timing cap pin 6.

The output voltage is sensed either by an internal voltage divider connected to Sense$^–$ pin 8 (LTC1149-3.3 and LTC1149-5) or an external divider returned to V_{FB} pin 10 (LTC1149). A voltage comparator V, and a gain block G, compare the divided output voltage with a reference voltage of 1.25V. To optimize efficiency, the LTC1149 series automatically switches between two modes of operation, burst and continuous. The voltage comparator is the primary control element for Burst Mode™ operation, while the gain block controls the output voltage in continuous mode.

A low dropout 10V regulator provides the operating voltage V_{CC} for the MOSFET drivers and control circuitry. The driver outputs at pins 4 and 13 are referenced to ground, which fulfills the N-channel MOSFET gate drive requirement. The P-channel gate drive at pin 1 must be referenced to the main supply input V_{IN}, which is accomplished by level-shifting the pin 4 signal via an internal 500k resistor and external capacitor.

During the switch "ON" cycle in continuous mode, current comparator C monitors the voltage between pins 8 and 9 connected across an external shunt in series with the inductor. When the voltage across the shunt reaches its threshold value, the P-gate output is switched to V_{IN}, turning off the P-channel MOSFET. The timing capacitor connected to pin 6 is now allowed to discharge at a rate determined by

OPERATION (Refer to Functional Diagram)

the off-time controller. The discharge current is made proportional to the output voltage (measured by pin 8) to model the inductor current, which decays at a rate which is also proportional to the output voltage. While the timing capacitor is discharging, the N-gate output is high, turning on the N-channel MOSFET.

When the voltage on the timing capacitor has discharged past V_{TH1}, comparator T trips, setting the flip-flop. This causes the N-gate output to go low (turning off the N-channel MOSFET) and the P-gate output to also go low (turning the P-channel MOSFET back on). The cycle then repeats.

As the load current increases, the output voltage decreases slightly. This causes the output of the gain stage to increase the current comparator threshold, thus tracking the load current.

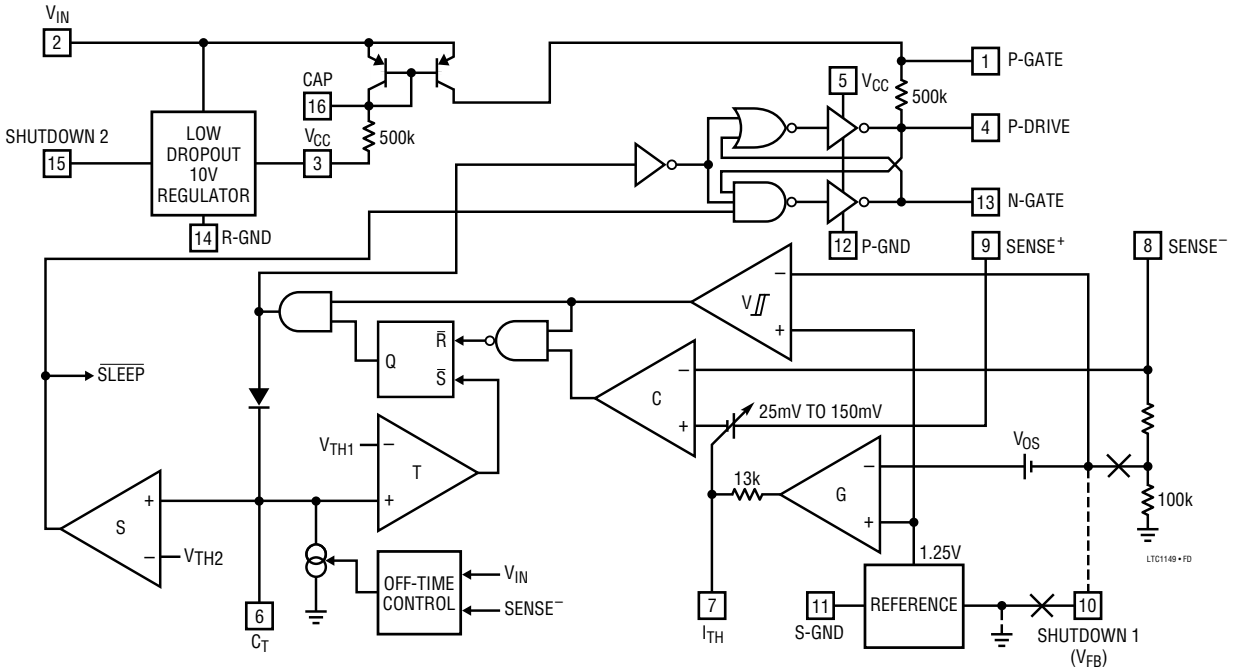
The sequence of events for Burst Mode™ operation is very similar to continuous operation with the cycle interrupted by the voltage comparator. When the output voltage is at or above the desired regulated value, the P-channel MOSFET is held off by comparator V and the timing capacitor continues to discharge below V_{TH1}. When the timing capacitor discharges past V_{TH2}, voltage comparator S trips, causing the internal sleep bar line to go low and the N-channel MOSFET to turn off.

The circuit now enters sleep mode with both power MOSFETs turned off. In sleep mode, much of the circuitry is turned off, dropping the supply current from several mA (with the MOSFETs switching) to 600μA. When the output capacitor has discharged by the amount of hysteresis in comparator V, the P-channel MOSFET is again turned on and this process repeats. To avoid the operation of the current loop interfering with Burst Mode™ operation, a built-in offset is incorporated in the gain stage. This prevents the current comparator threshold from increasing until the output voltage has dropped below a minimum threshold.

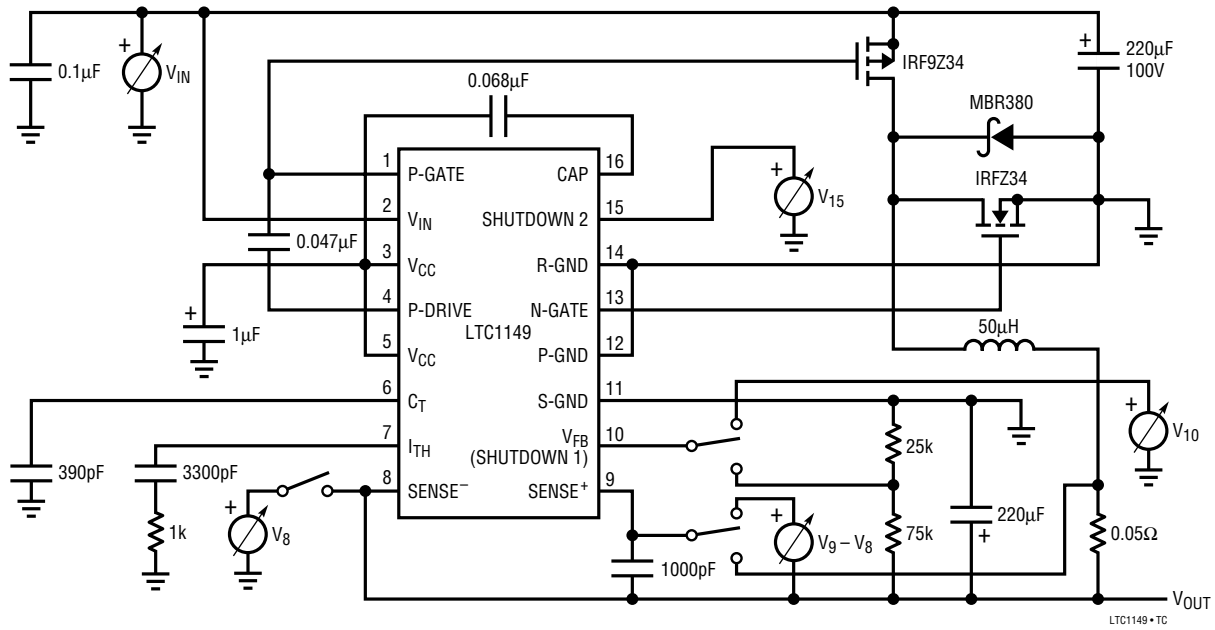
To prevent both the external MOSFETs from ever being turned on at the same time, feedback is incorporated to sense the state of the driver output pins. Before the N-gate output can go high, the P-drive output must also be high. Likewise, the P-drive output is prevented from going low when the N-gate output is high.

Using constant off-time architecture, the operating frequency is a function of the input voltage. To minimize the frequency variation as dropout is approached, the off-time controller increases the discharge current as V_{IN} drops below V_{OUT} + 1.5V. In dropout the P-channel MOSFET is turned on continuously.

FUNCTIONAL DIAGRAM Pin 10 connection shown for LTC1149-3.3 and LTC1149-5; changes create LTC1149.



TEST CIRCUIT



APPLICATIONS INFORMATION

Typical Application Circuit

The basic LTC1149 series application circuit is shown in Figure 1. External component selection is driven by the input voltage and output load requirement, and begins with the selection of R_{SENSE}. Once R_{SENSE} is known, C_T and L can be chosen. Next, the power MOSFETs and D1 are selected. Finally, C_{IN} and C_{OUT} are selected and the loop is compensated. The circuit shown in Figure 1 can be configured for operation up to an input voltage of 48V. If the application does not require greater than 15V operation, then the LTC1148 should be used.

R_{SENSE} Selection for Output Current

R_{SENSE} is chosen based on the required output current. The LTC1149 series current comparator has a threshold range which extends from a minimum of $25mV/R_{SENSE}$ to a maximum of $150mV/R_{SENSE}$. The current comparator threshold sets the peak of the inductor ripple current, yielding a maximum output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current. *For proper Burst Mode™ operation, $I_{RIPPLE(P-P)}$ must be less than or equal to the minimum current comparator threshold.*

Since efficiency generally increases with ripple current, the maximum allowable ripple current is assumed, i.e., $I_{RIPPLE(P-P)} = 25mV/R_{SENSE}$ (see **C_T and L Selection for Operating Frequency**). Solving for R_{SENSE} and allowing a margin for variations in the LTC1149 series and external component values yields:

$$R_{SENSE} = \frac{100mV}{I_{MAX}}$$

A graph for selecting R_{SENSE} versus maximum output current is given in Figure 2. The LTC1149 series works well with values of R_{SENSE} from 0.02Ω to 0.2Ω.

The load current below which Burst Mode™ operation commences, I_{BURST}, and the peak short-circuit current, $I_{SC(PK)}$, both track I_{MAX}. Once R_{SENSE} has been chosen, I_{BURST} and $I_{SC(PK)}$ can be predicted from the following equations:

$$I_{BURST} \approx \frac{15mV}{R_{SENSE}}$$

$$I_{SC(PK)} = \frac{150mV}{R_{SENSE}}$$

APPLICATIONS INFORMATION

The LTC1149 series automatically extends t_{OFF} during a short circuit to allow sufficient time for the inductor current to decay between switch cycles. The resulting ripple current causes the average short-circuit current $I_{SC(AVG)}$ to be reduced to approximately I_{MAX}.

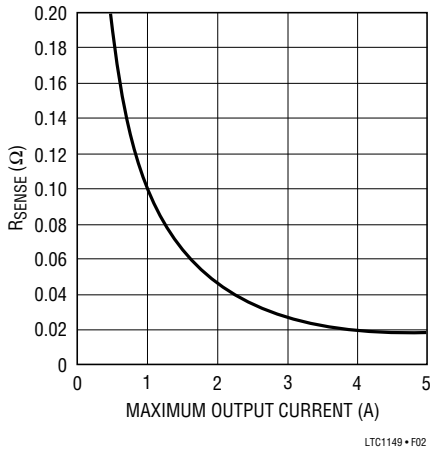


Figure 2. R_{SENSE} vs Maximum Output Current

L and C_T Selection for Operating Frequency

The LTC1149 series uses a constant off-time architecture with t_{OFF} determined by an external timing capacitor C_T. Each time the P-channel MOSFET switch turns on, the voltage on C_T is reset to approximately 3.3V. During the off-time, C_T is discharged by a current which is proportional to V_{OUT}. The voltage on C_T is analogous to the current in inductor L, which likewise decays at a rate proportional to V_{OUT}. Thus the inductor value must track the timing capacitor value.

The value of C_T is calculated from the desired continuous mode operating frequency, f:

$$C_T = \frac{7.8 \times 10^{-5}}{f}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

A graph for selecting C_T versus frequency including the effects of input voltage is given in Figure 3.

As the operating frequency is increased the gate charge losses will be higher, reducing efficiency (see **Efficiency Considerations**). The complete expression for operating frequency is given by:

$$f = \frac{1}{t_{OFF}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where:

$$t_{OFF} = 1.3 \times 10^4 \times C_T \times \left(\frac{V_{REG}}{V_{OUT}}\right)$$

V_{REG} is the desired output voltage (i.e., 5V, 3.3V), while V_{OUT} is the actual output voltage. Thus $V_{REG}/V_{OUT} = 1$ when in regulation.

Note that as V_{IN} decreases, the frequency decreases. When the input to output voltage differential drops below 1.5V, the LTC1149 series reduces t_{OFF} by increasing the discharge current in C_T. This prevents audible operation prior to dropout.

Once the frequency has been set by C_T, the inductor L must be chosen to provide no more than 25mV/R_{SENSE} of peak-to-peak inductor ripple current. This results in a minimum required inductor value of:

$$L_{MIN} = 5.1 \times 10^5 \times R_{SENSE} \times C_T \times V_{REG}$$

As the inductor value is increased from the minimum value, the ESR requirements for the output capacitor are eased at the expense of efficiency. If too small an inductor is used, the inductor current will decrease past zero and change polarity. A consequence of this is that the LTC1149 series may not enter Burst Mode™ operation and efficiency will be severely degraded at low currents.

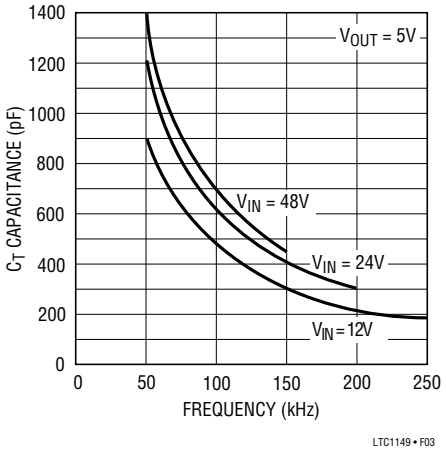


Figure 3. Timing Capacitor Selection

APPLICATIONS INFORMATION

Inductor Core Selection

Once the minimum value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy, or Kool Mμ® cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses increase.

Ferrite designs have very low core loss, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple which can cause Burst Mode™ operation to be falsely triggered in the LTC1149 series. Do not allow the core to saturate!

Molypermalloy (from Magnetics, Inc.) is a very good, low loss core material for toroids, but it is more expensive than ferrite. A reasonable compromise from the same manufacturer is Kool Mμ. Toroids are very space efficient, especially when you can use several layers of wire. Because they generally lack a bobbin, mounting is more difficult. However, new surface mount designs available from Coiltronics do not increase the height significantly.

P-Channel MOSFET Selection

Two external power MOSFETs must be selected for use with the LTC1149 series: a P-channel MOSFET for the main switch, and an N-channel MOSFET for the synchronous switch.

The minimum input voltage determines whether standard threshold or logic-level threshold MOSFETs must be used. For V_{IN} > 8V, standard threshold MOSFETs ($V_{GS(TH)}$ < 4V) may be used. If V_{IN} is expected to drop below 8V, logic-level threshold MOSFETs ($V_{GS(TH)}$ < 2.5V) are strongly recommended. When logic-level MOSFETs are used, the absolute maximum V_{GS} rating for the MOSFETs must be greater than the LTC1149 series internal regulator voltage V_{CC}.

Selection criteria for the P-channel MOSFET include the on- resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS}, input voltage, and maximum output current. When the LTC1149 is operating in continuous mode, the duty cycle for the P-channel MOSFET is given by:

$$\text{P-Ch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

The P-channel MOSFET dissipation at maximum output current is given by:

$$\text{P-Ch } P_D = \frac{V_{OUT}}{V_{IN}} (I_{MAX})^2 (1 + \partial_P) R_{DS(ON)} + k (V_{IN})^2 (I_{MAX}) (C_{RSS}) (f)$$

where ∂ is the temperature dependency of $R_{DS(ON)}$ and k is a constant related to the gate drive current. Note the two distinct terms in the equation. The first gives the I^2R losses, which are highest at low input voltages, while the second gives the transition losses, which are highest at high input voltages. For V_{IN} < 24V, the high current efficiency generally improves with larger MOSFETs (although gate charge losses begin eating into the gains. See **Efficiency Considerations**). For V_{IN} > 24V, the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{RSS} actually provides higher efficiency. This is illustrated in the **Design Example** section.

The term (1 + ∂) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but ∂ = 0.007/°C can be used as an approximation for low voltage MOSFETs. C_{RSS} is usually specified in the MOSFET electrical characteristics. The constant k is much harder to pin down, but k = 5 can be used for the LTC1149 series to estimate the relative contributions of the two terms in the P-channel dissipation equation.

N-Channel MOSFET and D1 Selection

The same input voltage constraints apply to the N-channel MOSFET as to the P-channel with regard to when logic-

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APPLICATIONS INFORMATION

level devices are required. However, the dissipation calculation is quite different. The duty cycle and dissipation for the N-channel MOSFET operating in continuous mode are given by:

$$\text{N-Ch Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

$$\text{N-Ch } P_D = \frac{V_{IN} - V_{OUT}}{V_{IN}} (I_{MAX})^2 (1 + \partial_N) R_{DS(ON)}$$

where ∂ is the temperature dependency of $R_{DS(ON)}$. Note that there is no transition loss term in the N-channel dissipation equation because the drain-to-source voltage is always low when the N-channel MOSFET is turning on or off. The remaining I^2R losses are the greatest at high input voltage or during a short circuit, when the N-channel duty cycle is nearly 100%. Fortunately, low $R_{DS(ON)}$ N-channel MOSFETs are readily available which reduce losses to the point that heat sinking is not required, even during continuous short-circuit operation.

The Schottky diode D1 shown in Figure 1 only conducts during the dead-time between the conduction of the two power MOSFETs. D1's sole purpose in life is to prevent the body diode of the N-channel MOSFET from turning on and storing charge during the dead-time, which could cost as much as 1% in efficiency (although there are no other harmful effects if D1 is omitted). Therefore, D1 should be selected for a forward voltage of less than 0.7V when conducting I_{MAX}.

Finally, both MOSFETs and D1 must be selected for breakdown voltages higher than the maximum V_{IN}.

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the P-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ Required } I_{RMS} \approx \frac{I_{MAX} [V_{OUT}(V_{IN} - V_{OUT})]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{MAX}/2$. This simple worst case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. An additional 0.1µF ceramic capacitor may also be required on V_{IN} for high frequency decoupling.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). The ESR of C_{OUT} must be less than twice the value of R_{SENSE} for proper operation of the LTC1149 series:

$$C_{OUT} \text{ Required ESR} < 2R_{SENSE}$$

Optimum efficiency is obtained by making the ESR equal to R_{SENSE}. As the ESR is increased up to $2R_{SENSE}$, the efficiency degrades by less than 1%. If the ESR is greater than $2R_{SENSE}$, the voltage ripple on the output capacitor will prematurely trigger Burst Mode™ operation, resulting in disruption of continuous mode and an efficiency hit which can be several percent.

Manufacturers such as Nichicon, Chemicon, and Sprague should be considered for high performance capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR for its size, at a somewhat higher price. Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement.

In surface mount applications multiple capacitors may have to be paralleled to meet the capacitance, ESR, or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. For example, if 200µF/10V is called for in an application requiring 3mm height, two AVX 100µF/10V (P/N TPSD 107K010) could be used. Consult the manufacturer for other specific recommendations.

APPLICATIONS INFORMATION

At low supply voltages, a minimum value of C_{OUT} is suggested to prevent an abnormal low frequency operating mode (see Figure 4). When C_{OUT} is too small, the output ripple at low frequencies will be large enough to trip the voltage comparator. This causes the Burst Mode™ operation to be activated when the LTC1149 series would normally be in continuous operation. The effect is most pronounced with low values of R_{SENSE} and can be improved by operating at higher frequencies with lower values of L. The output remains in regulation at all times.

Checking Transient Response

Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to $\Delta I_{LOAD} \times ESR$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} until the regulator loop adapts to the current change and returns V_{OUT} to its steady state value. During this recovery time V_{OUT} can be monitored for overshoot or ringing which would indicate a stability problem. The pin 7 external components shown in the Figure 1 circuit will prove adequate compensation for most applications.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately $25 \times C_{LOAD}$. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

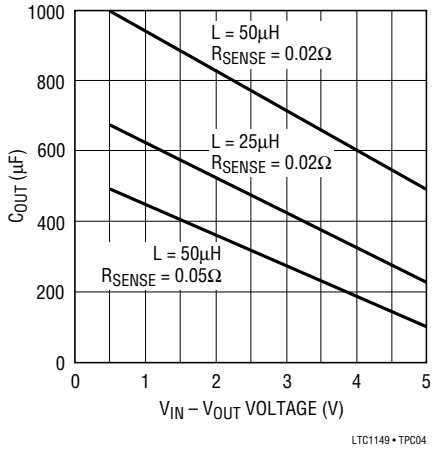


Figure 4. Minimum Suggested C_{OUT}

LTC1149 Adjustable Applications

When an output voltage other than 3.3V or 5V is required, the LTC1149 adjustable version is used with an external resistive divider from V_{OUT} to V_{FB} pin 10. The regulated voltage is determined:

$$V_{OUT} = 1.25\left(1 + \frac{R2}{R1}\right)$$

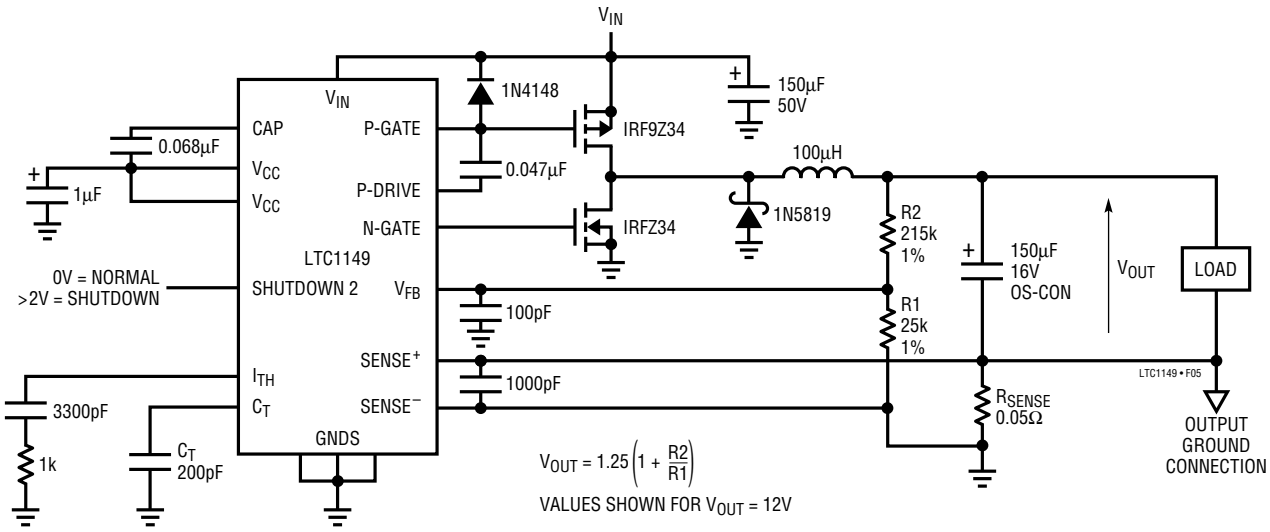


Figure 5. High Efficiency Step-Down Regulator with $V_{OUT} > V_{CC}$

APPLICATIONS INFORMATION

In applications where V_{OUT} is greater than the LTC1149 internally regulated V_{CC} voltage, R_{SENSE} must be moved to the ground side of the output to prevent the absolute maximum voltage ratings of the sense pins from being exceeded. This is shown in Figure 5. When the current sense comparator is operating at 0V common mode, the off-time increases approximately 40%, requiring the use of a smaller timing capacitor C_T.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\%\text{Efficiency} = 100 - (L1 + L2 + L3 + ...)$$

where L1, L2, etc., are the individual losses as a percentage of input power. (For high efficiency circuits only small errors are incurred by expressing losses as a percentage of output power.)

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC1149 series circuits: 1) LTC1149 DC supply current, 2) MOSFET gate charge current, 3) I^2R losses, and 4) P-channel transition losses.

1) The DC supply current is the current which flows into V_{IN} pin 2 less the gate charge current. For V_{IN} = 12V the LTC1149 DC supply current is 0.6mA for no load, and increases proportionally with load up to 2mA after the LTC1149 series has entered continuous mode. Because the DC supply current is drawn from V_{IN}, the resulting loss increases with input voltage. For V_{IN} = 24V, the DC bias losses are generally less than 3% for load currents over 300mA. However, at very low load currents the DC bias current accounts for nearly all of the loss.

2) MOSFET gate charge current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of V_{IN} which is typically much larger than the DC supply current. In continuous mode, $I_{GATECHG} = f (Q_N + Q_P)$. The typical gate charge for a 0.1Ω N-channel power MOSFET is 25nC, and for a P-channel about twice that value. This results in $I_{GATECHG}$ = 7.5mA in 100kHz continuous operation, for a 5% to 10% typical mid-current loss with V_{IN} = 24V.

Note that the gate charge loss increases directly with both input voltage and operating frequency. This is the principal reason why the highest efficiency circuits operate at moderate frequencies. Furthermore, it argues against using larger MOSFETs than necessary to control I^2R losses, since overkill can cost efficiency as well as money!

3) I^2R losses are easily predicted from the DC resistances of the MOSFET, inductor, and current shunt. In continuous mode all of the output current flows through L and R_{SENSE}, but is "chopped" between the P-channel and N-channel MOSFETs. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and R_{SENSE} to obtain I^2R losses. For example, if each $R_{DS(ON)}$ = 0.1Ω, R_L = 0.15Ω, and R_{SENSE} = 0.05Ω, then the total resistance is 0.3Ω. This results in losses ranging from 3% to 12% as the output current increases from 0.5A to 2A. I^2R losses cause the efficiency to roll-off at high output currents.

4) Transition losses apply only to the P-channel MOSFET, and only when operating at high input voltages (typically 24V or greater). Transition losses can be estimated from:

$$\text{Transition Loss} \approx 5(V_{IN})^2 (I_{MAX}) (C_{RSS}) (f)$$

For example, if V_{IN} = 48V, I_{MAX} = 2A, C_{RSS} = 300pF (a very large MOSFET), and f = 100kHz, the transition loss is 0.7W. A loss of this magnitude would not only kill efficiency but would probably require additional heat sinking for the MOSFET! See **Design Example** for further guidelines on how to select the P-channel MOSFET.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses, Schottky conduction losses during dead-time, and inductor core losses, generally account for less than 2% total additional loss.

LTC1149 Package Dissipation

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maxi-

APPLICATIONS INFORMATION

mum junction temperature rating for the LTC1149 series to be exceeded. The LTC1149 supply current is dominated by the gate charge supply current, which is given as a function of operating frequency in the Typical Performance Characteristics. The LTC1149 series junction temperature can be estimated by using the equations given in Note 1 of the Electrical Characteristics. For example, the LT1149CS is limited to less than 11mA from a 48V supply:

$T_J = 70°C + (11mA \times 48V \times 110°C/W)$
$= 128°C$ exceeds absolute maximum

To prevent the maximum junction temperature from being exceeded, the pin 2 supply current must be checked in continuous mode when operating at the maximum V_{IN}.

Design Example

As a design example, assume V_{IN} = 24V, V_{OUT} = 5V, I_{MAX} = 2.5A, and f = 100kHz. R_{SENSE}, C_T and L can immediately be calculated:

$$R_{SENSE} = \frac{100mV}{2.5} = 0.039\Omega$$

$$C_T = \frac{7.8 \times 10^{-5}}{100kHz}\left(1 - \frac{5V}{24V}\right) = 620pF$$

$$L_{MIN} = 5.1 \times 10^5 \times 0.039\Omega \times 620pF \times 5V = 62\mu H$$

Selection of the P-channel MOSFET involves doing calculations for different sized MOSFETs to determine the relative loss contributions. Taking an International Rectifier IRF9Z34 for example, $R_{DS(ON)}$ = 0.14Ω Max, Q_P = 35nC, and C_{RSS} = 200pF ($V_{DS} = V_{IN}/2$). These values can be used to estimate the I^2R losses, transition losses, and gate charge supply current losses:

Est. I^2R Loss (T_J = 100°C) =
$(5V/24V)\ (2.5)^2\ (1 + 0.5)0.14\Omega$ = 270mW

Est. Transition Loss =
$5\ (24V)^2\ (2.5A)\ (200pF)\ (100kHz)$ = 145mW

Est. Gate Charge Loss =
(100kHz) (35nC) (24V) = 85mW

The same calculations were repeated for a smaller device, the Motorola MTD2955 ($R_{DS(ON)}$ = 0.3Ω), and a larger one, the Harris RFP30P05 ($R_{DS(ON)}$ = 0.065Ω). The results are summarized in the table.

CONDITIONS V_{IN} = 24V, V_{OUT} = 5V F = 100kHz, I_{OUT} = 2.5A	P-CHANNEL MOSFET		
	MTD2955	IRF9Z34	RFP30P05
Est. I^2R Loss (100°C)	550mW	270mW	120mW
Est. Transition Loss	110mW	145mW	290mW
Est. Gate Charge Loss	60mW	85mW	240mW
Est. Total Loss	720mW	500mW	650mW

For this set of conditions, the mid-sized P-channel MOSFET actually produces the lowest total losses at I_{MAX}. The resulting efficiency differences will be even more pronounced at lower output currents. Note that only the I^2R and transition losses are dissipated in the MOSFET; the gate charge supply current loss is dissipated by the LTC1149 series.

Selection of the N-channel MOSFET is somewhat easier; it need only be sized for the anticipated I^2R losses at 100% duty cycle (worst case assumption for short circuit.) The Siliconix Si9410, for example, has $R_{DS(ON)}$ = 0.03Ω Max and Q_N = 30nC. This will produce an I^2R loss of 250mW at 100°C and a gate charge supply current loss of 75mW. As with the P-channel device, the use of a larger MOSFET may actually result in lower mid-current efficiency

C_{IN} will require an RMS current rating of at least 1.25A at temperature, and C_{OUT} will require an ESR of 0.04Ω for optimum efficiency. The output capacitor ESR requirement can be fulfilled by a single OS-CON or by two or more surface mount tantalums in parallel.

Auxiliary Windings – Suppressing Burst Mode™ Operation

The LTC1149 synchronous switch removes the normal limitation that power must be drawn from the inductor primary winding in order to extract power from auxiliary windings. With synchronous switching, auxiliary outputs may be loaded without regard to the primary output load, providing that the loop remains in continuous mode operation.

Burst Mode™ operation can be suppressed at low output currents with a simple external network which cancels the

APPLICATIONS INFORMATION

25mV minimum current comparator threshold. This technique is also useful for eliminating audible noise from certain types of inductors in high current (I_{OUT} > 5A) applications when they are lightly loaded.

An external offset is put in series with the Sense$^-$ pin to subtract from the built-in 25mV offset. An example of this technique is shown in Figure 6. Two 100Ω resistors are inserted in series with the leads from the sense resistor.

With the addition of R3, a current is generated through R1 causing an offset of:

$$V_{OFFSET} = V_{OUT} \times \left(\frac{R1}{R1 + R3}\right)$$

If V_{OFFSET} > 25mV, the minimum threshold will be cancelled and Burst Mode™ operation is prevented from occurring. Since V_{OFFSET} is constant, the maximum load current is also decreased by the same offset. Thus, to get back to the same I_{MAX}, the value of the sense resistor must be lower:

$$R_{SENSE} \approx \frac{75mV}{I_{MAX}}$$

To prevent noise spikes from erroneously tripping the current comparator, a 1000pF capacitor is needed across pins 8 and 9.

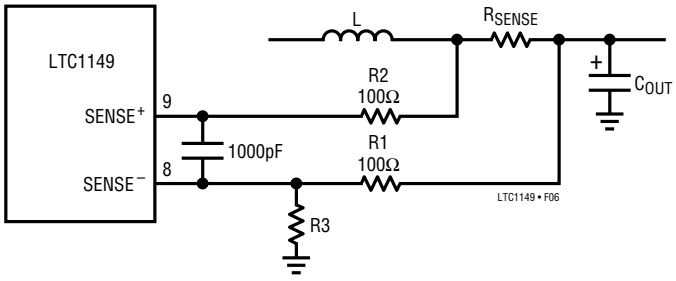


Figure 6. Suppressing Burst Mode™ Operation

Output Crowbar

An added feature to using an N-channel MOSFET as the synchronous switch is the ability to crowbar the output with the same MOSFET. Pulling the timing cap pin 6 above 1.5V when the output voltage is greater than the desired regulated value, will turn on the N-channel MOSFET.

A fault condition which causes the output voltage to go above a maximum value can be detected by external circuitry. Turning on the N-channel MOSFET when this fault is detected will then force the system fuse to blow.

The N-channel MOSFET needs to be sized so it will safely handle this over current condition. The typical delay from pulling the C_T pin 6 high to when the N-gate pin 13 goes high is 250ns. *Under shutdown conditions, the N-channel is held off and pulling pin 6 high will not cause the output to be crowbarred.*

A small N-channel FET can be used as an interface between the overvoltage detect circuitry and the LTC1149 as shown in Figure 7.

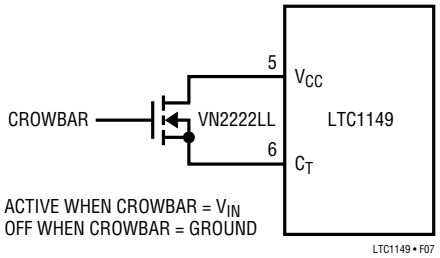


Figure 7. Output Crowbar Interface

Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1149 series. These items are also illustrated graphically in the layout diagram of Figure 8. Check the following in your layout:

1) Are the signal and power grounds segregated? The LTC1149 signal ground pin 11 must connect separately to the (–) plate of C_{OUT}. The other ground pins 12 and 14 should return to the source of the N-channel MOSFET, anode of the Schottky diode, and (–) plate of C_{IN}, which should have as short lead lengths as possible.

2) Does the LTC1149 Sense$^-$ pin 8 connect to a point close to R_{SENSE} and the (+) plate of C_{OUT}? In adjustable applications, the resistive divider R1, R2 must be connected between the (+) plate of C_{OUT} and signal ground.

3) Are the Sense$^-$ and Sense$^+$ leads routed together with minimum PC trace spacing? The differential decoupling capacitor between pins 8 and 9 should be as close as possible to the LTC1149. Up to 100Ω may be placed in series with each sense lead to help decouple pins 8

APPLICATIONS INFORMATION

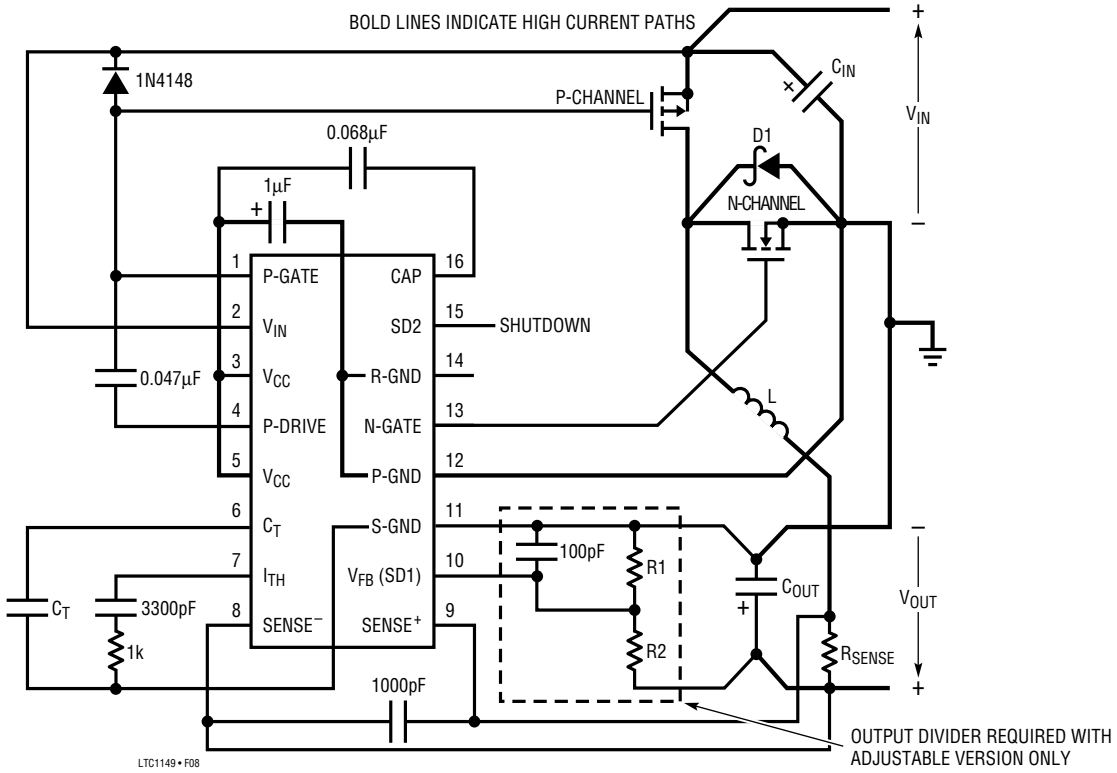


Figure 8. LTC1149 Series Layout Diagram (see Layout Checklist)

and 9. However, when these resistors are used, the capacitor should be no larger than 1000pF.

4) Does the (+) plate of C_{IN} connect to the source of the P-channel MOSFET as closely as possible? An additional 0.1µF ceramic capacitor between V_{IN} and power ground may be required in some applications.

5) Is the V_{CC} decoupling capacitor connected closely between pin 5 of the LTC1149 and power ground? This capacitor carries the MOSFET driver peak currents.

6) Is the shutdown 1 pin 10 (fixed output versions only) actively pulled to ground during normal operation? The shutdown 1 pin is high impedance and must not be allowed to float. In adjustable versions, pin 10 is the feedback pin and is very sensitive to pickup from the switch node. Care must be taken to isolate V_{FB} from possible capacitive coupling of the inductor switch signal.

Troubleshooting Hints

Since efficiency is critical to LTC1149 series applications, it is very important to verify that the circuit is functioning correctly in both continuous and Burst Mode™ operation. The waveform to monitor is the voltage on the timing capacitor pin 6.

In continuous mode ($I_{LOAD} > I_{BURST}$) the voltage on pin 6 should be a sawtooth with a $0.9V_{P-P}$ swing. This voltage should never dip below 2V as shown in Figure 9a.

When load currents are low ($I_{LOAD} < I_{BURST}$) Burst Mode™ operation should occur with the C_T pin waveform periodically falling to ground as shown in Figure 9b.

If pin 6 is observed falling to ground at high output currents, it indicates poor decoupling or improper grounding. Refer to the **Board Layout Checklist**.

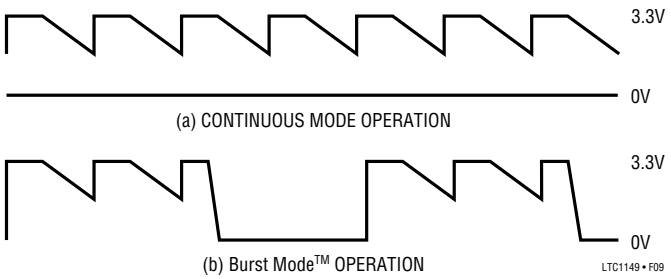


Figure 9. C_T Pin 6 Waveforms

TYPICAL APPLICATIONS

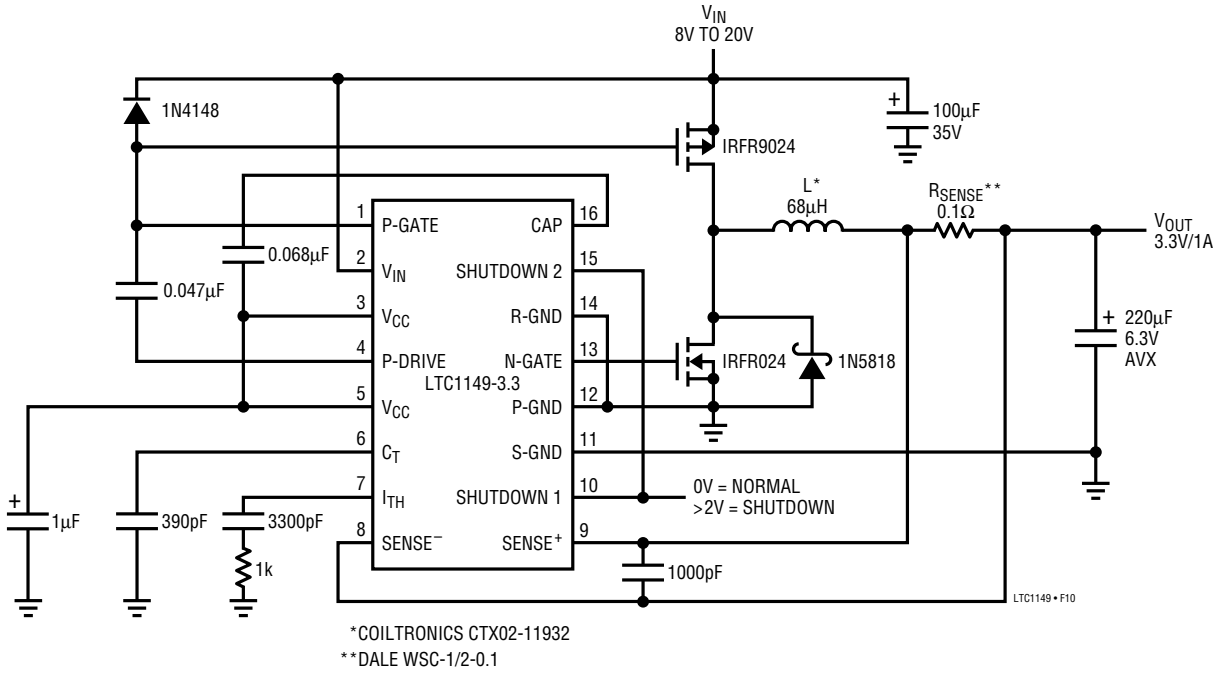


Figure 10. High Efficiency 8V to 20V Input 3.3V/1A Output Regulator

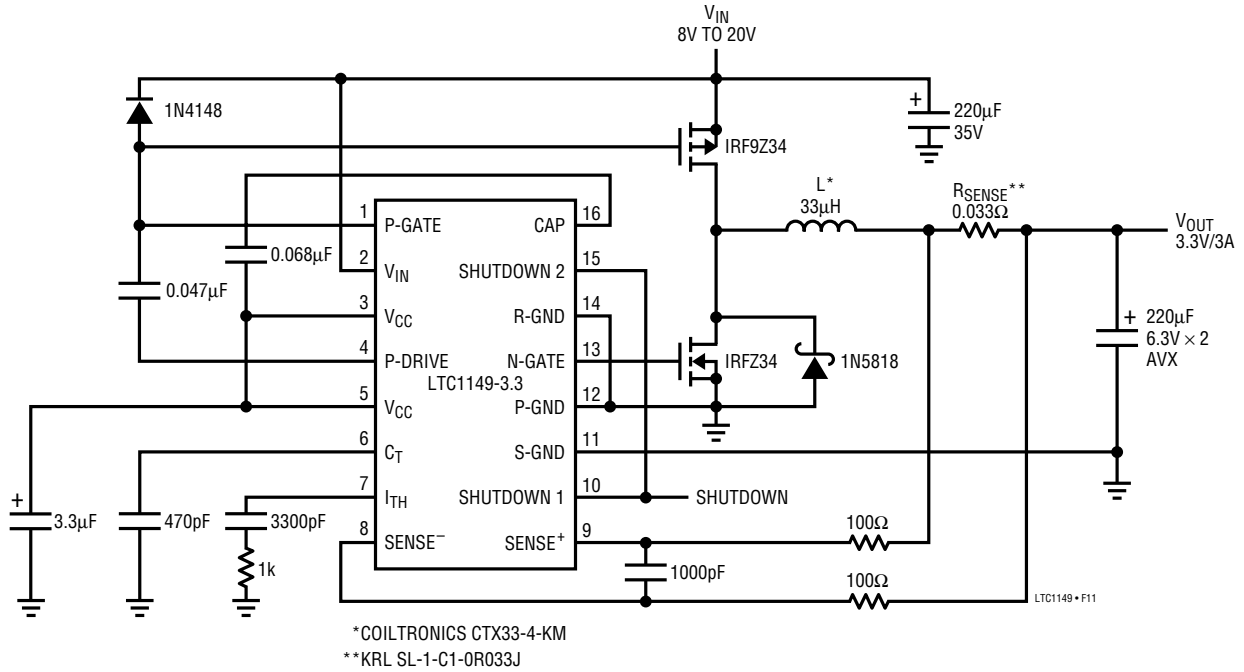


Figure 11. High Efficiency 8V to 20V Input 3.3V/3A Output Regulator

TYPICAL APPLICATIONS

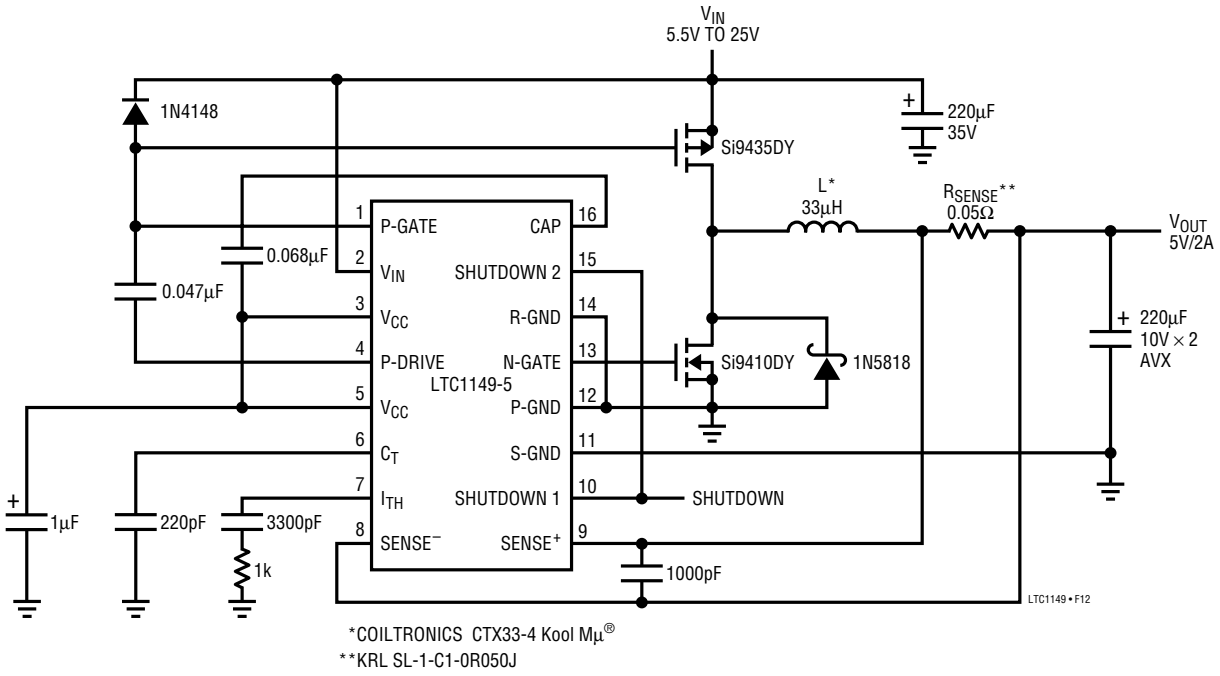


Figure 12. Ultra Wide Input Range (5.5V to 25V) High Efficiency 5V Regulator

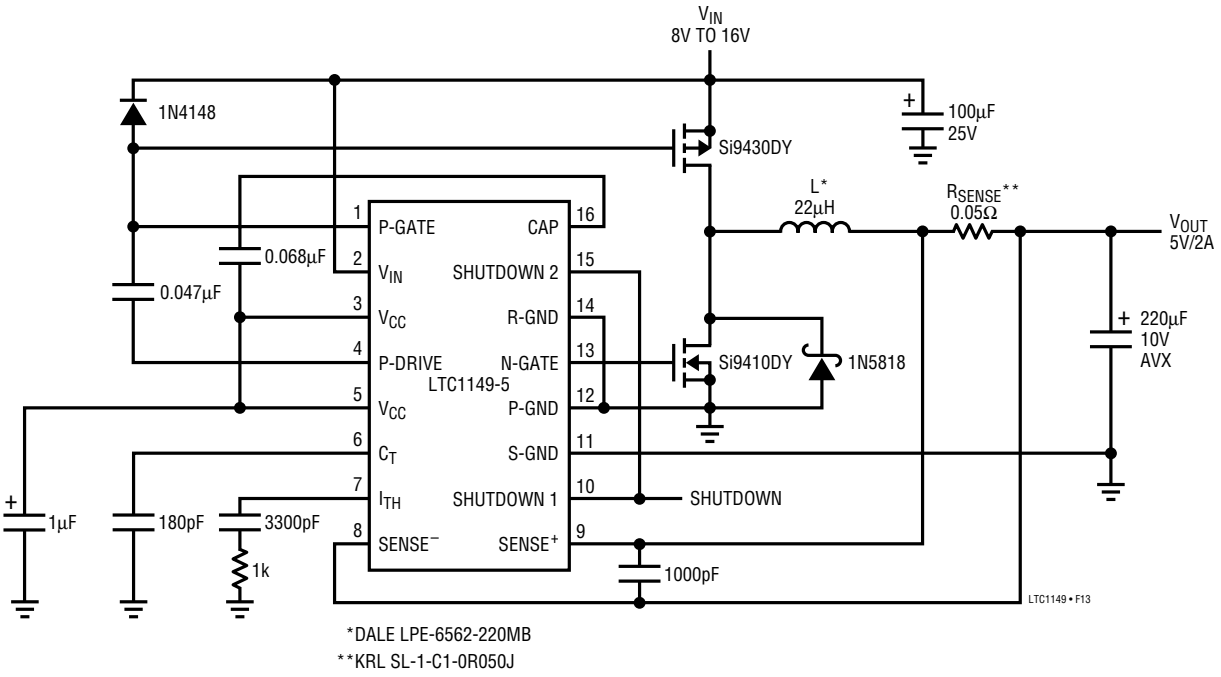


Figure 13. 250kHz High Efficiency 12V Input 5V/2A Output Regulator

TYPICAL APPLICATIONS

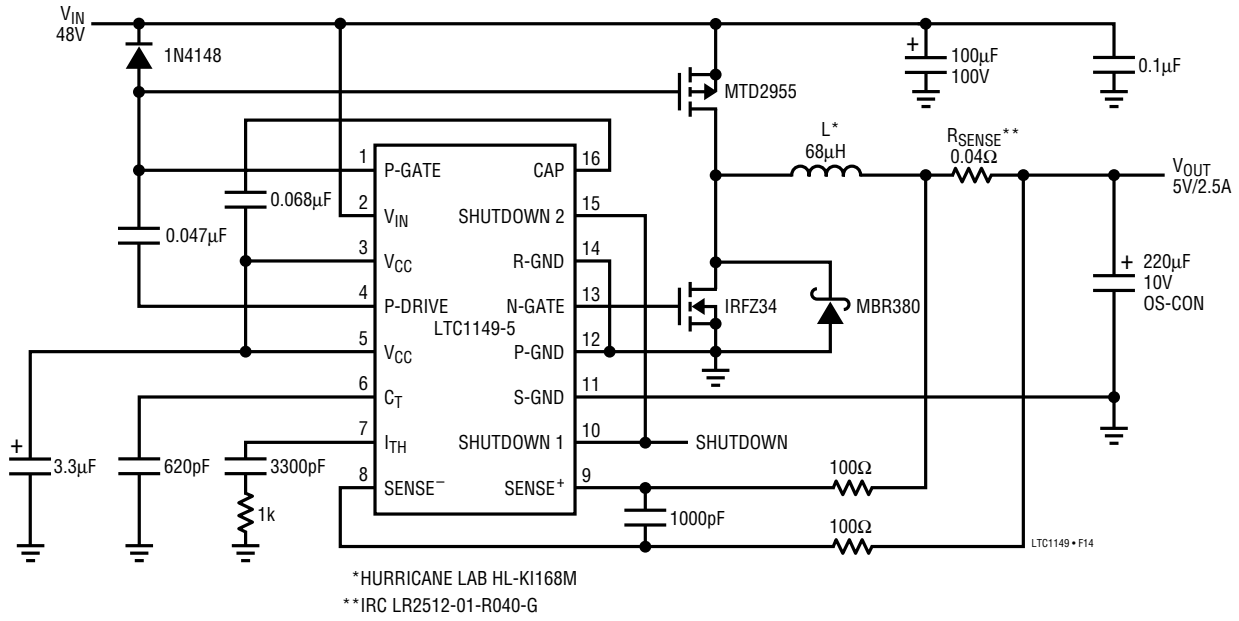


Figure 14. High Efficiency 48V Input 5V/2.5A Output Regulator

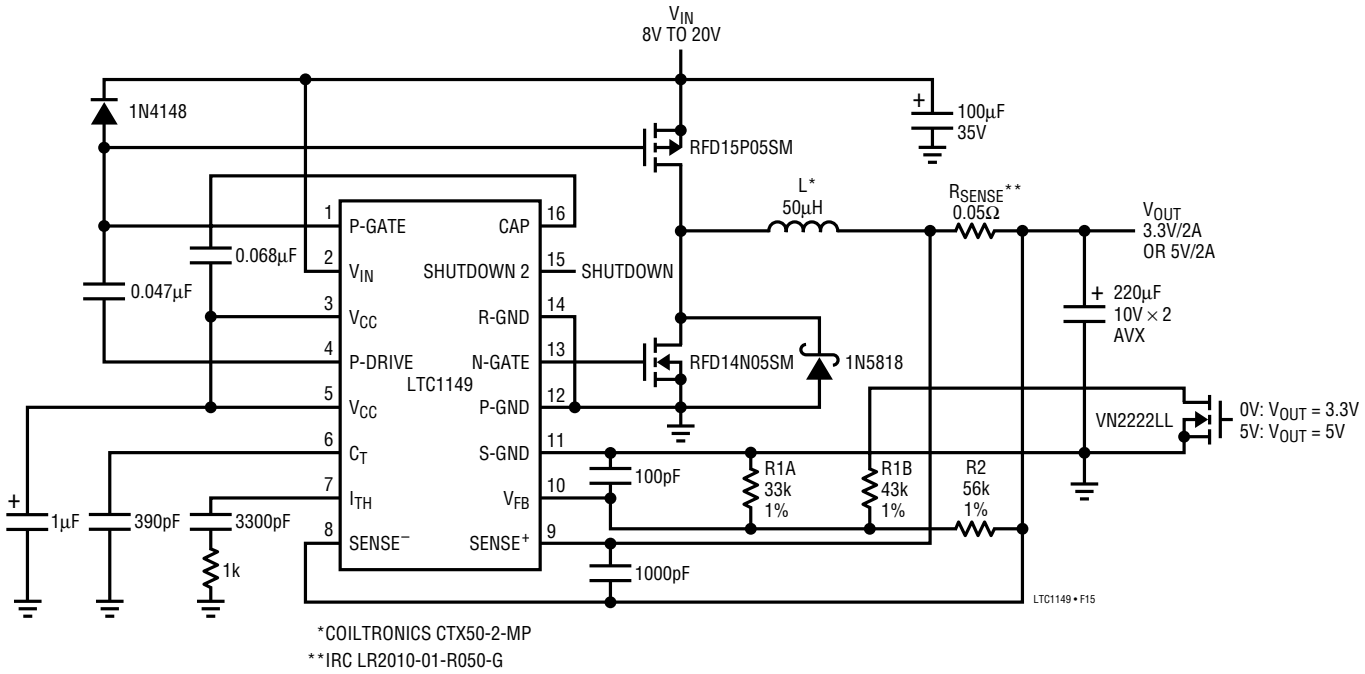


Figure 15. Logic Selectable 5V/2A or 3.3V/2A High Efficiency Regulator

TYPICAL APPLICATIONS

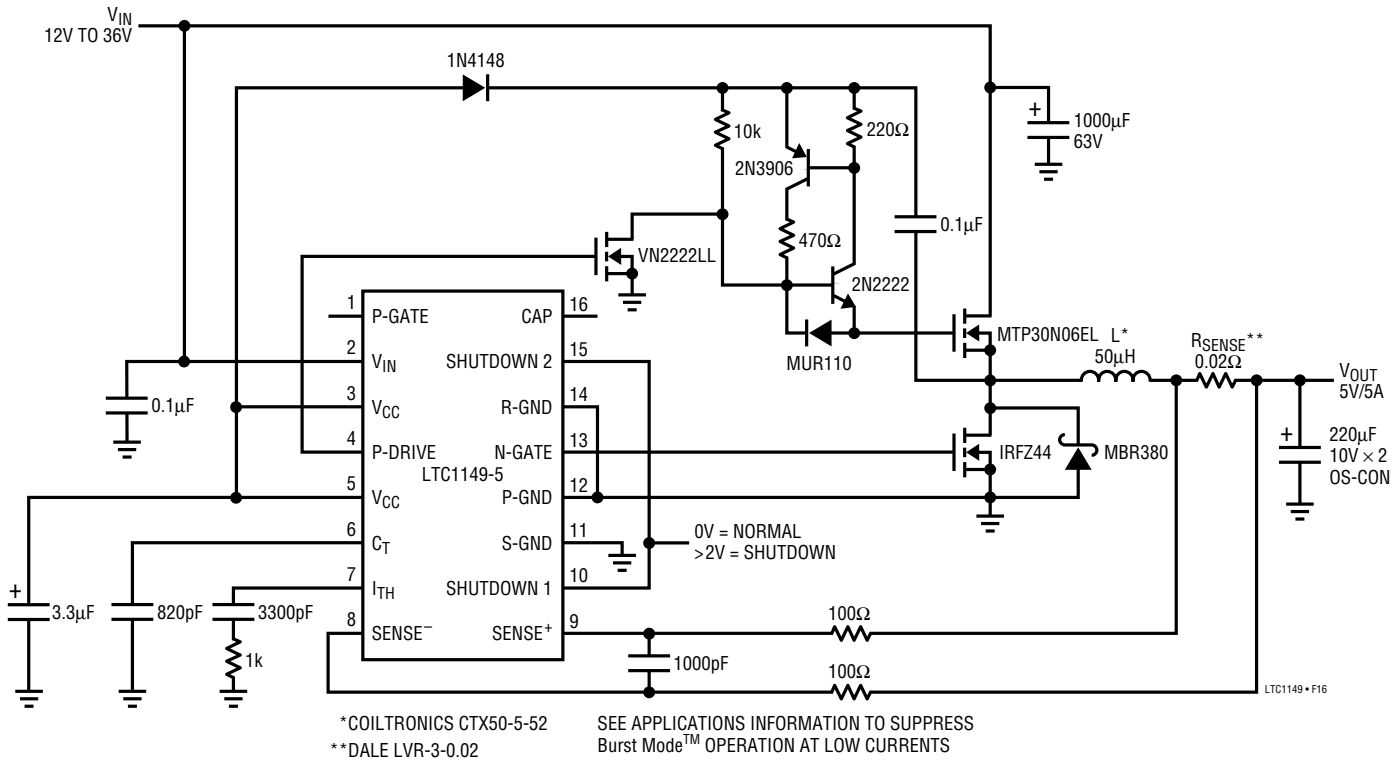


Figure 16. 25W High Efficiency Regulator Using N-Channel MOSFET Switches

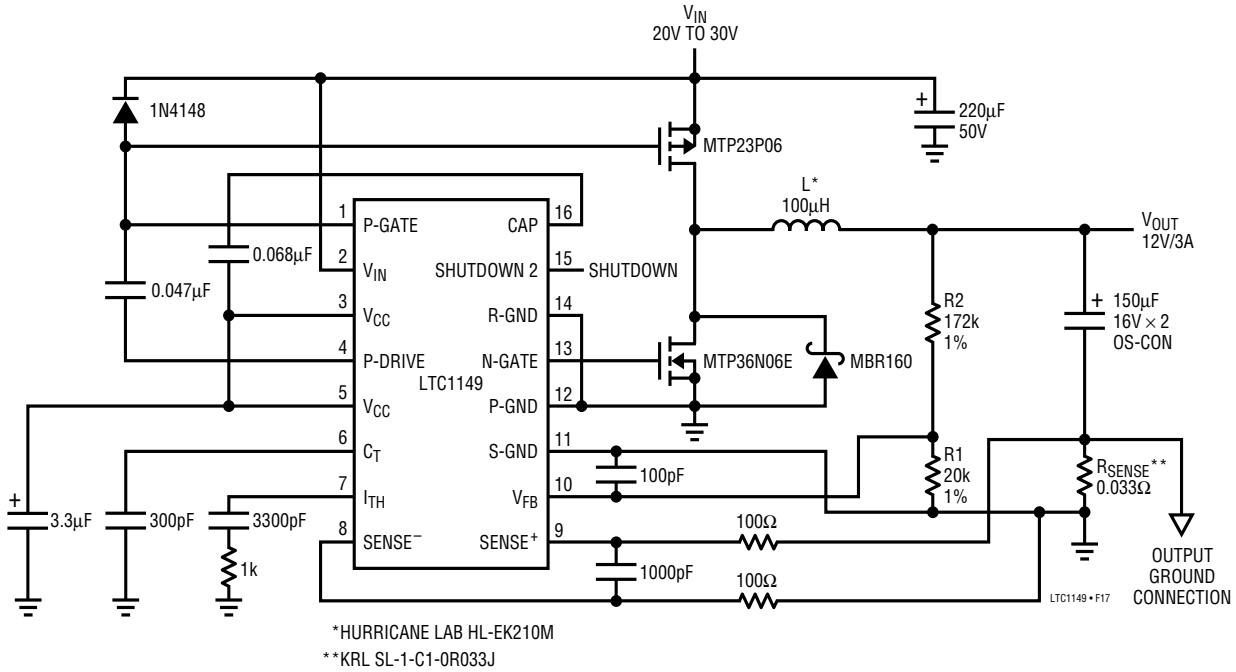
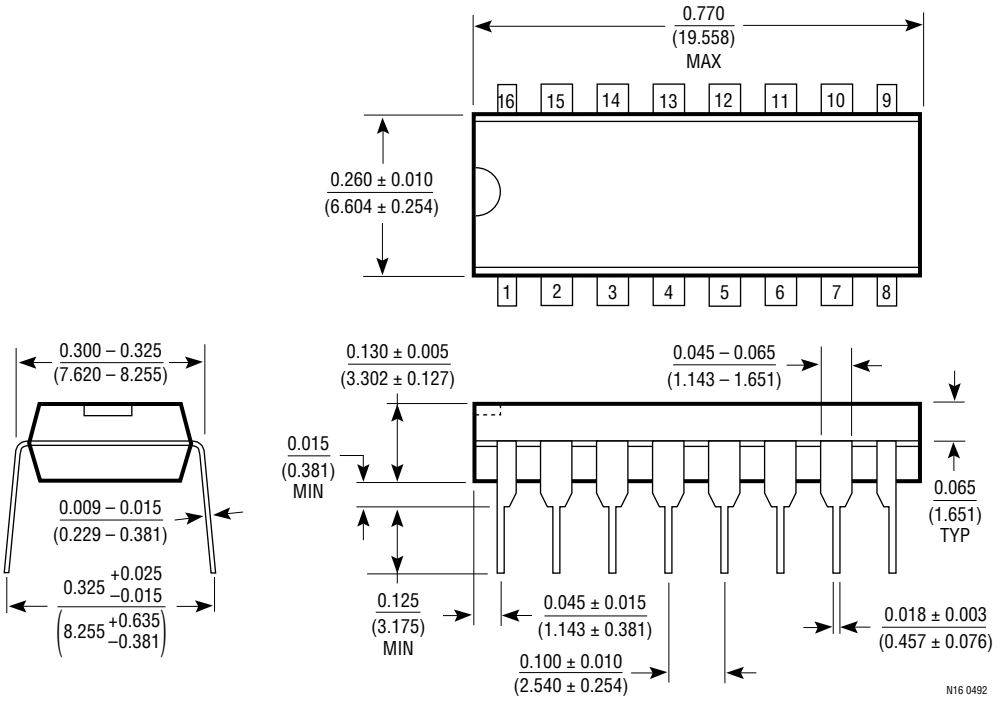


Figure 17. High Efficiency 24V Input 12V/3A Output Regulator

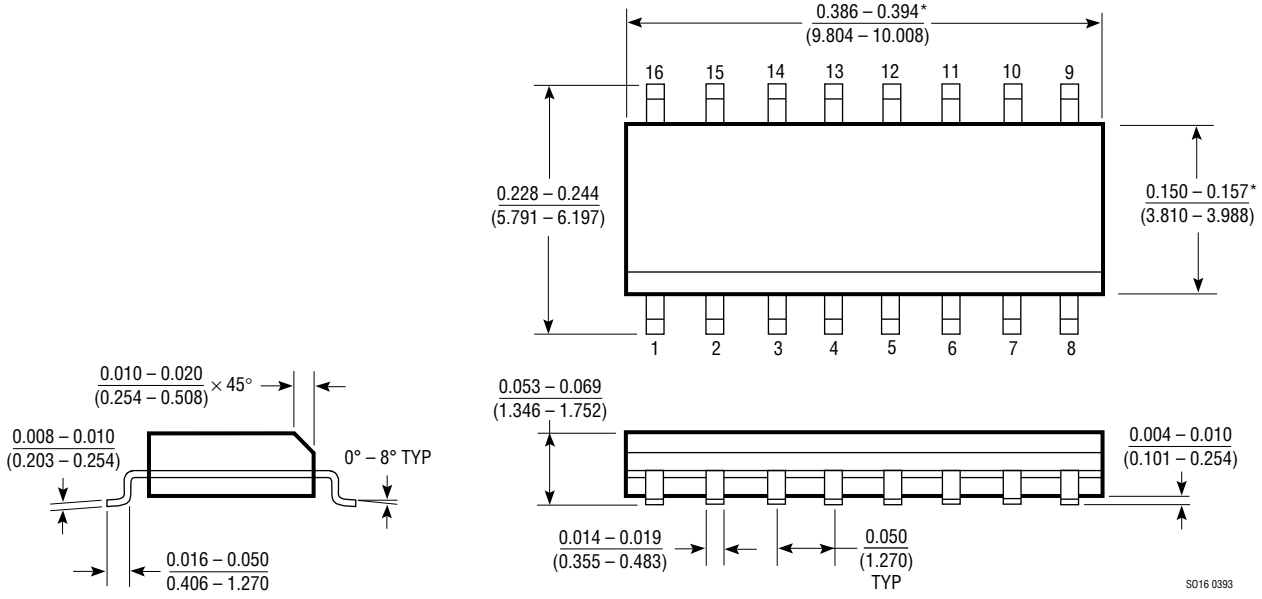
PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N Package
16-Lead Plastic DIP



S Package
16-Lead Plastic SOIC



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).

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LT/GP 0593 10K REV 0