# TwinDie™ DDR3 SDRAM

## MT41J512M4 – 32 Meg x 4 x 8 Banks x 2 Ranks
## MT41J256M8 – 16 Meg x 8 x 8 Banks x 2 Ranks

For component data sheets, refer to Micron's Web site: www.micron.com

## Functionality

The 2Gb (TwinDie™) DDR3 SDRAM uses Micron's 1Gb DDR3 die and has similar functionality. This data sheet provides ball assignments, a general description, functional block diagrams, electrical specifications, and package dimensions. Refer to Micron's 1Gb DDR3 SDRAM data sheet for complete specifications. (Specifications for base part number MT41J256M4 correlate to TwinDie manufacturing part number MT41J512M4; specifications for base part number MT41J128M8 correlate to TwinDie manufacturing part number MT41J256M8.)

## Features

- Uses 1Gb Micron die
- Two ranks (includes dual CS#, ODT, CKE, and ZQ balls)
- Each rank has 8 internal banks
- $V_{DD} = V_{DDQ} = +1.5V \pm 0.075V$
- 1.5V center-terminated push/pull I/O
- JEDEC-standard 78-ball ballout
- Low-profile package (1.35mm MAX thickness)
- $T_C$ of 0°C to 95°C
  - 0°C to 85°C: 8192 refresh cycles in 64ms
  - 85°C to 95°C: 8192 refresh cycles in 32ms

| Options | Marking |
|---|---|
| • Configuration | |
| – 32 Meg x 4 x 8 banks x 2 ranks | 512M4 |
| – 16 Meg x 8 x 8 banks x 2 ranks | 256M8 |
| • FBGA package (lead-free) | |
| – 78-ball FBGA (9mm x 11.5mm) | THR |
| – 78-ball FBGA (8mm x 11.5mm) | THV |
| • Timing – cycle time[1] | |
| – 1.5ns @ CL = 10 (DDR3-1333) | -15 |
| – 1.5ns @ CL = 9 (DDR3-1333) | -15E |
| – 1.87ns @ CL = 8 (DDR3-1066) | -187 |
| – 1.87ns @ CL = 7 (DDR3-1066) | -187E |
| – 2.5ns @ CL = 6 (DDR3-800) | -25 |
| – 2.5ns @ CL = 5 (DDR3-800) | -25E |
| • Self refresh | |
| – Standard | None |
| • Operating temperature | |
| – Commercial ($0°C \le T_C \le 95°C$) | None |
| • Revision | :D/F |

Notes: 1. CL = CAS (READ) latency.

**Table 1: Key Timing Parameters**

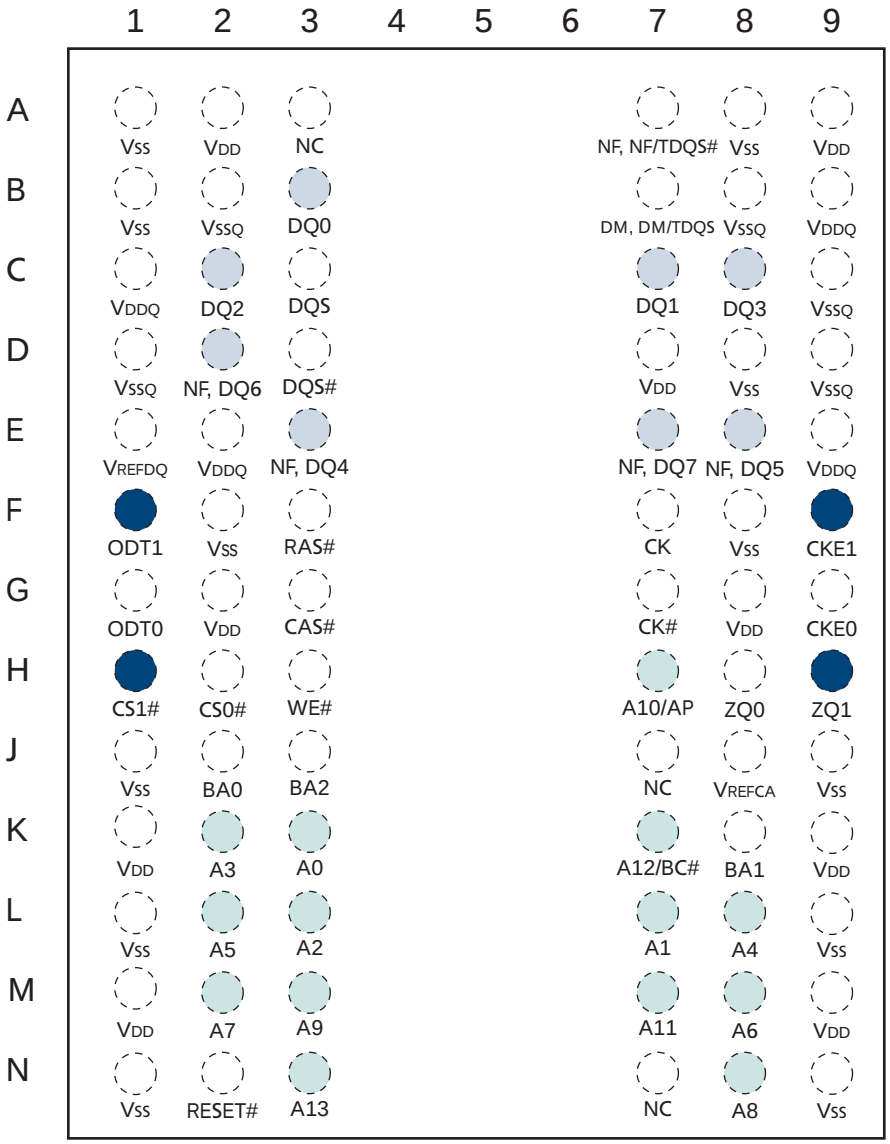
| Speed Grade | Data Rate (MT/s) | Target $^{t}$RCD-$^{t}$RP-CL | $^{t}$RCD (ns) | $^{t}$RP (ns) | CL (ns) |
|---|---|---|---|---|---|
| -15 | 1333 | 10-10-10 | 15 | 15 | 15 |
| -15E | 1333 | 9-9-9 | 13.5 | 13.5 | 13.5 |
| -187 | 1066 | 8-8-8 | 15 | 15 | 15 |
| -187E | 1066 | 7-7-7 | 13.1 | 13.1 | 13.1 |
| -25 | 800 | 6-6-6 | 15 | 15 | 15 |
| -25E | 800 | 5-5-5 | 12.5 | 12.5 | 12.5 |

**Table 2: Addressing**

| Parameter | 512 Meg x 4 | 256 Meg x 8 |
|---|---|---|
| Configuration | 32 Meg x 4 x 8 banks x 2 ranks | 16 Meg x 8 x 8 banks x 2 ranks |
| Refresh count | 8K | 8K |
| Row address | 16K A[13:0] | 16K A[13:0] |
| Bank address | 8 BA[2:0] | 8 BA[2:0] |
| Column address | 2K A[11, 9:0] | 1K A[9:0] |

# Ball Assignments and Descriptions

**Figure 1: 78-Ball FBGA Ball Assignments (Top View)**




Notes: 1. Dark shading designates balls that differ from the monolithic version.

**Table 3: 78-Ball FBGA Ball Descriptions**

| Symbol | Type | Description |
|---|---|---|
| A13, A12/BC#, A11, A10/AP, A[9:0] | Input | **Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to $V_{REFCA}$. A12/BC#: When enabled in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = burst length (BL) of 8 or no burst chop, LOW = burst chop (BC) of 4, burst chop). |
| BA[2:0] | Input | **Bank address inputs:** BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to $V_{REFCA}$. |
| CK, CK# | Input | **Clock:** CK and CK# are differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS, DQS#) is referenced to the crossings of CK and CK#. |
| CKE[1:0] | Input | **Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE power-down and SELF REFRESH operations (all banks idle) or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during power-down. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to $V_{REFCA}$. |
| CS#[1:0] | Input | **Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code. CS# is referenced to $V_{REFCA}$. |
| DM | Input | **Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with the input data, during a write access. Although the DM ball is input-only, the DM loading is designed to match that of the DQ and DQS balls. DM is referenced to $V_{REFDQ}$. DM has an optional use as TDQS on the x8. |
| ODT[1:0] | Input | **On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQ[7:0], DQS, DQS#, and DM for the x8; DQ[3:0], DQS, DQS#, and DM for the x4. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to $V_{REFCA}$. |
| RAS#, CAS#, WE# | Input | **Command inputs:** RAS#, CAS#, and WE# (along with CS#) define the command being entered and are referenced to $V_{REFCA}$. |
| RESET# | Input | **Reset:** RESET# is an active LOW CMOS input referenced to $V_{SS}$. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × $V_{DDQ}$ and DC LOW ≤ 0.2 × $V_{DDQ}$. RESET# assertion and desertion are asynchronous. |
| DQ[3:0] | I/O | **Data input/output:** Bidirectional data bus for the x4 configuration. DQ[3:0] are referenced to $V_{REFDQ}$. |
| DQ[7:0] | I/O | **Data input/output:** Bidirectional data bus for the x8 configuration. DQ[7:0] are referenced to $V_{REFDQ}$. |
| DQS, DQS# | I/O | **Data strobe:** DQS and DQS# are differential data strobes. Output with read data. Edge-aligned with read data. Input with write data. Center-aligned with write data. |
| TDQS, TDQS# | Output | **Termination data strobe:** Applies to the x8 configuration only. When TDQS is enabled, DM is disabled, and the TDQS and TDQS# balls provide termination resistance. |
| $V_{DD}$ | Supply | **Power supply:** 1.5V ±0.075V. |

**Table 3: 78-Ball FBGA Ball Descriptions (continued)**

| Symbol | Type | Description |
|---|---|---|
| $V_{DDQ}$ | Supply | **DQ power supply:** 1.5V ±0.075V. Isolated on the device for improved noise immunity. |
| $V_{REFCA}$ | Supply | **Reference voltage for control, command, and address:** $V_{REFCA}$ must be maintained at all times (including self refresh) for proper device operation. |
| $V_{REFDQ}$ | Supply | **Reference voltage for data:** $V_{REFDQ}$ must be maintained at all times (including self refresh) for proper device operation. |
| $V_{SS}$ | Supply | Ground. |
| $V_{SSQ}$ | Supply | **DQ ground:** Isolated on the device for improved noise immunity. |
| ZQ[1:0] | Reference | **External reference ball for output drive calibration:** This ball is tied to an external 240Ω resistor (RZQ), which is tied to $V_{SSQ}$ |
| NC | – | **No connect:** These balls should be left unconnected (the ball has no connection to the DRAM or to other balls). |
| NF | – | **No function:** When configured as a x4 device, these balls are NF. When configured as a x8 device, these balls are defined as TDQS#, DQ[7:4]. |

# Functional Description

The 2Gb (TwinDie) DDR3 SDRAM is a high-speed, CMOS dynamic random access memory device containing 2,147,483,648 bits and is internally configured as two 8-bank 1Gb DDR3 SDRAM.

Although each die is tested individually within the dual-die package, some TwinDie test results may vary from a like-die tested within a monolithic die package.

The DDR3 SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O balls. A single read or write access consists of a single 8*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O balls.

The differential data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the DDR3 SDRAM input receiver. DQS is center-aligned with data for WRITEs. The read data is transmitted by the DDR3 SDRAM and edge-aligned to the data strobes.

Read and write accesses to the DDR3 SDRAM are burst oriented. Accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits (including CS*n*#, BA*n*, and A*n*) registered coincident with the READ or WRITE command are used to select the rank, bank, and starting column location for the burst access.

This data sheet provides a general description, package dimensions, and the package ballout. Refer to the Micron 1Gb DDR3 data sheet for complete information regarding individual die initialization, register definition, command descriptions, and die operation.

# Functional Block Diagrams

**Figure 2: Functional Block Diagram (32 Meg x 4 x 8 Banks x 2 Ranks)**

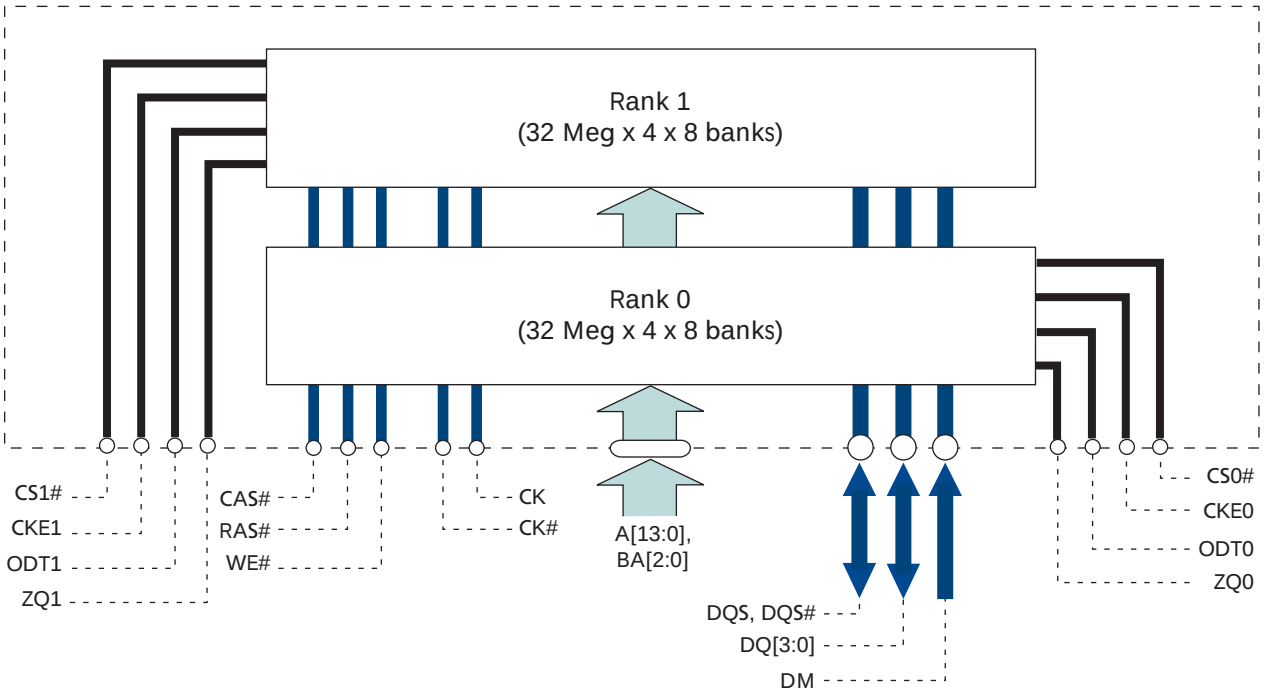
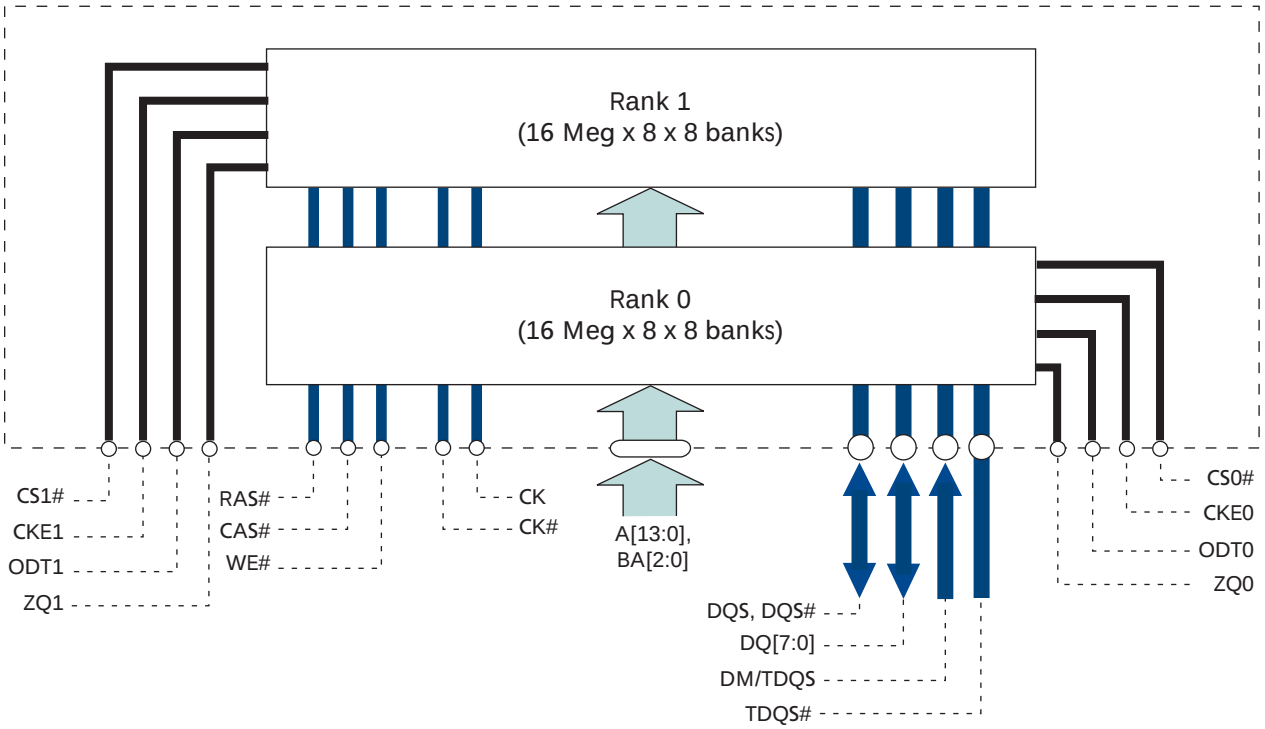



**Figure 3: Functional Block Diagram (16 Meg x 8 x 8 Banks x 2 Ranks)**



# Electrical Specifications

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the device data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

**Table 4: Absolute Maximum Ratings**

| Symbol | Parameter | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| $V_{DD}$ | $V_{DD}$ supply voltage relative to $V_{SS}$ | –0.4 | 1.975 | V | 1 |
| $V_{DDQ}$ | $V_{DD}$ supply voltage relative to $V_{SSQ}$ | –0.4 | 1.975 | V | |
| $V_{IN}$, $V_{OUT}$ | Voltage on any ball relative to $V_{SS}$ | –0.4 | 1.975 | V | |
| $T_C$ | Operating case temperature | 0 | 95 | °C | 2, 3 |
| $T_{STG}$ | Storage temperature | –55 | 150 | °C | |

Notes: 1. $V_{DD}$and $V_{DDQ}$ must be within 300mV of each other at all times, and $V_{REF}$ must not be greater than 0.6 × $V_{DDQ}$. When $V_{DD}$ and $V_{DDQ}$ are less than 500mV, $V_{REF}$ may be ≤300mV.
2. MAX operating case temperature. $T_C$ is measured in the center of the package (see Figure 4 on page 8).
3. Device functionality is not guaranteed if the DRAM device exceeds the maximum $T_C$ during operation.

## Temperature and Thermal Impedance

It is imperative that the DDR3 SDRAM device's temperature specifications, shown in Table 5 on page 8, be maintained to ensure the junction temperature is in the proper operating range to meet data sheet specifications. An important step in maintaining the proper junction temperature is using the device's thermal impedances correctly. Thermal impedances listed in Table 6 on page 8 apply to the current die revision and packages.

Incorrectly using thermal impedances can produce significant errors. Read Micron technical note TN-00-08: "Thermal Applications," prior to using the thermal impedances in Table 6. For designs that are expected to last several years and require the flexibility to use several DRAM die shrinks, consider using final target theta values (rather than existing values) to account for increased thermal impedances from the reduction in die size.

The DDR3 SDRAM device's safe junction temperature range can be maintained when the $T_C$ specification is not exceeded. In applications where the device's ambient temperature is too high, use of forced air and/or heat sinks may be required to satisfy the case temperature specifications.

**Table 5: Thermal Characteristics**

| Parameter/Condition | Symbol | Value | Units | Notes |
|---|---|---|---|---|
| Operating case temperature | $T_C$ | 0 to 85 | °C | 1, 2, 3 |
| | | 0 to 95 | °C | 1, 2, 3, 4 |

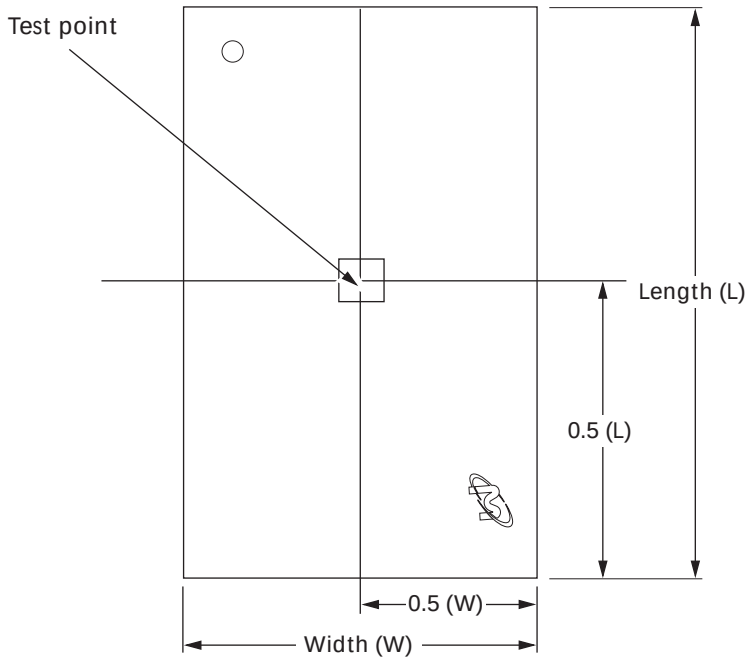
Notes:
1. MAX operating case temperature. $T_C$ is measured in the center of the package (see Figure 4).
2. A thermal solution must be designed to ensure the DRAM device does not exceed the maximum $T_C$ during operation.
3. Device functionality is not guaranteed if the DRAM device exceeds the maximum $T_C$ during operation.
4. If $T_C$ exceeds 85°C, the DRAM must be refreshed externally at 2X refresh, which is a 3.9µs interval refresh rate. The use of self refresh temperature (SRT) or automatic self refresh (ASR), if available, must be enabled.

**Table 6: Thermal Impedance**

| Die Rev | Package | Substrate | θJA (°C/W) Airflow = 0m/s | θJA (°C/W) Airflow = 1m/s | θJA (°C/W) Airflow = 2m/s | θJB (°C/W) | θJC (°C/W) | Notes |
|---|---|---|---|---|---|---|---|---|
| D | 78-ball | 2-layer | 55.4 | 41.9 | 35.5 | 25.3 | 2.93 | 1 |
| | | 4-layer | 41.0 | 33.2 | 29.5 | 24.7 | | |
| F | 78-ball | 2-layer | 65.4 | 51.3 | 44.6 | 34.5 | 3.67 | 2 |
| | | 4-layer | 49.3 | 41.7 | 37.9 | 33.5 | | |

Notes:
1. Thermal resistance data is based upon a number of samples from multiple lots and should be viewed as a typical number.
2. This represents a future die shrink and is an estimate; simulated number and actual results may vary.

**Figure 4: Temperature Test Point Location**



## $I_{DD}$ Specifications and Conditions

### Table 7: DDR3 $I_{CDD}$ Specifications and Conditions

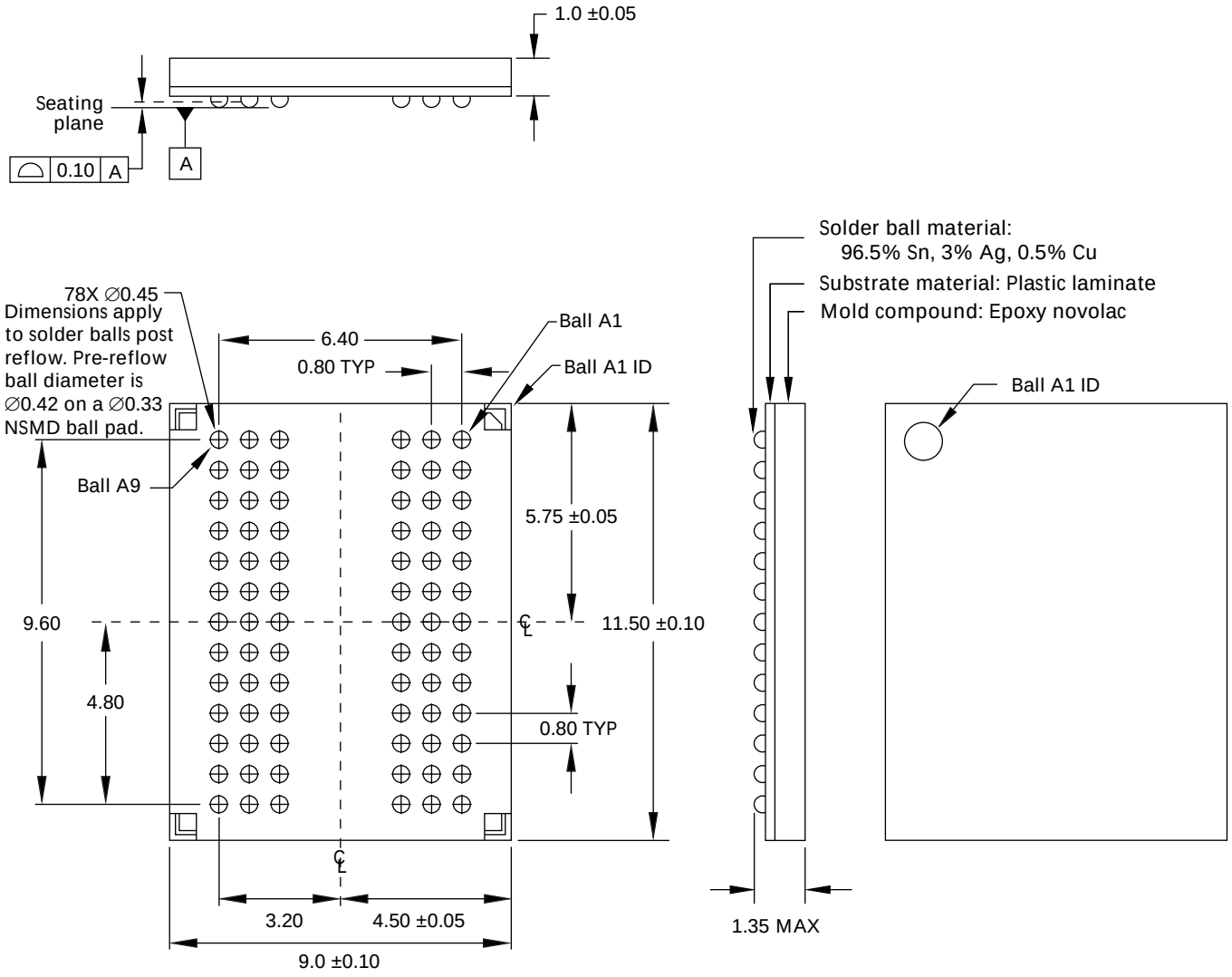
Note 1 applies to the entire table.

| Combined Symbol | Individual Die Status | Width | -25/ -25E | -187/ -187E | -15/ -15E | Units |
|---|---|---|---|---|---|---|
| $I_{CDD0}$ | $I_{CDD0} = I_{DD0} + I_{DD2P0} + 5$ | x4 | 82 | 92 | 102 | mA |
| | | x8 | 107 | 117 | 127 | mA |
| $I_{CDD1}$ | $I_{CDD1} = I_{DD1} + I_{DD2P0} + 5$ | x4 | 102 | 112 | 122 | mA |
| | | x8 | 127 | 137 | 147 | mA |
| $I_{CDD2P0}$ (slow exit) | $I_{CDD2P0} = I_{DD2P0} + I_{DD2P0}$ | x4/x8 | 24 | 24 | 24 | mA |
| $I_{CDD2P1}$ (fast exit) | $I_{CDD2P1} = I_{DD2P1} + I_{DD2P0}$ | | 42 | 47 | 52 | mA |
| $I_{CDD2Q}$ | $I_{CDD2Q} = I_{DD2Q} + I_{DD2P0}$ | x4/x8 | 58 | 65 | 72 | mA |
| $I_{CDD2N}$ | $I_{CDD2N} = I_{DD2N} + I_{DD2P0}$ | All | 62 | 67 | 77 | mA |
| $I_{CDD2NT}$ | $I_{CDD2NT} = I_{DD2NT} + I_{DD2P0}$ | | 77 | 87 | 97 | mA |
| $I_{CDD3P}$ | $I_{CDD3P} = I_{DD3P} + I_{DD2P0}$ | x4/x8 | 42 | 47 | 52 | mA |
| $I_{CDD3N}$ | $I_{CDD3N} = I_{DD3N} + I_{DD2P0}$ | x4/x8 | 64 | 69 | 74 | mA |
| $I_{CDD4W}$ | $I_{CDD4W} = I_{DD4W} + I_{DD2P0} + 5$ | x4 | 177 | 207 | 237 | mA |
| | | x8 | 177 | 207 | 237 | mA |
| $I_{CDD4R}$ | $I_{CDD4R} = I_{DD4R} + I_{DD2P0} + 5$ | x4 | 147 | 177 | 217 | mA |
| | | x8 | 147 | 177 | 217 | mA |
| $I_{CDD5B}$ | $I_{CDD5B} = I_{DD5B} + I_{DD2P0}$ | x4/x8 | 212 | 232 | 252 | mA |
| $I_{CDD6}$ | $I_{CDD6} = I_{DD6} + I_{DD6}$ | x4/x8 | 12 | 12 | 12 | mA |
| $I_{CDD6ET}$ | $I_{CDD6ET} = I_{DD6ET} + I_{DD6ET}$ | x4/x8 | 18 | 18 | 18 | mA |
| $I_{CDD7}$ | $I_{CDD7} = I_{DD7} + I_{DD2P0} + 5$ | x4 | 247 | 267 | 332 | mA |
| | | x8 | 367 | 407 | 507 | mA |
| $I_{CDD8}$ | $I_{CDD8} = 2 \times I_{DD2P0} + 4$ | All | 28 | 28 | 28 | mA |

Notes: 1. $I_{CDD}$ values reflect the combined current of both individual die. $I_{DDx}$ represents individual die values.

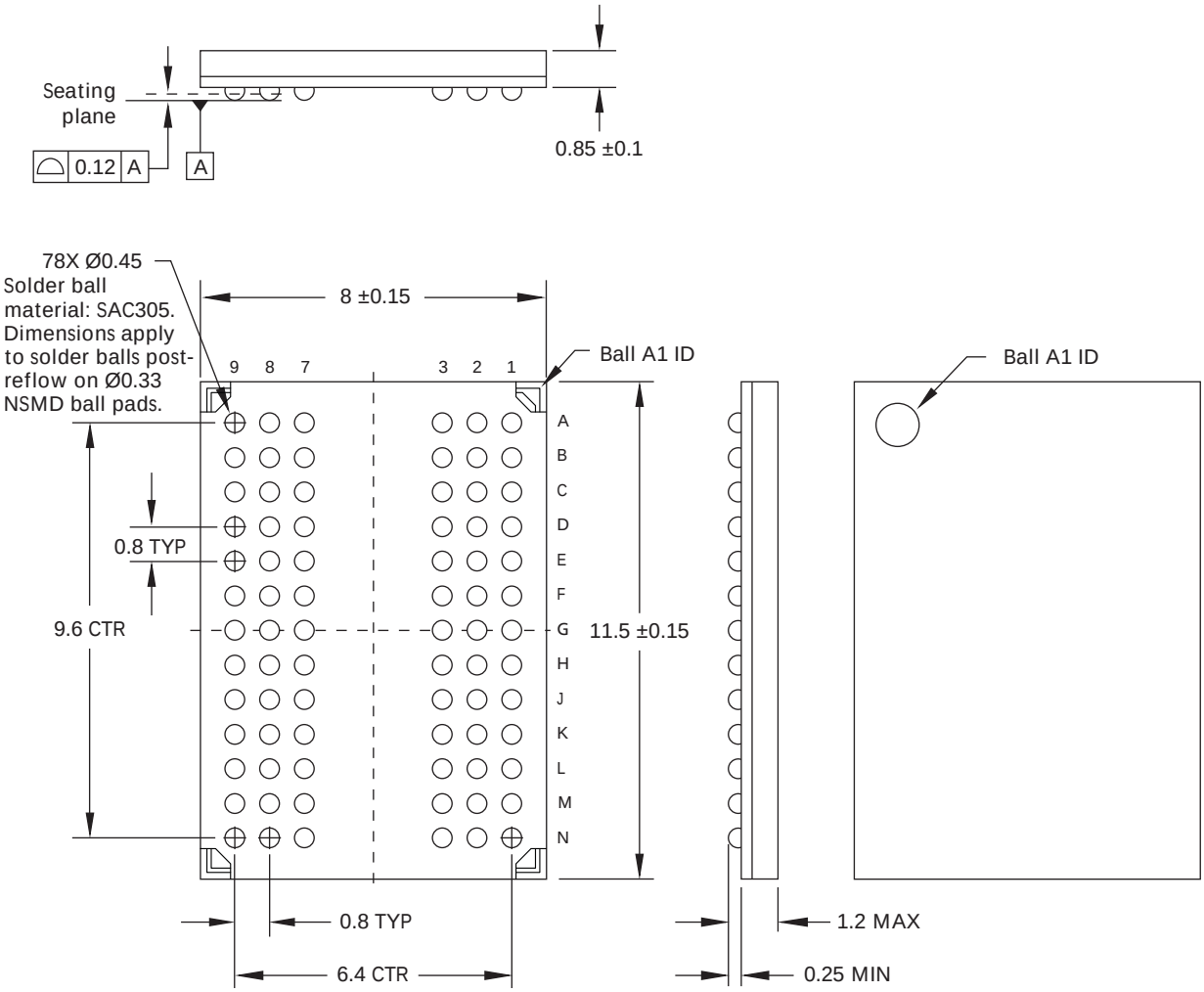
# Package Dimensions

**Figure 5: 78-Ball FBGA Package Dimensions (Package Code THR)**




Note: All dimensions are in millimeters.

**Figure 6: 78-Ball FBGA Package Dimensions (Package Code THV)**




Note: All dimensions are in millimeters.