

## General Description

The ICS843004I-01 is a 4 output LVPECL synthesizer optimized to generate Ethernet reference clock frequencies. Using a 25MHz 18pF parallel resonant crystal, the following frequencies can be generated based on the settings of 2 frequency select pins (F\_SEL[1:0]): 156.25MHz, 125MHz, 62.5MHz. The ICS843004I-01 uses IDT's 3<sup>rd</sup> generation low phase noise VCO technology and can achieve 1ps or lower typical rms phase jitter, easily meeting Ethernet jitter requirements. The ICS843004I-01 is packaged in a small 24-pin TSSOP package.

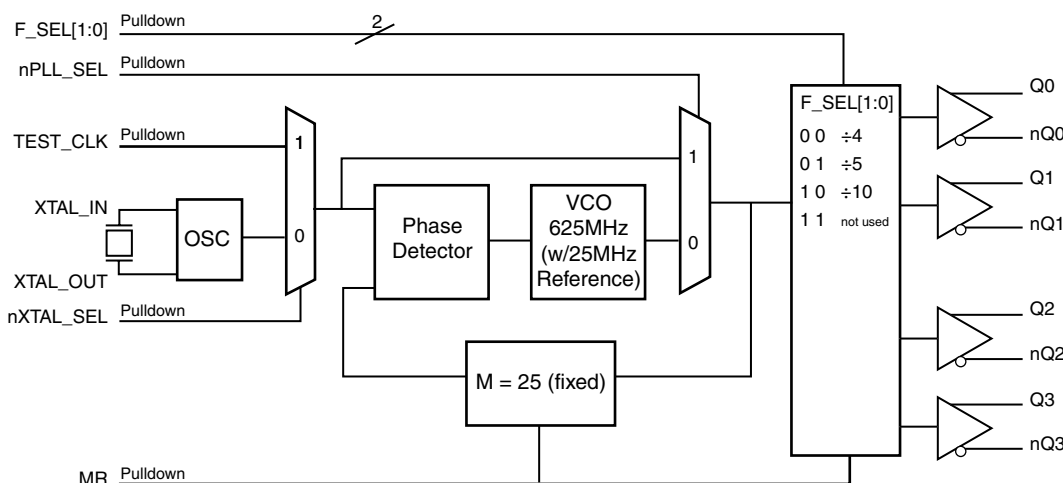
## Features

- Four 3.3V differential LVPECL output pairs
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended clock input
- Supports the following output frequencies: 156.25MHz, 125MHz, 62.5MHz
- VCO range: 560MHz – 680MHz
- RMS phase jitter @ 156.25MHz, using a 25MHz crystal (1.875MHz – 20MHz): 0.54ps (typical)
- Full 3.3V or 2.5V supply modes
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

## Frequency Select Function Table

| Inputs |        |              |              |                | Output Frequency (MHz)<br>(25MHz Reference) |
|--------|--------|--------------|--------------|----------------|---------------------------------------------|
| F_SEL1 | F_SEL0 | M Div. Value | N Div. Value | M/N Div. Value |                                             |
| 0      | 0      | 25           | 4            | 6.25           | 156.25                                      |
| 0      | 1      | 25           | 5            | 5              | 125                                         |
| 1      | 0      | 25           | 10           | 2.5            | 62.5                                        |
| 1      | 1      | 25           | Not Used     |                | Not Used                                    |

## Block Diagram



## Pin Assignment

|                  |    |    |                  |
|------------------|----|----|------------------|
| nQ1              | 1  | 24 | nQ2              |
| Q1               | 2  | 23 | Q2               |
| V <sub>CC0</sub> | 3  | 22 | V <sub>CC0</sub> |
| Q0               | 4  | 21 | Q3               |
| nQ0              | 5  | 20 | nQ3              |
| MR               | 6  | 19 | VEE              |
| nPLL_SEL         | 7  | 18 | V <sub>CC</sub>  |
| nc               | 8  | 17 | nXTAL_SEL        |
| V <sub>CCA</sub> | 9  | 16 | TEST_CLK         |
| F_SEL0           | 10 | 15 | VEE              |
| V <sub>CC</sub>  | 11 | 14 | XTAL_IN          |
| F_SEL1           | 12 | 13 | XTAL_OUT         |

**ICS843004I-01**

**24-Lead TSSOP**

**4.4mm x 7.8mm x 0.925mm  
package body  
G Package  
Top View**

**Table 1. Pin Descriptions**

| Number | Name              | Type   |          | Description                                                                                                                                                                                                                                                 |
|--------|-------------------|--------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1, 2   | nQ1, Q1           | Output |          | Differential output pair. LVPECL interface levels.                                                                                                                                                                                                          |
| 3, 22  | V <sub>CCO</sub>  | Power  |          | Output supply pins.                                                                                                                                                                                                                                         |
| 4, 5   | Q0, nQ0           | Output |          | Differential output pair. LVPECL interface levels.                                                                                                                                                                                                          |
| 6      | MR                | Input  | Pulldown | Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels. |
| 7      | nPLL_SEL          | Input  | Pulldown | Selects either the PLL or the active input reference to be routed to the output dividers. When LOW, selects PLL (PLL Enable). When HIGH, selects the reference clock (PLL Bypass). LVCMOS/LVTTL interface levels.                                           |
| 8      | nc                | Unused |          | No connect.                                                                                                                                                                                                                                                 |
| 9      | V <sub>CCA</sub>  | Power  |          | Analog supply pin.                                                                                                                                                                                                                                          |
| 10, 12 | F_SEL0, F_SEL1    | Input  | Pulldown | Frequency select pins. LVCMOS/LVTTL interface levels.                                                                                                                                                                                                       |
| 11, 18 | V <sub>CC</sub>   | Power  |          | Core supply pins.                                                                                                                                                                                                                                           |
| 13, 14 | XTAL_OUT, XTAL_IN | Input  |          | Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.                                                                                                                                                                          |
| 15, 19 | V <sub>EE</sub>   | Power  |          | Negative supply pins.                                                                                                                                                                                                                                       |
| 16     | TEST_CLK          | Input  | Pulldown | Single-ended clock input. LVCMOS/LVTTL interface levels.                                                                                                                                                                                                    |
| 17     | nXTAL_SEL         | Input  | Pulldown | Selects between the single-ended TEST_CLK or crystal interface as the PLL reference source. When HIGH, selects TEST_CLK. When LOW, selects XTAL inputs. LVCMOS/LVTTL interface levels.                                                                      |
| 20, 21 | nQ3, Q3           | Output |          | Differential output pair. LVPECL interface levels.                                                                                                                                                                                                          |
| 23, 24 | Q2, nQ2           | Output |          | Differential output pair. LVPECL interface levels.                                                                                                                                                                                                          |

NOTE: *Pulldown* refers to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

| Symbol                | Parameter               | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|-----------------|---------|---------|---------|-------|
| C <sub>IN</sub>       | Input Capacitance       |                 |         | 4       |         | pF    |
| R <sub>PULLDOWN</sub> | Input Pulldown Resistor |                 |         | 51      |         | kΩ    |

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item                                                           | Rating                   |
|----------------------------------------------------------------|--------------------------|
| Supply Voltage, $V_{CC}$                                       | 4.6V                     |
| Inputs, $V_I$                                                  | -0.5V to $V_{CC} + 0.5V$ |
| Outputs, $I_O$ (LVPECL)<br>Continuous Current<br>Surge Current | 50mA<br>100mA            |
| Package Thermal Impedance, $\theta_{JA}$                       | 70°C/W (0 mps)           |
| Storage Temperature, $T_{STG}$                                 | -65°C to 150°C           |

## DC Electrical Characteristics

**Table 3A. Power Supply DC Characteristics,  $V_{CC} = V_{CCO} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

| Symbol    | Parameter             | Test Conditions      | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|----------------------|---------|---------|---------|-------|
| $V_{CC}$  | Core Supply Voltage   |                      | 3.135   | 3.3     | 3.465   | V     |
| $V_{CCA}$ | Analog Supply Voltage |                      | 3.135   | 3.3     | 3.465   | V     |
| $V_{CCO}$ | Output Supply Voltage |                      | 3.135   | 3.3     | 3.465   | V     |
| $I_{EE}$  | Power Supply Current  |                      |         |         | 130     | mA    |
| $I_{CCA}$ | Analog Supply Current | Included in $I_{EE}$ |         |         | 15      | mA    |

**Table 3B. Power Supply DC Characteristics,  $V_{CC} = V_{CCO} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

| Symbol    | Parameter             | Test Conditions      | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|----------------------|---------|---------|---------|-------|
| $V_{CC}$  | Core Supply Voltage   |                      | 2.375   | 2.5     | 2.625   | V     |
| $V_{CCA}$ | Analog Supply Voltage |                      | 2.375   | 2.5     | 2.625   | V     |
| $V_{CCO}$ | Output Supply Voltage |                      | 2.375   | 2.5     | 2.625   | V     |
| $I_{EE}$  | Power Supply Current  |                      |         |         | 120     | mA    |
| $I_{CCA}$ | Analog Supply Current | Included in $I_{EE}$ |         |         | 12      | mA    |

**Table 3C. LVCMOS/LVTTL DC Characteristics,  $V_{CC} = V_{CCO} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

| Symbol   | Parameter          |                                               | Test Conditions                   | Minimum | Typical | Maximum        | Units   |
|----------|--------------------|-----------------------------------------------|-----------------------------------|---------|---------|----------------|---------|
| $V_{IH}$ | Input High Voltage |                                               | $V_{CC} = 3.3V \pm 5\%$           | 2       |         | $V_{CC} + 0.3$ | V       |
|          |                    |                                               | $V_{CC} = 2.5V \pm 5\%$           | 1.7     |         | $V_{CC} + 0.3$ | V       |
| $V_{IL}$ | Input Low Voltage  |                                               | $V_{CC} = 3.3V \pm 5\%$           | -0.3    |         | 0.8            | V       |
|          |                    |                                               | $V_{CC} = 2.5V \pm 5\%$           | -0.3    |         | 0.7            | V       |
| $I_{IH}$ | Input High Current | TEST_CLK, MR, F_SEL[0:1], nPLL_SEL, nXTAL_SEL | $V_{CC} = V_{IN} = 3.465V$        |         |         | 150            | $\mu A$ |
| $I_{IL}$ | Input Low Current  | TEST_CLK, MR, F_SEL[0:1], nPLL_SEL, nXTAL_SEL | $V_{CC} = 3.465V$ , $V_{IN} = 0V$ | -5      |         |                | $\mu A$ |

**Table 3D. LVPECL DC Characteristics,  $V_{CC} = V_{CCO} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

| Symbol      | Parameter                         | Test Conditions | Minimum         | Typical | Maximum         | Units |
|-------------|-----------------------------------|-----------------|-----------------|---------|-----------------|-------|
| $V_{OH}$    | Output High Voltage; NOTE 1       |                 | $V_{CCO} - 1.4$ |         | $V_{CCO} - 0.9$ | V     |
| $V_{OL}$    | Output Low Voltage; NOTE 1        |                 | $V_{CCO} - 2.0$ |         | $V_{CCO} - 1.7$ | V     |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing |                 | 0.6             |         | 1.0             | V     |

NOTE 1: Outputs termination with  $50\Omega$  to  $V_{CCO} - 2V$ .**Table 3E. LVPECL DC Characteristics,  $V_{CC} = V_{CCO} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

| Symbol      | Parameter                         | Test Conditions | Minimum         | Typical | Maximum         | Units |
|-------------|-----------------------------------|-----------------|-----------------|---------|-----------------|-------|
| $V_{OH}$    | Output High Voltage; NOTE 1       |                 | $V_{CCO} - 1.4$ |         | $V_{CCO} - 0.9$ | V     |
| $V_{OL}$    | Output Low Voltage; NOTE 1        |                 | $V_{CCO} - 2.0$ |         | $V_{CCO} - 1.5$ | V     |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing |                 | 0.4             |         | 1.0             | V     |

NOTE 1: Outputs termination with  $50\Omega$  to  $V_{CCO} - 2V$ .**Table 4. Crystal Characteristics**

| Parameter                          | Test Conditions | Minimum     | Typical | Maximum | Units    |
|------------------------------------|-----------------|-------------|---------|---------|----------|
| Mode of Oscillation                |                 | Fundamental |         |         |          |
| Frequency                          |                 |             | 25      |         | MHz      |
| Equivalent Series Resistance (ESR) |                 |             |         | 50      | $\Omega$ |
| Shunt Capacitance                  |                 |             |         | 7       | pF       |

NOTE: Characterized using an 18pF parallel resonant crystal.

## AC Electrical Characteristics

**Table 5A. AC Characteristics,  $V_{CC} = V_{CCO} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

| Symbol               | Parameter                          | Test Conditions               | Minimum | Typical | Maximum | Units |
|----------------------|------------------------------------|-------------------------------|---------|---------|---------|-------|
| $f_{OUT}$            | Output Frequency Range             | $F\_SEL[1:0] = 00$            | 140     |         | 170     | MHz   |
|                      |                                    | $F\_SEL[1:0] = 01$            | 112     |         | 136     | MHz   |
|                      |                                    | $F\_SEL[1:0] = 10$            | 56      |         | 68      | MHz   |
| $t_{sk(o)}$          | Output Skew; NOTE 1, 2             |                               |         |         | 50      | ps    |
| $f_{jit}(\emptyset)$ | RMS Phase Jitter, (Random); NOTE 3 | 156.25MHz, (1.875MHz – 20MHz) |         | 0.54    |         | ps    |
|                      |                                    | 125MHz, (1.875MHz – 20MHz)    |         | 0.58    |         | ps    |
|                      |                                    | 62.5MHz, (637kHz – 10MHz)     |         | 0.70    |         | ps    |
| $t_R / t_F$          | Output Rise/Fall Time              | 20% to 80%                    | 300     |         | 600     | ps    |
| odc                  | Output Duty Cycle                  |                               | 48      |         | 52      | %     |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions

NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Please refer to the Phase Noise Plots.

**Table 5B. AC Characteristics,  $V_{CC} = V_{CCO} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

| Symbol               | Parameter                          | Test Conditions               | Minimum | Typical | Maximum | Units |
|----------------------|------------------------------------|-------------------------------|---------|---------|---------|-------|
| $f_{OUT}$            | Output Frequency Range             | $F\_SEL[1:0] = 00$            | 140     |         | 170     | MHz   |
|                      |                                    | $F\_SEL[1:0] = 01$            | 112     |         | 136     | MHz   |
|                      |                                    | $F\_SEL[1:0] = 10$            | 56      |         | 68      | MHz   |
| $t_{sk(o)}$          | Output Skew; NOTE 1, 2             |                               |         |         | 50      | ps    |
| $f_{jit}(\emptyset)$ | RMS Phase Jitter, (Random); NOTE 3 | 156.25MHz, (1.875MHz – 20MHz) |         | 0.54    |         | ps    |
|                      |                                    | 125MHz, (1.875MHz – 20MHz)    |         | 0.58    |         | ps    |
|                      |                                    | 62.5MHz, (637kHz – 10MHz)     |         | 0.74    |         | ps    |
| $t_R / t_F$          | Output Rise/Fall Time              | 20% to 80%                    | 300     |         | 600     | ps    |
| odc                  | Output Duty Cycle                  |                               | 48      |         | 52      | %     |

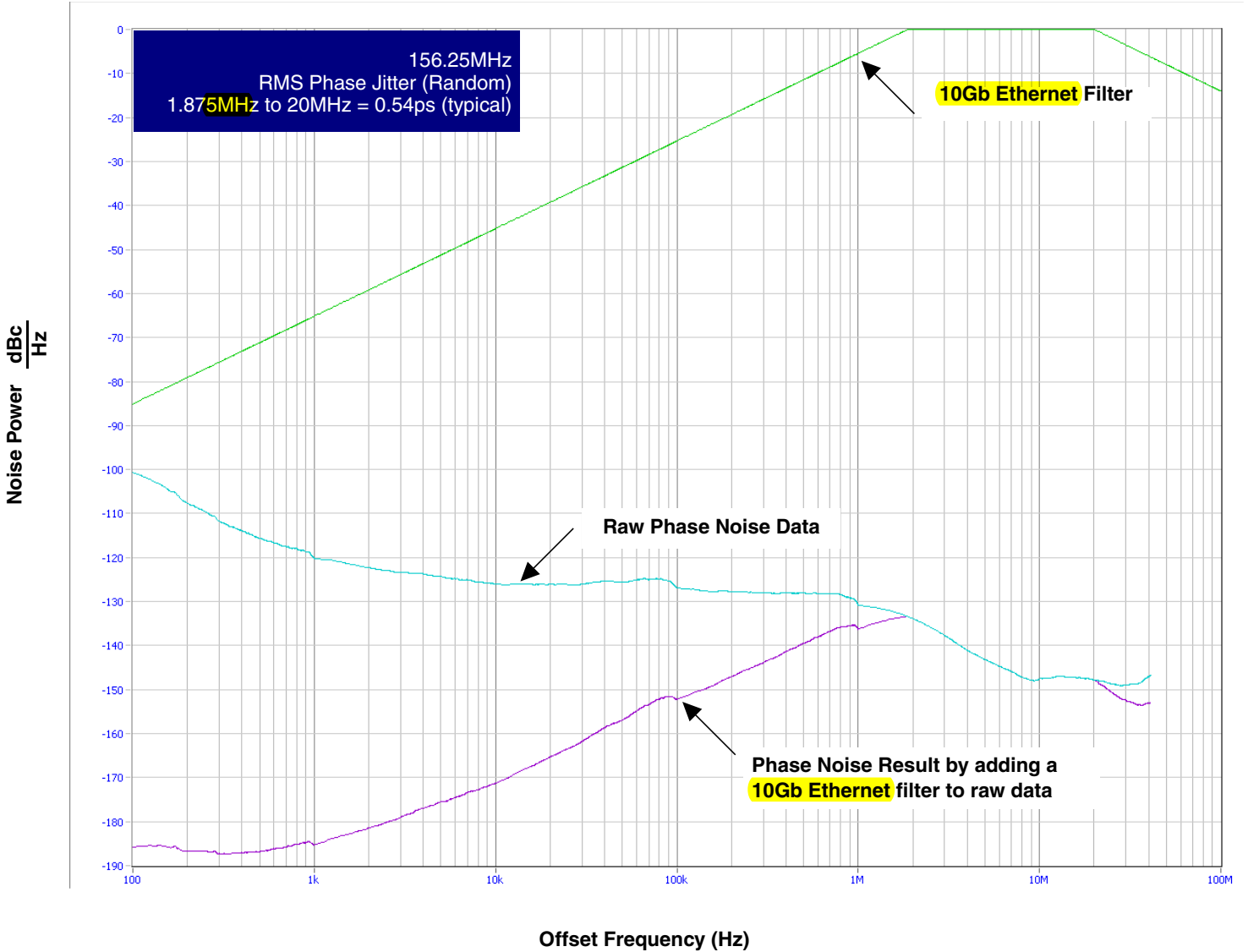
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions

NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.

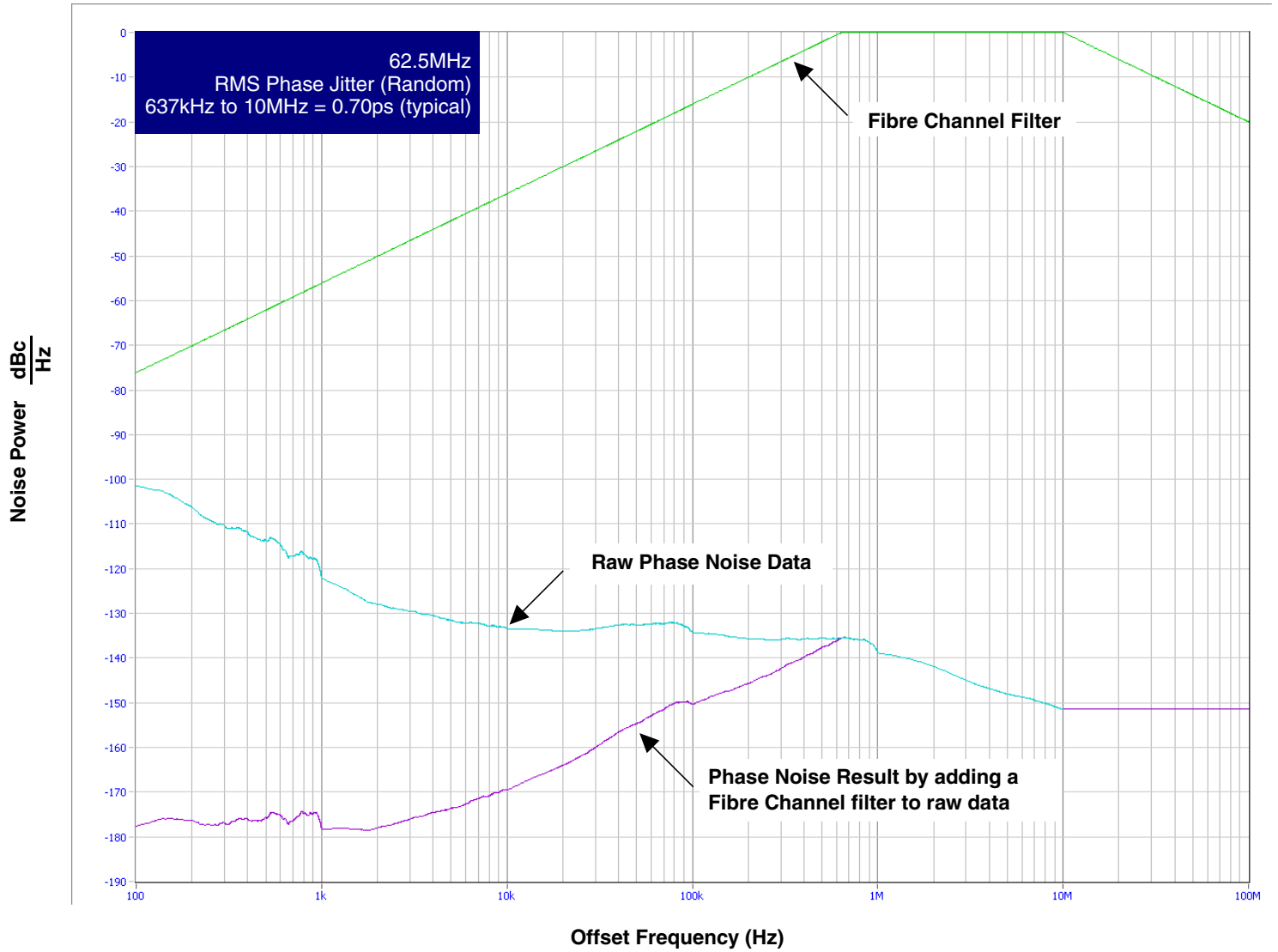
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Please refer to the Phase Noise Plots.

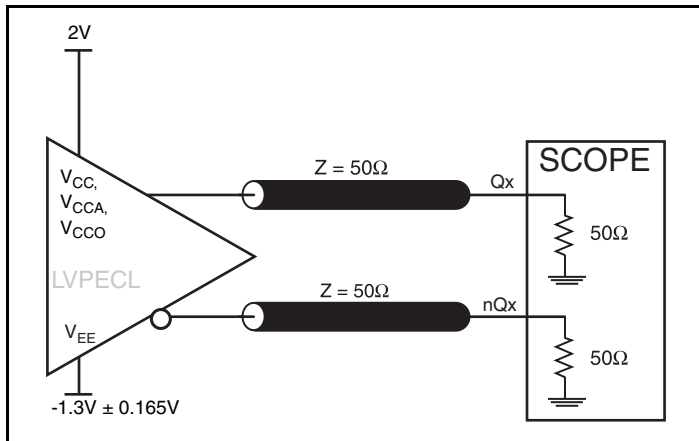
Typical Phase Noise at 156.25MHz (3.3V)



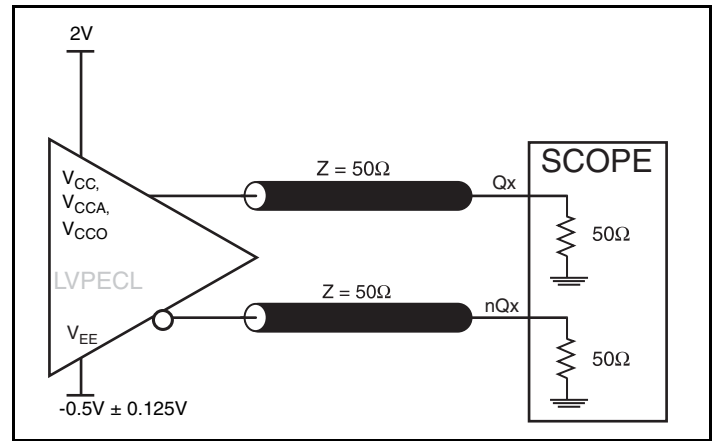
Typical Phase Noise at 62.5MHz (3.3V)



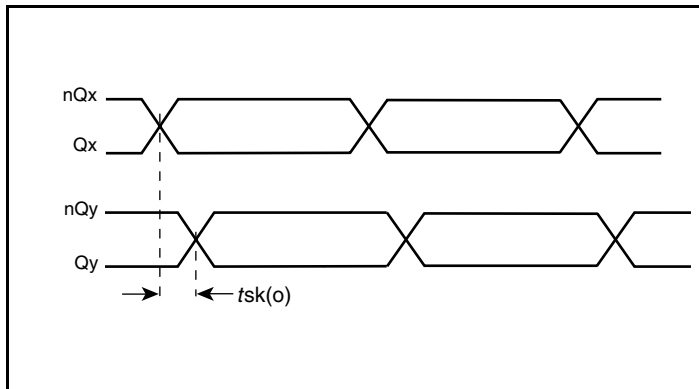
## Parameter Measurement Information



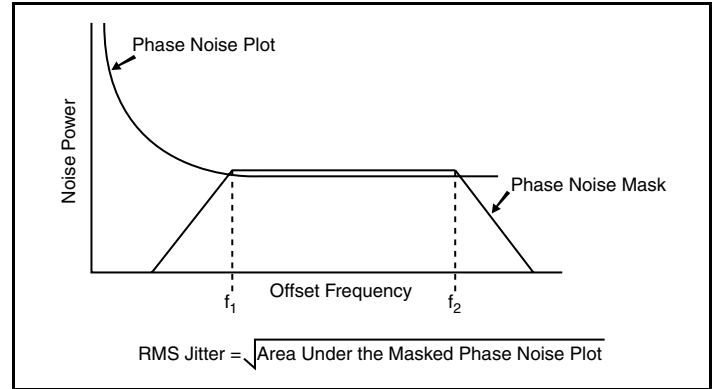
3.3V LVPECL Output Load AC Test Circuit



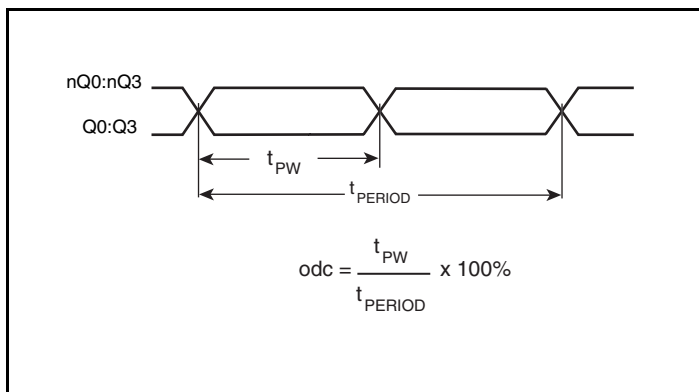
2.5V LVPECL Output Load AC Test Circuit



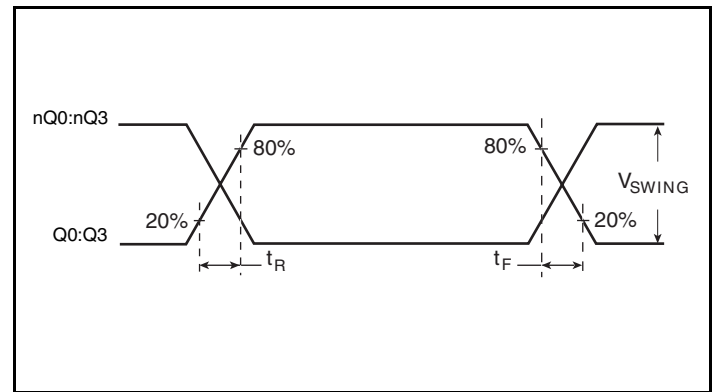
Output Skew



RMS Phase Jitter



Output Duty Cycle/Pulse Width/Period

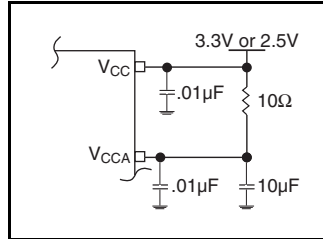


Output Rise/Fall Time

## Application Information

### Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS843004I-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{CC}$ ,  $V_{CCA}$  and  $V_{CCO}$  should be individually connected to the power supply plane through vias, and  $0.01\mu\text{F}$  bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic  $V_{CC}$  pin and also shows that  $V_{CCA}$  requires that an additional  $10\Omega$  resistor along with a  $10\mu\text{F}$  bypass capacitor be connected to the  $V_{CCA}$  pin.



**Figure 1. Power Supply Filtering**

### Recommendations for Unused Input and Output Pins

#### Inputs:

##### Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL\_IN and XTAL\_OUT can be left floating. Though not required, but for additional protection, a  $1\text{k}\Omega$  resistor can be tied from XTAL\_IN to ground.

##### TEST\_CLK Input

For applications not requiring the use of the clock, it can be left floating. Though not required, but for additional protection, a  $1\text{k}\Omega$  resistor can be tied from the TEST\_CLK to ground.

##### LVCMOS Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A  $1\text{k}\Omega$  resistor can be used.

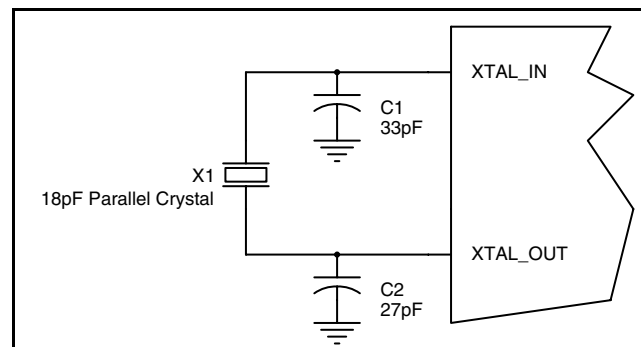
#### Outputs:

##### LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

### Crystal Input Interface

The ICS843004I-01 has been characterized with  $18\text{pF}$  parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a  $25\text{MHz}$ ,  $18\text{pF}$  parallel resonant crystal and were chosen to minimize the ppm error.

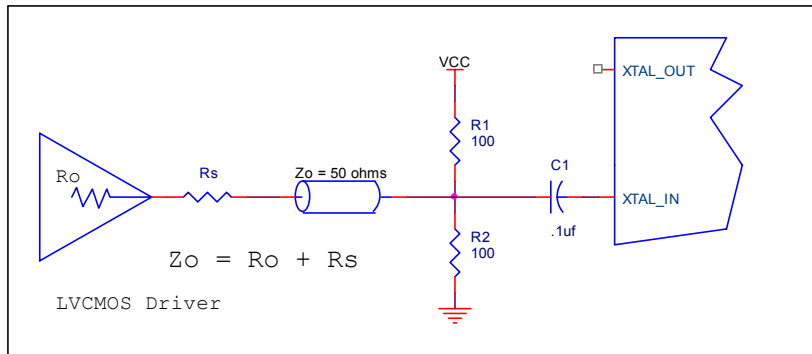


**Figure 2. Crystal Input Interface**

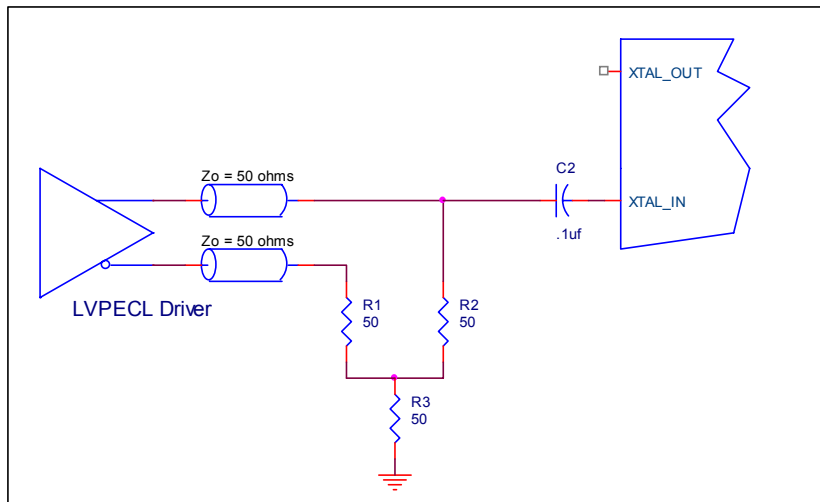
## Overdriving the XTAL Interface

The XTAL\_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL\_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 3A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This

can be done in one of two ways. First,  $R_1$  and  $R_2$  in parallel should equal the transmission line impedance. For most 50Ω applications,  $R_1$  and  $R_2$  can be 100Ω. This can also be accomplished by removing  $R_1$  and changing  $R_2$  to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 3B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL\_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.



**Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface**



**Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface**

## Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion.

*Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

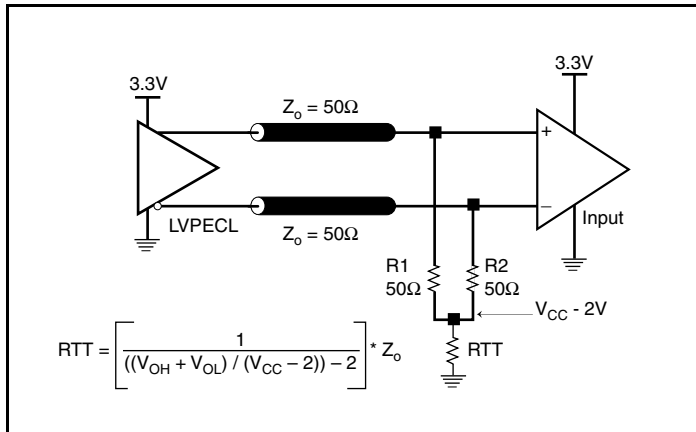


Figure 4A. 3.3V LVPECL Output Termination

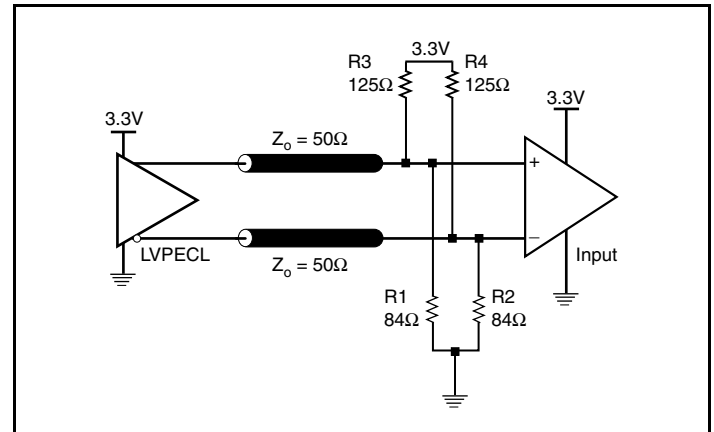


Figure 4B. 3.3V LVPECL Output Termination

## Termination for 2.5V LVPECL Outputs

Figure 5A and Figure 5B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating  $50\Omega$  to  $V_{CC} - 2V$ . For  $V_{CC} = 2.5V$ , the  $V_{CC} - 2V$  is very close to ground level.

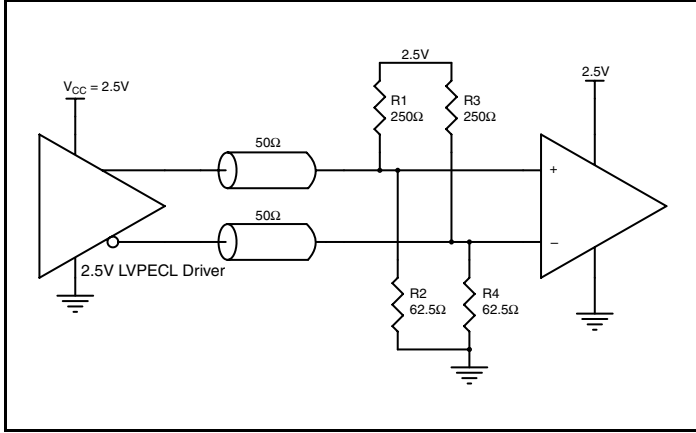


Figure 5A. 2.5V LVPECL Driver Termination Example

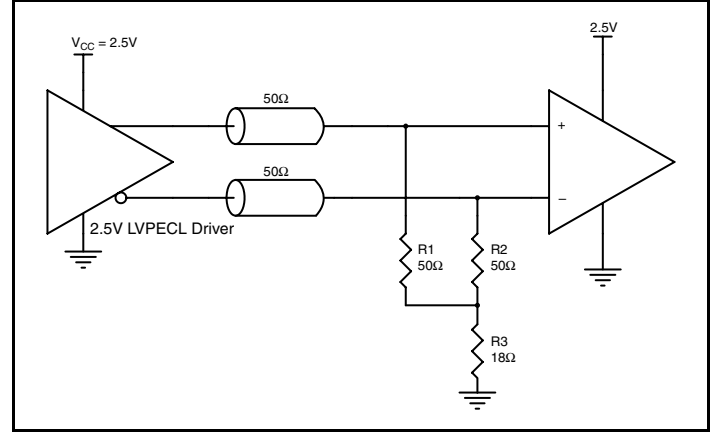


Figure 5B. 2.5V LVPECL Driver Termination Example

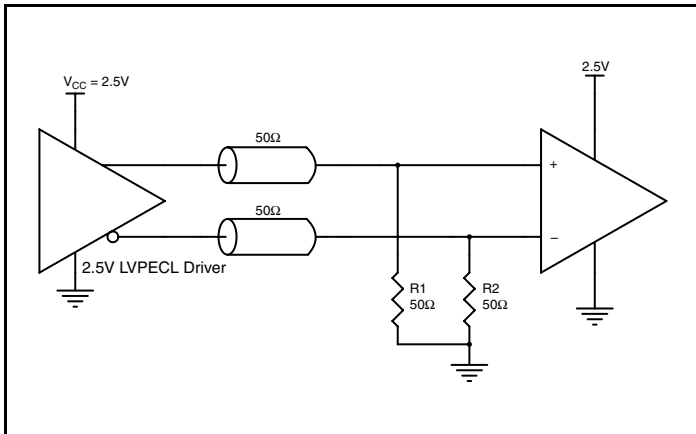


Figure 5C. 2.5V LVPECL Driver Termination Example

The R3 in Figure 5B can be eliminated and the termination is shown in Figure 5C.

## Layout Guideline

Figure 6 shows a schematic example of the ICS843004I-01. An example of LVEPCL termination is shown in this schematic. Additional LVPECL termination approaches are shown in the LVPECL Termination Application Note. In this example, an 18pF

parallel resonant 25MHz crystal is used. The C1= 27pF and C2 = 33pF are recommended for frequency accuracy. For a different board layout, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy.

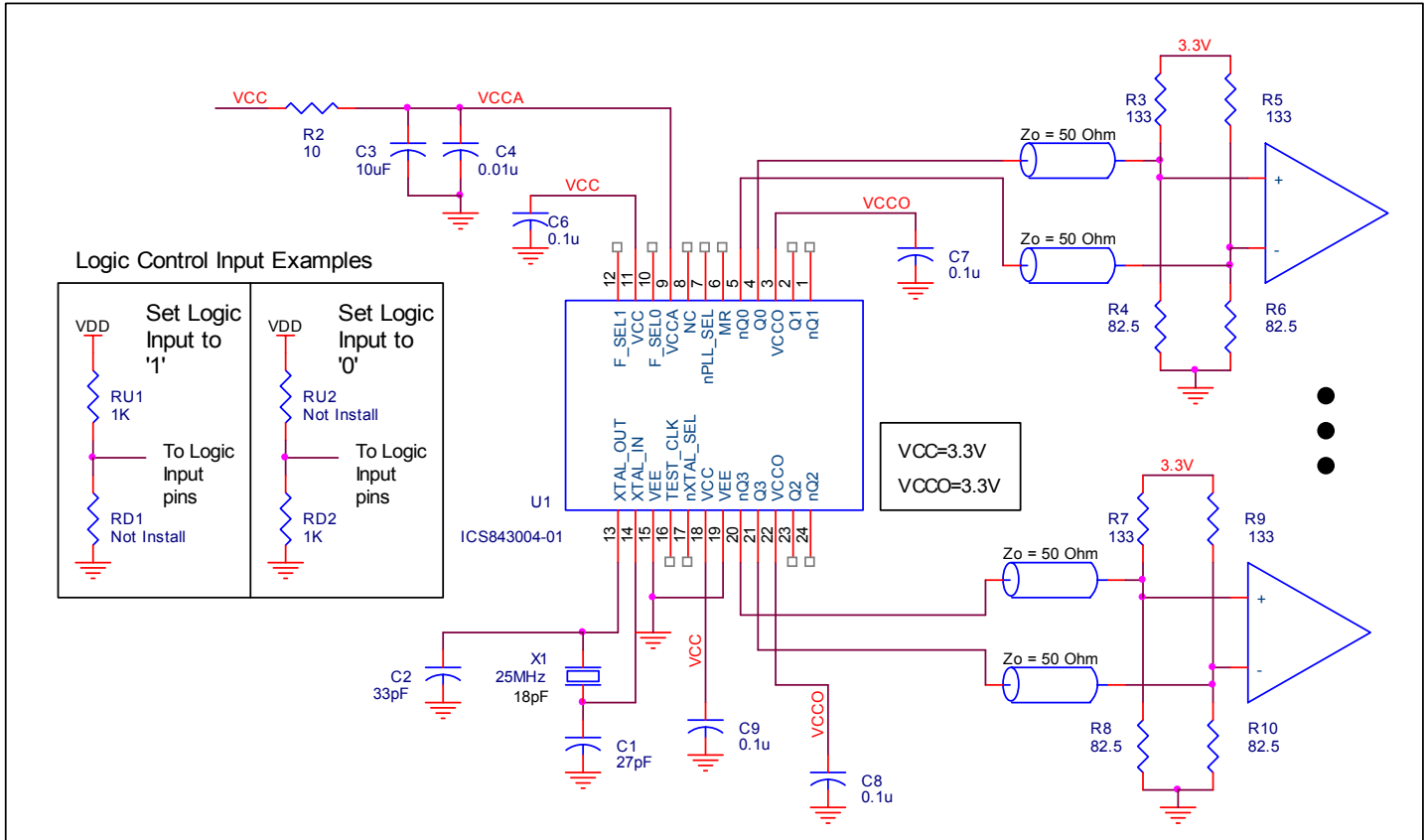


Figure 6. ICS843004I-01 Schematic Example

## Power Considerations

This section provides information on power dissipation and junction temperature for the ICS843004I-01. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS843004I-01 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 130mA = \mathbf{450.45mW}$
- Power (outputs)<sub>MAX</sub> = **30mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $4 * 30mW = \mathbf{120mW}$

**Total Power**<sub>MAX</sub> (3.465V, with all outputs switching) =  $450.45mW + 120mW = \mathbf{570.45mW}$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 65°C/W per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 0.570W * 65^\circ\text{C/W} = 122^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

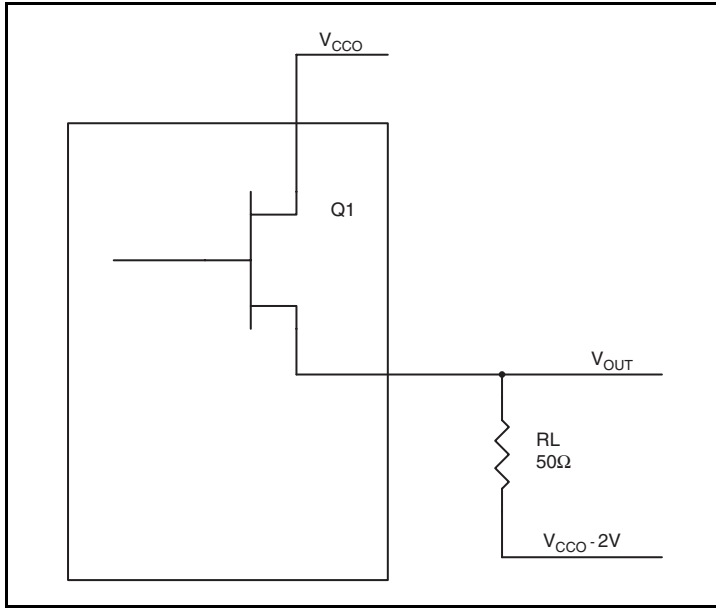
**Table 6. Thermal Resistance  $\theta_{JA}$  for 24 Lead TSSOP, Forced Convection**

| $\theta_{JA}$ vs. Air Flow                  |        |        |        |
|---------------------------------------------|--------|--------|--------|
| Meters per Second                           | 0      | 1      | 2.5    |
| Multi-Layer PCB, JEDEC Standard Test Boards | 70°C/W | 65°C/W | 62°C/W |

### 3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 7*.



**Figure 7. LVPECL Driver Circuit and Termination**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CCO} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CCO\_MAX} - 0.9V$   
 $(V_{CCO\_MAX} - V_{OH\_MAX}) = 0.9V$
- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CCO\_MAX} - 1.7V$   
 $(V_{CCO\_MAX} - V_{OL\_MAX}) = 1.7V$

$Pd\_H$  is power dissipation when the output drives high.

$Pd\_L$  is the power dissipation when the output drives low.

$$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = \mathbf{19.8mW}$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$$

$$\text{Total Power Dissipation per output pair} = Pd\_H + Pd\_L = \mathbf{30mW}$$

## Reliability Information

**Table 7.  $\theta_{JA}$  vs. Air Flow Table for a 24 Lead TSSOP**

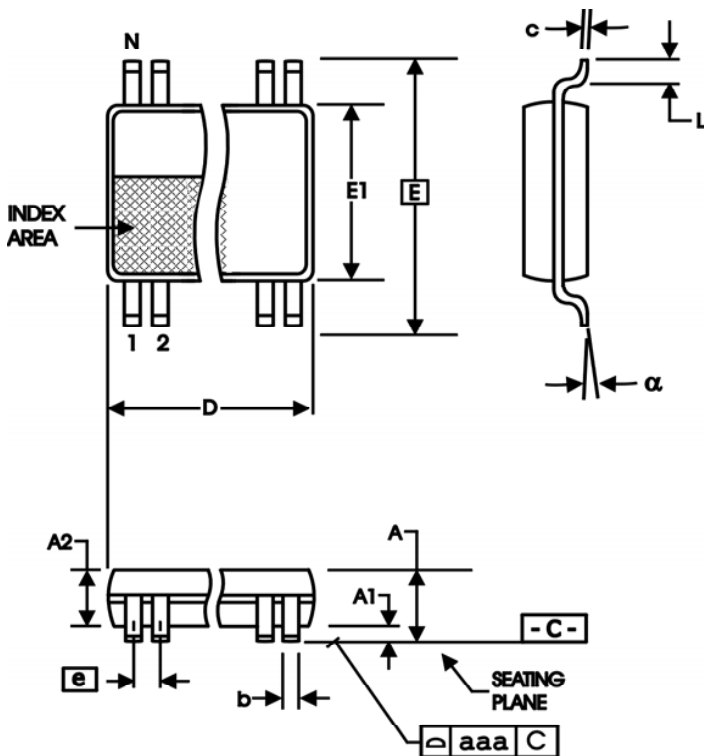
| $\theta_{JA}$ vs. Air Flow                  |        |        |        |
|---------------------------------------------|--------|--------|--------|
| Meters per Second                           | 0      | 1      | 2.5    |
| Multi-Layer PCB, JEDEC Standard Test Boards | 70°C/W | 65°C/W | 62°C/W |

## Transistor Count

The transistor count for ICS843004I-01 is: 3183

## Package Outline and Package Dimensions

**Package Outline - G Suffix for 24 Lead TSSOP**



**Table 8. Package Dimensions**

| All Dimensions in Millimeters |            |         |
|-------------------------------|------------|---------|
| Symbol                        | Minimum    | Maximum |
| N                             | 24         |         |
| A                             |            | 1.20    |
| A1                            | 0.5        | 0.15    |
| A2                            | 0.80       | 1.05    |
| b                             | 0.19       | 0.30    |
| c                             | 0.09       | 0.20    |
| D                             | 7.70       | 7.90    |
| E                             | 6.40 Basic |         |
| E1                            | 4.30       | 4.50    |
| e                             | 0.65 Basic |         |
| L                             | 0.45       | 0.75    |
| $\alpha$                      | 0°         | 8°      |
| aaa                           |            | 0.10    |

Reference Document: JEDEC Publication 95, MO-153

## Ordering Information

Table 9. Ordering Information

| Part/Order Number | Marking       | Package                   | Shipping Packaging | Temperature   |
|-------------------|---------------|---------------------------|--------------------|---------------|
| 843004AGI-01      | ICS843004AI01 | 24 Lead TSSOP             | Tube               | -40°C to 85°C |
| 843004AGI-01T     | ICS843004AI01 | 24 Lead TSSOP             | 2500 Tape & Reel   | -40°C to 85°C |
| 843004AGI-01LF    | ICS43004AI01L | "Lead-Free" 24 Lead TSSOP | Tube               | -40°C to 85°C |
| 843004AGI-01LFT   | ICS43004AI01L | "Lead-Free" 24 Lead TSSOP | 2500 Tape & Reel   | -40°C to 85°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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## Revision History Sheet

| Rev | Table    | Page | Description of Change                                                                                                         | Date    |
|-----|----------|------|-------------------------------------------------------------------------------------------------------------------------------|---------|
| B   | T3E      | 4    | Added 2.5V LVPECL DC Characteristics Table.                                                                                   | 4/22/09 |
|     |          | 10   | Added <i>LVC MOS to XTAL Interface</i> section.                                                                               |         |
|     | T9       | 17   | Ordering Information Table - added Lead-Free marking.                                                                         |         |
| B   | T1       | 2    | Pin Description Table - revised pin 7 description.                                                                            | 8/11/09 |
|     | T3D, T3E | 4    | LVPECL Tables - corrected $V_{OH}/V_{OL}$ Parameter rows from current to voltage and corrected units from $\mu A$ to V.       |         |
|     |          | 10   | LVC MOS to XTAL Interface section - added sentence to end.                                                                    |         |
|     |          | 14   | Power Considerations, 2. Junction Temperature - reworded sentence.                                                            |         |
|     | T9       | 17   | Ordering Information Table - corrected Temperature column from -30 to -40.<br>Updated header/footer of datasheet.             |         |
| B   |          | 6    | 156.25MHz Phase Noise Plot - corrected filter from Fibre Channel to 10Gb Ethernet and corrected typo 1.875MHz from 1.875MkHz. | 1/26/10 |
| B   |          | 10   | Updated Overdriving the XTAL Interface application note.                                                                      | 3/24/11 |
|     | T9       | 17   | Ordering Information Table - corrected LF marking.                                                                            |         |

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