

DATA SHEET

74LVT16543A

**3.3V LVT 16-bit registered transceiver
(3-State)**

Product specification
Supersedes data of 19
IC23 Data Handbook

1998 Feb 19

3.3V 16-bit registered transceiver (3-State)

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FEATURES

- 16-bit universal bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74LVT16543A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

The 74LVT16543A contains two sets of eight D-type latches, with separate control pins for each set. Using data flow from A to B as an example, when the A-to-B Enable ($n\overline{EAB}$) input and the A-to-B Latch Enable ($n\overline{LEAB}$) input are Low, the A-to-B path is transparent.

A subsequent Low-to-High transition of the $n\overline{LEAB}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With $n\overline{EAB}$ and $n\overline{OEAB}$ both Low, the 3-State B output buffers are active and display the data present at the outputs of the A latches.

Control of data flow from B to A is similar, but using the $n\overline{EBA}$, $n\overline{LEBA}$, and $n\overline{OEBA}$ inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

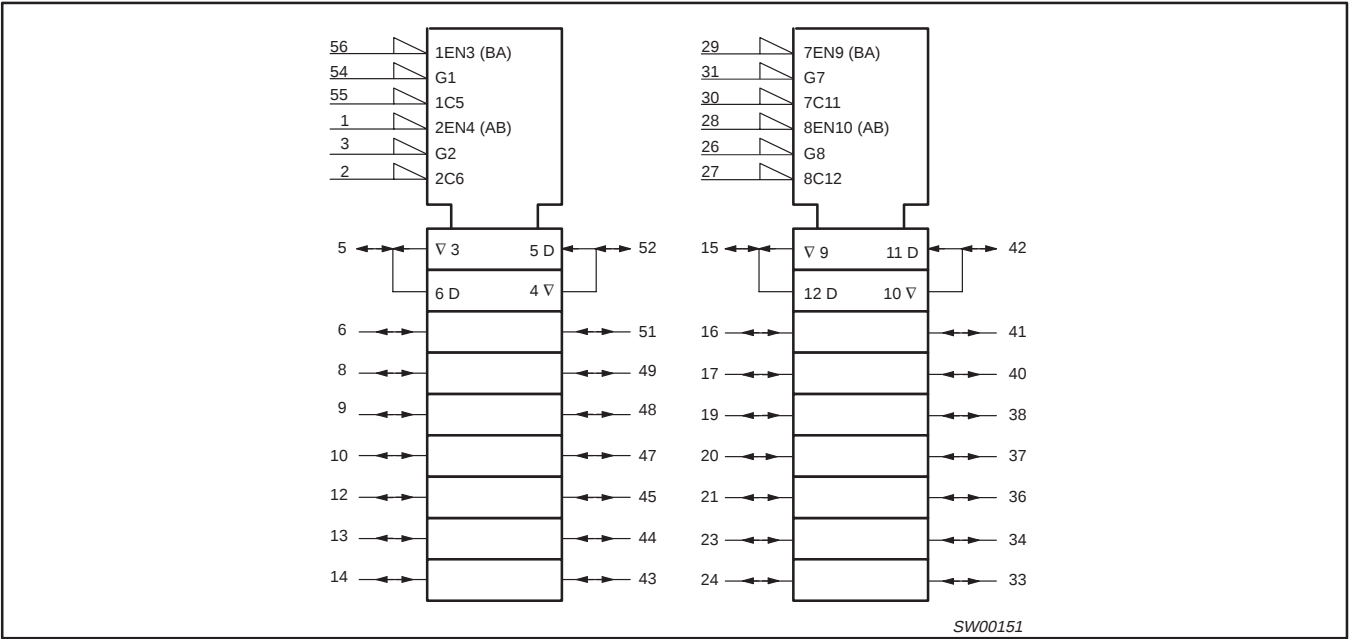
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}C$; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	$C_L = 50pF$; $V_{CC} = 3.3V$	2.2	ns
C_{IN}	Input capacitance control pins	$V_I = 0V$ or $3.0V$	3	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O} = 0V$ or $3.0V$	9	pF
I_{CCZ}	Total supply current	Outputs disabled; $V_{CC} = 3.6V$	70	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	$-40^{\circ}C$ to $+85^{\circ}C$	74LVT16543A DL	VT16543A DL	SOT371-1
56-Pin Plastic TSSOP Type II	$-40^{\circ}C$ to $+85^{\circ}C$	74LVT16543A DGG	VT16543A DGG	SOT364-1

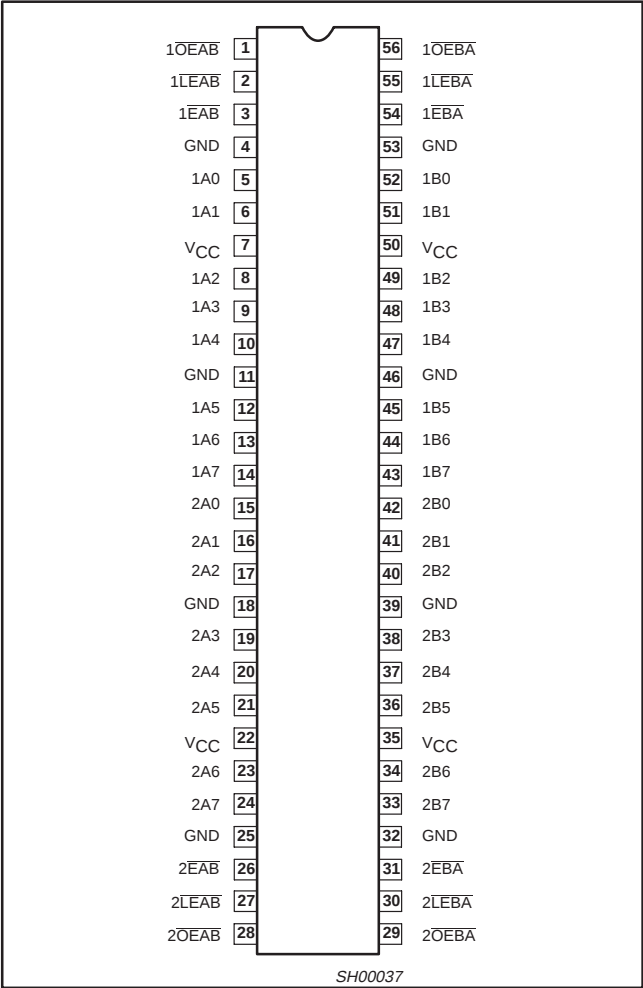
LOGIC SYMBOL (IEEE/IEC)



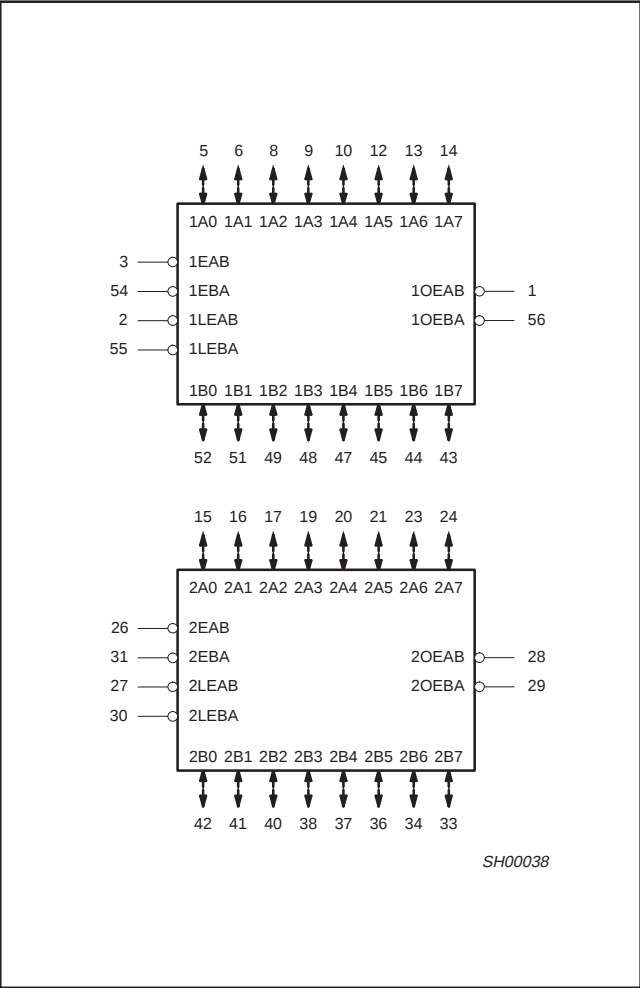
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PIN CONFIGURATION



LOGIC SYMBOL



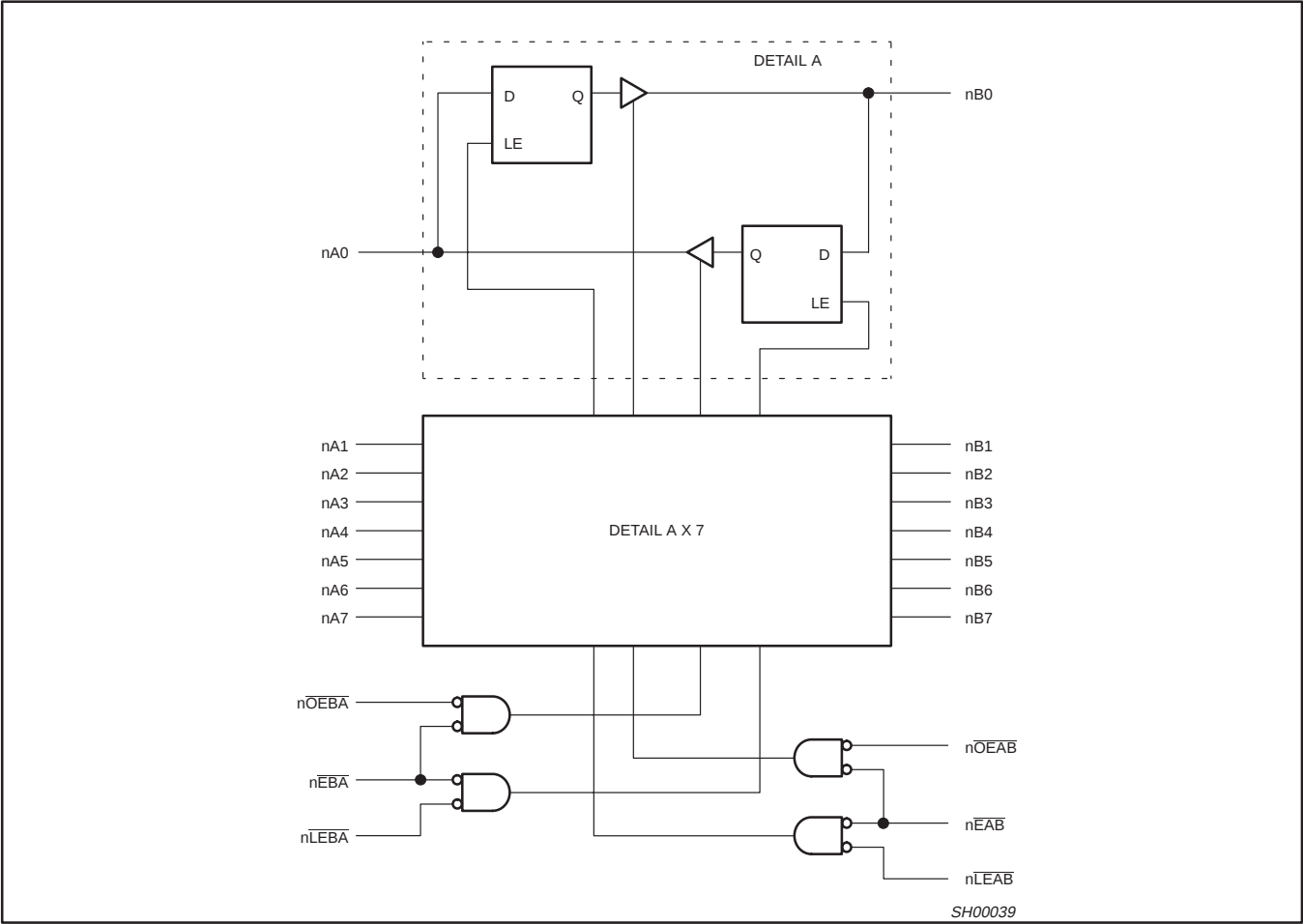
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24	1A0 – 1A7, 2A0 – 2A7	A Data inputs/outputs
52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33	1B0 – 1B7, 2B0 – 2B7	B Data inputs/outputs
1, 56 28, 29	1OEAB, 1OEBA, 2OEAB, 2OEBA	A to B / B to A Output Enable inputs (active-Low)
3, 54 26, 31	1EAB, 1EBA, 2EAB, 2EBA	A to B / B to A Enable inputs (active-Low)
2, 55 27, 30	1LEAB, 1LEBA, 2LEAB, 2LEBA	A to B / B to A Latch Enable inputs (active-Low)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V _{CC}	Positive supply voltage

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LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
nOE $\overline{\text{XX}}$	nE $\overline{\text{XX}}$	nLE $\overline{\text{XX}}$	nAx or nBx	nBx or nAx	
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disabled
L	$\uparrow$	L	h	Z	Disabled + Latch
L	$\uparrow$	L	l	Z	
L	L	$\uparrow$	h	H	Latch + Display
L	L	$\uparrow$	l	L	
L	L	L	H	H	Transparent
L	L	L	L	L	
L	L	H	X	NC	Hold

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High transition of nLE $\overline{\text{XX}}$ or nE $\overline{\text{XX}}$ (XX = AB or BA)
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High transition of nLE $\overline{\text{XX}}$ or nE $\overline{\text{XX}}$ (XX = AB or BA)
X = Don't care
 $\uparrow$ = Low-to-High transition of nLE $\overline{\text{XX}}$ or nE $\overline{\text{XX}}$ (XX = AB or BA)
NC= No change
Z = High impedance or "off" state

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ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	−50	mA
V_I	DC input voltage ³		−0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage ³	Output in Off or High state	−0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	−64	
T_{stg}	Storage temperature range		−65 to +150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; $f \geq 1\text{kHz}$		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP ¹	MAX	
V _{IK}	Input clamp voltage	V _{CC} = 2.7V; I _{IK} = −18mA			−0.85	−1.2	V
V _{OH}	High-level output voltage	V _{CC} = 2.7 to 3.6V; I _{OH} = −100μA		V _{CC} −0.2	V _{CC}		V
		V _{CC} = 2.7V; I _{OH} = −8mA		2.4	2.54		
		V _{CC} = 3.0V; I _{OH} = −32mA		2.0	2.36		
V _{OL}	Low-level output voltage	V _{CC} = 2.7V; I _{OL} = 100μA			0.07	0.2	V
		V _{CC} = 2.7V; I _{OL} = 24mA			0.3	0.5	
		V _{CC} = 3.0V; I _{OL} = 16mA			0.2	0.4	
		V _{CC} = 3.0V; I _{OL} = 32mA			0.3	0.5	
		V _{CC} = 3.0V; I _{OL} = 64mA			0.35	0.55	
V _{RST}	Power-up output low voltage ⁵	V _{CC} = 3.6V; I _O = 1mA; V _I = GND or V _{CC}			0.13	0.55	V
I _I	Input leakage current	V _{CC} = 3.6V; V _I = V _{CC} or GND	Control pins		0.1	±1	μA
		V _{CC} = 0 or 3.6V; V _I = 5.5V			0.1	10	
		V _{CC} = 3.6V; V _I = 5.5V	I/O Data pins ⁴		0.5	20	
		V _{CC} = 3.6V; V _I = V _{CC}			0.5	10	
		V _{CC} = 3.6V; V _I = 0			1.0	−5	
I _{OFF}	Output off current	V _{CC} = 0V; V _I or V _O = 0 to 4.5V			1.0	±100	μA
I _{HOLD}	Bus Hold current A or B outputs ⁷	V _{CC} = 3V; V _I = 0.8V		75	130		μA
		V _{CC} = 3V; V _I = 2.0V		−75	−140		
		V _{CC} = 0V to 3.6V; V _{CC} = 3.6V		±500			
I _{EX}	Current into an output in the High state when V _O > V _{CC}	V _O = 5.5V; V _{CC} = 3.0V			45	125	μA
I _{PU/PD}	Power up/down 3-State output current ³	V _{CC} ≤ 1.2V; V _O = 0.5V to V _{CC} ; V _I = GND or V _{CC} ; OE/OE = Don't care			35	±100	μA
I _{CCH}	Quiescent supply current	V _{CC} = 3.6V; Outputs High, V _I = GND or V _{CC} , I _O = 0			0.07	0.12	mA
I _{CCL}		V _{CC} = 3.6V; Outputs Low, V _I = GND or V _{CC} , I _O = 0			4.5	6	
I _{CCZ}		V _{CC} = 3.6V; Outputs Disabled; V _I = GND or V _{CC} , I _O = 0 ⁶			0.07	0.12	
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 3V to 3.6V; One input at V _{CC} −0.6V, Other inputs at V _{CC} or GND			0.1	0.2	mA

NOTES:

1. All typical values are at $V_{CC} = 3.3V$ and .
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND .
3. This parameter is valid for any V_{CC} between $0V$ and $1.2V$ with a transition time of up to $10msec$. From $V_{CC} = 1.2V$ to $V_{CC} = 3.3V \pm 0.3V$ a transition time of $100\mu sec$ is permitted. This parameter is valid for $T_{amb} = 25^\circ C$ only.
4. Unused pins at V_{CC} or GND .
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
6. I_{CCZ} is measured with outputs pulled to V_{CC} or GND .
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

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AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$; $T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$	
			MIN	TYP ¹	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	2	1.0 1.0	2.2 2.2	3.7 3.7	4.4 4.4	ns
t_{PLH} t_{PHL}	Propagation delay nLEBA to nAx, nLEAB to nBx	1 2	1.5 1.5	2.7 2.7	4.8 4.8	6.2 6.2	ns
t_{PZH} t_{PZL}	Output enable time nOEBA to nAx, nOEAB to nBx	4 5	1.5 1.5	2.8 2.6	4.6 5.0	6.1 6.6	ns
t_{PHZ} t_{PLZ}	Output disable time nOEBA to nAx, nOEAB to nBx	4 5	2.0 2.0	3.1 3.2	5.2 4.6	5.7 4.7	ns
t_{PZH} t_{PZL}	Output enable time nEBA to nAx, nEAB to nBx	4 5	1.5 1.5	2.9 2.6	4.8 5.1	6.1 6.6	ns
t_{PHZ} t_{PLZ}	Output disable time nEBA to nAx, nEAB to nBx	4 5	2.0 2.0	3.1 3.2	5.1 4.3	5.7 4.5	ns

NOTE:

1. All typical values are at $V_{CC} = 3.3V$ and $T_{\text{amb}} = 25^\circ\text{C}$.

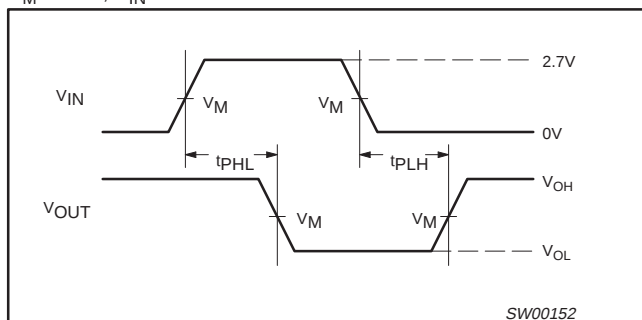
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$; $T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

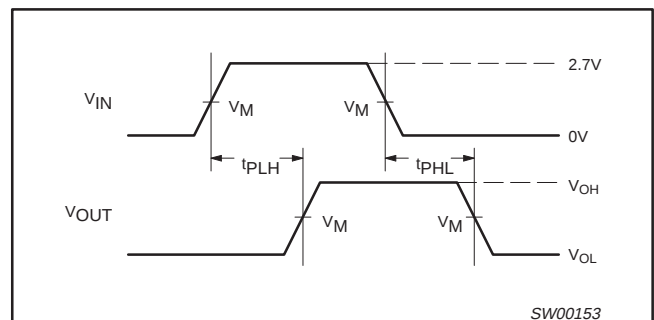
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$	
			MIN	TYP	MIN	
$t_s(H)$ $t_s(L)$	Setup time nAx to nLEAB, nBx to nLEBA	3	0.8 1.0	0.4 0.1	0.5 1.5	ns
$t_h(H)$ $t_h(L)$	Hold time nAx to nLEAB, nBx to nLEBA	3	1.0 1.2	0.2 0.4	0.5 1.3	ns
$t_s(H)$ $t_s(L)$	Setup time nAx to nEAB, nBx to nEBA	3	0.7 1.3	0.1 0.1	0.4 1.5	ns
$t_h(H)$ $t_h(L)$	Hold time nAx to nEAB, nBx to nEBA	3	1.2 1.3	0.2 0.4	0.8 1.4	ns
$t_W(L)$	Latch enable pulse width, Low	3	1.8	1.0	1.8	ns

AC WAVEFORMS

$V_M = 1.5V$, $V_{IN} = \text{GND to } 3.0V$



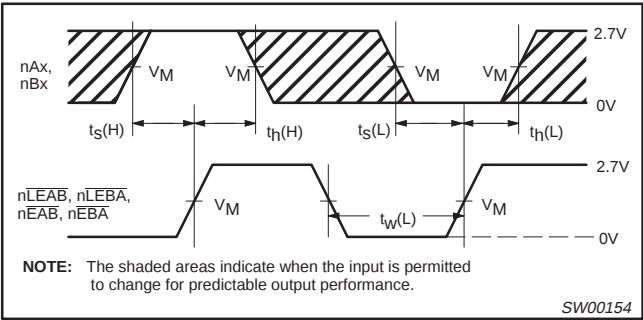
Waveform 1. Propagation Delay For Inverting Output



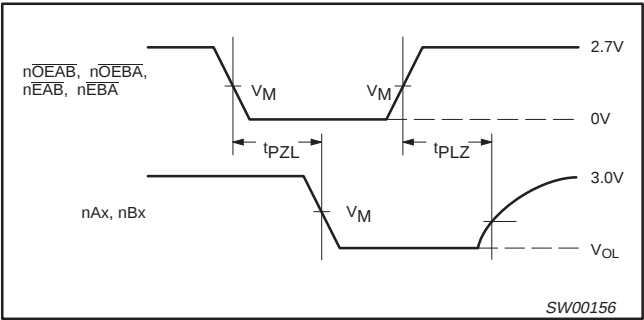
Waveform 2. Propagation Delay For Non-Inverting Output

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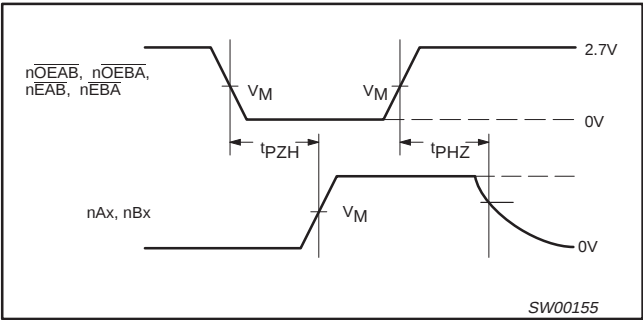
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Waveform 3. Data Setup and Hold Times and Latch Enable Pulse Width

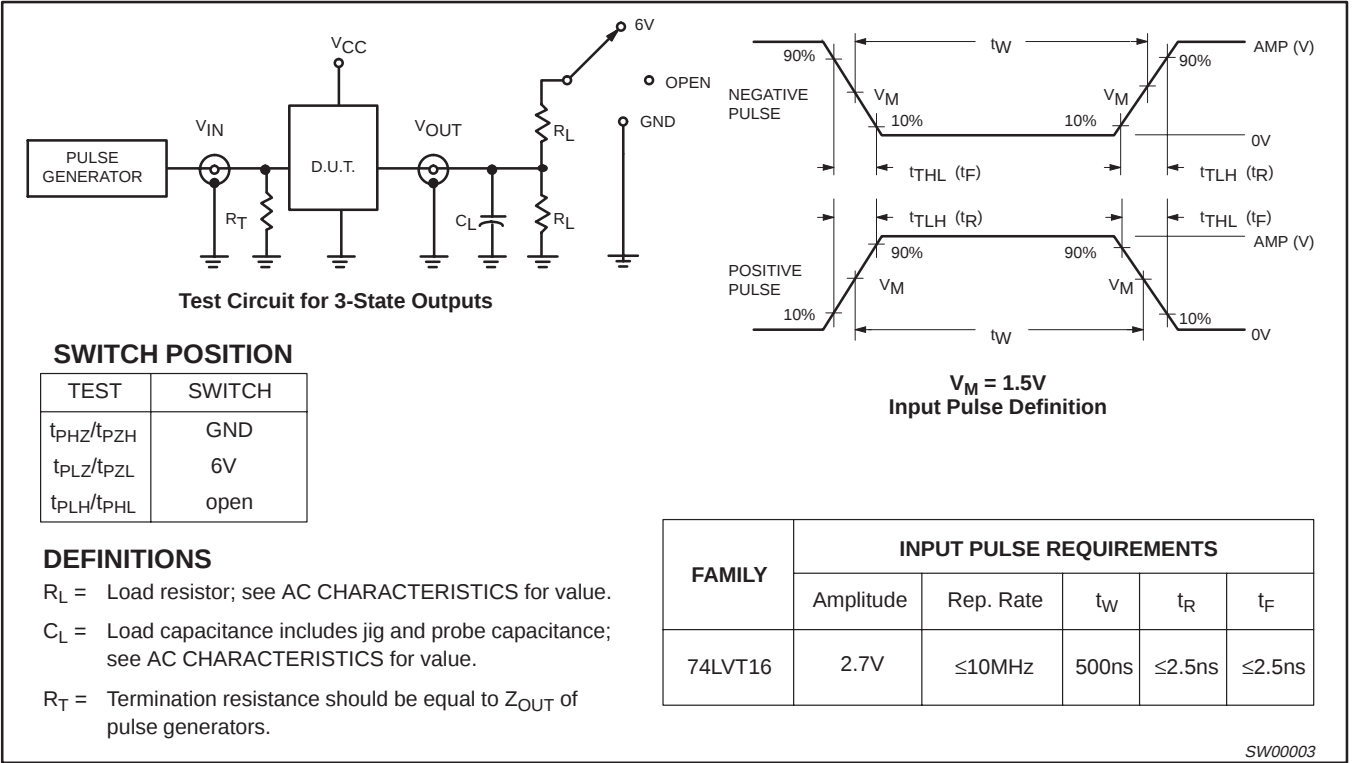


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level



Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

TEST CIRCUIT AND WAVEFORMS

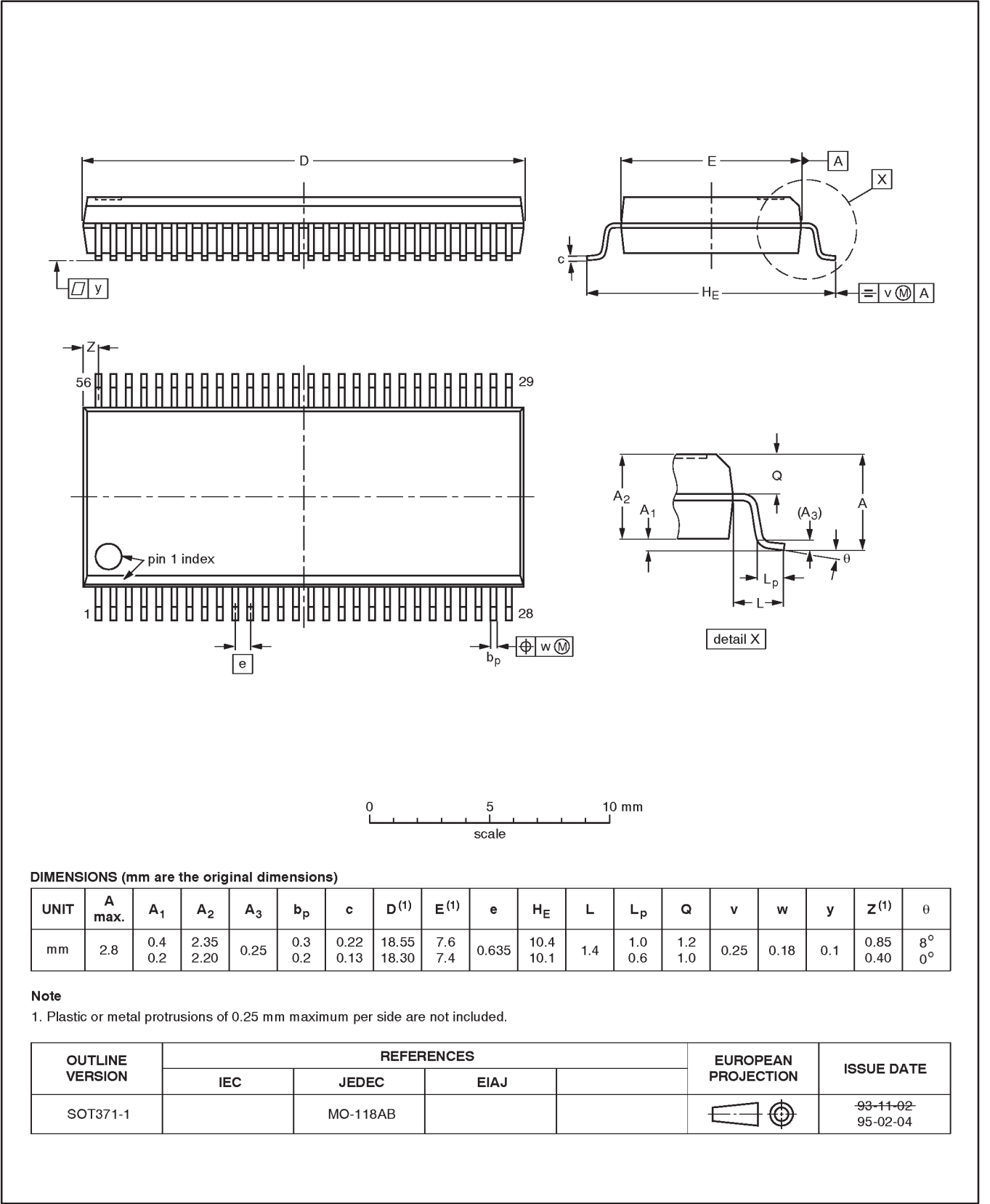


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SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1

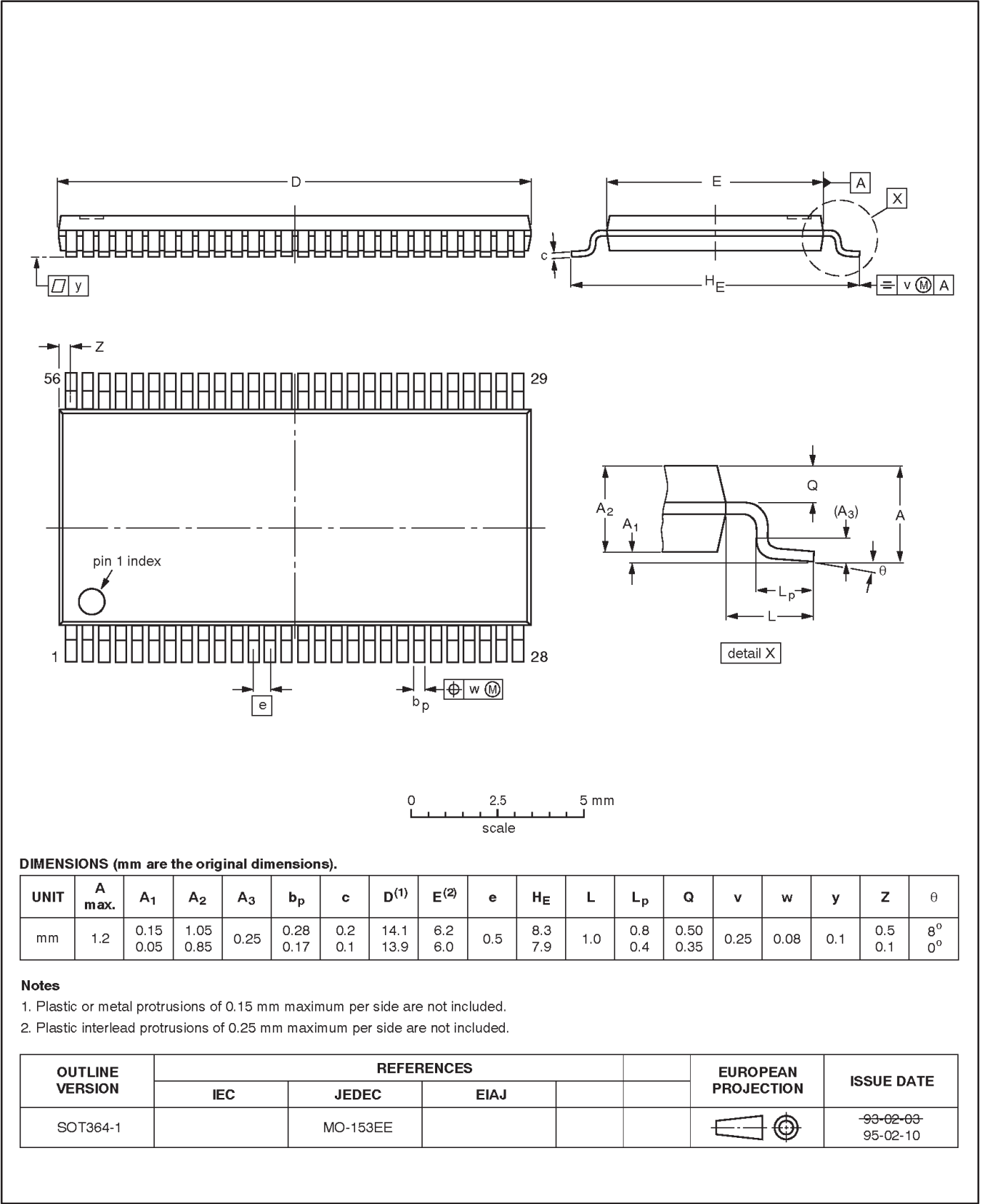


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TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1



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NOTES

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088-3409
Telephone 800-234-7381

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