# CURRENT-LIMITED, POWER-DISTRIBUTION SWITCHES

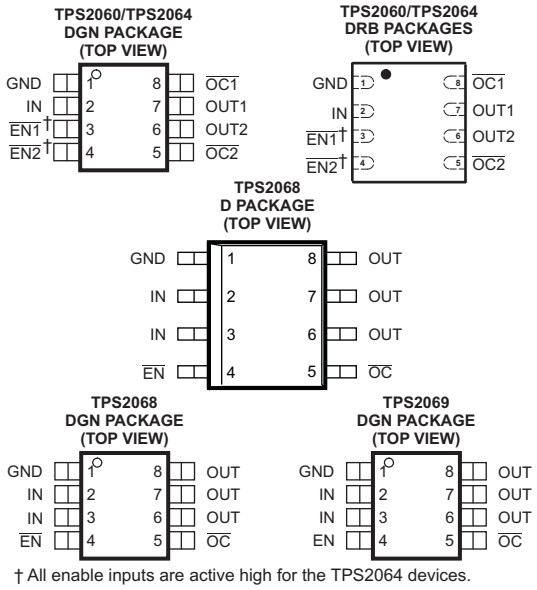
**Check for Samples: TPS2060, TPS2064, TPS2068, TPS2069**

## FEATURES

- **70-mΩ High-Side MOSFET**
- **1.5-A Continuous Current**
- **Thermal and Short-Circuit Protection**
- **Accurate Current Limit (1.6 A min, 2.6 A max)**
- **Operating Range: 2.7 V to 5.5 V**
- **0.6-ms Typical Rise Time**
- **Undervoltage Lockout**
- **Deglitched Fault Report ($\overline{OC}$)**
- **No $\overline{OC}$ Glitch During Power Up**
- **1-µA Maximum Standby Supply Current**
- **Reverse Current Blocking**
- **TPS2060/64 Temperature Range: 0°C to 70°C**
- **TPS2068/69 DGN Package Temperature Range: –40°C to 85°C**
- **TPS2068 D Package Temperature Range: 0°C to 70°C**
- **UL Listed – File No. E169910**
- **TPS2068/69: CB Certified**

## APPLICATIONS

- **Heavy Capacitive Loads**
- **Short-Circuit Protections**




† All enable inputs are active high for the TPS2064 devices.

## DESCRIPTION

The TPS206x power-distribution switches are intended for applications where heavy capacitive loads and short-circuits are likely to be encountered. This device incorporates 70-mΩ N-channel MOSFET power switches for power-distribution systems that require single or dual power switches in a single package. Each switch is controlled by a logic enable input. Gate drive is provided by an internal charge pump designed to control the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

When the output load exceeds the current-limit threshold or a short is present, the device limits the output current to a safe level by switching into a constant-current mode, pulling the overcurrent ($\overline{OCx}$) logic output low. When continuous heavy overloads and short-circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal protection circuit shuts off the switch to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures that the switch remains off until valid input voltage is present. Current limit is typically 2.1 A.

**GENERAL SWITCH CATALOG**

| 33 mΩ, Single | | 80 mΩ, Single | | 80 mΩ, Dual | | 80 mΩ, Dual | | 80 mΩ, Triple | | 80 mΩ, Quad | | 80 mΩ, Quad | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS201xA | 0.2 A to 2 A | TPS2014 | 600 mA | TPS2042B | 500 mA | TPS2080 | 500 mA | TPS2043B | 500 mA | TPS2044B | 500 mA | TPS2085 | 500 mA |
| TPS202x | 0.2 A to 2 A | TPS2015 | 1 A | TPS2052B | 500 mA | TPS2081 | 500 mA | TPS2053B | 500 mA | TPS2054B | 500 mA | TPS2086 | 500 mA |
| TPS203x | 0.2 A to 2 A | TPS2041B | 500 mA | TPS2046B | 250 mA | TPS2082 | 500 mA | TPS2047B | 250 mA | TPS2048A | 250 mA | TPS2087 | 500 mA |
| | | TPS2051B | 500 mA | TPS2056 | 250 mA | TPS2090 | 250 mA | TPS2057A | 250 mA | TPS2058 | 250 mA | TPS2095 | 250 mA |
| | | TPS2045A | 250 mA | TPS2062 | 1 A | TPS2091 | 250 mA | TPS2063 | 1 A | | | TPS2096 | 250 mA |
| | | TPS2049 | 100 mA | TPS2066 | 1 A | TPS2092 | 250 mA | TPS2067 | 1 A | | | TPS2097 | 250 mA |
| | | TPS2055A | 250 mA | TPS2060 | 1.5 A | | | | | | | | |
| | | TPS2061 | 1 A | TPS2064 | 1.5 A | | | | | | | | |
| | | TPS2065 | 1 A | | | | | | | | | | |
| | | TPS2068 | 1.5 A | | | | | | | | | | |
| | | TPS2069 | 1.5 A | | | | | | | | | | |

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPad is a trademark of Texas Instruments.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## AVAILABLE OPTION AND ORDERING INFORMATION

| $T_A$ | ENABLE | RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT | TYPICAL SHORT-CIRCUIT CURRENT LIMIT AT 25°C | NUMBER OF SWITCHES | PACKAGED DEVICES (1) (2) | |
|---|---|---|---|---|---|---|
| | | | | | MSOP (DGN) | SON (DRB) |
| 0°C to 70°C | Active low | 1.5 A | 2.1 A | Dual | TPS2060DGN | TPS2060DRB |
| | Active high | | | | TPS2064DGN | TPS2064DRB |
| –40°C to 85°C | Active low | | | Single | TPS2068DGN | |
| | Active high | | | | TPS2069DGN | |
| 0°C to 70°C | Active low | | | Single | TPS2068D | |

(1) The package is available taped and reeled. Add an R suffix to device types (e.g., TPS2060DGN).
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

| | | | UNIT |
|---|---|---|---|
| $V_I$ | Input voltage range, $V_{I(IN)}$ | | –0.3 V to 6 V |
| | Input voltage range, $V_{I(/ENx)}$, $V_{I(ENx)}$ | | –0.3 V to 6 V |
| | Voltage range, $V_{I(/OC)}$, $V_{I(/OCx)}$ | | –0.3 V to 6 V |
| $V_O$ | Output voltage range, $V_{O(OUT)}$, $V_{O(OUTx)}$ | | –0.3 V to 6 V |
| $I_O$ | Continuous output current, $I_{O(OUT)}$, $I_{O(OUTx)}$ | | Internally limited |
| | Continuous total power dissipation | | See Dissipation Rating Table |
| $T_J$ | Operating virtual junction temperature range | TPS2060/64 | 0°C to 105°C |
| | | TPS2068/69 (DGN Package) | –40°C to 105°C |
| | | TPS2068 (D Package) | 0°C to 105°C |
| $T_{stg}$ | Storage temperature range | | –65°C to 150°C |
| ESD | Electrostatic discharge protection | Human body model MIL-STD-883C | 2 kV |
| | | Charge device model (CDM) | 500 V |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## DISSIPATING RATING TABLE(1)

| PACKAGE | THERMAL RESISTANCE $\theta_{JA}$ | $T_A$ < 25°C POWER RATING | DERATING FACTOR ABOVE $T_A$ = 25°C | $T_A$ = 70°C POWER RATING | $T_A$ = 85°C POWER RATING |
|---|---|---|---|---|---|
| DGN-8(2) | | 1370 mW | 17 mW/°C | 600 mW | 342 mW |
| D-8 | | 585.82 mW | 5.8582 mW/°C | 322.20 mW | 234.32 mW |
| DRB-8 (Low-K)(3) | 270 °CW | 370 mW | 3.71 mW/°C | 203 mW | 148 mW |
| DRB-8 (High-K)(4) | 60 °CW | 1600 mW | 16.67 mW/°C | 916 mW | 866 mW |

(1) Heatsink the PowerPad™per the recommendations of SLMA002. PCB used for recommendations per appendix A4.
(2) See *Recommended Operating Conditions* Table for PowerPad connection guidelines to meet qualifying conditions for CB Certificate.
(3) Soldered PowerPAD on a standard 2-layer PCB without vias for thermal pad. See TI application note SLMA002 for further details.
(4) Soldered PowerPAD on a standard 4-layer PCB with vias for thermal pad. See TI application note SLMA002 for further details.

## RECOMMENDED OPERATING CONDITIONS(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_I$ | Input voltage, $V_{I(IN)}$ | | 2.7 | 5.5 | V |
| | Input voltage, $V_{I(ENx)}$, $V_{I(/ENx)}$ | | 0 | 5.5 | V |
| $I_O$ | Continuous output current, $I_{O(OUTx)}$ | | 0 | 1.5 | A |
| $T_J$ | Operating virtual junction temperature | TPS2060/64 | 0 | 105 | °C |
| | | TPS2068/69 (DGN Package) | –40 | 105 | |
| | | TPS2068 (D Package) | 0 | 105 | |

(1) The PowerPad must be connected externally to GND pin to meet qualifying conditions for CB Certificate (DGN package only).

## ELECTRICAL CHARACTERISTICS

0°C ≤ $T_J$ ≤ 105°C for the TPS2060/64 and TPS2068 (D package), plus –40°C ≤ $T_J$ ≤ 105° for the TPS2068/69 (DGN package), $V_{I(IN)}$ = 5.5 V, $I_O$ = 1 A, $V_{I(/ENx)}$ = 0 V, or $V_{I(ENx)}$ = 5.5 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS(1) | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| **POWER SWITCH** | | | | | | | | |
| $r_{DS(on)}$ | Static drain-source on-state resistance, 5-V operation and 3.3-V operation | $V_{I(IN)}$ = 5 V or 3.3 V, $I_O$ = 1.5 A | | | | 70 | 115 | mΩ |
| | Static drain-source on-state resistance, 2.7-V operation | $V_{I(IN)}$ = 2.7 V, $I_O$ = 1.5 A | | | | 75 | 125 | mΩ |
| $t_r$ | Rise time, output | $V_{I(IN)}$ = 5.5 V | $C_L$ = 1 µF, $R_L$ = 5 Ω | $T_J$ = 25°C | | 0.6 | 1.5 | ms |
| | | $V_{I(IN)}$ = 2.7 V | | | | 0.4 | 1 | |
| $t_f$ | Fall time, output | $V_{I(IN)}$ = 5.5 V | | | 0.05 | | 0.5 | |
| | | $V_{I(IN)}$ = 2.7 V | | | 0.05 | | 0.5 | |
| **ENABLE INPUT $\overline{EN}$ OR EN** | | | | | | | | |
| $V_{IH}$ | High-level input voltage | 2.7 V < $V_{I(IN)}$ < 5.5 V | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | 2.7 V < $V_{I(IN)}$ < 5.5 V | | | | | 0.8 | |
| $I_I$ | Input current | $V_{I(/ENx)}$ = 0 V or 5.5 V, $V_{I(ENx)}$ = 0 V or 5.5 V | | | -0.5 | | 0.5 | µA |
| $t_{on}$ | Turnon time | $C_L$ = 100 µF, $R_L$ = 5 Ω | | | | | 3 | ms |
| $t_{off}$ | Turnoff time | $C_L$ = 100 µF, $R_L$ = 5 Ω | | | | | 10 | |
| **CURRENT LIMIT** | | | | | | | | |
| $I_{OS}$ | Short-circuit output current | $V_{I(IN)}$ = 5 V, OUT connected to GND, device enabled into short-circuit | | | 1.6 | 2.1 | 2.6 | A |
| $I_{OC\_TRIP}$ | Overcurrent trip threshold | $V_{I(IN)}$ = 5 V, Current ramp (≤ 100 A/s) on OUT | | TPS2060/64 | | 3.2 | 3.9 | A |
| | | | | TPS2068/69 | 2.3 | 2.85 | 3.4 | |
| $I_{OS}$ (2) | Short-circuit output current | $V_{I(IN)}$ = 5 V, OUT1 and OUT2 connected to GND, Device enabled into short-circuit, current measured at $V_{I(IN)}$ | | | 3.2 | 4.2 | 5.2 | A |
| $I_{OC\_TRIP}$ (2) | Overcurrent trip threshold TPS2060/64 | $V_{I(IN)}$ = 5 V, Current ramp (≤ 100 A/s) on OUT1 and OUT2 tied together, current measured at $V_{I(IN)}$ | | | | 6.4 | 7.8 | A |
| $I_{OL}$ | Supply current, low-level output | No load on OUT, $V_{I(/ENx)}$ = 5.5 V, or $V_{I(ENx)}$ = 0 V | | $T_J$ = 25°C | | 0.5 | 1 | µA |
| | | | | Over $T_J$ range | | 0.5 | 5 | |
| $I_{OH}$ | Supply current, high-level output TPS2060/64 | No load on OUT, $V_{I(/ENx)}$ = 0 V, or $V_{I(ENx)}$ = 5.5 V | | $T_J$ = 25°C | | 50 | 70 | µA |
| | | | | Over $T_J$ range | | 50 | 90 | |
| $I_{OH}$ | Supply current, high-level output TPS2068/69 | No load on OUT, $V_{I(/ENx)}$ = 0 V, or $V_{I(ENx)}$ = 5.5 V | | $T_J$ = 25°C | | 43 | 60 | µA |
| | | | | Over $T_J$ range | | 43 | 70 | |
| $I_{lkg}$ | Leakage current | OUT connected to ground, $V_{I(/ENx)}$ = 5.5 V, or $V_{I(ENx)}$ = 0 V | | | | 1 | | µA |
| | Reverse leakage current | $V_{I(OUTx)}$ = 5.5 V, IN = ground | | $T_J$ = 25°C | | 0.2 | | µA |
| **UNDERVOLTAGE LOCKOUT** | | | | | | | | |
| | Low-level input voltage, IN | | | | 2 | | 2.5 | V |
| | Hysteresis, IN | $T_J$ = 25°C | | | | 75 | | mV |

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
(2) This configuration has not been tested for UL certification.

## ELECTRICAL CHARACTERISTICS (continued)

0°C ≤ $T_J$ ≤ 105°C for the TPS2060/64 and TPS2068 (D package), plus –40°C ≤ $T_J$ ≤ 105° for the TPS2068/69 (DGN package), $V_{I(IN)}$ = 5.5 V, $I_O$ = 1 A, $V_{I(/ENx)}$ = 0 V, or $V_{I(ENx)}$ = 5.5 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS[1] | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OVERCURRENT $\overline{OCx}$** | | | | | | |
| $V_{OL(/OCx)}$ | Output low voltage | $I_{O(/OCx)}$ = 5 mA | | | 0.4 | V |
| | Off-state current | $V_{O(/OCx)}$ = 5 V or 3.3 V | | | 1 | µA |
| | $\overline{OC}$ deglitch | $\overline{OCx}$ assertion or deassertion | 4 | 8 | 15 | ms |
| **THERMAL SHUTDOWN[3]** | | | | | | |
| | Thermal shutdown threshold | | 135 | | | °C |
| | Recovery from thermal shutdown | | 125 | | | °C |
| | Hysteresis | | | 10 | | °C |

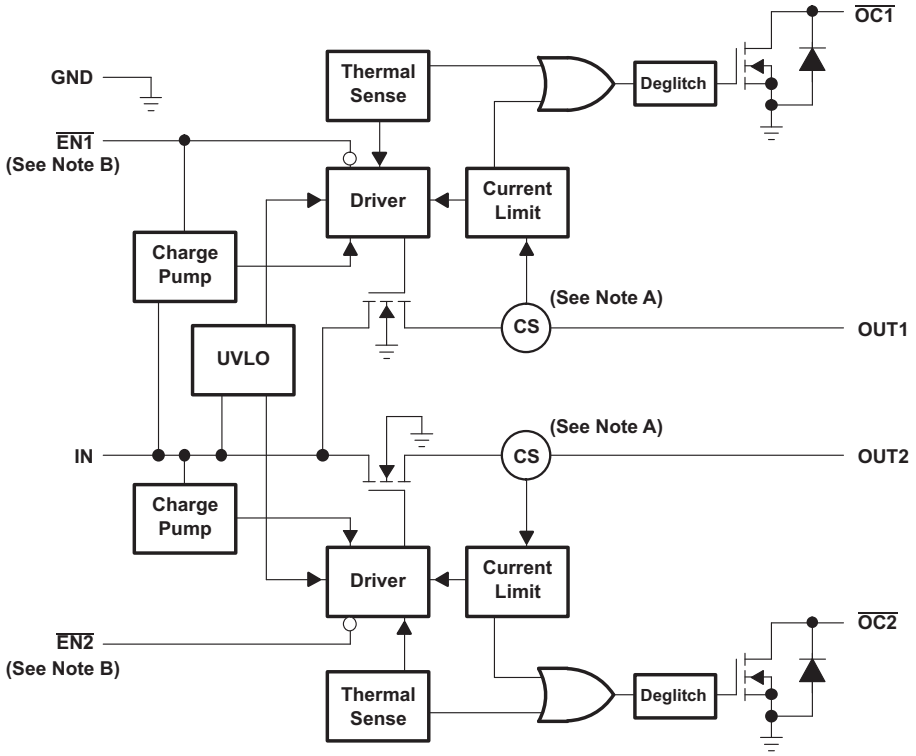
(3) The thermal shutdown only reacts under overcurrent conditions.

## DEVICE INFORMATION

### Pin Functions

| PINS | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| DGN and DRB PACKAGES | | | | |
| NAME | TPS2060 | TPS2064 | | |
| $\overline{EN1}$ | 3 | — | I | Enable input, logic low turns on power switch IN-OUT1 |
| $\overline{EN2}$ | 4 | — | I | Enable input, logic low turns on power switch IN-OUT2 |
| EN1 | — | 3 | I | Enable input, logic high turns on power switch IN-OUT1 |
| EN2 | — | 4 | I | Enable input, logic high turns on power switch IN-OUT2 |
| GND | 1 | 1 | | Ground |
| IN | 2 | 2 | I | Input voltage |
| $\overline{OC1}$ | 8 | 8 | O | Overcurrent, open-drain output, active low, IN-OUT1 |
| $\overline{OC2}$ | 5 | 5 | O | Overcurrent, open-drain output, active low, IN-OUT2 |
| OUT1 | 7 | 7 | O | Power-switch output, IN-OUT1 |
| OUT2 | 6 | 6 | O | Power-switch output, IN-OUT2 |
| | PowerPad | PowerPad | | Connect to GND |

## Functional Block Diagram (TPS2060 and TPS2064)




A. Current sense.

B. Active low ($\overline{ENx}$) for TPS2060. Active high (ENx) for TPS2064.

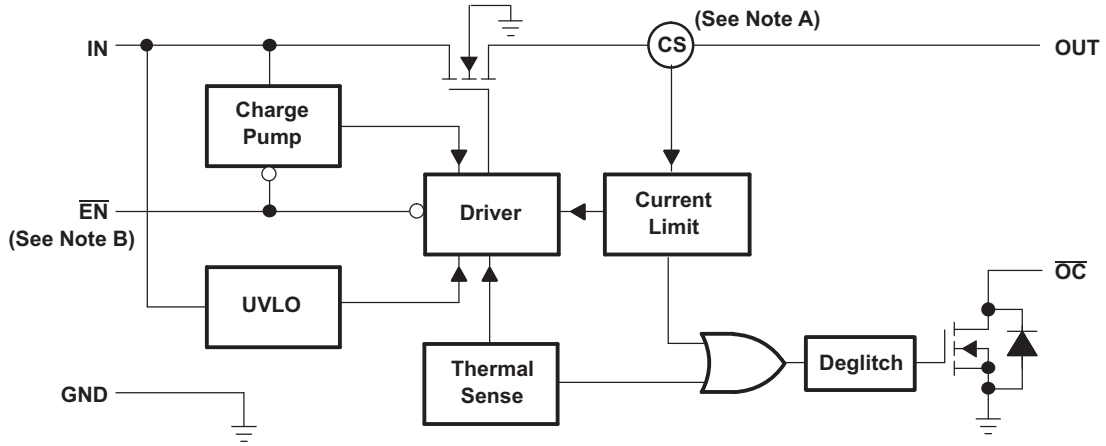
## DEVICE INFORMATION

### Pin Functions (TPS2068 and TPS2069)

| PINS | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | TPS2068 | TPS2069 | | |
| $\overline{EN}$ | 4 | — | I | Enable input, logic low turns on power switch |
| EN | — | 4 | I | Enable input, logic high turns on power switch |
| GND | 1 | 1 | | Ground |
| IN | 2, 3 | 2, 3 | I | Input voltage |
| $\overline{OC}$ | 5 | 5 | O | Overcurrent, open-drain output, active-low |
| OUT | 6, 7, 8 | 6, 7, 8 | O | Power-switch output |
| | PowerPad | PowerPad | | Connect to GND (DGN Package Only)(1) |

(1) See the *Recommended Operating Conditions* Table for PowerPad connection guidelines to meet qualifying conditions for CB Certificate (DGN package only).

### Functional Block Diagram (TPS2068 and TPS2069)




A. Current sense.

B. Active low ($\overline{EN}$) for TPS2068. Active high (EN) for TPS2069.

## PARAMETER MEASUREMENT INFORMATION

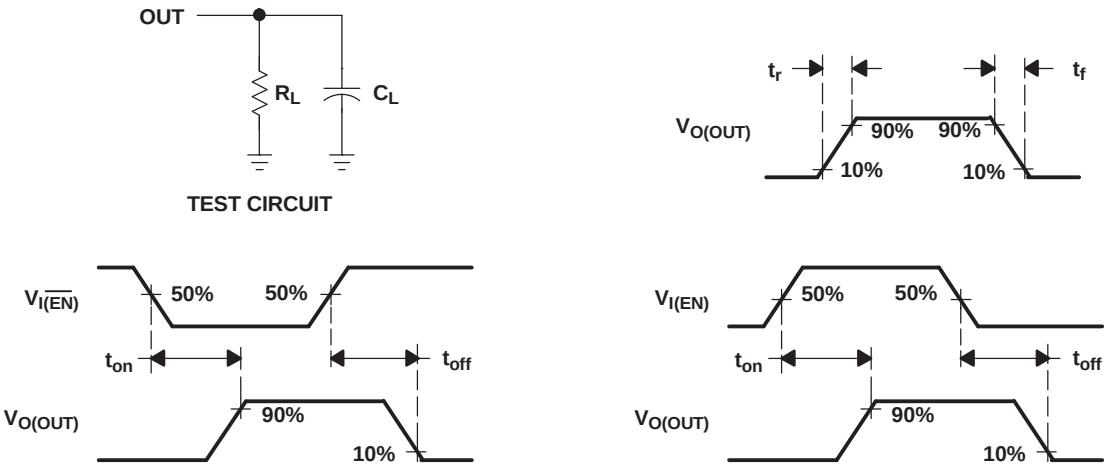



**Figure 1. Test Circuit and Voltage Waveforms**

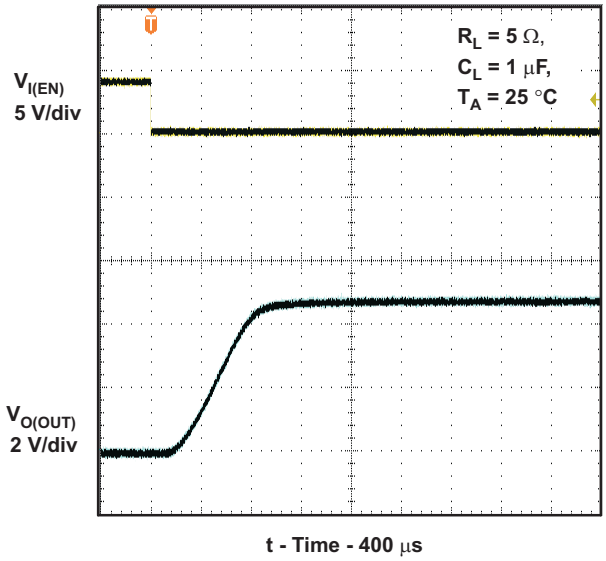



**Figure 2. Turnon Delay and Rise Time With 1-μF Load**

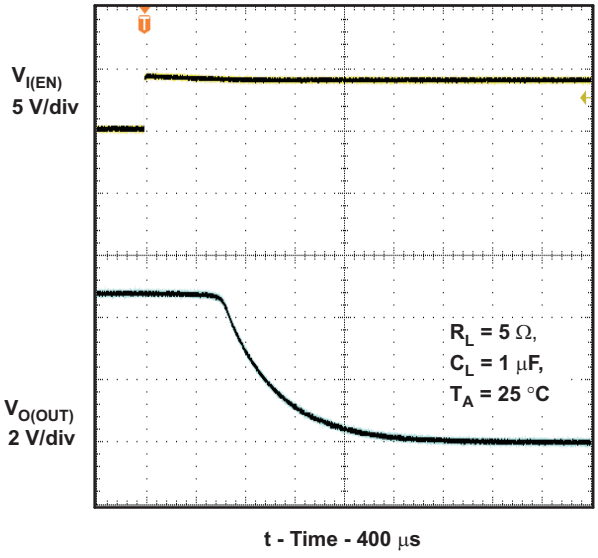



**Figure 3. Turnoff Delay and Fall Time With 1-μF Load**

## PARAMETER MEASUREMENT INFORMATION (continued)

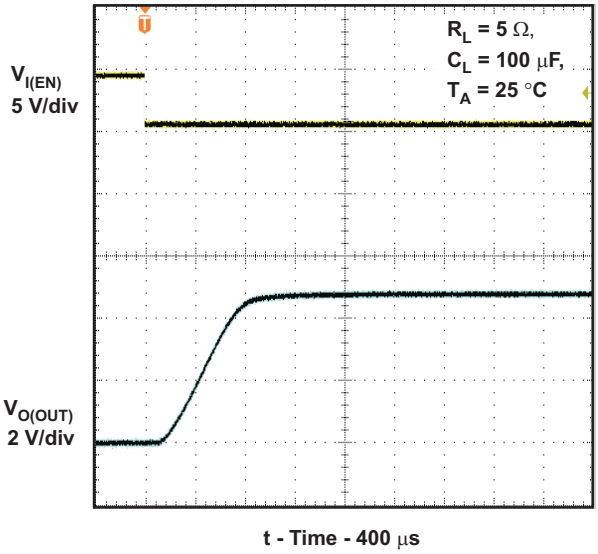



**Figure 4. Turnon Delay and Rise Time With 100-μF Load**

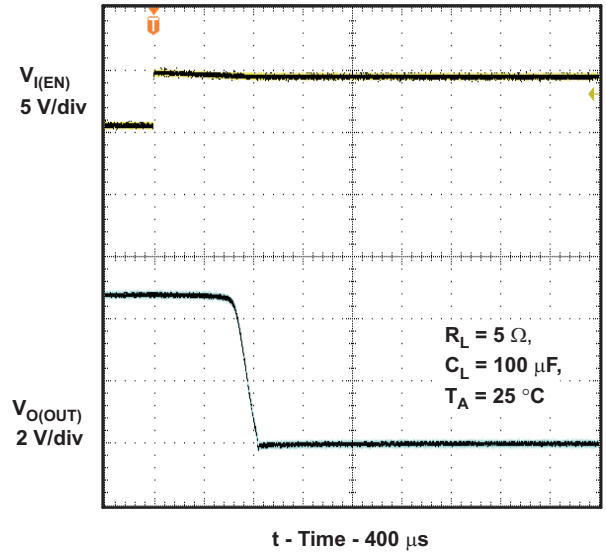



**Figure 5. Turnoff Delay and Fall Time With 100-μF Load**

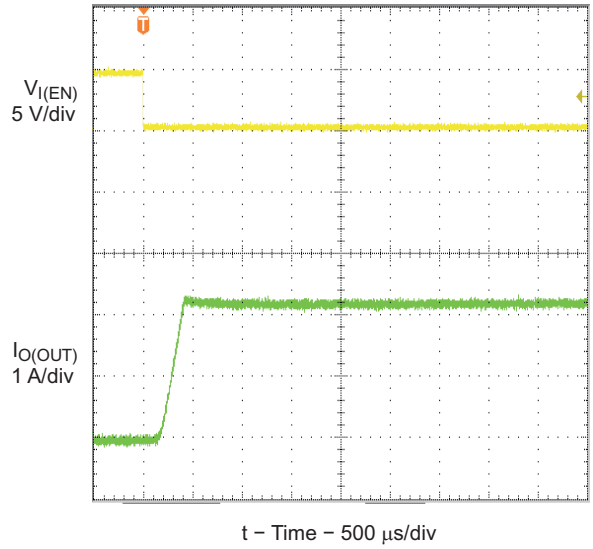



**Figure 6. Short-Circuit Current, Device Enabled Into Short**

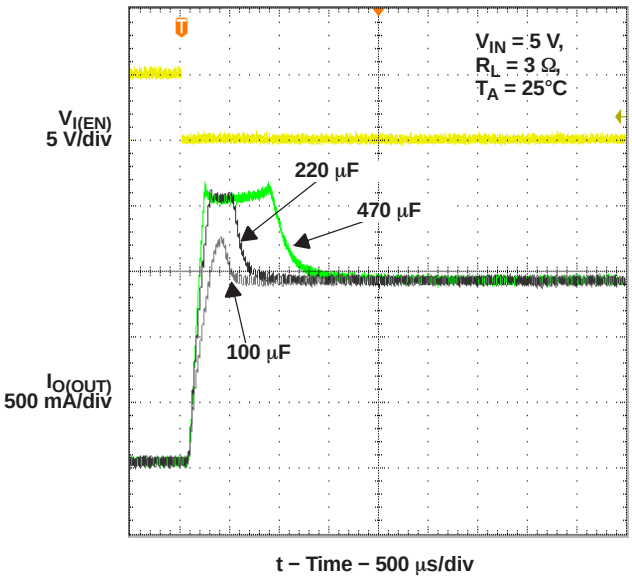



**Figure 7. Inrush Current With Different Load Capacitance**

## PARAMETER MEASUREMENT INFORMATION (continued)

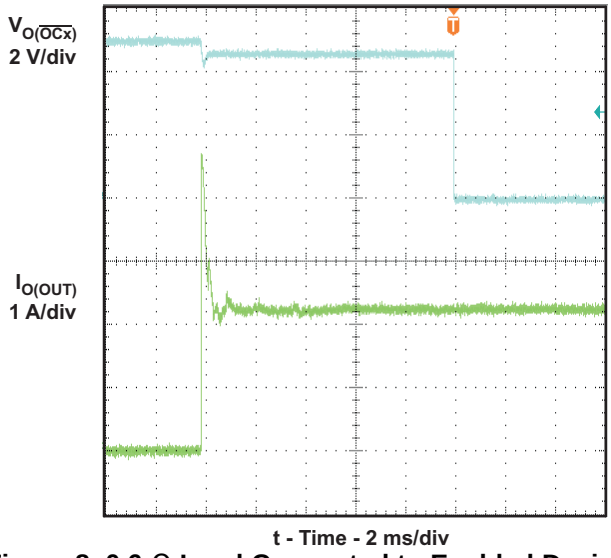



**Figure 8. 0.6-Ω Load Connected to Enabled Device**

## TYPICAL CHARACTERISTICS

**TURNON TIME vs INPUT VOLTAGE**

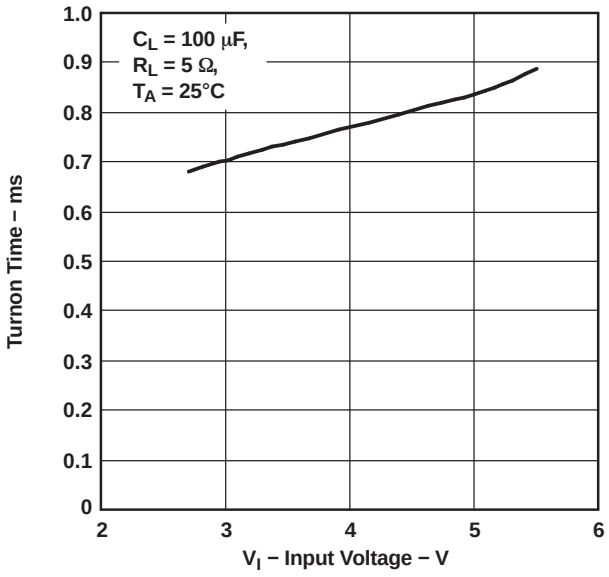



**Figure 9.**

**TURNOFF TIME vs INPUT VOLTAGE**

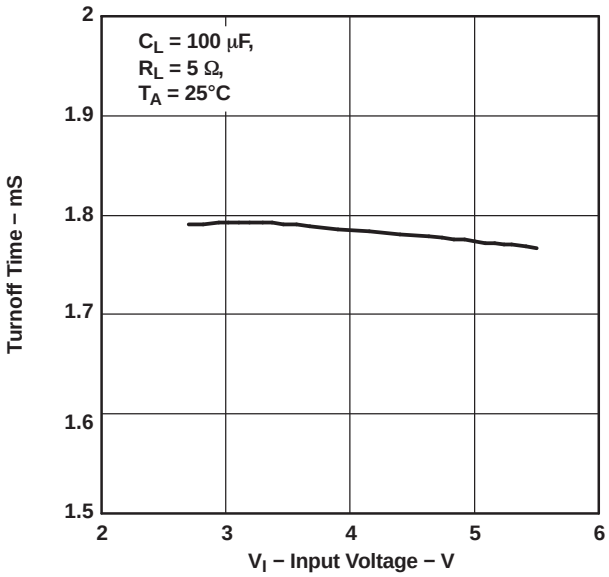



**Figure 10.**

## TYPICAL CHARACTERISTICS (continued)

**RISE TIME vs INPUT VOLTAGE**

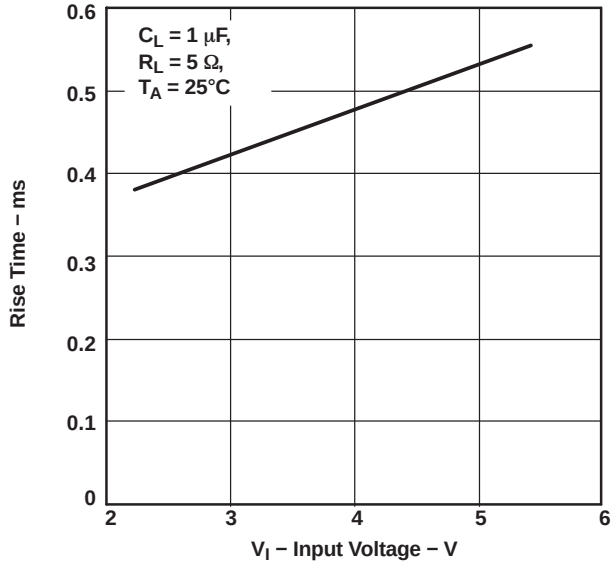



Figure 11.

**FALL TIME vs INPUT VOLTAGE**

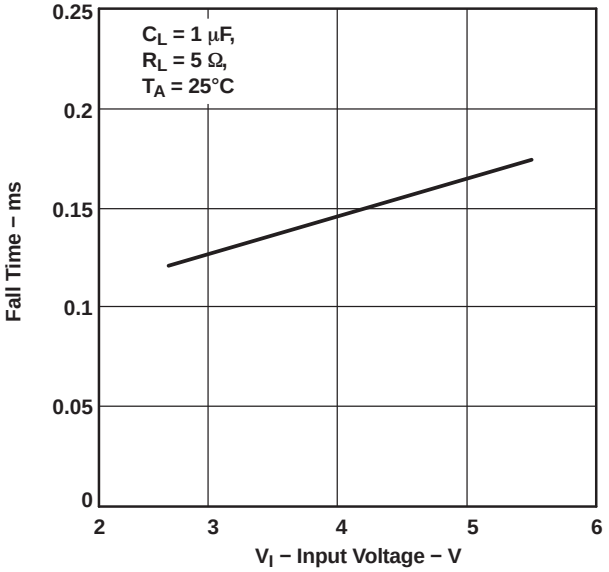



Figure 12.

**TPS2060, TPS2064 SUPPLY CURRENT, OUTPUT ENABLED vs JUNCTION TEMPERATURE**

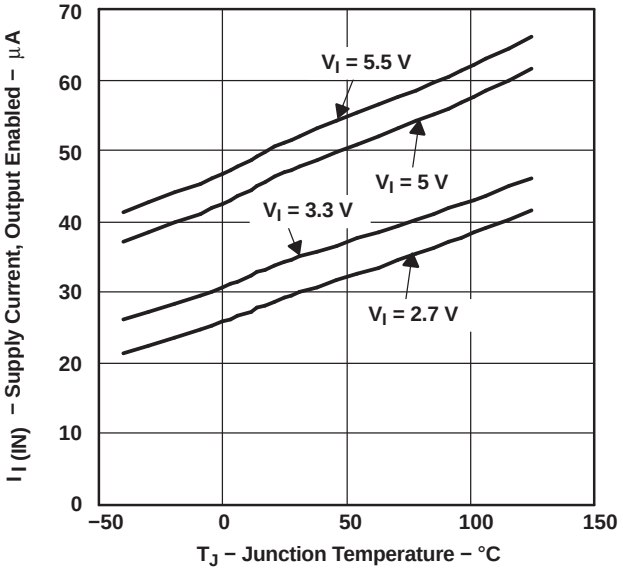



Figure 13.

**TPS2068, TPS2069 SUPPLY CURRENT, OUTPUT ENABLED vs JUNCTION TEMPERATURE**

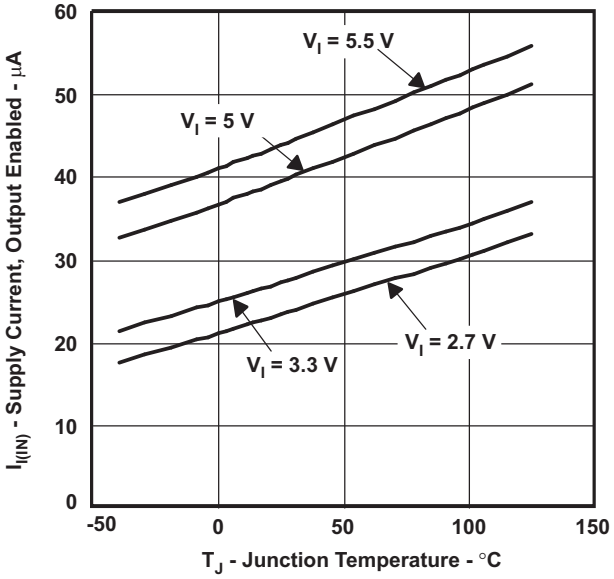



Figure 14.

## TYPICAL CHARACTERISTICS (continued)

**SUPPLY CURRENT, OUTPUT DISABLED vs JUNCTION TEMPERATURE**

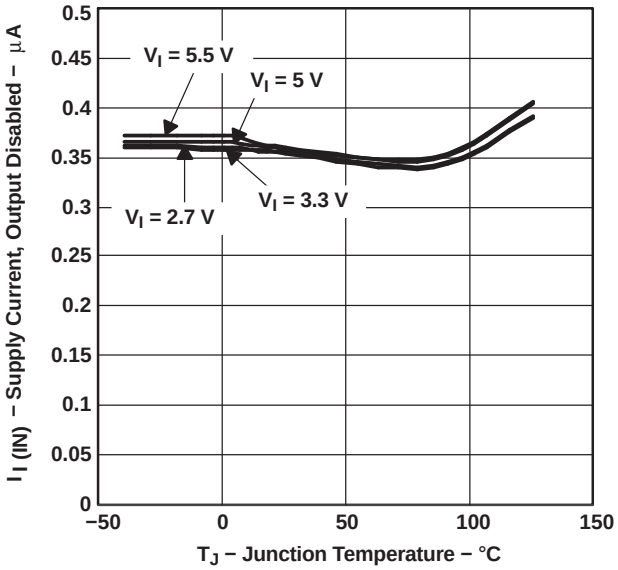



Figure 15.

**STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE**

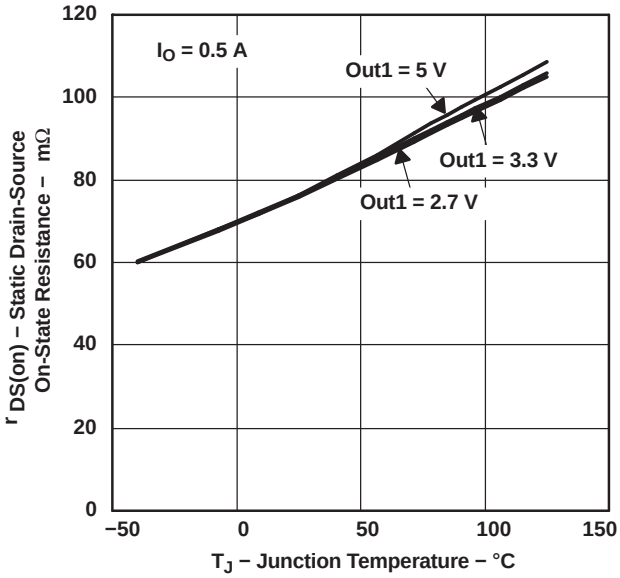



Figure 16.

**SHORT-CIRCUIT OUTPUT CURRENT vs JUNCTION TEMPERATURE**

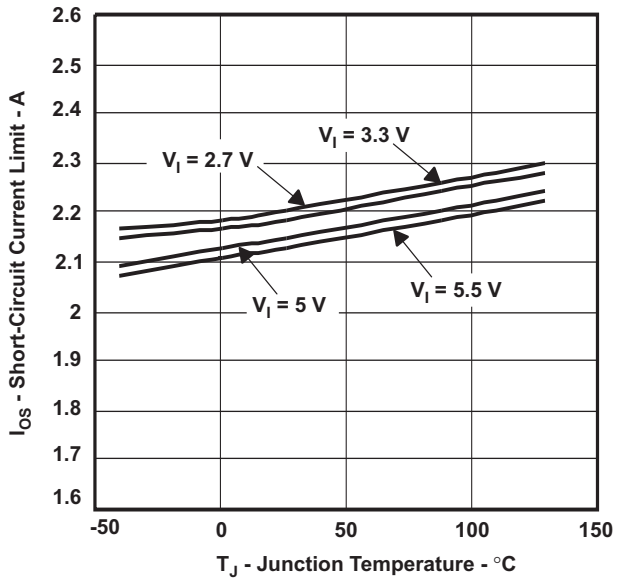



Figure 17.

**UNDERVOLTAGE LOCKOUT vs JUNCTION TEMPERATURE**

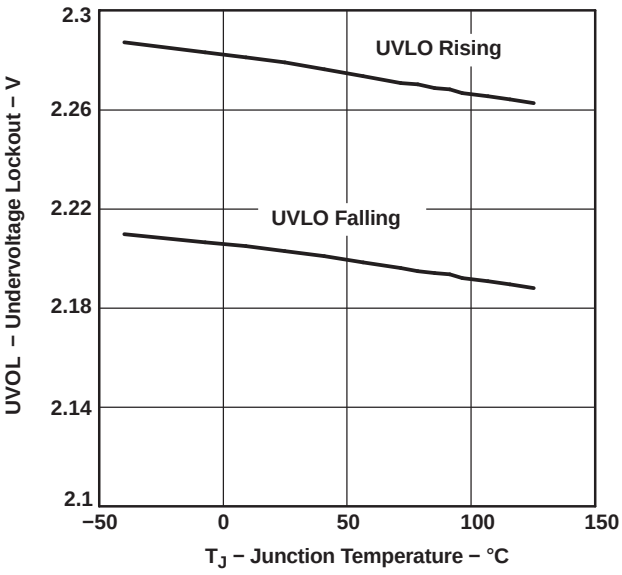



Figure 18.

## TYPICAL CHARACTERISTICS (continued)

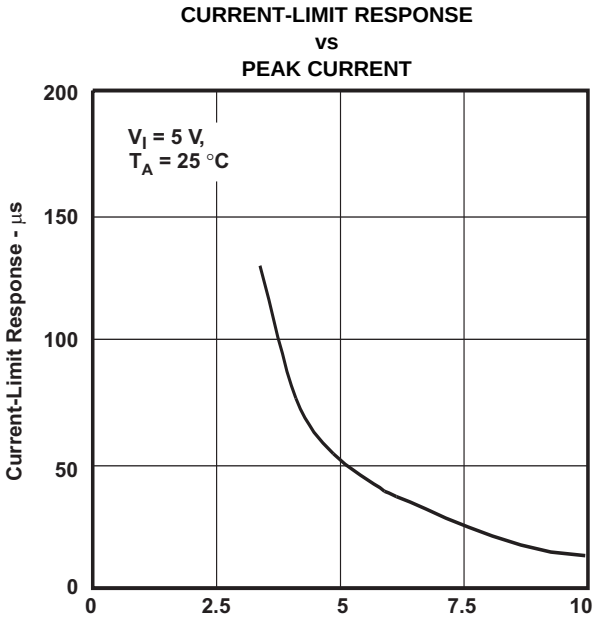



**Figure 19.**

# APPLICATION INFORMATION

## POWER-SUPPLY CONSIDERATIONS

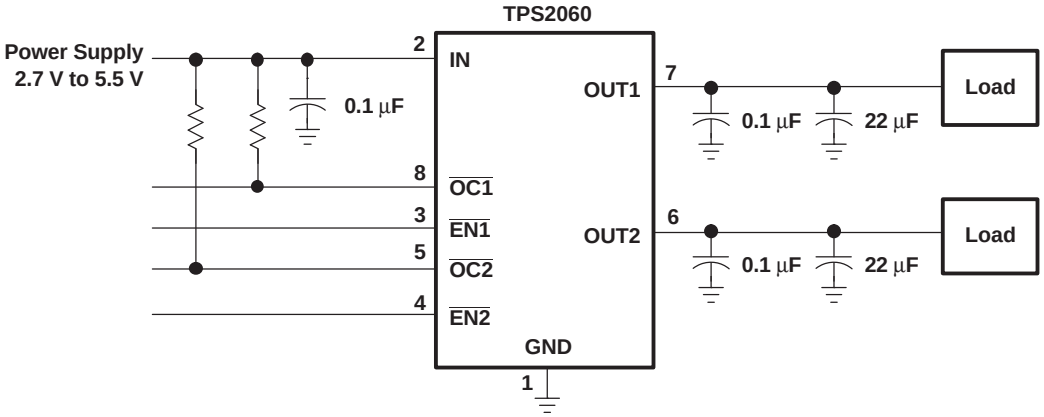



**Figure 20. Typical Application**

A 0.01-µF to 0.1-µF ceramic bypass capacitor between IN and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01-µF to 0.1-µF ceramic capacitor improves the immunity of the device to short-circuit transients.

## OVERCURRENT

A sense FET is employed to check for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see Figure 6). The TPS206x senses the short and immediately switches into a constant-current output.

In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, high currents may flow for a short period of time before the current-limit circuit can react (see Figure 8). After the current-limit circuit has tripped (reached the overcurrent trip threshold), the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded. The TPS206x is capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

## $\overline{\text{OC}}$ RESPONSE

The $\overline{\text{OC}}$x open-drain output is asserted (active low) when an overcurrent or overtemperature shutdown condition is encountered after a 10-ms deglitch timeout. The output remains asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause a momentary overcurrent condition; however, no false reporting on $\overline{\text{OC}}$x occurs due to the 10-ms deglitch circuit. The TPS206x is designed to eliminate false overcurrent reporting. The internal overcurrent deglitch eliminates the need for external components to remove unwanted pulses. $\overline{\text{OC}}$x is not deglitched when the switch is turned off due to an overtemperature shutdown.

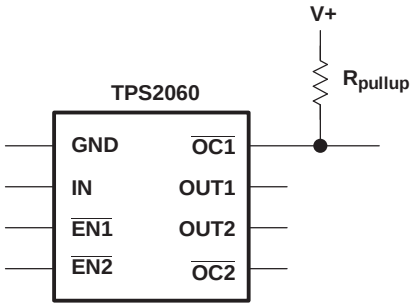



**Figure 21. Typical Circuit for the $\overline{OC}$ Pin**

## POWER DISSIPATION AND JUNCTION TEMPERATURE

The low on-resistance on the N-channel MOSFET allows the small surface-mount packages to pass large currents. The thermal resistance of these packages are high compared to those of power packages; it is good design practice to check power dissipation and junction temperature. Begin by determining the $r_{DS(on)}$ of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from Figure 16. Using this value, the power dissipation per switch can be calculated by:

$$P_D = r_{DS(on)} \times I^2$$

Multiply this number by the number of switches being used. This step renders the total power dissipation from the N-channel MOSFETs.

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

$T_A$= Ambient temperature °C
$R_{\theta JA}$ = Thermal resistance
$P_D$ = Total power dissipation based on number of switches being used.

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

## THERMAL PROTECTION

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The TPS206x implements a thermal sensing to monitor the operating junction temperature of the power distribution switch. In an overcurrent or short-circuit condition, the junction temperature rises due to excessive power dissipation. Once the die temperature rises to approximately 140°C due to overcurrent conditions, the internal thermal sense circuitry turns the power switch off, thus preventing the power switch from damage. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 10°C, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed. The $\overline{OC}$x open-drain output is asserted (active low) when an overtemperature shutdown or overcurrent occurs.

## UNDERVOLTAGE LOCKOUT (UVLO)

An undervoltage lockout ensures that the power switch is in the off state at power up. Whenever the input voltage falls below approximately 2 V, the power switch is quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO also keeps the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. On reinsertion, the power switch is turned on, with a controlled rise time to reduce EMI and voltage overshoots.

## UNIVERSAL SERIAL BUS (USB) APPLICATIONS

The universal serial bus (USB) interface is a 12-Mb/s, or 1.5-Mb/s, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (e.g., keyboards, printers, scanners, and mice). The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply.

The USB specification defines the following five classes of devices, each differentiated by power-consumption requirements:

- Hosts/self-powered hubs (SPH)
- Bus-powered hubs (BPH)
- Low-power, bus-powered functions
- High-power, bus-powered functions
- Self-powered functions

SPHs and BPHs distribute data and power to downstream functions. The TPS206x has higher current capability than required by one USB port; so, it can be used on the host side and supplies power to multiple downstream ports or functions.

## HOST/SELF-POWERED AND BUS-POWERED HUBS

Hosts and SPHs have a local power supply that powers the embedded functions and the downstream ports (see Figure 22). This power supply must provide from 5.25 V to 4.75 V to the board side of the downstream connection under full-load and no-load conditions. Hosts and SPHs are required to have current-limit protection and must report overcurrent conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.

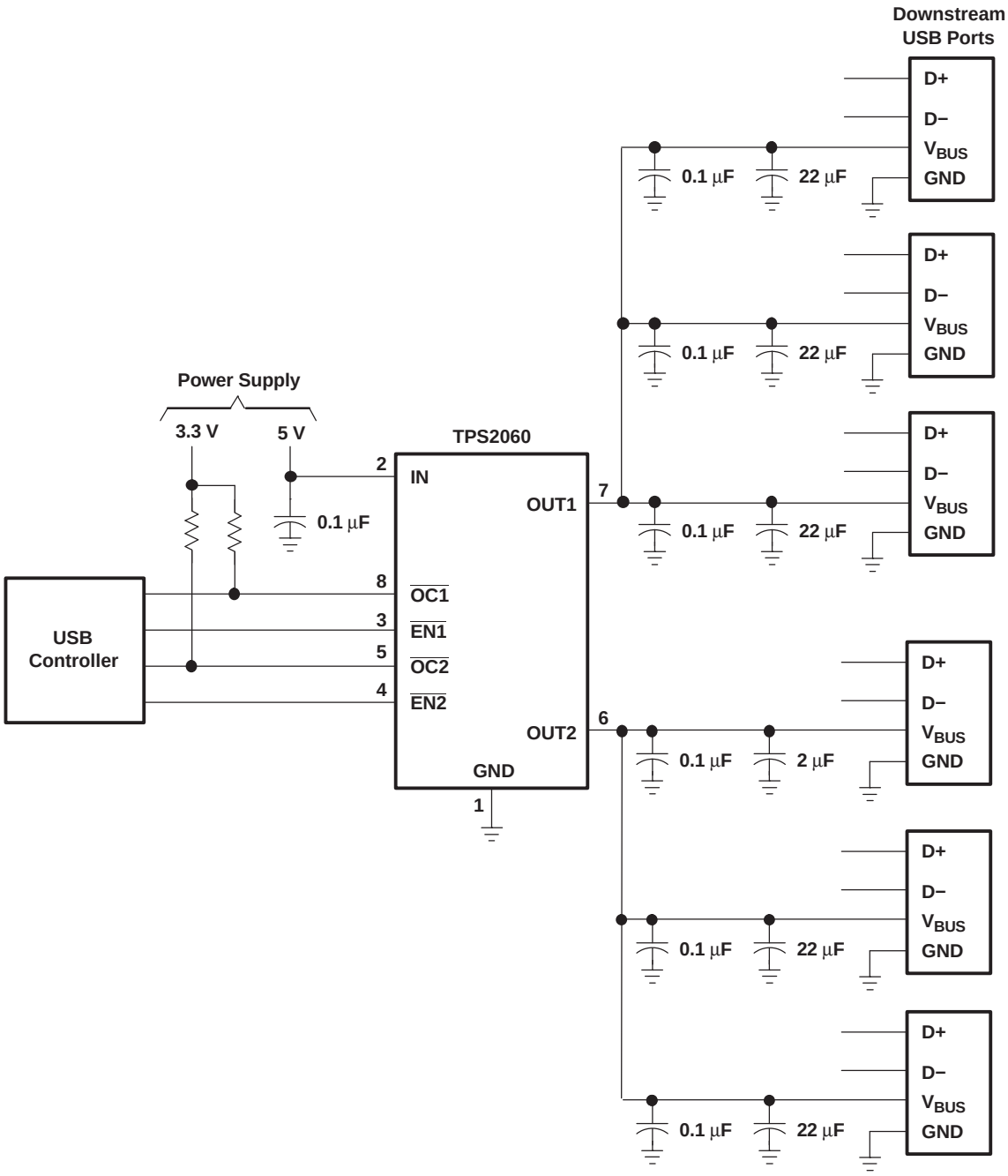



**Figure 22. Typical Six-Port USB Host/Self-Powered Hub**

BPHs obtain all power from upstream ports and often contain an embedded function. The hubs are required to power up with less than one unit load. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on power up, the power to the embedded function may need to be kept off until enumeration is completed. This can be accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than one unit load. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

## LOW-POWER BUS-POWERED AND HIGH-POWER BUS-POWERED FUNCTIONS

Both low-power and high-power bus-powered functions obtain all power from upstream ports; low-power functions always draw less than 100 mA; high-power functions must draw less than 100 mA at power up and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 µF at power up, the device must implement inrush current limiting (see Figure 23). With TPS206x, the internal functions could draw more than 500 mA, which fits the needs of some applications such as motor driving circuits.

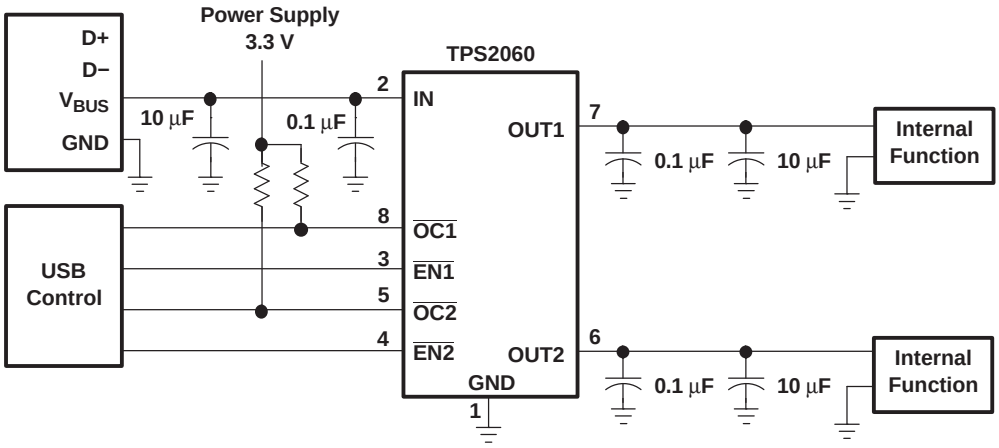



**Figure 23. High-Power Bus-Powered Function**

## USB POWER-DISTRIBUTION REQUIREMENTS

USB can be implemented in several ways, and, regardless of the type of USB device being developed, several power-distribution features must be implemented.

- Hosts/SPHs must:
  - Current-limit downstream ports
  - Report overcurrent conditions on USB $V_{BUS}$
- BPHs must:
  - Enable/disable power to downstream ports
  - Power up at <100 mA
  - Limit inrush current (<44 Ω and 10 µF)
- Functions must:
  - Limit inrush currents
  - Power up at <100 mA

The feature set of the TPS206x allows them to meet each of these requirements. The integrated current-limiting and overcurrent reporting is required by hosts and self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-powered hubs, as well as the input ports for bus-powered functions (see Figure 24).

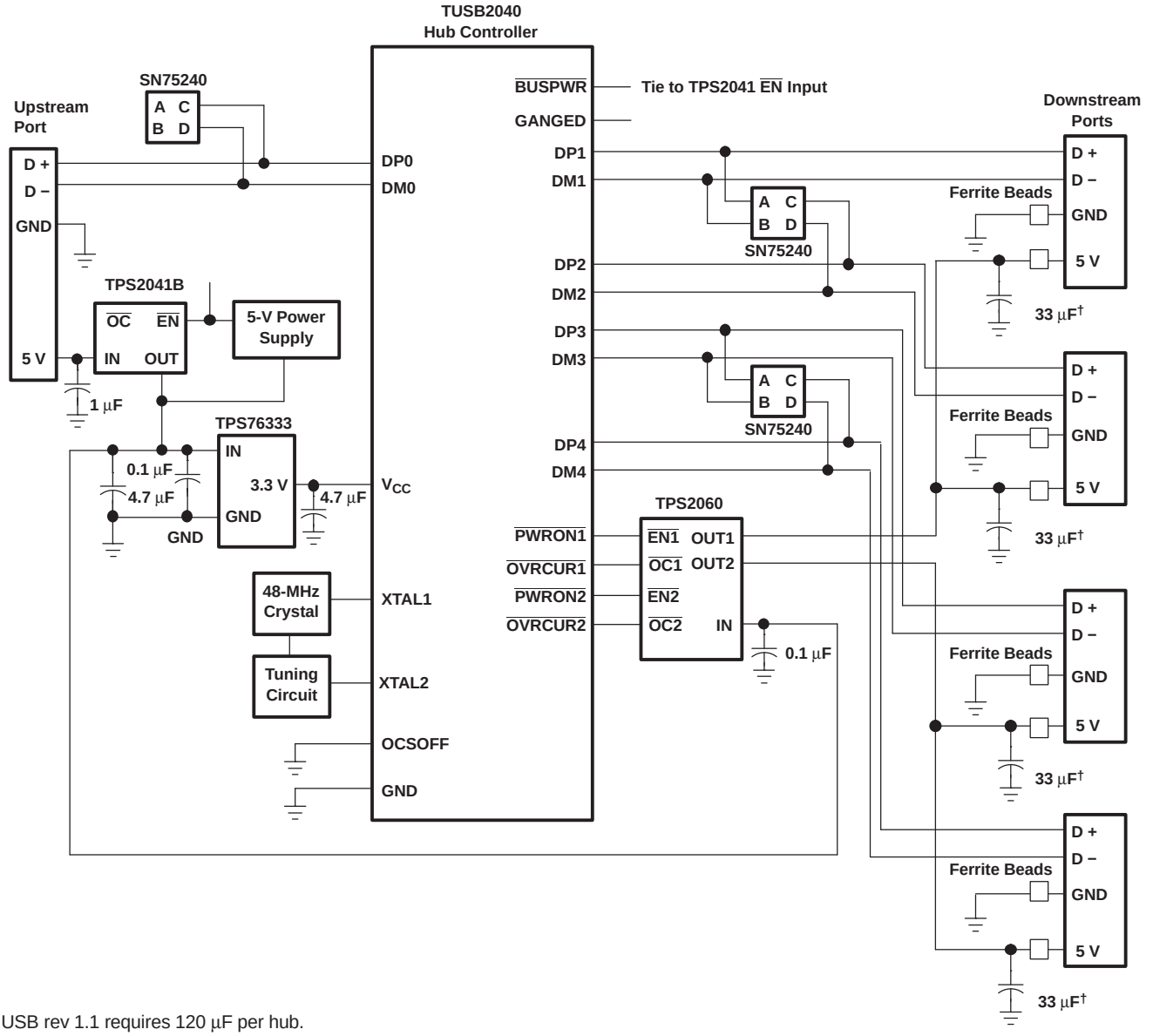



**Figure 24. Hybrid Self / Bus-Powered Hub Implementation**

## GENERIC HOT-PLUG APPLICATIONS

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the TPS206x, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS206x also ensures that the switch is off after the card has been removed, and that the switch is off during the next insertion. The UVLO feature insures a soft start with a controlled rise time for every insertion of the card or module.

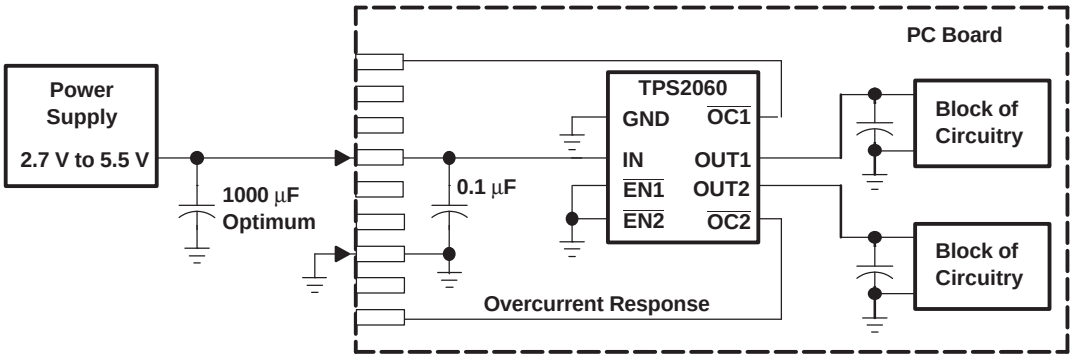



**Figure 25. Typical Hot-Plug Implementation**

By placing the TPS206x between the $V_{CC}$ input and the rest of the circuitry, the input power reaches these devices first after insertion. The typical rise time of the switch is approximately 1 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

## DETAILED DESCRIPTION

### Power Switch

The power switch is an N-channel MOSFET with a low on-state resistance. Configured as a high-side switch, the power switch prevents current flow from OUT to IN and IN to OUT when disabled. The power switch supplies a minimum current of 1.5 A.

### Charge Pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires little supply current.

### Driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage.

### Enable ($\overline{\text{ENx}}$)

The logic enable disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current. The supply current is reduced to less than 1 µA when a logic high is present on $\overline{\text{ENx}}$, or when a logic low is present on ENx. A logic zero input on $\overline{\text{ENx}}$, or a logic high input on ENx restores bias to the drive and control circuits and turns the switch on. The enable input is compatible with both TTL and CMOS logic levels.

### Overcurrent ($\overline{\text{OCx}}$)

The $\overline{\text{OCx}}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output remains asserted until the overcurrent or overtemperature condition is removed. A 10-ms deglitch circuit prevents the $\overline{\text{OCx}}$ signal from oscillation or false triggering. If an overtemperature shutdown occurs, the $\overline{\text{OCx}}$ is asserted instantaneously.

## Current Sense

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant-current mode and holds the current constant while varying the voltage on the load.

## Thermal Sense

The TPS206x implements a thermal sensing to monitor the operating temperature of the power distribution switch. In an overcurrent or short-circuit condition the junction temperature rises. When the die temperature rises to approximately 140°C due to overcurrent conditions, the internal thermal sense circuitry turns off the switch, thus preventing the device from damage. Hysteresis is built into the thermal sense, and after the device has cooled approximately 10 degrees, the switch turns back on. The switch continues to cycle off and on until the fault is removed. The open-drain false reporting output ($\overline{OC}$x) is asserted (active low) when an overtemperature shutdown or overcurrent occurs.

## Undervoltage Lockout

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS2060DGN | Active | Production | HVSSOP (DGN) \| 8 | 80 \| TUBE | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | 0 to 105 | 2060 |
| TPS2060DGN.A | Active | Production | HVSSOP (DGN) \| 8 | 80 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 105 | 2060 |
| TPS2060DGNR | Active | Production | HVSSOP (DGN) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | 0 to 105 | 2060 |
| TPS2060DGNR.A | Active | Production | HVSSOP (DGN) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 105 | 2060 |
| TPS2060DRBR | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 105 | 2060 |
| TPS2060DRBR.A | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 105 | 2060 |
| TPS2060DRBT | Active | Production | SON (DRB) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 2060 |
| TPS2060DRBT.A | Active | Production | SON (DRB) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 2060 |
| TPS2064DGN | Active | Production | HVSSOP (DGN) \| 8 | 80 \| TUBE | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | 0 to 105 | 2064 |
| TPS2064DGN.A | Active | Production | HVSSOP (DGN) \| 8 | 80 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 105 | 2064 |
| TPS2064DGNR | Active | Production | HVSSOP (DGN) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | 0 to 105 | 2064 |
| TPS2064DGNR.A | Active | Production | HVSSOP (DGN) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 105 | 2064 |
| TPS2064DRBR | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 105 | 2064 |
| TPS2064DRBR.A | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 105 | 2064 |
| TPS2064DRBT | Active | Production | SON (DRB) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 105 | 2064 |
| TPS2064DRBT.A | Active | Production | SON (DRB) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 105 | 2064 |
| TPS2068D | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | 0 to 105 | 2068 |
| TPS2068D.A | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | 0 to 105 | 2068 |
| TPS2068DGN | Active | Production | HVSSOP (DGN) \| 8 | 80 \| TUBE | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 105 | 2068 |
| TPS2068DGN.A | Active | Production | HVSSOP (DGN) \| 8 | 80 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | 2068 |
| TPS2068DGNR | Active | Production | HVSSOP (DGN) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 105 | 2068 |
| TPS2068DGNR.A | Active | Production | HVSSOP (DGN) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | 2068 |
| TPS2068DR | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | 0 to 105 | 2068 |
| TPS2068DR.A | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | 0 to 105 | 2068 |
| TPS2069DGN | Active | Production | HVSSOP (DGN) \| 8 | 80 \| TUBE | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 105 | 2069 |
| TPS2069DGN.A | Active | Production | HVSSOP (DGN) \| 8 | 80 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | 2069 |
| TPS2069DGNG4 | Active | Production | HVSSOP (DGN) \| 8 | 80 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | 2069 |
| TPS2069DGNR | Active | Production | HVSSOP (DGN) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 105 | 2069 |
| TPS2069DGNR.A | Active | Production | HVSSOP (DGN) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | 2069 |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS2069DGNRG4 | Active | Production | HVSSOP (DGN) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | 2069 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

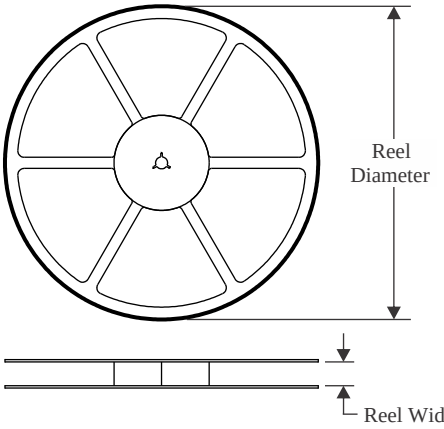
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

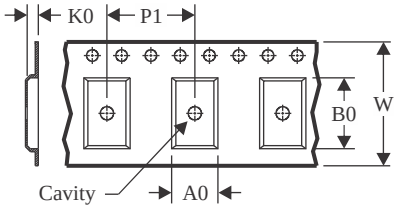
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

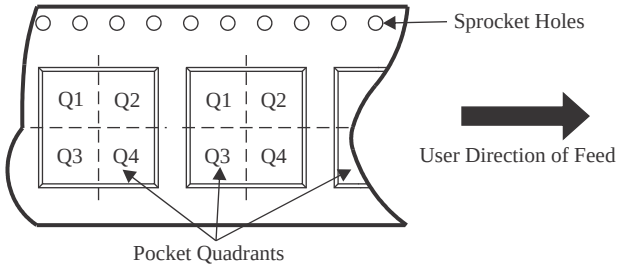



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

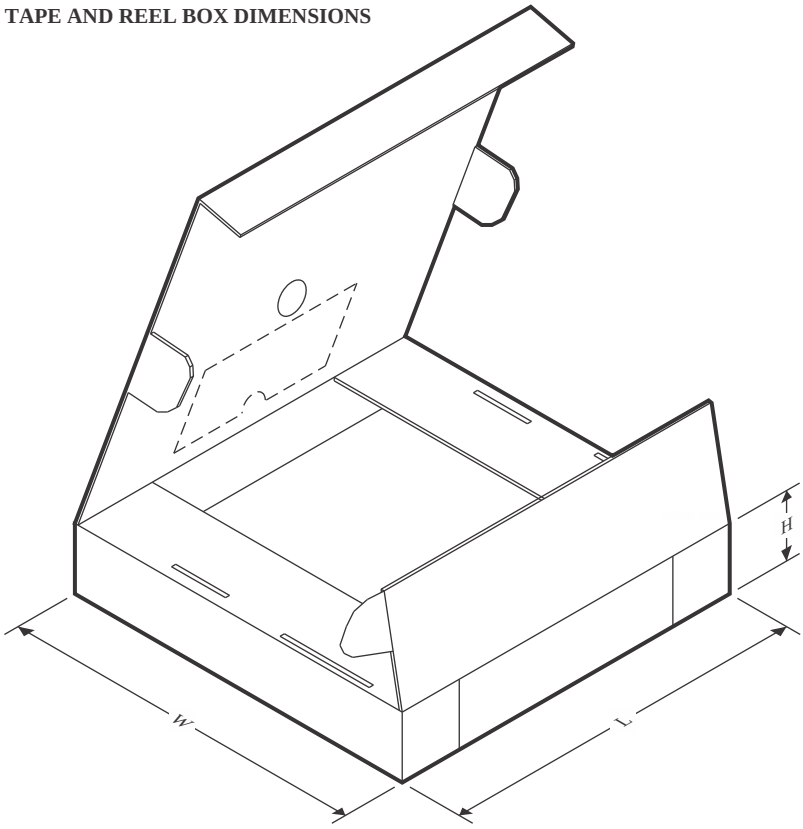
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS2060DGNR | HVSSOP | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.3 | 1.3 | 8.0 | 12.0 | Q1 |
| TPS2060DGNR | HVSSOP | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS2060DRBR | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.0 | 8.0 | 12.0 | Q2 |
| TPS2060DRBT | SON | DRB | 8 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.0 | 8.0 | 12.0 | Q2 |
| TPS2064DGNR | HVSSOP | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.3 | 1.3 | 8.0 | 12.0 | Q1 |
| TPS2064DGNR | HVSSOP | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS2064DRBR | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.0 | 8.0 | 12.0 | Q2 |
| TPS2064DRBT | SON | DRB | 8 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.0 | 8.0 | 12.0 | Q2 |
| TPS2068DGNR | HVSSOP | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS2068DGNR | HVSSOP | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.3 | 1.3 | 8.0 | 12.0 | Q1 |
| TPS2068DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS2069DGNR | HVSSOP | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.3 | 1.3 | 8.0 | 12.0 | Q1 |
| TPS2069DGNR | HVSSOP | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |

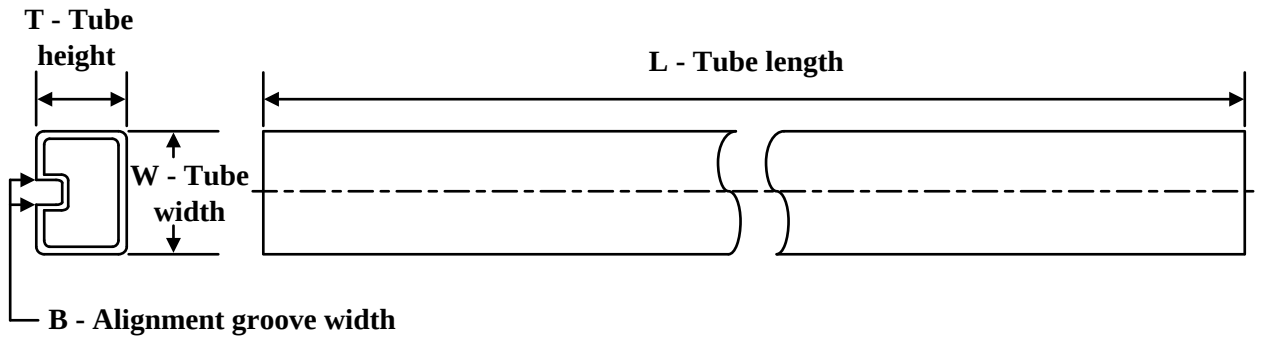
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS2060DGNR | HVSSOP | DGN | 8 | 2500 | 346.0 | 346.0 | 35.0 |
| TPS2060DGNR | HVSSOP | DGN | 8 | 2500 | 364.0 | 364.0 | 27.0 |
| TPS2060DRBR | SON | DRB | 8 | 3000 | 346.0 | 346.0 | 35.0 |
| TPS2060DRBT | SON | DRB | 8 | 250 | 200.0 | 183.0 | 25.0 |
| TPS2064DGNR | HVSSOP | DGN | 8 | 2500 | 346.0 | 346.0 | 35.0 |
| TPS2064DGNR | HVSSOP | DGN | 8 | 2500 | 364.0 | 364.0 | 27.0 |
| TPS2064DRBR | SON | DRB | 8 | 3000 | 346.0 | 346.0 | 35.0 |
| TPS2064DRBT | SON | DRB | 8 | 250 | 200.0 | 183.0 | 25.0 |
| TPS2068DGNR | HVSSOP | DGN | 8 | 2500 | 364.0 | 364.0 | 27.0 |
| TPS2068DGNR | HVSSOP | DGN | 8 | 2500 | 346.0 | 346.0 | 35.0 |
| TPS2068DR | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |
| TPS2069DGNR | HVSSOP | DGN | 8 | 2500 | 346.0 | 346.0 | 35.0 |
| TPS2069DGNR | HVSSOP | DGN | 8 | 2500 | 364.0 | 364.0 | 27.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| TPS2060DGN | DGN | HVSSOP | 8 | 80 | 322 | 6.55 | 1000 | 3.01 |
| TPS2060DGN | DGN | HVSSOP | 8 | 80 | 330 | 6.55 | 500 | 2.88 |
| TPS2060DGN.A | DGN | HVSSOP | 8 | 80 | 330 | 6.55 | 500 | 2.88 |
| TPS2060DGN.A | DGN | HVSSOP | 8 | 80 | 322 | 6.55 | 1000 | 3.01 |
| TPS2064DGN | DGN | HVSSOP | 8 | 80 | 322 | 6.55 | 1000 | 3.01 |
| TPS2064DGN | DGN | HVSSOP | 8 | 80 | 330 | 6.55 | 500 | 2.88 |
| TPS2064DGN.A | DGN | HVSSOP | 8 | 80 | 322 | 6.55 | 1000 | 3.01 |
| TPS2064DGN.A | DGN | HVSSOP | 8 | 80 | 330 | 6.55 | 500 | 2.88 |
| TPS2068D | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TPS2068D.A | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TPS2068DGN | DGN | HVSSOP | 8 | 80 | 330 | 6.55 | 500 | 2.88 |
| TPS2068DGN | DGN | HVSSOP | 8 | 80 | 322 | 6.55 | 1000 | 3.01 |
| TPS2068DGN.A | DGN | HVSSOP | 8 | 80 | 330 | 6.55 | 500 | 2.88 |
| TPS2068DGN.A | DGN | HVSSOP | 8 | 80 | 322 | 6.55 | 1000 | 3.01 |
| TPS2069DGN | DGN | HVSSOP | 8 | 80 | 322 | 6.55 | 1000 | 3.01 |
| TPS2069DGN | DGN | HVSSOP | 8 | 80 | 330 | 6.55 | 500 | 2.88 |
| TPS2069DGN.A | DGN | HVSSOP | 8 | 80 | 330 | 6.55 | 500 | 2.88 |
| TPS2069DGN.A | DGN | HVSSOP | 8 | 80 | 322 | 6.55 | 1000 | 3.01 |
| TPS2069DGNG4 | DGN | HVSSOP | 8 | 80 | 330 | 6.55 | 500 | 2.88 |
| TPS2069DGNG4 | DGN | HVSSOP | 8 | 80 | 322 | 6.55 | 1000 | 3.01 |

## GENERIC PACKAGE VIEW

# DRB 8

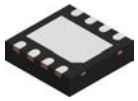
# VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L

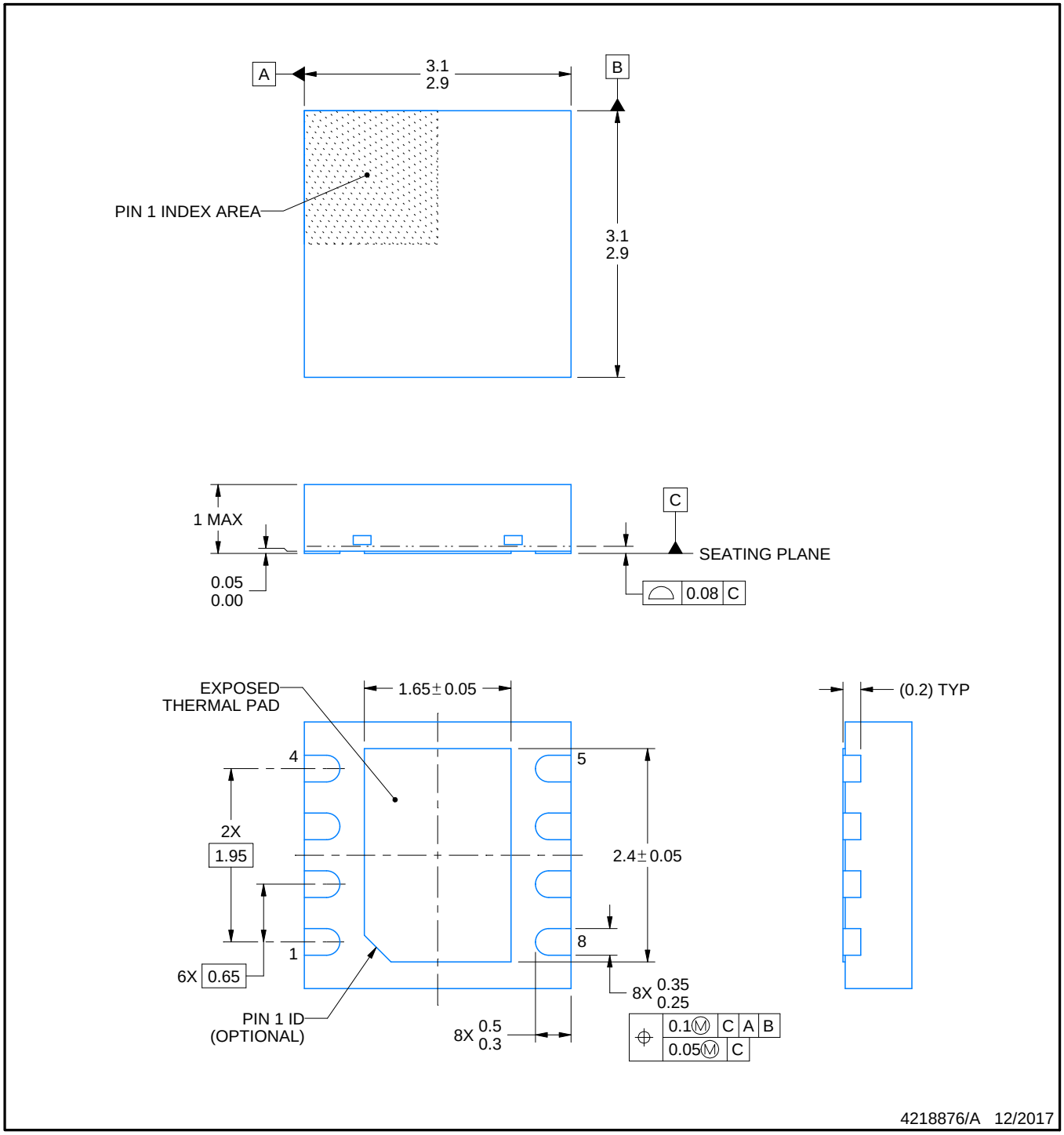
# DRB0008B



# PACKAGE OUTLINE

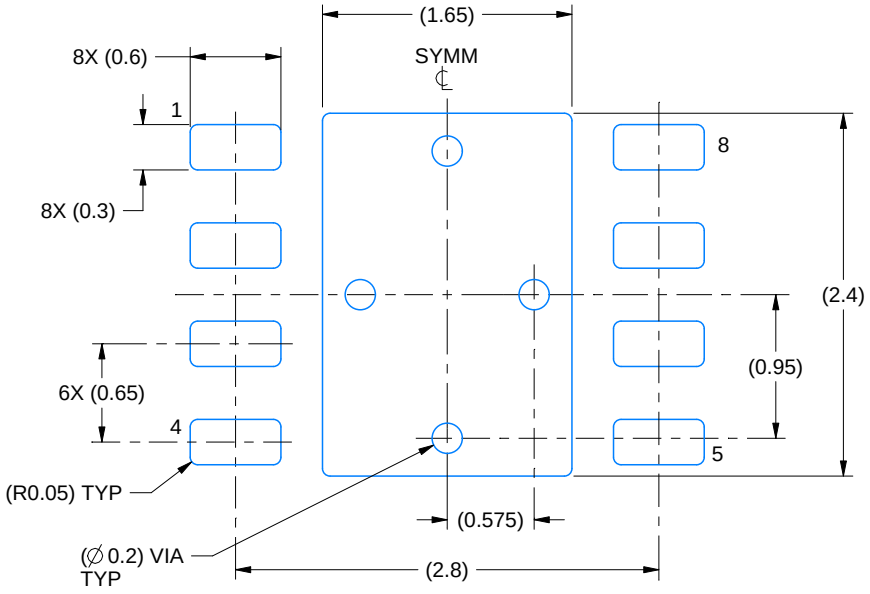
## VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

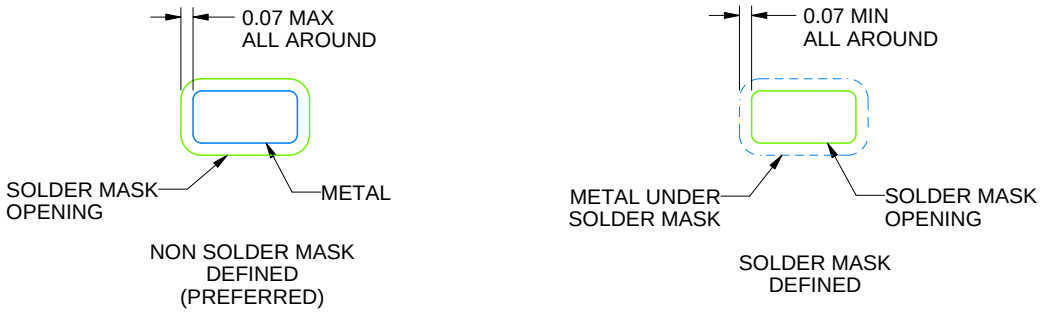



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
SCALE:20X

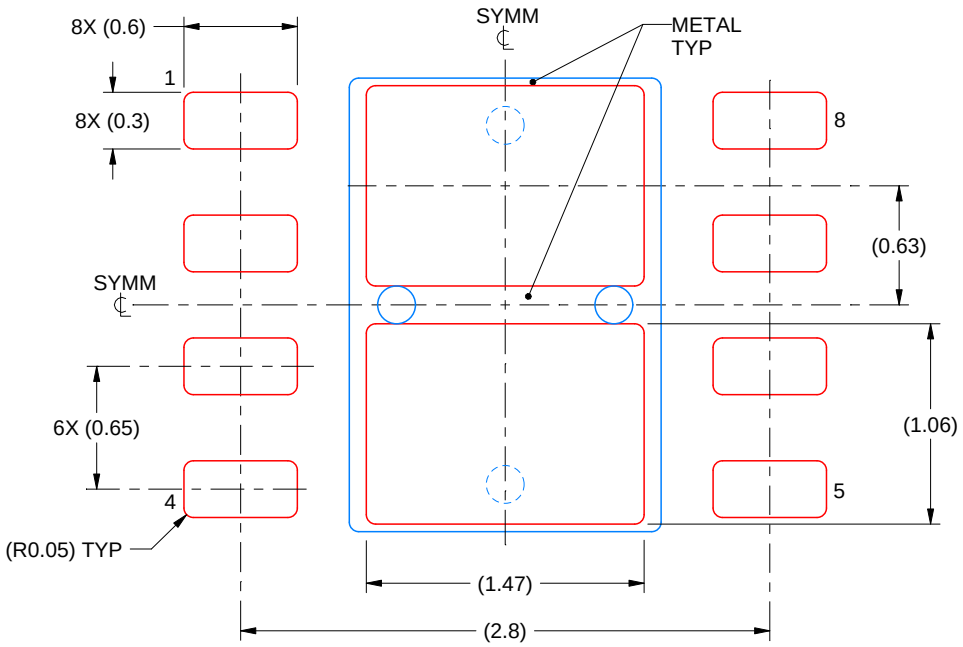



SOLDER MASK DETAILS

4218876/A 12/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218876/A 12/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# GENERIC PACKAGE VIEW

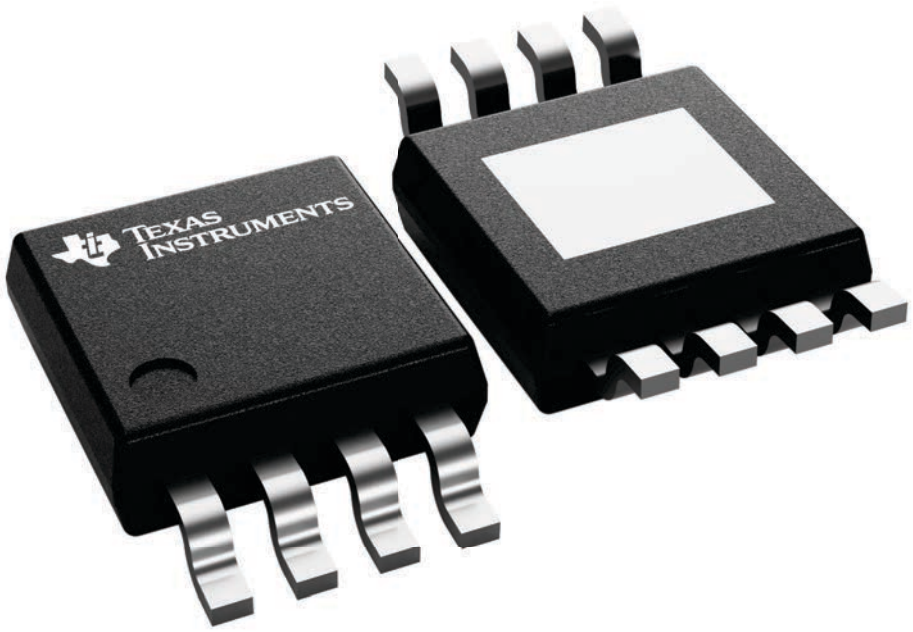
## DGN 8

## PowerPAD™ HVSSOP - 1.1 mm max height

**3 x 3, 0.65 mm pitch**

SMALL OUTLINE PACKAGE

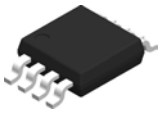
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.




4225482/B

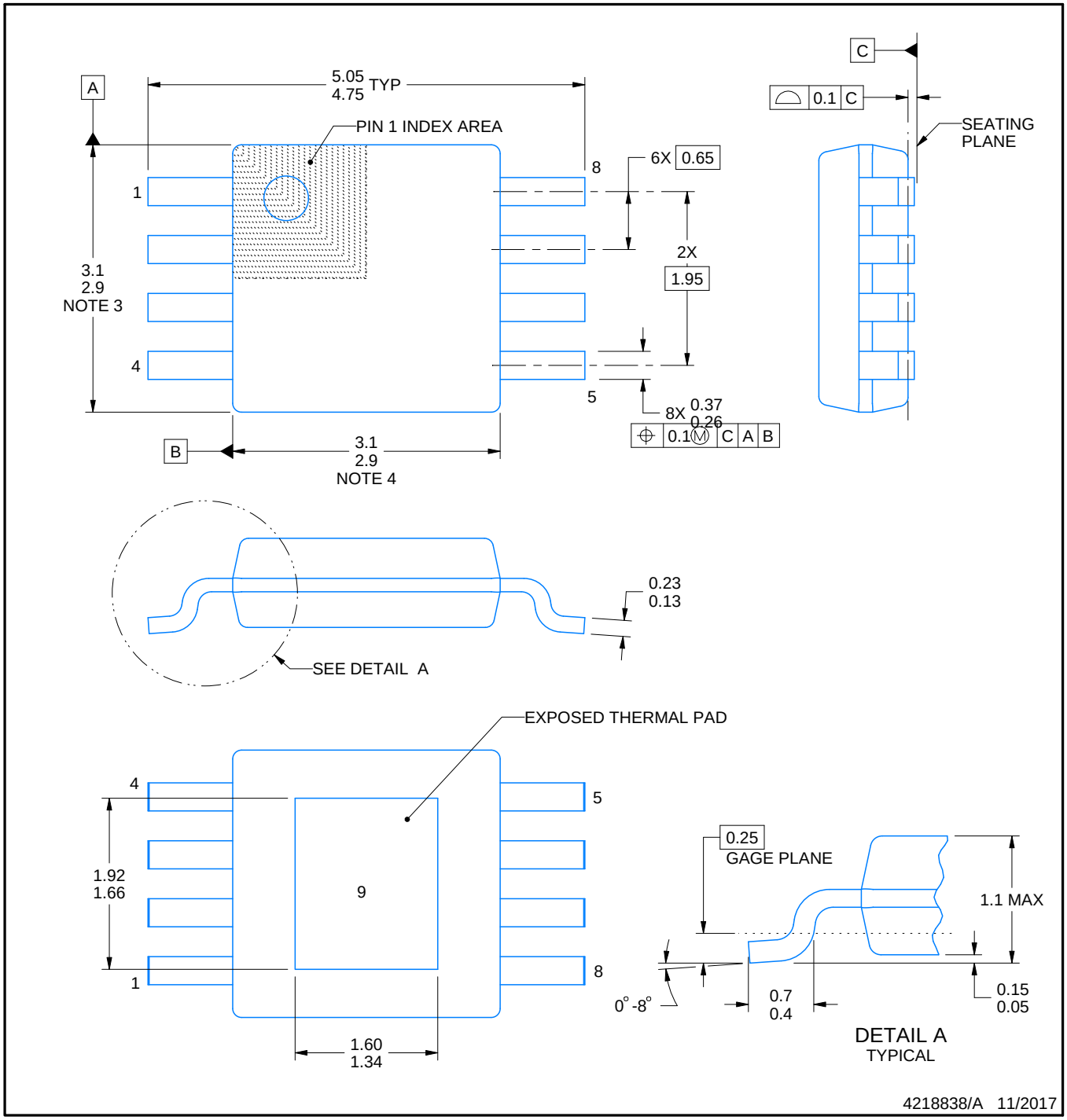
# PACKAGE OUTLINE

## DGN0008C



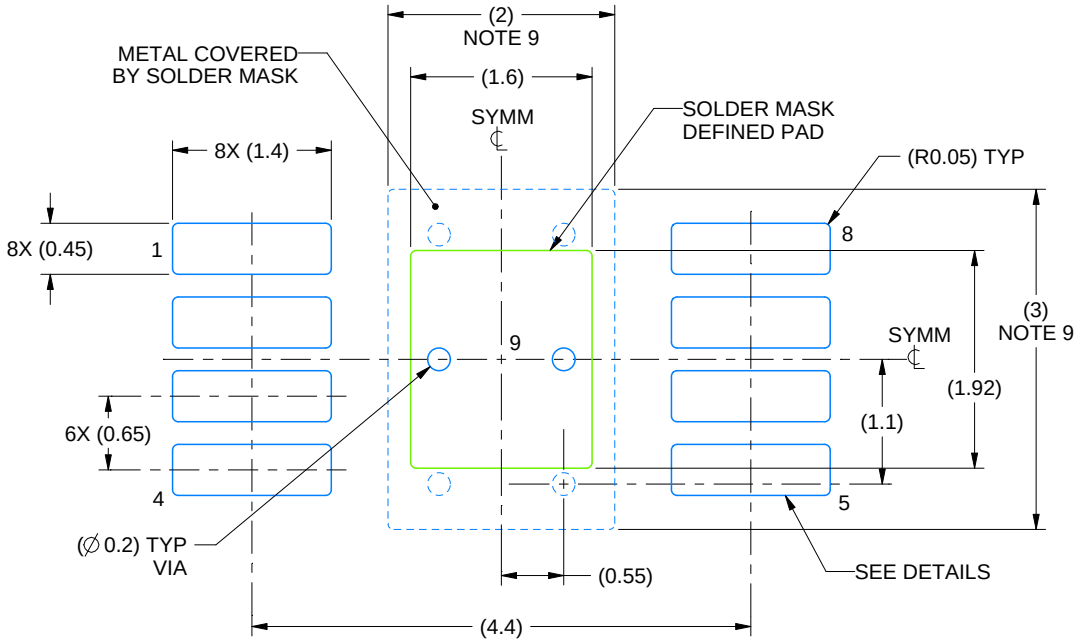
## HVSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

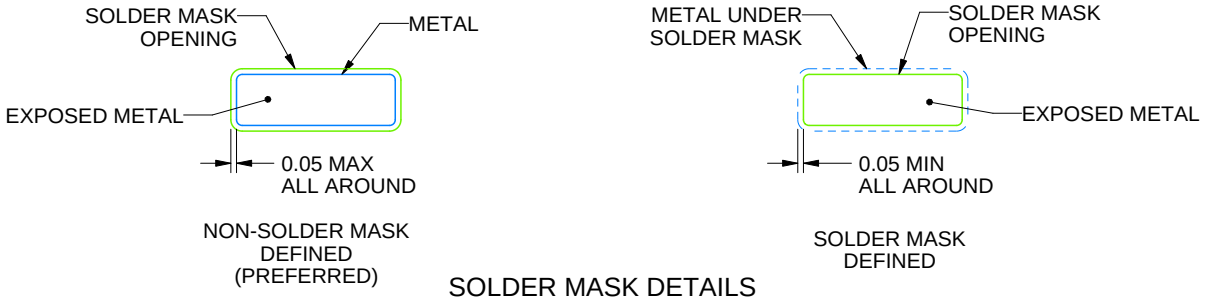



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

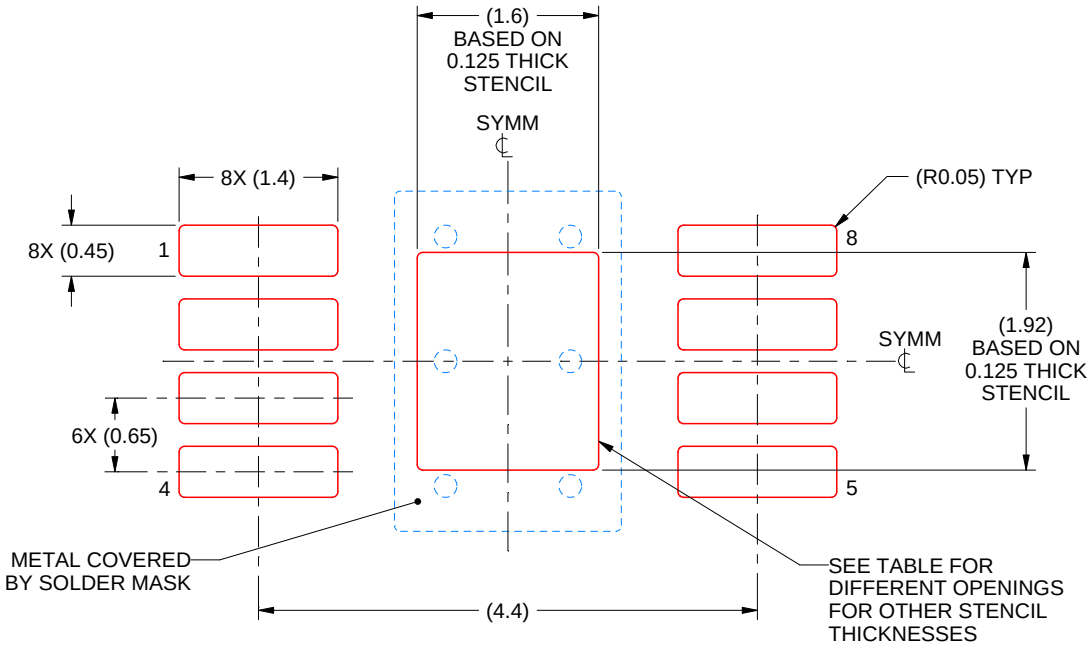



SOLDER MASK DETAILS

4218838/A 11/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.




SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 1.79 X 2.15 |
| 0.125 | 1.60 X 1.92 (SHOWN) |
| 0.15 | 1.46 X 1.75 |
| 0.175 | 1.35 X 1.62 |

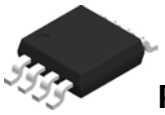
4218838/A 11/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

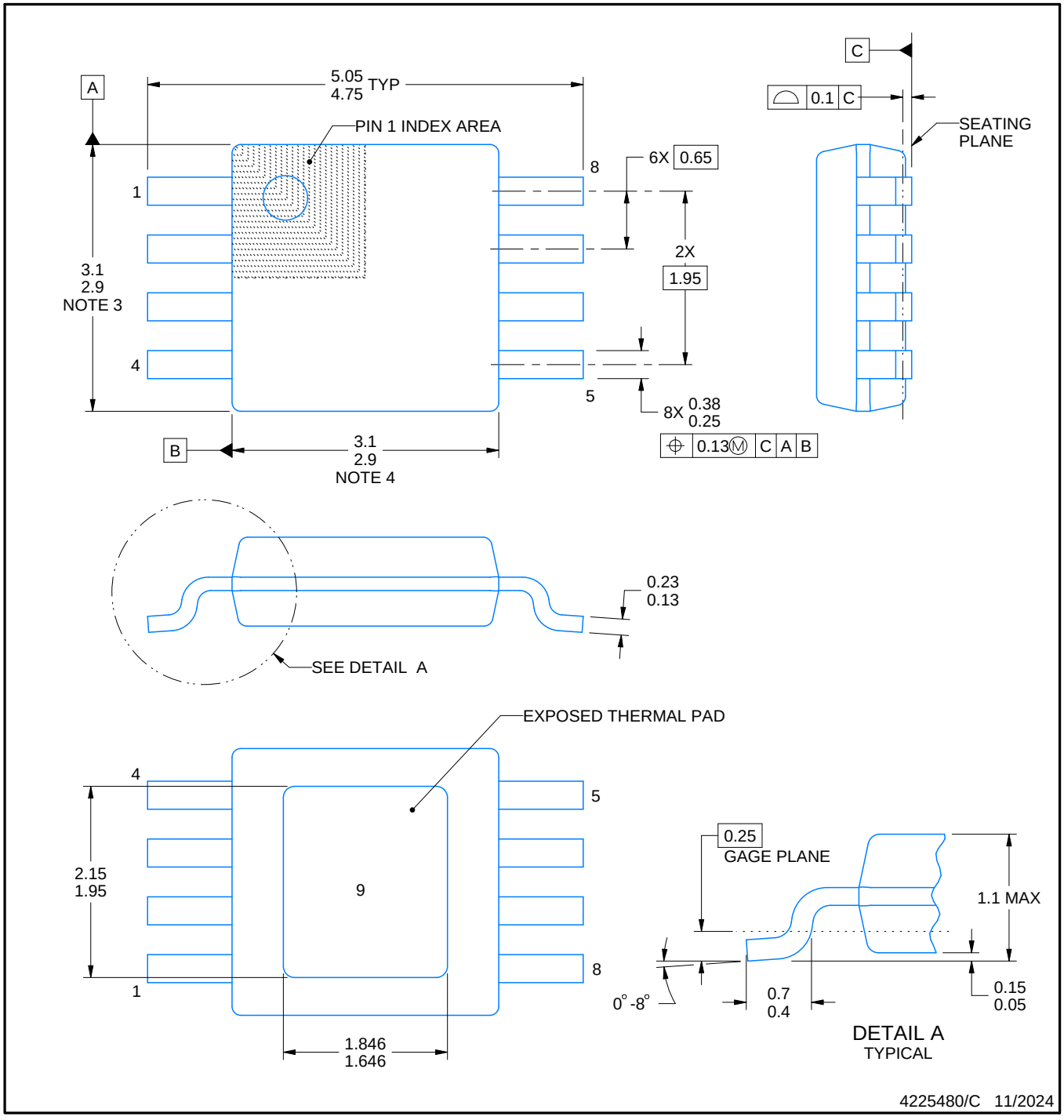
# PACKAGE OUTLINE

## DGN0008G



## PowerPAD™ HVSSOP - 1.1 mm max height

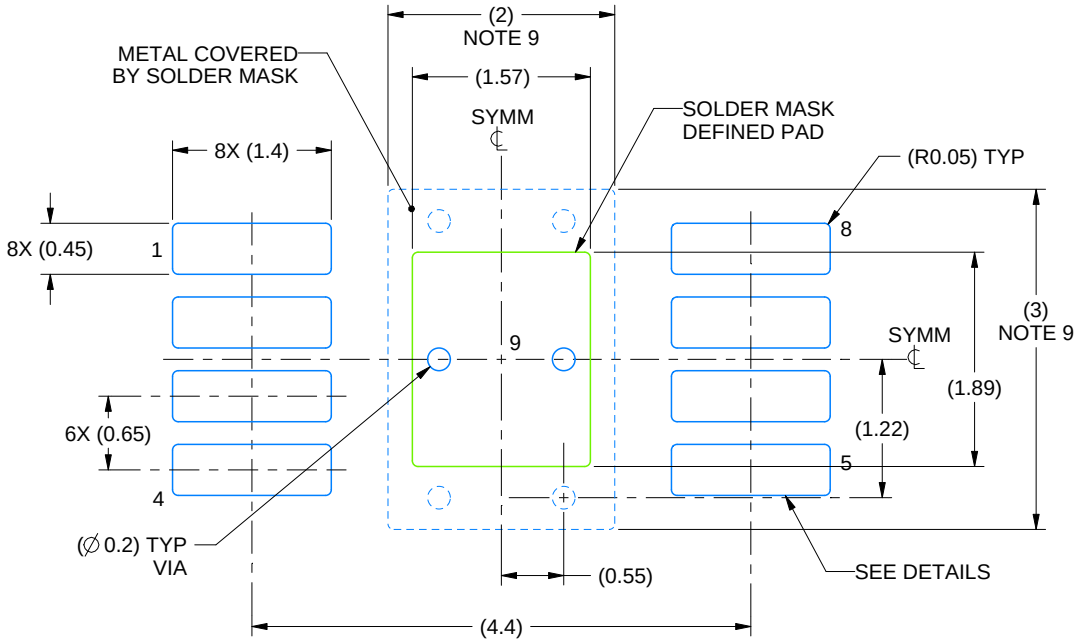
SMALL OUTLINE PACKAGE



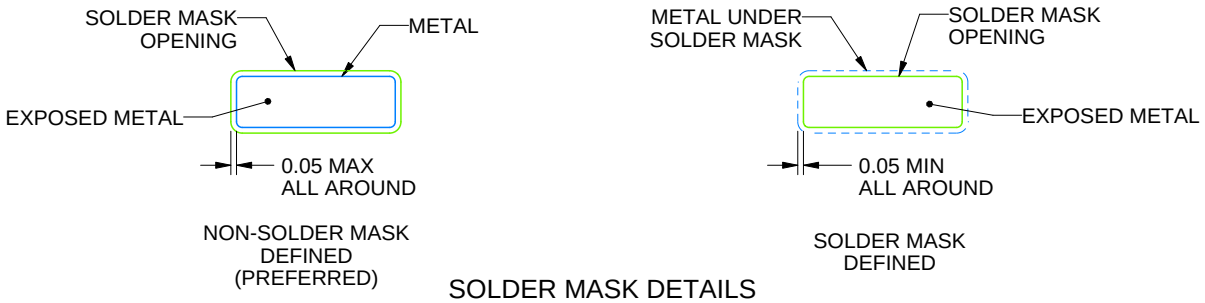

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

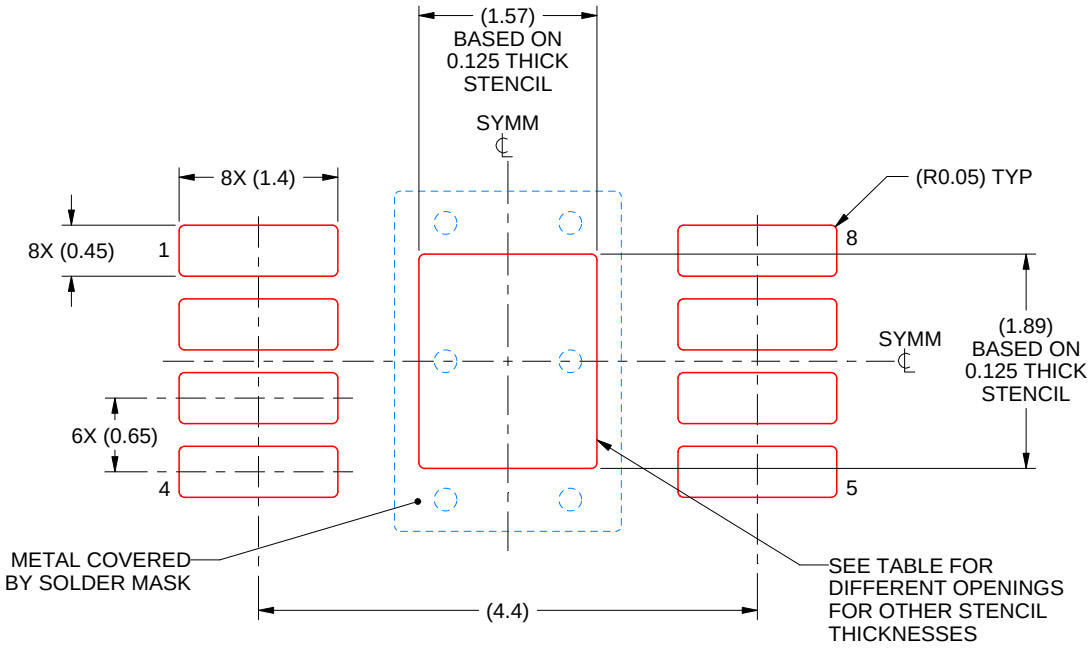



SOLDER MASK DETAILS

4225480/C 11/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



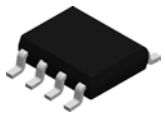

SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 1.76 X 2.11 |
| 0.125 | 1.57 X 1.89 (SHOWN) |
| 0.15 | 1.43 X 1.73 |
| 0.175 | 1.33 X 1.60 |

4225480/C 11/2024

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

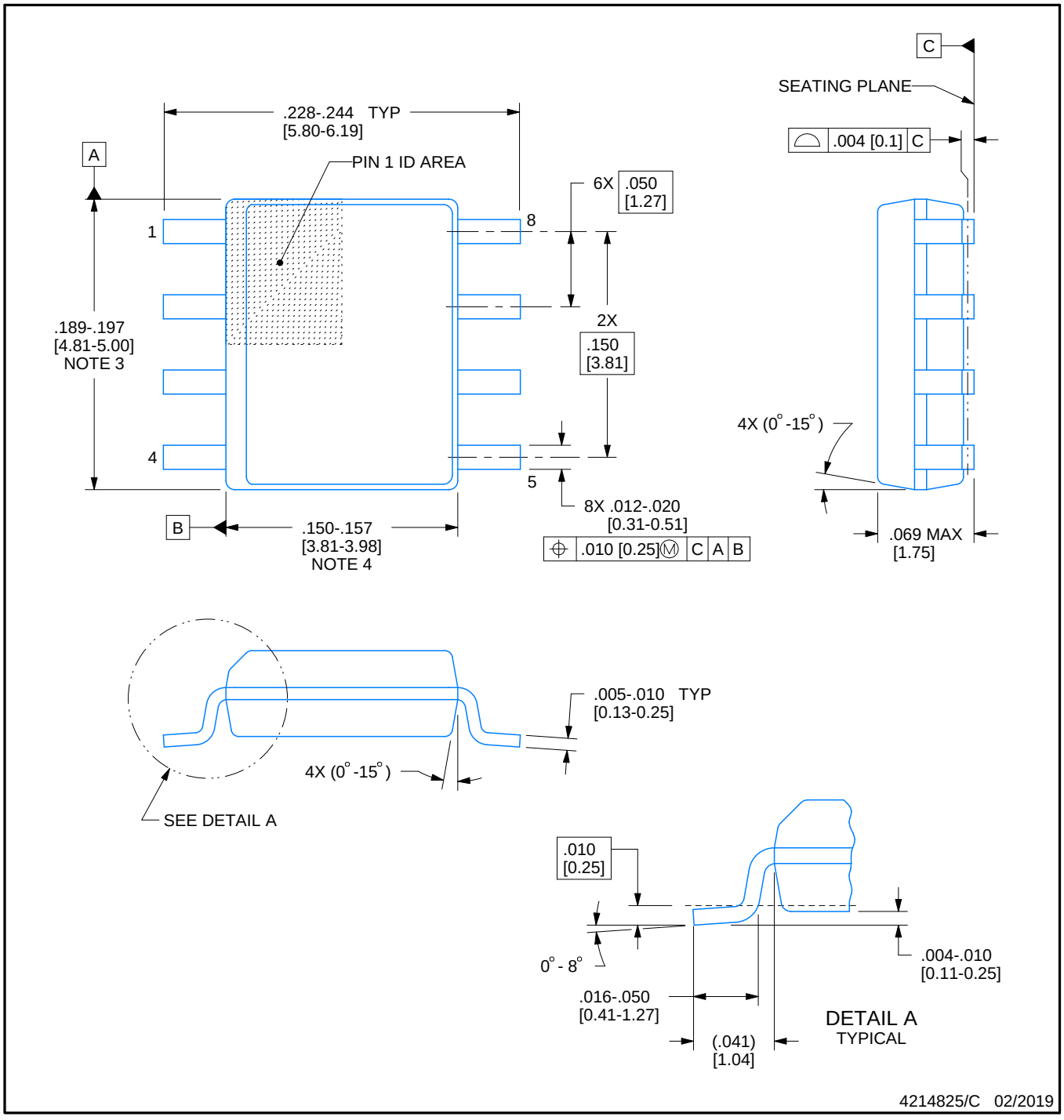


# PACKAGE OUTLINE

## D0008A

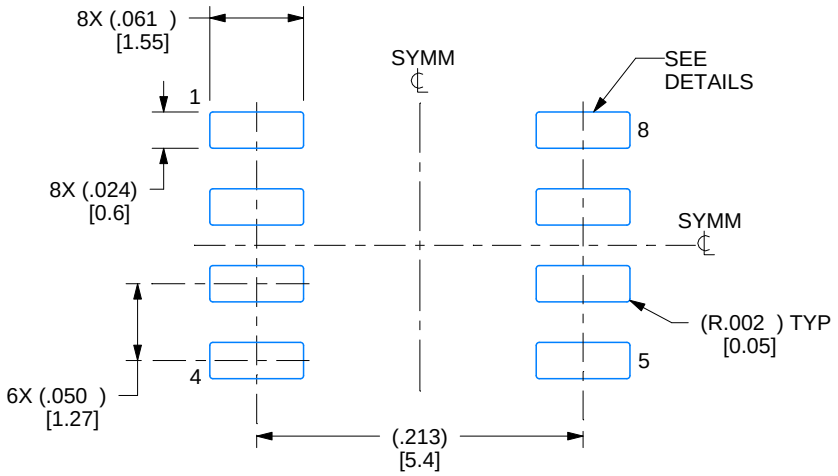
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

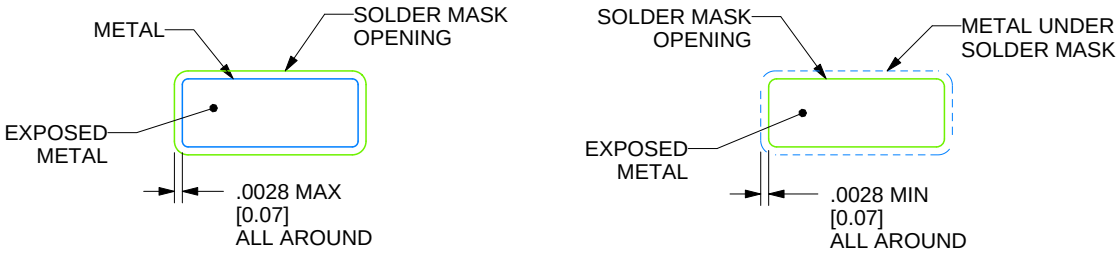



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

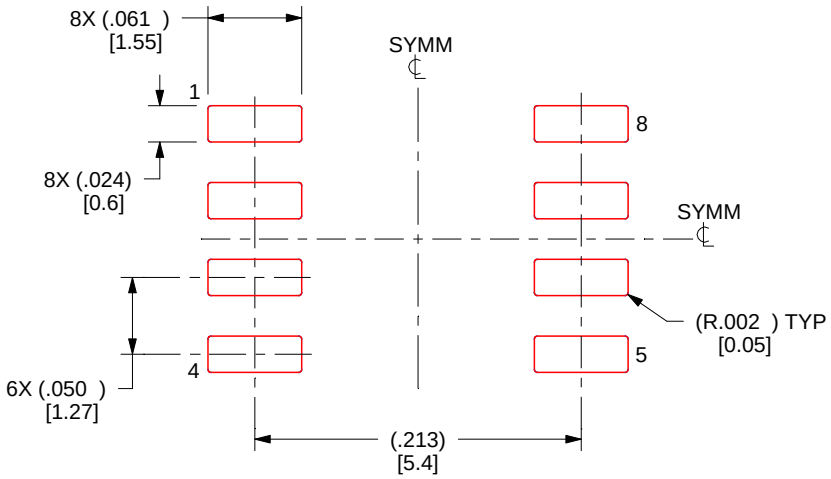
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265