Document Number: MC33781
Rev. 5.0, 11/2009

RoHS

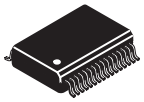
Quad DSI 2.02 Master with Differential Drive and Frequency Spreading

33781

DIFFERENTIAL DSI 2.02 MASTER

The 33781 is a master device for four differential DSI 2.02 buses. It contains the logic to interface the buses to a standard serial peripheral interface (SPI) port and the analog circuitry to drive data and power over the bus, as well as receive data from the remote slave devices.

The differential mode of the 33781 generates lower electromagnetic interference (EMI) in situations where data rates and wiring make this a problem. Frequency spreading further reduces interference by spreading the energy across many frequencies, reducing the energy in any single frequency.



EK SUFFIX (PB-FREE)
98ASA10556D
32-PIN SOICW EP

Features

- Four independent differential DSI (DBUS) channels
- Dual SPI interface
- Enhanced bus fault performance
- Automatic message cyclical redundancy checking (CRC) generation and checking for each channel
- Enhanced register set with addressable buffer allows queuing of 4 independent slave commands at one time for each channel
- 8- to 16-Bit messages with 0- to 8-Bit CRC
- Independent frequency spreading for each channel
- Pseudo bus switch feature on channel 0
- Pb-free packaging designated by suffix code EK

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MCZ33781EK/R2	-40°C to 90°C	32 SOICW EP

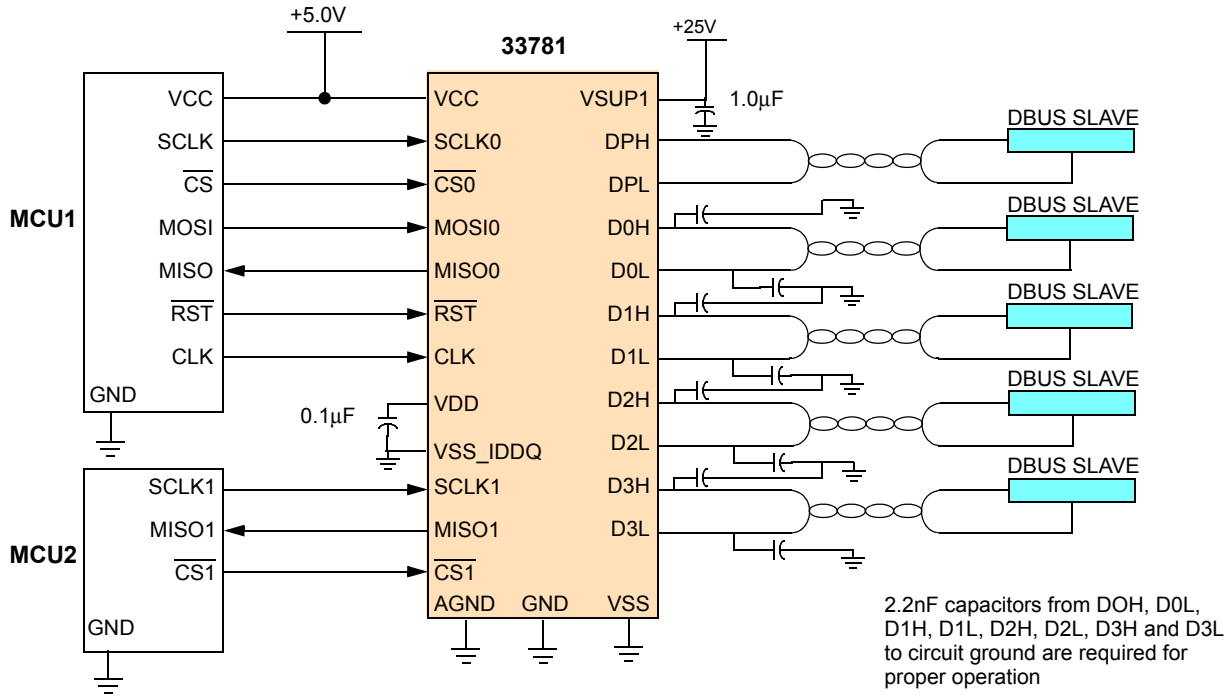


Figure 1. 33781 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

freescale semiconductor

INTERNAL BLOCK DIAGRAM

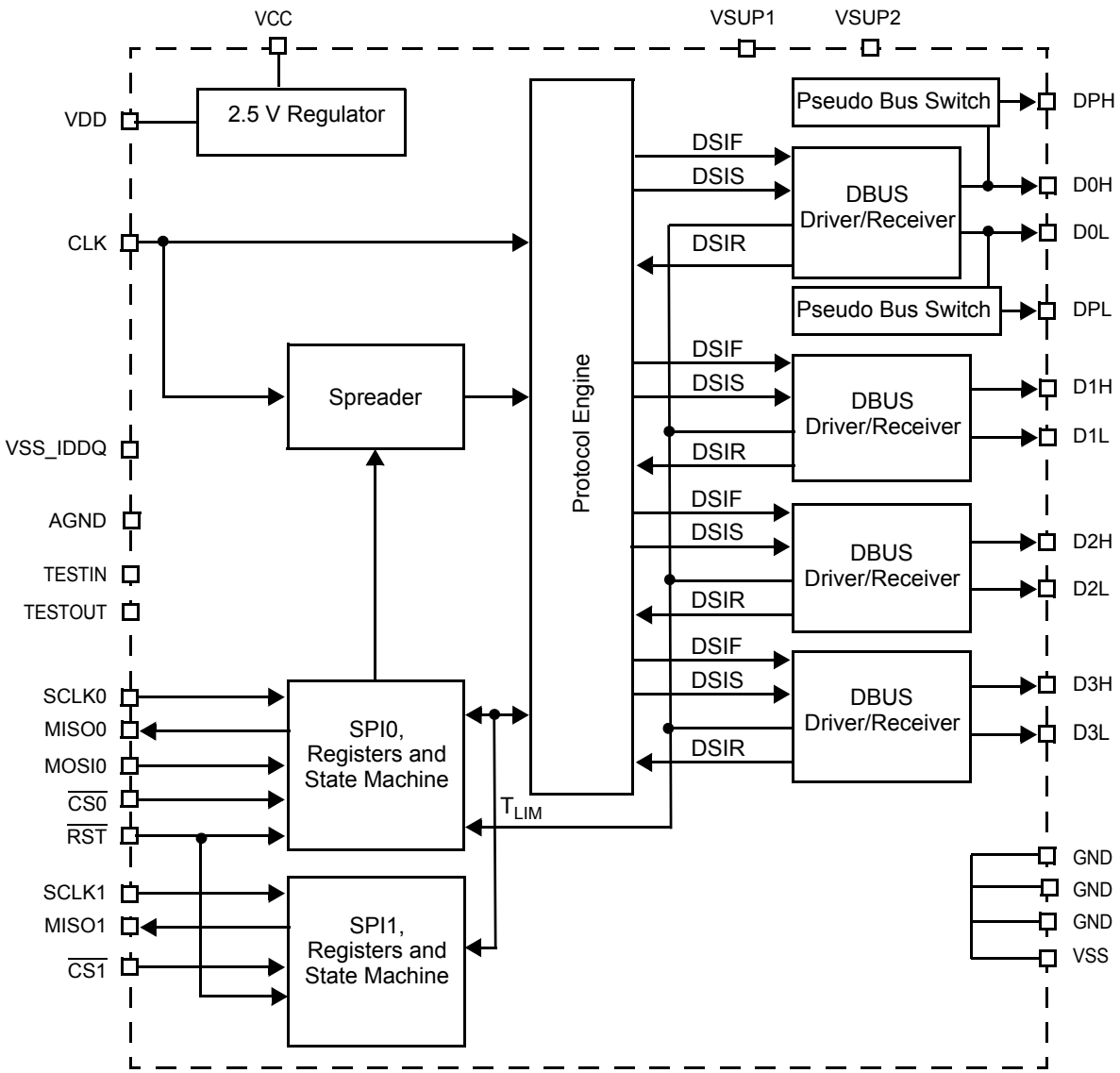


Figure 2. 33781 Internal Block Diagram

PIN CONNECTIONS

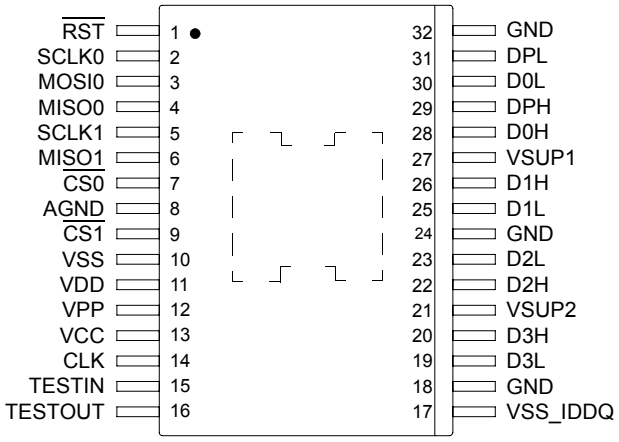


Figure 3. 33781 Pin Connections

Table 1. 33781 Pin Definitions

A functional description of each Pin can be found in the Functional Pin Descriptions section beginning on page 15.

Pin	Pin Name	Pin Function	Formal Name	Definition
1	$\overline{\text{RST}}$	Reset	IC Reset	A low level on this pin returns all registers to a known state as indicated in the sections entitled SPI0 Register and Bit Descriptions and SPI1 Communications.
2	SCLK0	Input	SPI0 Serial Data Clock	Clocks data in from and out to SPI0. MISO0 data changes on the negative transition of SCLK0. MOSI0 is sampled on the positive edge of SCLK0.
3	MOSI0	Input	SPI0 Master Out Slave In	SPI data into SPI0. This data input is sampled on the positive edge of SCLK0
4	MISO0	Output	SPI0 Master In Slave Out	SPI0 data sent to the MCU by this device. This data output changes on the negative edge of SCLK0. When $\overline{\text{CS0}}$ is high, this Pin is high-impedance.
5	SCLK1	Input	SPI1 Serial Data Clock	Clocks data out from SPI1. MISO1 data changes on the negative transition of SCLK1.
6	MISO1	Output	SPI1 Master In Slave Out	SPI1 data sent to the MCU by this device. This data output changes on the negative edge of SCLK1. When $\overline{\text{CS1}}$ is high, this Pin is high-impedance.
7	$\overline{\text{CS0}}$	Input	SPI0 Chip Select	When this signal is high, SPI signals on SPI0 are ignored. Asserting this pin low starts an SPI0 transaction. The SPI0 transaction is signaled as completed when this signal returns high.
8	AGND	Ground	Analog Ground	Ground for the analog circuits. This pin is not connected internally to the other grounds on the chip. It should be connected to a quiet ground on the board.
9	$\overline{\text{CS1}}$	Input	SPI1 Chip Select	When this signal is high, SPI signals on SPI1 are ignored. Asserting this pin low starts an SPI1 transaction. The SPI1 transaction is signaled as completed when this signal returns high.
10	VSS	Ground	Digital Ground	Digital ground connected internally to the other on-chip grounds. This ground is connected to circuits that will consume current during IDDQ testing.
11	VDD	Power	Digital Voltage	Output of the Internal 2.5V regulator for the digital circuits. No external current draw is allowed from this pin.

Table 1. 33781 Pin Definitions

A functional description of each Pin can be found in the Functional Pin Descriptions section beginning on page 15.

Pin	Pin Name	Pin Function	Formal Name	Definition
12	VPP	Input	Test Mode	A high-voltage on this pin puts the device in test mode for IC manufacturing test. It must be grounded in the application.
13	VCC	Input	Logic Supply	Regulated 5V input
14	CLK	Input	Clock Input	4.0MHz clock input
15	TESTIN	Test	Test Input	Input pin for device test. This pin must be tied to ground in the application.
16	TESTOUT	Test	Test Output	Output pin for device test. This pin is left floating in the application.
17	VSS_IDDQ	Ground	Digital Ground and IDDQ Test	Ground reference for the digital circuits that should not consume current during IDDQ testing. This ground is not connected to the other grounds internally.
18	GND	Ground	Power Ground	Bus power return
19	D3L	Output Driver	Low Side Bus 3	Bus 3 low side
20	D3H	Output Driver	High Side Bus 3	Bus 3 high side
21	VSUP2	Power	Positive Supply for Bus Outputs	This supply input is used to provide the positive level output of buses 2 and 3.
22	D2H	Output Driver	High Side Bus 2	Bus 2 high side
23	D2L	Output Driver	Low Side Bus 2	Bus 2 low side
24	GND	Ground	Power Ground	Bus power return
25	D1L	Output Driver	Low Side Bus 1	Bus 1 low side
26	D1H	Output Driver	High Side Bus 1	Bus 1 high side
27	VSUP1	Power	Positive Supply for Bus Outputs	This supply input is used to provide the positive level output of buses 0 and 1.
28	D0H	Output Driver	High Side Bus 0	Bus 0 high side
29	DPH	Output Driver	High Side Pseudo Bus	Pseudo Bus high side
30	D0L	Output Driver	Low Side Bus 0	Bus 0 low side
31	DPL	Output Driver	Low Side Pseudo Bus	Pseudo Bus low side
32	GND	Ground	Power Ground	Bus power return

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to GND unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Supply Voltages			V
VSUPn	V_{SUP1} and V_{SUP2}	-0.3 to 26.5	
Load Dump VSUPn (300ms maximum - either pin)	V_{SUPLD}	40	
VCC	V_{CC}	-0.3 to 7.0	
VDD	V_{DD}	-0.3 to 3.1	
VPP	V_{PP}	-0.3 to 10.0	
Maximum Voltage on Logic Input/Output Pins	–	-0.3 to V_{CC} + 0.3	V
Maximum Voltage on DBUS Pins	V_{DBUS}	-0.3 to V_{SUPn} + 0.3	V
Maximum DBUS Pin Current	I_{DBUS}	400	mA
Maximum Logic Pin Current	I_{LOGIC}	20	mA
ESD Voltage[1]			V
Human Body Model (HBM)	V_{ESD}	±2000	
Machine Model (MM)		±200	
Charge Device Model (CDM)			
Corner pins		±750	
All other pins		±500	
THERMAL RATINGS			
Storage Temperature	T_{STG}	-55 to 150	°C
Operating Ambient Temperature	T_A	-40 to 90	°C
Operating Junction Temperature	T_J	-40 to 150	°C
Thermal Shutdown (Bus Drivers and Pseudo Bus Switch)	T_{SD}	155 to 190	°C
Resistance, Junction-to-Ambient	$R_{\theta JA}$	71	°C/W
Resistance, Junction-to-Board	$R_{\theta JB}$	6	°C/W
Soldering Reflow Temperature	T_{SOLDER}	260	°C
Peak Package Reflow Temperature During Reflow[2],[3]	T_{PPRT}	Note 3	°C

Notes

1. ESD1 testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100pF, R_{ZAP} = 1500Ω); ESD2 testing is performed in accordance with the Machine Model (MM) (C_{ZAP} = 200pF, R_{ZAP} = 0Ω); and Charge Body Model (CBM).
2. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
3. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 4.75V ≤ V_{CC} ≤ 5.25V, 9.0V ≤ V_{SUPn} ≤ 25V,-40°C ≤ T_A ≤ 90°C, unless otherwise noted. Voltages relative to GND, unless otherwise noted. Typical values noted reflect the approximate mean values of the parameter at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT REQUIREMENTS (VSUPn, VCC)					
I_{VSUPT} Supply Current (Test Mode, CLK = 4.0MHz)	I_{VSUPT}				mA
High Z		–	–	16	
Signal, Idle (Ibus = 0)		–	–	33	
Signal, Idle (Ibus = 10mA on all channels, a total of 40mA)		–	–	61	
I_{VCC} Supply Current (CLK = 4.0MHz, RST = high)	I_{VCC}				mA
Signal, Idle (Ibus = 0)		–	–	10.0	
Signal, Idle (Ibus = 10mA on all channels, a total of 40mA)		–	–	12.0	
V_{SUPn} Low Detect Threshold Vcc > 4.75V	$V_{VSUPnLO}$	9.1	–	9.9	V
V_{SUPn} Low Mask Time Vcc > 4.75V	t_{MASK}	20	–	25	µs
MICROCONTROLLER INTERFACE ($\overline{RST}$, $\overline{CSn}$, MOSI0, MISOn, SCLKn, and CLK)					
I/O Logic Levels (RST, CSn, MOSI0, SCLKn, and CLK)					V
Input High Voltage	V_{IH}	2.0	-	V_{CC} +0.3	
Input Low Voltage	V_{IL}	-0.3	-	1.0	
Input Hysteresis[4]	V_{HYST}	0.1	-	0.5	
Input Capacitance[4]	C_I				pF
CSn, MOSI0, and SCLKn		–	–	10	
RST and CLK		–	–	20	
Output Low Voltage MISOn Pin = 0.3mA	V_{OL}	0	–	0.8	V
Output High Voltage MISOn Pin = -0.3mA	V_{OH}	V_{CC} - 0.8	–	V_{CC}	V
Output Leakage Current	I_{MISO}				µA
MISOn Pin = 0V		-10	–	10	
MISOn Pin = V_{CC}		-10	–	10	
SCLKn, CSn Pull-up Current VOUT = V_{CC} - 2.0 V	I_{PU}	-50	-30	-10	µA
$\overline{RST}$ Pull-down Current V_{OUT} = 1.0V	$I_{\overline{RST}PD}$	5.0	-	13	µA
CLK, MOSI0 Pull-down Current V_{OUT} = 1.0V	I_{PD}	5.0	10	13	µA

Notes

4. Not measured in production.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 4.75V ≤ V_{CC} ≤ 5.25V, 9.0V ≤ V_{SUPn} ≤ 25V,-40°C ≤ T_A ≤ 90°C, unless otherwise noted. Voltages relative to GND, unless otherwise noted. Typical values noted reflect the approximate mean values of the parameter at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
BUS TRANSMITTER (DnH, DnL)					
Output Bus Idle Voltage (Drop) I_{nH} = -200mA, I_{nL} = 200mA(6)	$V_{DnD(Drop)}$(7)(8)	–	–	1.6	V
Output Signal High Voltage (Differential) -12.5mA ≤ InH ≤ 1.0mA, -1.0mA ≤ InL ≤ 12.5mA (6)	$V_{DnD(HIGH)}$(7)	4.175	4.5	4.825	V
Output Signal Low Voltage (Differential) -12.5mA ≤ InH ≤ 1.0mA, -1.0mA ≤ InL ≤ 12.5mA(6)	$V_{DnD(LOW)}$(7)	1.175	1.5	1.825	V
Vmid, (DnH + DnL)/2 (Voltage Halfway Between Bus High Side and Bus Low Side	V_{MID}(8)	V_{SUPn}/ 2 - 0.8	V_{SUPn}/2	V_{SUPn}/ 2 +0.8	V
VCM Peak to Peak (Maximum Vmid-Minimum Vmid) For Vmid (Idle), Vmid (Signal_H), Vmid (Signal_L)(5)	V_{CMP}	0	–	30	mV
Bus Driver Vmid Peak to Peak, (DnH+DnL)/2(5) For Signal to Idle, Idle, Idle to Signal, VmidPP(Idle)=Vmid(Max)- Vmid (Min)	$V_{MIDPP(IDLE)}$	–	–	300	mV
Bus Driver Vmid Peak to Peak (Dnh+DnL)/2(5) For Signal_H to Signal_L, Signal_L, Signal_L to Signal_H, Signal_H VmidPP(Signal)=Vmid(Max)-Vmid(Min)	$V_{MIDPP(SIGNAL)}$	–	–	80	mV
Output High Side (DnH) Driver Current Limit Fault Condition: DnH = 0V Normal Operation Fault Condition: DnH = V_{SUPn}	$I_{CL(HIGH)}$	 -600 -400 150	 – – –	 -200 -200 350	mA
Output Low Side (DnL) Driver Current Limit Fault Condition: DnL = 0V Fault Condition: DnL = V_{SUPn}	$I_{CL(LOW)}$	 -350 200	 – –	 -150 400	mA
Signal mode Over-current Shutdown I ISSD I DnH, DnL	I_{SSD}	20		60	mA
Disabled High Side (DnH) Bus Leakage (DnL open) DnH = 0V DnH = V_{SUPn}	$I_{LK(HIGH)}$	 -1.0 -1.0	 – –	 1.0 1.0	mA
Disabled Low Side (DnL) Bus Leakage (DnH open)(9) DnL = 0V DnL = V_{SUPn}	$I_{LK(LOW)}$	 -1.0 -1.0	 – –	 1.0 1.0	mA

Notes

5. Not measured in production.
6. InH=bus current at DnH, InL=bus current at DnL
7. V_{DnD}=V_{DnH}-V_{DnL}
8. Max V_{DnD} = VSUPn - 2 * V_{MID_OFFSET} - $V_{DnD(Drop)}$, V_{MID_OFFSET} = |V_{MID} - V_{SUPn} / 2|
9. Worst Case Disabled Low Side Bus Leakage for DnL occurs with DnL = V_{SUP} and DnH = 0V. In this configuration, the DnL leakage current can exceed 1mA. This is not measured in production.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 4.75V ≤ V_{CC} ≤ 5.25V, 9.0V ≤ V_{SUPn} ≤ 25V,-40°C ≤ T_A ≤ 90°C, unless otherwise noted. Voltages relative to GND, unless otherwise noted. Typical values noted reflect the approximate mean values of the parameter at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
BUS TRANSMITTER (DnH, DnL) (CONTINUED)					
High Side Pseudo Bus Switch Resistance I_{SWH}=160mA	R_{SWH}	–	8.0	16.0	Ω
Low Side Pseudo Bus Switch Resistance I_{SWL}=160mA	R_{SWL}	–	8.0	16.0	Ω
Pseudo Bus Switch Matching	$R_{PSMATCH}$	–	–	1.0	Ω
High Side Pseudo Bus Switch Leakage Current DPH = Open: CH0 drivers in Idle, DPH = 0V or CH0 drivers in Signal_H, DPH = 25V	I_{DPHLK}	-20	–	20	µA
Low Side Pseudo Bus Switch Leakage Current DPL = Open: CH0 drivers in Idle, DPL = 25V,or CH0 drivers in Signal_H, DPL = 0V	I_{DPLLK}	-20	–	20	µA
BUS RECEIVER (DnH, DnL)					
Comparator Trip Point for High Side	$COMP_{HIGH}$	5.0	6.0	7.0	mA
Comparator Trip Point for Low Side	$COMP_{LOW}$	5.0	6.0	7.0	mA
Comparator Trip Point for Adder	$COMP_{ADD}$	6.0	12	18	mA

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 4.75V ≤ V_{CC} ≤ 5.25V, 9.0V ≤ V_{SUPn} ≤ 25V,-40°C ≤ T_A ≤ 90°C, unless otherwise noted. Voltages relative to GND, unless otherwise noted. Typical values noted reflect the approximate mean values of the parameter at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CLOCK					
CLK Periods (System requirement)(10)					ns
Time High	t_{CLKHI}	75	–	–	
Time Low	t_{CLKLO}	75	–	–	
Period	t_{CLKPER}	245	250	255	
CLK Transition (System requirement)(10)					ns
Time for Low-to-High Transition of the CLK Input Signal	t_{CLKLH}	–	–	100	
Time for High-to-Low Transition of the CLK Input Signal	t_{CLKHL}	–	–	100	
Reset Low Time	t_{RSTLO}	100	–	–	ns
SPI INTERFACE TIMING					
SPI Clock Cycle Time	t_{CYC}	100	–	–	ns
SPI Clock High Time	t_{HI}	40	–	–	ns
SPI Clock Low Time	t_{LO}	40	–	–	ns
SPI $\overline{CSn}$ Lead Time(11)	t_{LEAD}	50	–	–	ns
SPI $\overline{CSn}$ Lag Time(11)	t_{LAG}	50	–	–	ns
SPI $\overline{CS0}$ Time Between Bursts(10)	$t_{\overline{CS0}HI}$	80	–	–	ns
SPI $\overline{CS1}$ Time Between Bursts(10)	$t_{\overline{CS1}HI}$	300	–	–	ns
Data Setup Time MOSI0 Valid Before SCLK0 Rising Edge(11)	t_{SU}	10	–	–	ns
Data Hold Time MOSI0 Valid After SCLK0 Rising Edge(11),(10)	t_H	10	–	–	ns
Data Valid Time SCLKn Falling Edge to MISOn Valid, C = 50pF(12)	t_V	–	–	25	ns
Output Disable Time $\overline{CSn}$ Rise to MISOn Hi-Z	t_{DIS}	–	–	50	ns
Rise Time (30% V_{CC} to 70% V_{CC})(10) SCLKn, MOSI0	t_R	–	–	10	ns
Fall Time (70% V_{CC} to 30% V_{CC})(10) SCLKn, MOSI0	t_F	–	–	10	ns

Notes
10. Not measured in production.
11. SPI signal timing from the production test equipment is programmed to ensure compliance.
12. Conditions are verified indirectly during test.

Table 4. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 4.75V ≤ V_{CC} ≤ 5.25V, 9.0V ≤ V_{SUPn} ≤ 25V,-40°C ≤ T_A ≤ 90°C, unless otherwise noted. Voltages relative to GND, unless otherwise noted. Typical values noted reflect the approximate mean values of the parameter at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
BUS TRANSMITTER					
Idle-to-Signal and Signal-to-Idle Slew Rate[13]	$t_{SLEW(IDLE)}$	3.0	6.0	8.0	V/µs
Signal High-to-Low and Signal Low-to-High Slew Rate[13],[14] (See Data Valid DSIS to DnD Timing)	$t_{SLEW(SIGNAL)}$	3.0	6.0	8.0	V/µs
Communication Data Rate Capability[14] (Ensured by Transmitter Data Valid and Receiver Delay Measurements) Data Rate(before frequency spreading)	D_{RATE}	77.1	–	200	kbps
Signal Bit Time (1 / D_{RATE})[14] The Max value depends on the settings in the FSEL bits	t_{BIT}	5.0	–	–	µs
DBUS Start Delay, $\overline{CS0}$ Rising Edge to DBUS[14] note: DLY is the inter-message delay selected in the DnCTRL register	$t_{DBUSSTART2}$	2/3t_{BIT} + (DLY-2) * t_{BIT}	–	5/3t_{BIT} + (DLY-2) * t_{BIT}	µs
Data Valid[13]					µs
DSIF = 0.5 * V_{CC} to DnD Fall = 5.5 V (9V ≤ V_{SUPn} ≤ 40V)	t_{DVLD1}	–	–	5.3	
DSIS = 0.5 * V_{CC} to DnD Fall = 2.8V (9V ≤ V_{SUPn} ≤ 40V)	t_{DVLD2}	–	–	1.0	
DSIS = 0.5 * V_{CC} to DnD Rise = 3.2V (9V ≤ V_{SUPn} ≤ 40V)	t_{DVLD3}	–	–	**1.0**	
DSIF = 0.5 * V_{CC} to DnD Rise = 6.5 V (9V ≤ V_{SUPn} ≤ 40V)	t_{DVLD4}	–	–	1.0	
Signal mode Over-current Shutdown Delay[14]	t_{OC}	3.0	5.0	7.0	µs
Signal Low Time for Logic Zero 33.3% Duty Cycle (2/3*t_{BIT}) ± 10% for threshold delta	$t0_{LO}$	0.6 * t_{BIT}	2/3 * t_{BIT}	0.73 * t_{BIT}	µs
Signal Low Time for Logic One 66.7% Duty Cycle (1/3*t_{BIT}) ± 10% for threshold delta	$t1_{LO}$	0.3 * t_{BIT}	1/3 * t_{BIT}	0.37 * t_{BIT}	µs

Notes
13. C = 2.8nF from DnH to DnL and 2.2nF from DnH and DnL to GND, capacitor tolerance = ±10%.
14. Not measured in production.

Table 4. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 4.75V ≤ V_{CC} ≤ 5.25V, 9.0V ≤ V_{SUPn} ≤ 25V,-40°C ≤ T_A ≤ 90°C, unless otherwise noted. Voltages relative to GND, unless otherwise noted. Typical values noted reflect the approximate mean values of the parameter at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
BUS RECEIVER					
Receiver Delay Time (I_{RSP} = 0mA / 11mA step)(15)					ns
I_{RSP} = -6.0mA to DSIR = 0.5 * V_{CC}	t_{DRH}	–	–	500	
I_{RSP} = -6.0mA to DSIR = 0.5 * V_{CC}	t_{DRL}	–	–	500	
Common Mode Current Noise Rejection (2.5ms max.)	I_{CMNR}	-50	–	+50	mA
SPREAD SPECTRUM					
Base Frequency Range	f_{CEN}	77.1 - 2%	–	200 + 2%	kHz
PSEUDO BUS					
Pseudo Bus On Delay Time	t_{PBD1}	–	5	10	µs
Pseudo Bus Off Delay Time	t_{PBD2}	–	5	10	µs

Notes

15. Not measured in production.

TIMING DIAGRAMS

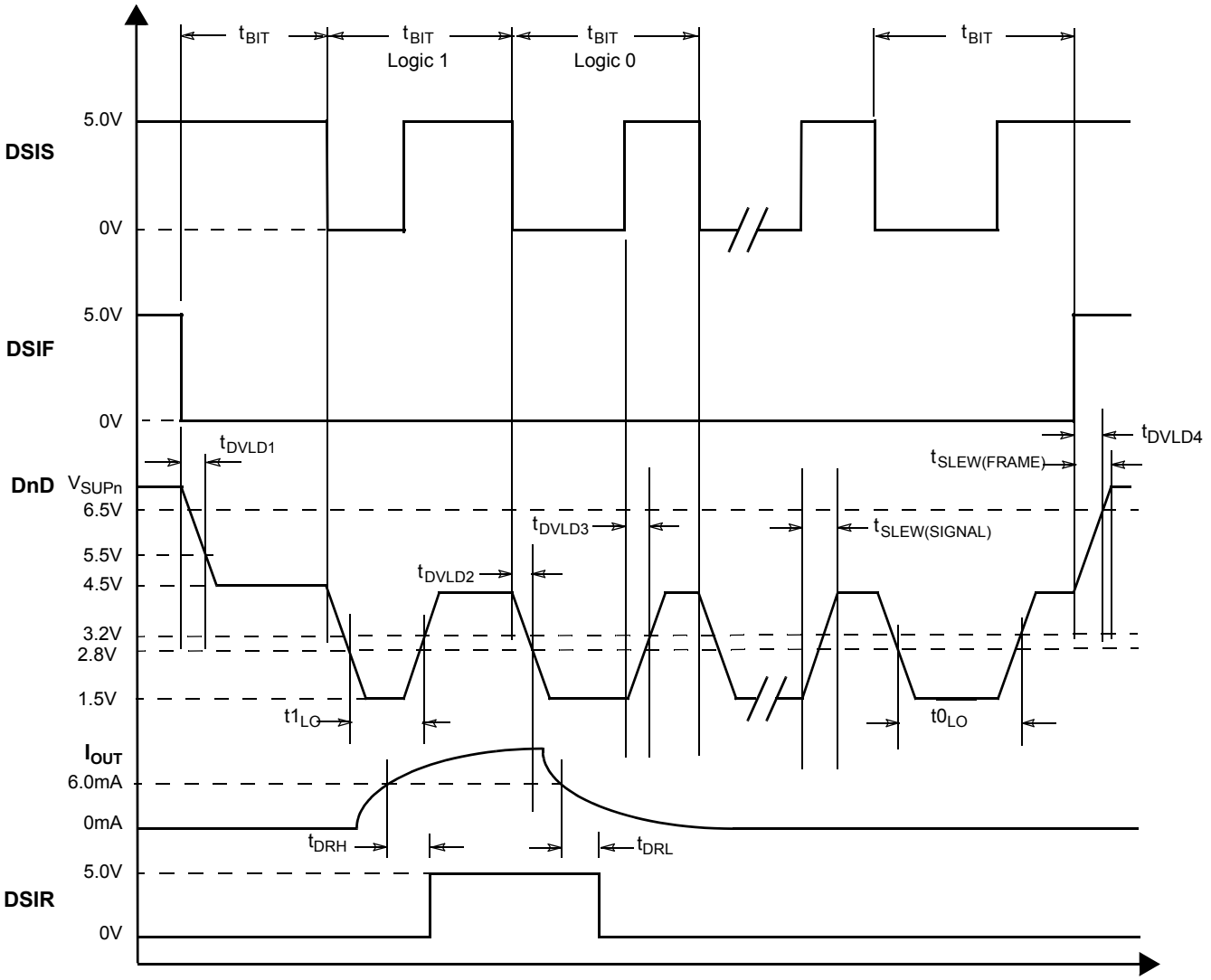


Figure 4. DBUS Timing Characteristics

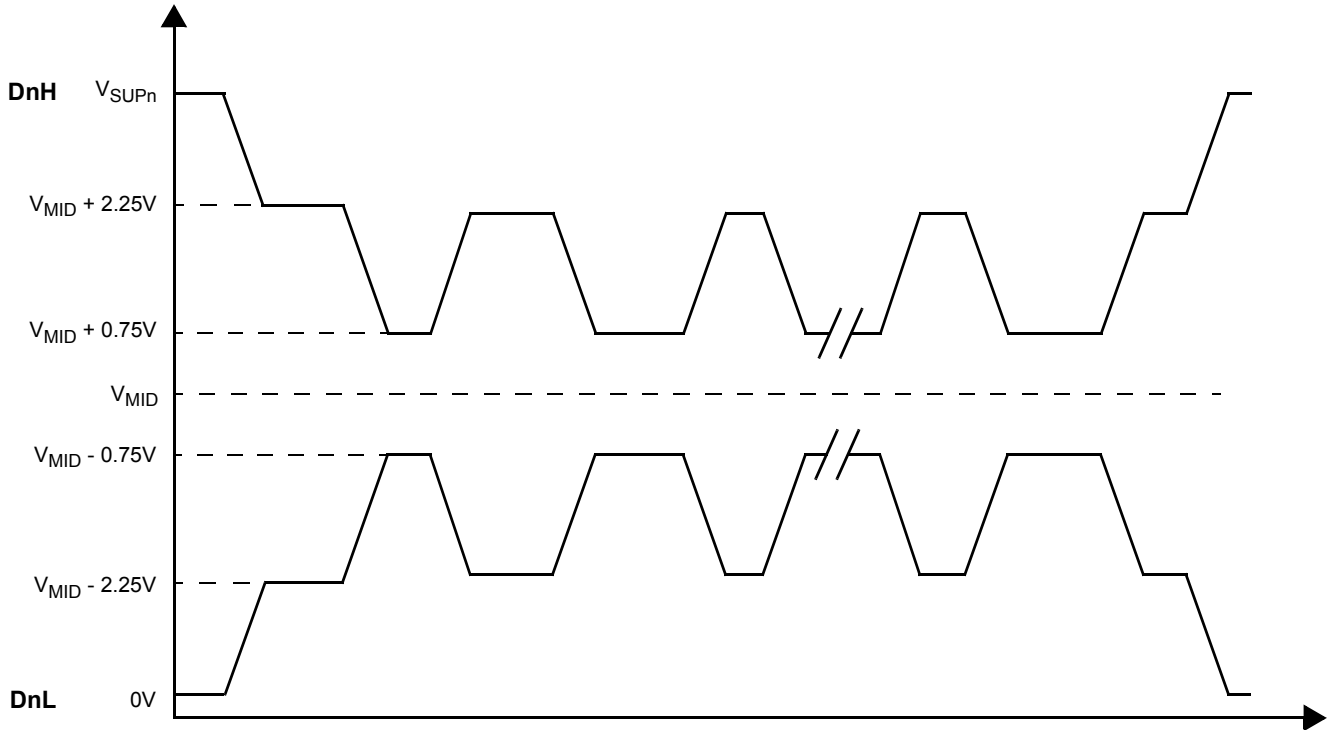


Figure 5. DBUS Normal Bus Waveforms

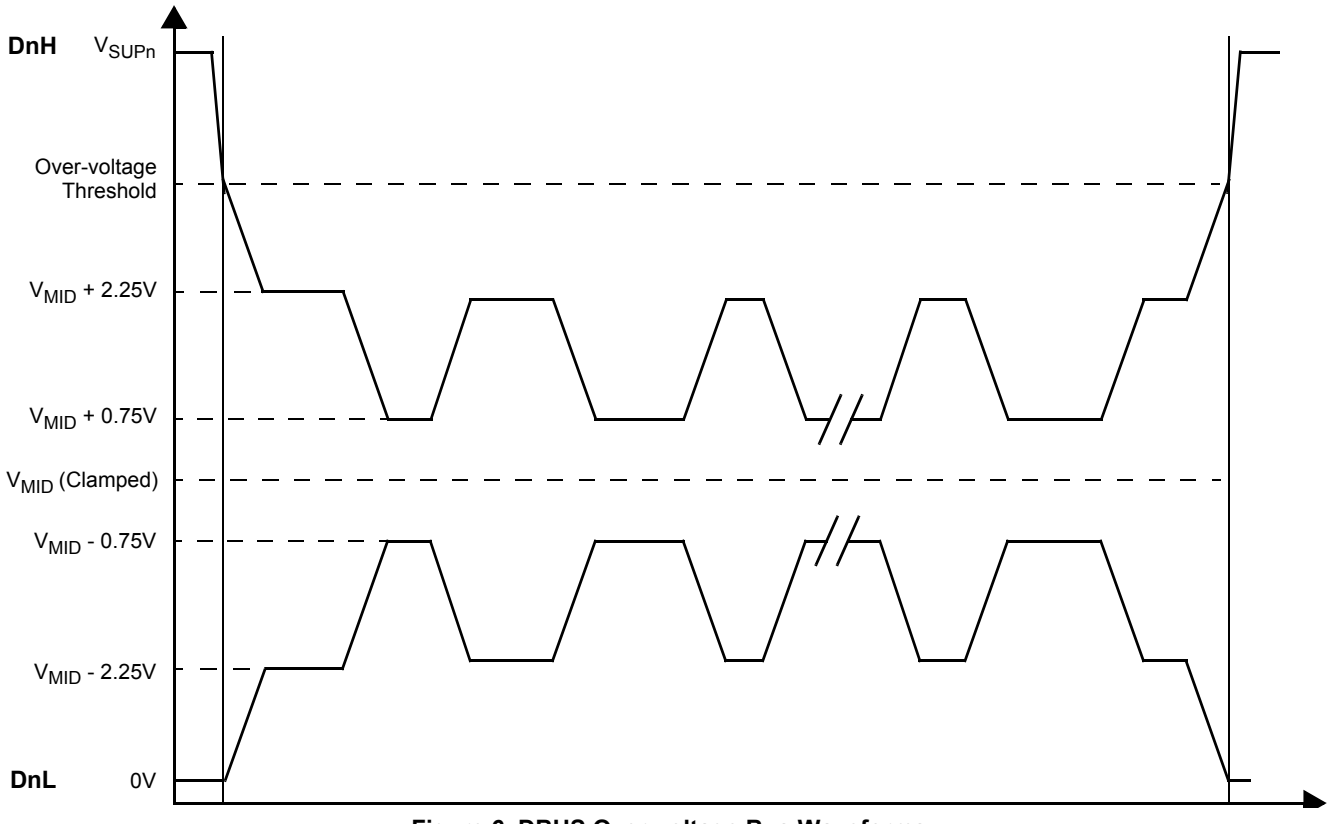
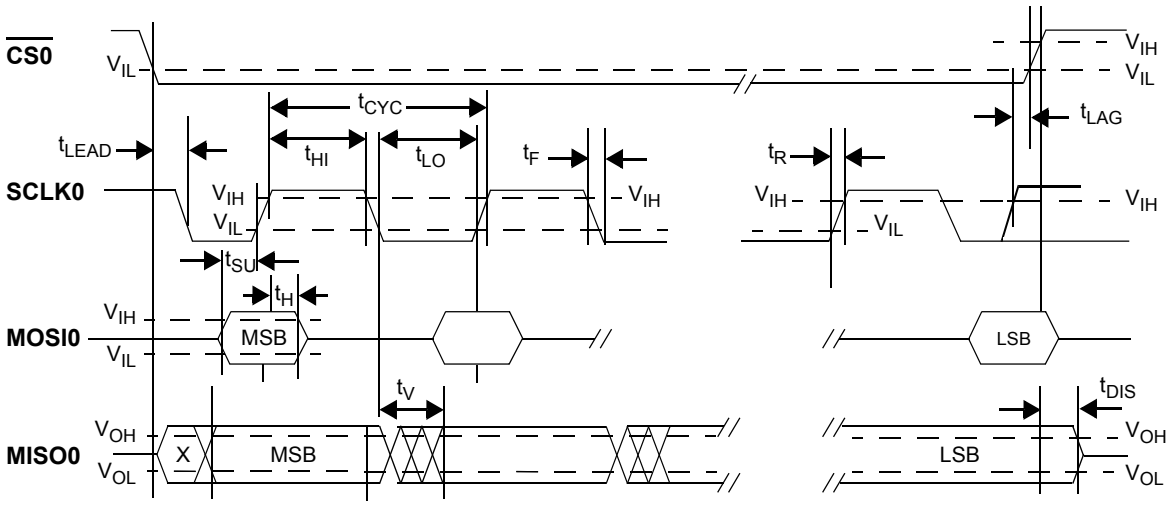


Figure 6. DBUS Over-voltage Bus Waveforms

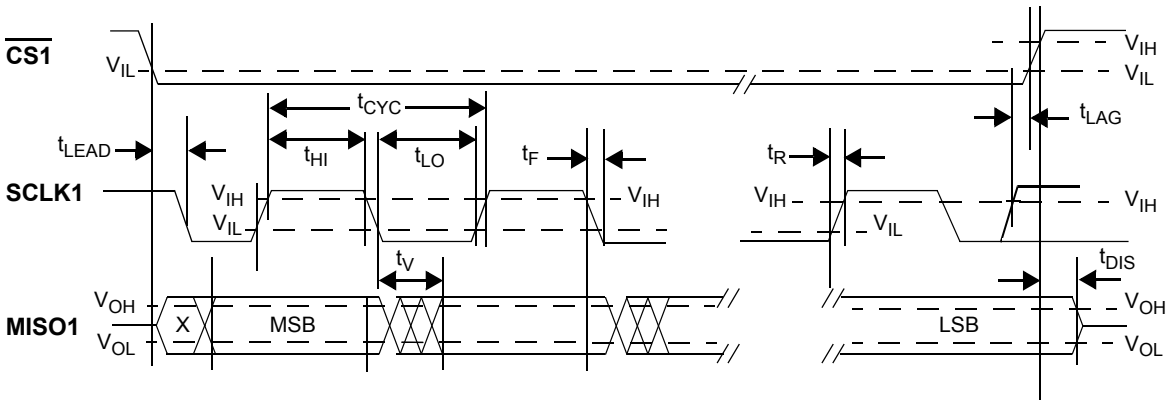


X = Don't care

V_{IH} = 70% V_{CC}, V_{OH} = 70% V_{CC}

VIL = 30% VCC, VOL = 30% VCC

Figure 7. SPI0 Interface Timing



X = Don't care

V_{IH} = 70% V_{CC}, V_{OH} = 70% V_{CC}

VIL = 30% VCC, VOL = 30% VCC

Figure 8. SPI1 Interface Timing

FUNCTIONAL DESCRIPTIONS

INTRODUCTION

The 33781 is intended to be used as a master device in a distributed system. It contains both protocol generators and physical interfaces, to allow an MCU to communicate with devices on the bus using two different SPI interfaces. Four differential buses are provided. The physical layer uses a two-wire bus to carry power and signal. The physical layer uses wave-shaped voltage signals for commands from the master and wave-shaped current signals for responses from the slaves. The protocol and physical layer conform to the DSI 2.02 specification.

The equivalent bus capacitance consists of capacitors connected between the two bus wires and capacitors between the bus wires and ground. Because the voltage change on either of the bus wires to ground is only 1/2 the amount of change between the two bus wires, the capacitance to ground only conducts half as much current as it would if connected directly across the bus. The equivalent bus capacitance of a capacitor to ground from the bus wires is one half of the actual amount of the capacitor. The amount of capacitance from either bus wire to ground should be kept the same in order to achieve the lowest radiated EMI energy. The 2.2nF capacitors required between the bus wires and ground result in an equivalent of 1.1nF of capacitance across the bus as seen by either bus wire.

Table 5 shows the voltages used for operation. Low side (LS) is the bus wire that is the most negative and high side (HS) is the bus wire that is the most positive. Figure 5 shows the bus waveforms in normal operation.

Table 5. High Side and Low Side Typical Voltages (Voltage Relative to Ground)

Low Side			High Side		
IDLE	HIGH	LOW	IDLE	HIGH	LOW
0	Vmid-2.25 (16)	Vmid-0.75 (16)	V_{SUPn}	Vmid+2.25 (16)	Vmid+0.75 (16)

Notes
16. $V_{MID} = V_{SUPn}/2$.

FUNCTIONAL PIN DESCRIPTIONS

RESET ($\overline{RST}$)

When pulled low, this will reset all internal registers to a known state as indicated in the section entitled SPI0 Register and Bit Descriptions on page 29.

CHIP SELECT n ($\overline{CSn}$)

This input is used to select the SPIn port when pulled to ground. When high, the associated SPIn port signals are ignored. The SPIn transaction is signaled as completed when this signal returns high.

MASTER OUT/SLAVE IN 0 (MOSI0)

This is the SPI data input to the device. This data is sampled on the positive (rising) edge of SCLK0. There is no MOSI pin or function for SPI1.

SERIAL CLOCK (SCLKn)

This is the clock signal from the SPIn master device. It controls the clocking of data to SPIn and data reads from the SPIn.

MASTER IN/SLAVE OUT (MISOn)

This is the SPIn data from SPIn to the SPIn master. Data changes on the negative (falling) transition of the associated SCLKn.

CLOCK (CLK)

This is the main clock source for the internal logic. It must be 4.0MHz.

GROUND (GND)

Ground source for DSI/DBUS return.

DIGITAL GROUND (VSS)

Ground source for logic.

DIGITAL GROUND AND IDDQ (VSS_IDDQ)

Used for IDDQ testing during IC manufacturing test.

ANALOG GROUND (AGND)

Ground source for analog circuits.

POWER SOURCE (VCC)

Nominal +5.0V Regulated Input.

DIGITAL REGULATOR OUTPUT (VDD)

Nominal +2.5V internal regulator Pin. This must be bypassed with a small capacitor to ground (100nF)

LOW SIDE BUS (DnL)

There are four independent low side outputs, D0L, D1L, D2L and D3L. They comprise the low side differential output signal of the DBUS physical layer as shown in Figure 5. They also provide power to the slave modules during the DBUS idle time. The output of DnL should have a bypass capacitor of 2.2nF to ground.

HIGH SIDE BUS (DnH)

There are four independent high side outputs, D0H, D1H, D2H, and D3H. They comprise the high side differential output signal of the DBUS physical layer. They also provide power to the slave modules during the DBUS idle time. See Figure 5. The output of DnH should have a bypass capacitor of 2.2nF to ground.

POSITIVE SUPPLY FOR BUS OUTPUT (VSUPn)

This 9.0V to 25V power supply is used to provide power to the slave devices attached to the DBUS. During the bus idle time, the storage capacitors in the slave modules are charged up to maintain a regulated supply to the slave device. V_{SUP1} powers devices DBUS0 and DBUS1, and V_{SUP2} powers devices on DBUS2 and DBUS3. See Figure 9.

The two supplies are interdependent internally, however, as can be seen in Figure 9: V_{SUP1} is used to create the V_{CM_REF} voltage for all four driver buffers, and V_{SUP2} is used to supply the charge pump voltage. Consequently, both V_{SUP1} and V_{SUP2} are required for internal functions: for example, the internal voltage regulator V_{REG_8V} is supplied from V_{SUP1}, but uses the V_{SUP2}-derived charge pump voltage to supply the output NMOS devices.

PSEUDO BUS (DPH AND DPL)

These bus high and bus low pins are created by closing the pseudo bus switches attached to the D0H and D0L bus lines internal to the 33781. This allows a second external set of bus lines to communicate over the D0 Channel. The pseudo bus switches are controlled by the system MCU through SPI0.

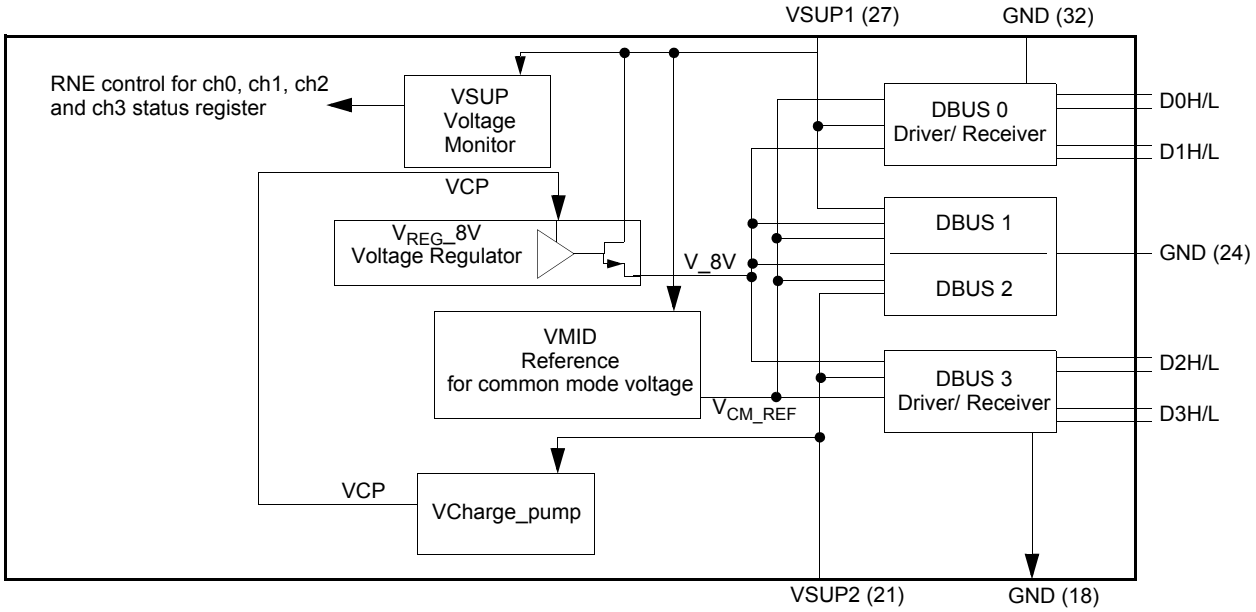


Figure 9. VSUP Block Diagram

FUNCTIONAL INTERNAL BLOCK DESCRIPTION

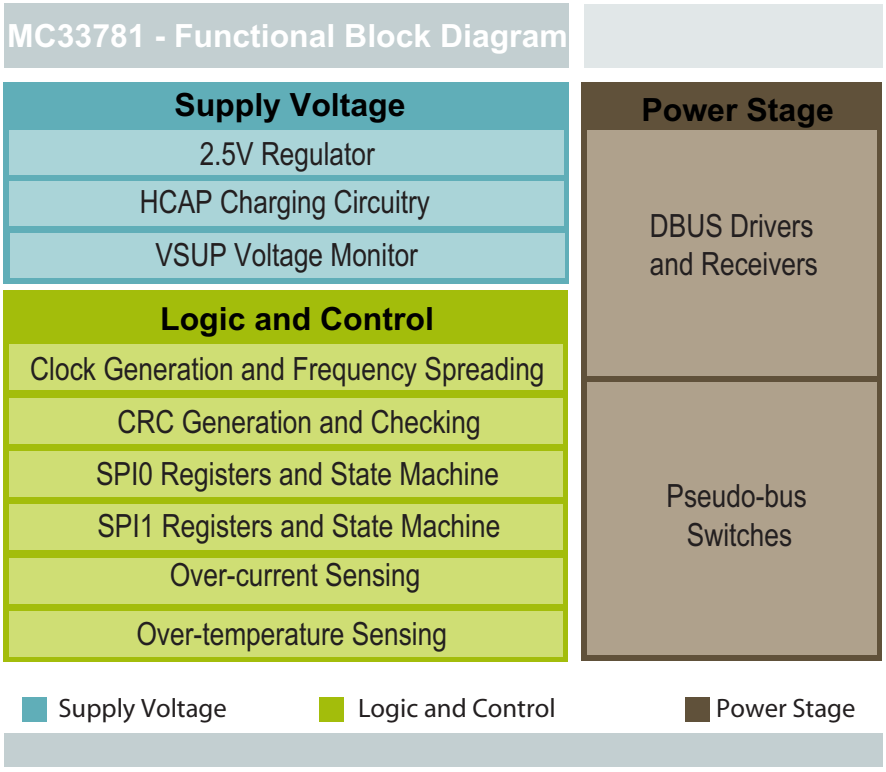


Figure 10. Block Illustration

The 33781 is controlled by an MCU through the SPI0 interface. It handles the digital and physical layer portions of a DBUS master node. Four separate DBUS channels are included. The physical layer uses a two-wire bus with analog wave-shaped voltage and current signals. Refer to Figure 1.

Major subsystems include the following:

- SPI0 interface and registers to a main MCU
- SPI1 interface and registers to a second MCU
- Four channels of DSI 2.02 protocol state logic
- CRC block for each channel
- Control and status registers
- Four addressable register sets per channel for queuing up to four commands and data per bus. The addressable buffer acts as a circular buffer for command writes and data reads.
- Pseudo Bus Switch from D0H/L to DPH/L

SPI0 AND REGISTERS

This block contains the SPI0 interface logic and the control and response registers that are written to and read from the SPI interface.

The IC is an SPI slave-type device, so MOSI0 (Master-Out-Slave-In) is an input and MISO0 (Master-In-Slave-Out) is an output. $\overline{CS0}$ and SCLK0 are also inputs.

The SPI0 port can handle 2-byte and 4-byte transfers. It addresses 87 registers. The organization of the registers is described in the section entitled SPI0 Register and Bit Descriptions on page 29.

SPI1 AND REGISTERS

The 33781 has a second SPI port (called SPI1) that allows valid response data from Bus Channel 2 and 3, along with the slave address, to be read independently by a second MCU. This block contains the SPI1 interface logic and the response registers that are read from the SPI1 interface.

The IC is an SPI slave-type device, so MISO1 (Master-In-Slave-Out) is an output, and $\overline{CS1}$ and SCLK1 are inputs. SPI1 does not use the MOSI (Master-Out-Slave-In) pin or function as it does not receive commands.

The SPI1 port handles only 16-bit transfers. It addresses eight registers which are read only.

PROTOCOL ENGINE

This block converts the data to be transmitted from the registers into the DBUS sequences, and converts DBUS response sequences to data in the registers.

The DBUS transmit protocol uses *a return to 1* type data with a duty cycle determined by the logic state. The protocol includes Cyclical Redundancy Check (CRC) generation and validation.

VSUPn VOLTAGE MONITOR

This function monitors the voltage on the V_{SUPn} pin. If the voltage on the pin drops below the defined voltage threshold for longer than the voltage threshold mask time, the 33781 will continue to send queued DBUS commands, but not set any RNE bits in the DnSTAT registers to 1, until either the device is reset by the $\overline{RST}$ pin or the EN bits in the DnEN registers are first set to zero, and then to one (disabled and then enabled). By monitoring the RNE bits the MCU will know that communications have been disrupted and can take the appropriate action.

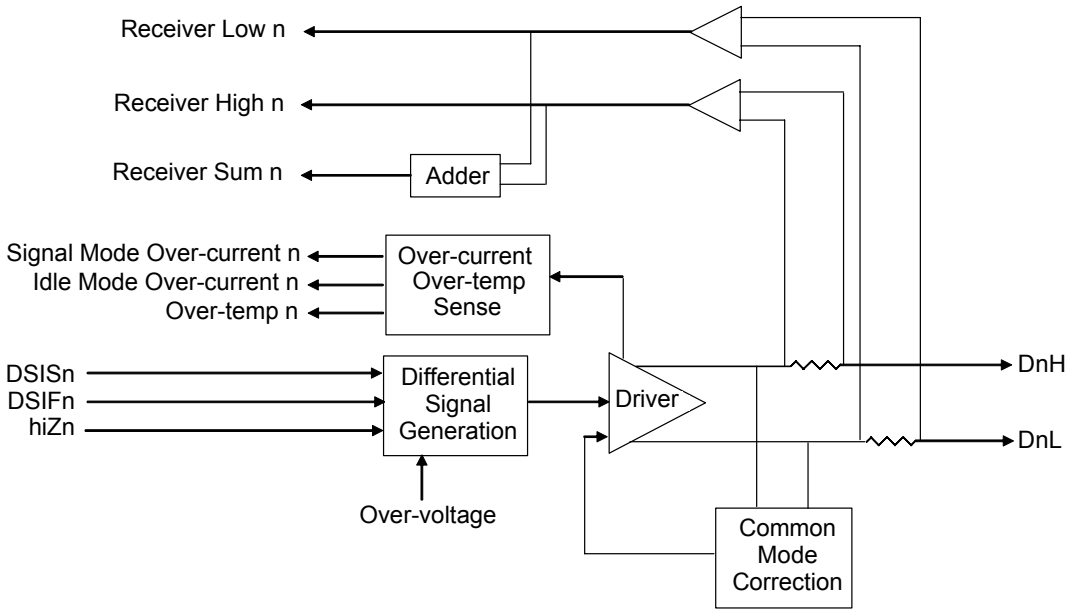


Figure 11. Driver/Receiver Block Diagram

DBUS DRIVER/RECEIVER (PHYSICAL LAYER)

There are four independent differential bus driver/receiver blocks on the 33781. These blocks translate the transmit data to the voltage and current needed to drive the DBUS. They also detect the response current from the slave devices and translate that current into digital levels. These circuits can drive their outputs to the levels listed in Table 5.

The DBUS driver/receiver block diagram is shown in Figure 11. The circuit uses a common driver for both the Idle and Signal modes to minimize common mode noise. The drivers are disabled in HiZ.

During Idle mode the driver is required to supply a high current to recharge the Slave device storage capacitors. In both Idle and Signal modes it is required to drive the DBUS load capacitances and control the slew rate over a wide supply voltage range and load conditions. Current limit, over-current shutdown and thermal shutdown are included to protect the device from fault conditions. More information can be found in the Protection and Diagnostic Features and SPI0 Register and Bit Descriptions sections.

To ensure stability of the bus drivers, capacitors must be connected between each output and ground. These are the DBUS common mode capacitors. In addition, a bypass capacitor is required at V_{SUPn}. These capacitors must be located close to the IC Pins and provide a low-impedance path to ground.

The internal signal DSIF controls the Idle to Signalling state change, and internal signal DSIS controls the signal level, high or low. DSIR is the slave device response signal to the logic. This is shown in Table 6.

Table 6. Internal Signal Truth Table

DSIF	DSIS	T_S	DSIR	DnD
0	0	0	Return Data	Signal Low
0	1	0	Return Data	Signal High
1	0	0	0	High-impedance
1	1	0	0	Idle
X	X	1	0	High-impedance

Bus wire faults on a bus do not disrupt communications on another bus. In addition, each bus channel has independent thermal shutdown protection. Once the channel thermal limit is reached the bus drivers become high-impedance, the TS bit is set to a 1 and the EN bit set to 0 in the channel DEN register. In addition the channel address buffer registers and pointers are reset. There is a 4 usec filter on Tlim to prevent false triggering.

The *Differential Signal Generation* block converts the DSIS signal to the DBUS differential signal voltage levels. This differential signal is buffered and slew rate controlled by

the driver. The over-voltage input causes the driver characteristics to be modified under over-voltage conditions. This is described in more detail in the Load Dump Operation section.

A special requirement of the differential bus is to maintain a low common mode voltage. This is accomplished by monitoring the common mode voltage and modifying the driver slew rates. This is the function of the *Common Mode Correction* block.

Current signals sent by the slave are detected on both the high side and the low side of the bus using a differential current sense architecture. Sense resistors between the Signal driver and the DnH and DnL outputs detect the slave device response current. Sensing the current on both bus lines improves the fault diagnostics of the bus. Also included is an adder circuit which is used to improve the reception of sensor data in the presence of common mode noise. The comparators in the blocks output a high or low value depending on if the input is above or below the signal threshold.

The Receiver High, Receiver Low, and Receiver Sum outputs are sent to the device logic block which is shown in Figure 23. The data is sampled at the falling edge of DSIS. In the presence of faults or common mode noise it is possible that all three receiver circuits will not produce the same bit pattern. To check for this, each of the three receiver filter outputs is passed to a CRC generation and checking block. A logic block determines which (if any) of the receiver filter blocks has produced the correct result, by comparing the CRC results along with the bit-by-bit XOR of the high side and low side bit pattern. Table 7 shows how the logic determines which (if any) receiver outputs contain a valid response. The data is selected from either the Receiver High, Receiver Low or Receiver Sum circuit and the ER bit is set accordingly in the DnRnSTAT register.

If either Receiver High or Receiver Low has all 1's for data, including the CRC bits, then the ER bit will be set. For either of these two conditions, the ER bit will be set regardless of the Receiver Sum data value and regardless of whether or not all the 1's caused a CRC error on the High or Low side.

Note that SPI0 and SPI1 do not use the same sources for their respective output data streams. SPI0 chooses between Receiver High or Receiver Sum0; SPI1 chooses between Receiver Low and Receiver Sum1.

In order to provide the maximum protection against a single-point failure causing a disruption in communication, the decision paths for the two SPI channels are internally independent . For example, Receiver Sum0 and Receiver Sum1 use different holding registers in the Receiver logic. These registers are duplicates, although they will always hold the same data unless there is a fault in one of the data paths.

Table 7. Receiver Decision Logic

Bus Pin Conditions	Receiver High 6 ± 1 mA	Receiver Low 6 ± 1 mA	Receiver Sum 12 ± 6mA	High and Low XOR (bit/bit)	High and Sum XOR (bit/bit)	Low and Sum XOR (bit/bit)	ER Bit	SPI0 DnRnxData	SPI1 DnRnxData
Normal	CRC Ok	CRC Ok	CRC Ok	H*L Ok	N/A	N/A	0	Receiver High	Receiver Low
				H*L Not OK			1	Receiver High	Receiver Low
Out of Spec	CRC Ok	CRC Ok	Bad CRC	H*L Ok	N/A	N/A	0	Receiver High	Receiver Low
				H*L Not OK			1	Receiver High	Receiver Low
Fault	CRC Ok	Bad CRC	CRC Ok	N/A	H*S Ok	N/A	0	Receiver High	Receiver Sum1
					H*S Not OK		1	Receiver High	Receiver Low
Fault L	CRC Ok	Bad CRC	Bad CRC	N/A	N/A	N/A	1	Receiver High	Receiver Low
Fault	Bad CRC	CRC OK	CRC OK	N/A	N/A	L*S Ok	0	Receiver Sum0	Receiver Low
						L*S Not OK	1	Receiver High	Receiver Low
Fault H	Bad CRC	CRC Ok	Bad CRC	N/A	N/A	N/A	1	Receiver High	Receiver Low
Common Mode Noise	Bad CRC	Bad CRC	CRC Ok	N/A	N/A	N/A	0	Receiver Sum0	Receiver Sum1
Fault	Bad CRC	Bad CRC	Bad CRC	N/A	N/A	N/A	1	Receiver High	Receiver Low

PSEUDO BUS SWITCHES

Pseudo Bus Switches are provided on the Channel 0 bus. They allow one channel to communicate via two external bus wire sets (D0H/D0L and DPH/DPL). There is a pseudo bus switch on both the bus high and bus low driver. Upon device reset the bus switches are open. This allows the master to initialize devices on D0H/D0L. After all of these slaves are initialized, the pseudo bus switches can be closed, allowing the devices on DPH/DPL to be initialized.

The Pseudo Bus Switches can only be commanded closed by the BSWH and BSWL bits in the D0EN register. These bits can also open the switch at any time.

The Pseudo Bus Switches have independent thermal shutdown protection. Once the thermal shutdown point is reached, the bus switch is opened (becoming high-impedance) and the BSWH and/or BSWL bit is cleared in the channel 0 DEN register. If this occurs, the Pseudo Bus Switches can only be closed again by setting the BSWH and/or BSWL bit to a 1 with a write command to the channel 0 DEN register.

SPREAD SPECTRUM

The dominant source of radiated electromagnetic interference (EMI) from the DBUS bus is due to the regular periodic frequency of the data bits. At a steady bit rate, the time period for each bit is the same, which results in a steady fundamental frequency plus harmonics. This results in undesired signals appearing at multiples of the frequency that can be strong enough to interfere with a desired signal.

A significant decrease in radiated EMI can be achieved by randomly changing the duration of each bit. This can significantly reduce the amplitude by having the signal spend a much smaller percentage of time at any specific frequency. The signal strength of the fundamental and harmonics are reduced directly by the percentage of time it spends on a specific frequency.

A circuit to do this is included in this IC, and can perform the *spreading* of the signal independently for each channel, while generating the bit clock timing for the channel. This is done in the Spread Spectrum (SS) Block Diagram shown in Figure 12.

To implement the channel bit clock a common 64MHz clock is created from the on board 4MHz oscillator using a digital PLL. Multiples of this clock period (15.625 nsec) are used to select the minimum channel bit time. The Spread

Spectrum block does this by multiplying the 8-bit value in the DxFSEL register by 2 and then adding it to the number 320 (decimal). The user must choose a minimum bit time appropriate for his system. Factors which must be considered are the slave response time, bus wire delays, and the minimum idle time needed to recharge the slave H_CAPs for the channel.

To spread the spectrum beyond this minimum bit time a random delay based on a multiple of 1/64 MHz periods can be added to each bit. This delay is created by a Pseudo Random Bit Sequence Generator from which a 7-bit random number is created. This number is further qualified by the maximum number of counts (chosen by the DEV[2:0] bits in the DxSSCTL registers) allowed beyond the base time period. The resulting value is added to the minimum bit time and fed to the bit clock logic, which generates the DSI bit clock.

It is important for the user to select a maximum deviation value that is appropriate for the system. A larger maximum deviation results in spreading the bit energy to more frequencies. However, this number also establishes the maximum period for any random bit on that channel. If the system requires that a minimum number of bits be transferred within a fixed time period, then the user must select a minimum base bit time and maximum deviation time that will meet the criteria.

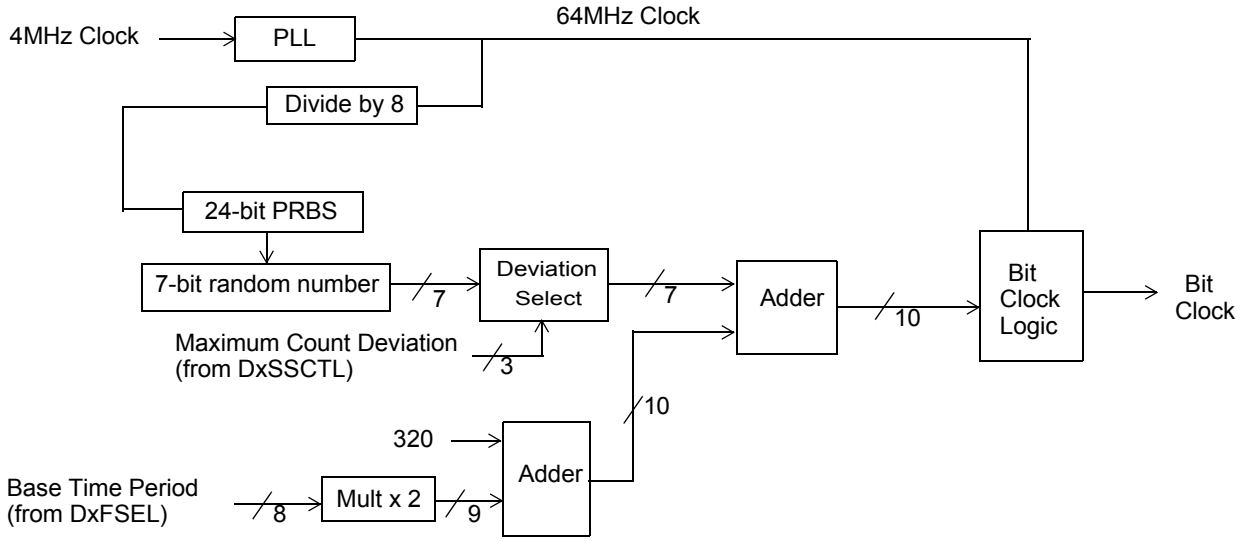


Figure 12. Spread Spectrum Block Diagram

FUNCTIONAL DEVICE OPERATION

LOGIC COMMANDS AND REGISTERS

SPI0 COMMUNICATIONS

All SPI0 transactions are either 16 or 32-bits long. They start with a command byte and can be followed by 1 or 3 bytes of data. The start of an SPI transaction is signaled by CS0 being asserted low. The first bit sent (bit 7) of the first byte signals a read or write (write = 1) of data. The last seven bits (bits 6–0) of the command set a pointer to the desired register. The 33781 uses 16-bit commands to access control registers, and 32-bit commands to access both control registers, and to queue up transfers over the DBUS. Figure 13 is a diagram of 16-bit transfers and Figure 14 is a diagram of 32-bit transfers. In these multi-byte transfers, as long as CS0 is asserted low, each additional byte sent over the SPI will be a read/write of data to the sequential next register.

33781 utilizes, transmit, and receive addressable FIFOs for sending commands and responses over the DBUS. There are separate command and response registers, and a transmit queue is used to allow up to 4 bus commands to be scheduled for each bus. The transmit queue schedules commands as a circular buffer, accessing the appropriate command register for the command and data to be sent as the bus becomes available. Data received in response to the commands is queued up for sequential response back to the MCU during the next set of SPI commands. If an SPI0 attempts to write to a transmit register that is not empty the new command will be ignored.

Figure 14 shows an example of a write operation. During the first byte of the SPI transaction, the first MOSI bit is 1 (write), and the last seven are the address of the register to be accessed. During this command byte, MISO returns dummy bits set to all zeros. During the next SPI transactions, MOSI updates the data in the register pointed to in the previous byte with new data, while reading back the old data via MISO.

During an SPI0 transaction the 33781 checks for SPI framing errors. A framing error is defined as any number of clocks received that is not either 16 or 32. If that occurs, all bits sent by the SPI master are discarded and no registers are update.

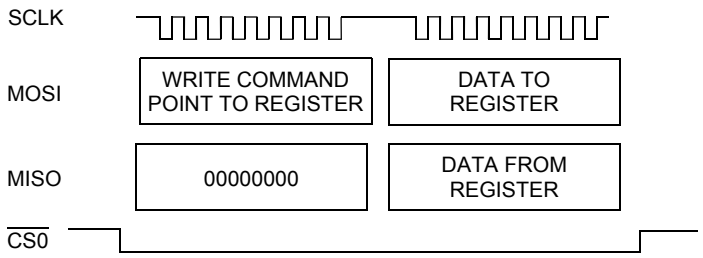


Figure 13. SPI016-Bit Burst Transfer Example.

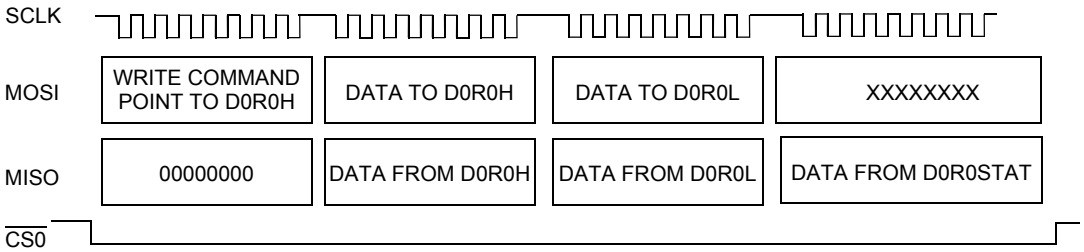


Figure 14. SPI0 32-Bit Burst Transfer Example

The bit definitions for SPI0 depend on the type of SPI transfer, and if the transfer will be to/from the addressable FIFOs, whether the DBUS for that channel is set for Long Words or Enhanced Short words.

Figure 13 shows the bit encoding for 16-bit SPI0 burst transfers. In this transfer the first byte contains the address of the control register to be written to or read from, and the second byte is the data to be written. The SPI0 response is the data from that register, latched at the falling edge of CS0. If the address pointed to by the first byte is not a control

register, the transfer is considered to have a framing error and no write will occur.

Figure 16 shows the bit encoding for 32-bit SPI0 burst transfers when the DBUS channel is set for long words. In this transfer, the first byte contains the address of the control register to be written to and read from, the second byte is the data to/from that register, and the next two bytes are the data to/from the next numerically successive registers. In the case of reading or writing from the addressable FIFO registers, the 1st data byte would be the DnRnH byte, the next byte would be the DnRnL byte, and the third byte would be the DnRnSTAT byte as shown in Figure 15. Notice that in this case, the 4th Tx byte is don't care and is not written. If this transfer would be sent to an address in the control register section of the register bank, the bytes sent and returned would be first the addressed register, and then the next consecutive registers.

Figure 17 shows the bit encoding for 32-bit SPI0 burst transfers when the DBUS channel is set for enhanced short words. This transfer mode is only valid when accessing the addressable FIFO portion of the register set. In this case, the first byte is again the 1st address of the register to be accessed in this read/write, the second byte contains the upper two bits of the data to be written, and the third byte is the lower 8-bits of data to be written. The SPI0 response encoding begins with the 2nd byte in the transfer with the 4-bit DBUS address of the slave, which sent the data contained in the rest of the word. This is followed by the 10-bits of data from the DBUS slave, and then the value in the DnRnSTAT register.

Although it looks like the read and write for an address are occurring at the same time, the changes caused earlier during the same burst would not be reflected by the data returned, because the DnRnSTAT register is latched at $\overline{CS0}$ going low.

Refer to the section SPI0 Register and Bit Descriptions on page 29 for the bit descriptions in Figure 15, Figure 16, and Figure 17.

	Bit 7	Bit6	BIt5	Bit4	Bit3	Bit2	Bit1	Bit0
First TX Byte	R/W	ADDR6	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0
Second TX Byte	D7	D6	D5	D4	D3	D2	D1	D0
	Bit 7	Bit6	BIt5	Bit4	Bit3	Bit2	Bit1	Bit0
First RX Byte	0	0	0	0	0	0	0	0
Second RX Byte	D7	D6	D5	D4	D3	D2	D1	D0

Figure 15. SPI0 Communications, 16-Bit Burst Transfer Bit Definitions

	Bit 7	Bit6	BIt5	Bit4	Bit3	Bit2	Bit1	Bit0
First TX Byte	R/W	ADDR6	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0
Second TX Byte	D15	D14	D13	D12	D11	D10	D9	D8
Third TX Byte	D7	D6	D5	D4	D3	D2	D1	D0
Fourth TX Byte	X	X	X	X	X	X	X	X
	Bit 7	Bit6	BIt5	Bit4	Bit3	Bit2	Bit1	Bit0
First RX Byte	0	0	0	0	0	0	0	0
Second RX Byte	D15	D14	D13	D12	D11	D10	D9	D8
Third RX Byte	D7	D6	D5	D4	D3	D2	D1	D0
Fourth RX Byte	ER	TE	SDS	RNE	ICL	0	FIX1	FIX0

Figure 16. SPI0 Communications, 32-Bit Burst Transfer Long Word DBUS Transfer Bit Definitions

	Bit 7	Bit6	BIt5	Bit4	Bit3	Bit2	Bit1	Bit0
First TX Byte	R/W	ADDR6	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0
Second TX Byte	X	X	X	X	X	X	D9	D8
Third TX Byte	D7	D6	D5	D4	D3	D2	D1	D0
Fourth TX Byte	X	X	X	X	X	X	X	X
	Bit 7	Bit6	BIt5	Bit4	Bit3	Bit2	Bit1	Bit0
First RX Byte	0	0	0	0	0	0	0	0
Second RX Byte	SA3	SA2	SA1	SA0	0	0	D9	D8
Third RX Byte	D7	D6	D5	D4	D3	D2	D1	D0
Fourth RX Byte	ER	TE	SDS	RNE	ICL	0	FIX0	FIX1

Figure 17. SPI0 Communications, 32-Bit Burst Transfer Enhanced Short Word DBUS Bit Definitions

SPI1 COMMUNICATIONS

All SPI1 transactions are read only, are 16-bits in length, and are asynchronous to SPI0. There is no MOSI pin or function associated with SPI1, since there are no commands sent. Figure 18 shows the signals associated with an SPI1 transfer, and Figure 19 contains the order of bits sent for each SPI1 transaction.

SPI1 transfers start with the 1st SCLK1 transition after CS1 asserts and ends once CS1 negates. The start of an SPI transaction is signaled by CS1 being asserted low. If the SPI1 logic sees more than 16 SCLK1 pulses while CS1 is asserted, zeros are returned for all additional bits (bits beyond bit 15). If a SPI1 transaction contains less than 16-bits (too few SCLK cycles), the data that was in process of being sent during the transaction is discarded and not saved for retry.

There are eight registers which can be read by SPI1 in a cyclic fashion. Four of these registers are associated with bus channel 2, and four are associated with bus channel 3. Data is deposited into these registers under the following conditions:

When the bus channel 2 is set for enhanced 10-bit short words, the SPI1 state machine monitors outgoing bus addresses and commands on the channel. If the command sent is $2 (Request AN0), the address portion of the command is saved. The response received on the next command is stored into one of the four 16-bit register pointed to by the channel 2 cyclic buffer write pointer, along with the address that generated that response (saved from the previous transaction) with the bits “01”, completing the 16 bit write. These last two bits indicate that the transaction occurred on channel 2. The data bits will only be written if the status bits for that bus transaction all indicate no errors. If a status error is indicated, the address and channel indicator bits are stored as described, but the data bits are all set to zeros. If there was a bus driver shutdown during the transaction, no buffer write will occur. Further transactions are written to the next cyclic buffer register in the same way, overwriting data if necessary.

This same sequence occurs for channel three transactions, except that the channel indicator bits are “10”, and writes occur to a separate set of four 16-bit cyclic registers.

If the channel has been put into loop mode, the same sequence is used except the buffer write occurs only if the data is all ones or all zeros, and the saved address from the previous transaction is the complement of the data. The channel indicator bits are written the same as if the channel were in normal mode. The buffer pointer always advances, even if the buffer is not written, so that it is synchronous with the SPI0 RX buffer pointer.

The channel buffers are not cleared, in the case of a channel abort.

Reads from this register by the SPI1 master are also accomplished in a cyclic buffer way, except the two channels are concatenated, with channel 3 following channel 2 in the cyclic sequence. During these buffer reads, if a buffer position does not contain data, it is skipped. After each buffer location is read it is cleared by the SPI1 logic.

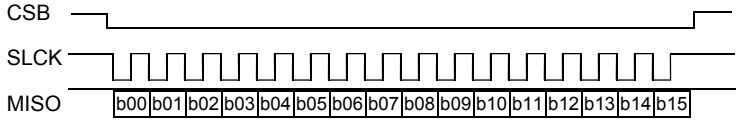


Figure 18. SPI1 16-Bit Burst Transfer Example

.

SPI Data Bit	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15
Read Only	DO0	DO1	DO2	DO3	DO4	DO5	DO6	DO7	DO8	DO9	A0	A1	A2	A3	C0	C1

Figure 19. SPI1 Bit Encoding

DO[0:9]- Data Bits

The received data bits from the bus channel transaction. If the transaction had any CRC or SDS errors (See page 32 and page 33), then these bits are set to all zeros.

A[0:3] - Sensor Address Bits

The address of the slave that sent the data. This is a copy of the address sent out during the previous bus transaction.

C[0:1] - Channel indicator Bits

The bits indicate which bus channel the data came from. “01” indicates channel 2, and “10” indicates channel 3.

DBUS COMMUNICATIONS

The DBUS messages contain data from the DnH and DnL registers. A CRC pattern is automatically appended to each message. The data and CRC lengths are programmed by the DnLENGTH register. Figure 20 shows the structure of the DBUS message.

Bit n	.....	Bit 0	CRC n	.....	CRC 0

Figure 20. DBUS Communications Message

DBUS Driver/Receiver communications involve a frame (DSIF), a data signal (DSIS), and a data return (DSIR) signal. These are signals internal to the IC associated with the protocol engine.

A message starts with a falling edge on the DSIF signal, which marks the start of a frame. There is a one bit-time delay before the MSB of data appears on DSIS. Data bits start with a falling edge on DSIS. The low time is 1/3 of the bit time for a 1, and 2/3 of a bit time for a 0. Data is transmitted on DSIS and received on DSIR simultaneously. Receive data is the captured level on DSIR at the end of each bit time. As a message is received, it is stored bit-by-bit into the appropriate receive register. For each data value received, there is a one-bit status flag (ER) to indicate whether or not there was a CRC error while receiving the data. At the end of the bit time for the last CRC bit, DSIF returns to a logic high (Idle level). A minimum delay is imposed between successive frames as determined by the DnCTRL register.

Users initiate a message by writing (via the SPI0 interface from the MCU) to the high and low byte of the data registers (DnRnH/L). Transactions are scheduled once the CS0 for that transfer rises. When 9- to 16-bit messages are to be sent, the user writes to the DnH register first, and then the DnL register, before the combined 9 to 16-bit data value DnH:DnL is sent on the DBUS. The user should first check the TE status flag to be sure the command register is not full before writing a new data value to DnH and/or DnL. When the minimum inter-frame delay has been satisfied, and $\overline{CS0}$ has risen, and if no SPI0 framing error has occurred, DSIF will go low, indicating the start of a new transfer frame.

At the end of a DBUS transfer (and after the CRC error status is stable), the RNE flag is set to indicate there is data in the register available to be read.

DATA RATE

The base data rate is determined by the system clock (CLK) and the values in the DnFSEL register. The CLK is assumed to be 4MHz. The CLK is converted to a 64MHz internal clock with a digital PLL, which is used to form the bit rate clock. The minimum bit clock period which may be programmed is:

$(1/16*f_{CLK})$ x 320 = 5 usec

However, this period may not meet overall system requirements for minimum bit time. Longer base clock periods can be selected by using the DxFSEL register. There are 8 bits in the DxFSEL register representing values from 0 to 255. The complete equation for determining the base clock period is:

$((1/16*f_{CLK})$ x (320 +2x)) where x = 0 to 255

Table 8 gives some examples of the base data rate for f_{CLK} = 4.0MHz.

Table 8. Examples of Base Data Rate

FSEL	Base Bit Period (usec)	Base Bit Frequency (kbps)
00000000	5.000	200.0
00000001	5.031	198.8
00001101	5.406	184.9
00101000	6.250	160.0
11111110	12.938	77.3
11111111	12.969	77.1

CRC GENERATION / CHECKING

Whenever a message is sent on the DBUS, a 0- to 8-bit CRC value is computed and serially sent as the next n bits after the LSB of the data. The CRC length, polynomial, and initial seed are determined by the CRCLEN[3:0], CRCPOLY[7:0], and CRCSEED[7:0] control register fields. The message, including the CRC bits, is passed along to a remote peripheral, which computes a separate CRC value as the message data is received. If this computed and CRC does not agree with the CRC value received in the message, the peripheral device considers the message invalid.

Messages received include a 0- to 8-bit CRC value, which was computed in the peripheral device that is responding. As the message is received, a separate 0- to 8-bit CRC value is computed and is compared with the CRC value in the received message. If these values do not agree, the message is considered invalid and the ER status bit in the associate DnRnSTAT register is set at the end of the message along with the RNE bit.

When no remote peripheral responds to a message, the data pattern received will be all zeros with a CRC value of 0, which may be detected as a CRC error depending on the values of CRCLEN[3:0], CRCPOLY[7:0], and CRCSEED[7:0].

CRC COMPUTATION

The CRC algorithm uses a programmable initialization value, or seed of CRCSEED[7:0], and a programmable polynomial of CRCPOLY[7:0]. Figure 21 is a VHDL description of the CRC algorithm for the DBUS standard 4-bit CRC, with its initial value of 1010. A seed value is chosen so that a zero data value will generate a CRC value of 1010. A block diagram of the default CRC calculation is shown in Figure 22.

```
--------------------------------------------------------------------------
-- Calculates the 4-bit CRC (x^4 + 1) serially for 8 to 16 bits of data.
--------------------------------------------------------------------------
   constant CRCPoly: std_logic_vector: = "0001"; -- x^4 +1
   constant InitCrc: std_logic_vector: = "1010";
   procedure SerialCalculateCRC4(CRC: input std_logic_vector;Data: in std_logic) is vari-
able Xor1: std_logic;
   begin
        Xor1: = CRC(3) xor Data;
        CRC: = CRC(2 downto 0) & '0'; -- Shift left 1 bit
        if Xor1 = '1' then
            CRC: = CRC xor CRCPoly
        end if;
end SerialCalculateCRC4;
```

Figure 21. CRC Algorithm

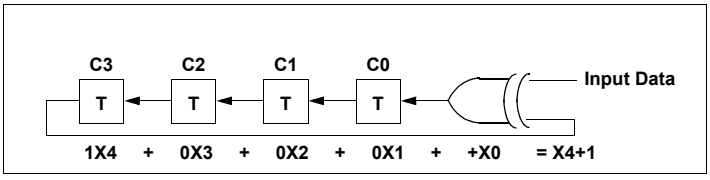


Figure 22. Default CRC Block Diagram

MESSAGE SIZE SPECIAL CASES

The response to any 8- to 15-bit message is expected to be another 8- to 15-bit message, and the response to any 16-bit message is expected to be another 16-bit message. This gives rise to some special cases when there is a transition from one message size to a different message size. Some messages must be long words (16 bits of data), and others can be short words (8 to 15 bits of data).

The following are examples where the word is a standard DSI formatted short word (8 bits of data and 4 bits of CRC).

Example 1: If the previous message was a short word and the current message is a long word, the response message (which is also a short word) finishes before the current message frame, and the CRC bits look like data bits in the long word format. Since the CRC validation of this short word message response is not reliable, this short word response should not be used.

Example 2: If the previous message was a long word and the current message is a short word, the response message (which is also a long word) cannot finish before the current message frame. Bits three to zero of the data and the CRC bits are lost. Data bits seven to four of the 16-bit response

message look like the CRC bits of an 8-bit response and almost certainly would not be correct. Because the response is incomplete and the CRC check is probably not valid, this response is not useful.

The long word to short word message size transition normally only occurs after setting up the DBUS peripherals. During address setup, a message with address 0000 is sent to attempt to set the address of the next peripheral on the daisy-chained bus. Before any peripherals have been assigned an address, their bus switches are opened so the addressing message only goes to the first peripheral in line. As each peripheral gets an address, it closes its bus switch so the next address assignment command can reach the next peripheral in line on the bus. Each peripheral responds to an address assignment only once (during the next message after the command that set its address). After the last peripheral has been assigned an address, any subsequent address assignments will receive no response. When the master MCU fails to receive a response, it knows it has passed the last peripheral. At this point, short word messages may be sent. The first such message will have no meaningful response associated with it.

The first message after reset is also a special case, because there was no previous message, therefore there will be no meaningful response during the first message transfer.

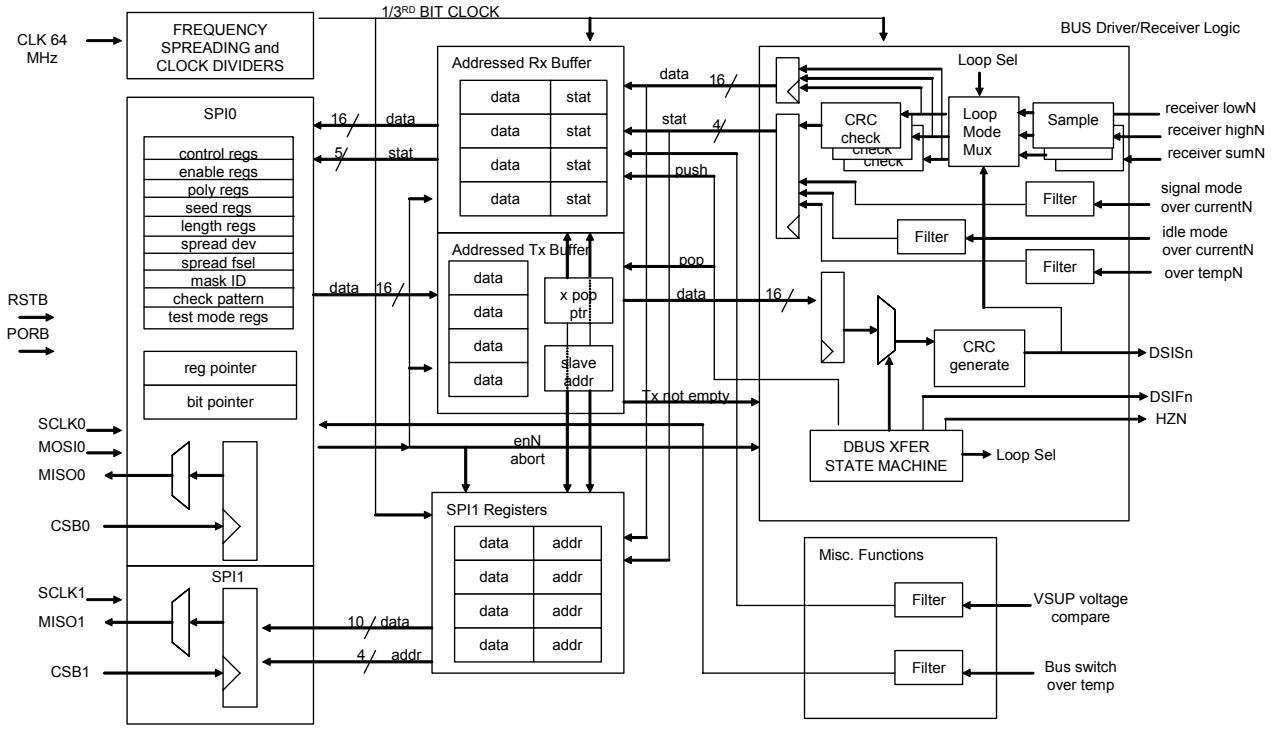


Figure 23. Logic Block Diagram

LOGIC BLOCK DIAGRAM DESCRIPTION

Figure 23, Logic Block Diagram, shows a block diagram of the major logic blocks in the IC.

SPI0

The SPI0 is a standard slave serial peripheral interface. This interface provides two-way communications between the IC and an MCU. The MCU can write to registers that control the operation of the IC, and read back the conditions in the IC using the SPI. It can also write data to be sent out on the DBUS, and read data that was returned on the DBUS. The register pointer and bit pointer are used to control which registers and bits are being written to, and read from using the SPI. Its operation is described in detail in the section entitled SPI0 COMMUNICATIONS on page 22.

The register set consists of transmit, receive, control, and status registers. They are written and read using the SPI0 interface, and are affected by events in the IC. Detailed descriptions of their operation and use can be found in section SPI0 Register and Bit Descriptions.

SPI1

The SPI1 is a slave serial peripheral interface. It operates asynchronously to the SPI0. It uses 16-bit transfers and is read only. The MOSI function is not implemented. SPI1 only reads the SPI1 8 16-bit circular buffer registers.

SPI1 REGISTERS

An eight position circular buffer made up of 16-bit words.

Reads of these registers occur in a round robin (sequential order with wrap around at the end) fashion. If a buffer does not contain any data it is skipped during the round robin sequence. More information on this buffer can be found in the section SPI1 Communications.

RST

Asserting this pin low will cause the part to reset, forcing registers to a known state and resetting the SPI0 and SPI1 buffer pointers. All bus activity will be halted and not allowed to restart, and no SPI activity will be recognized until the $\overline{\text{RST}}$ goes to a logic high level.

ADDRESSED TX BUFFER

The Addressed TX Buffer is a cyclic register set that allows up to four transmit data packets to be stored for future transmission on the DBUS. This is done to prevent the overwrite of transmit data if the transmission of the previous data has not been completed. Each buffer is a 2-byte set that contains the high byte and low byte of a DBUS command.

The transmit buffer queue looks for the lowest register number in the channel with data to be sent, and sends it over the DBUS. It then checks the next sequential buffer - if there is data to be sent it will send it. If not, that buffer will be skipped and the next buffer sent if it contains data. If no other buffers have data ready to be sent, the queue moves back to the top of the buffer and continues checking until data is available.

ADDRESSED RX BUFFER

The Addressed RX Buffer is a cyclic register set that allows up to four responses to be stored without being transferred to the MCU via the SPI. This is done so that data will not be lost, even if the MCU takes time to read the response data. Each buffer is a 3-byte set that contains the data high byte, data low byte, and status word of a DBUS response.

The received data from DBUS transactions is stored in the same receive buffer number as the transmit buffer for that transaction.

BUS DRIVER/RECEIVER LOGIC

This block controls the physical layer drivers and receive data from the physical layer receivers. The physical layer converts the 0V to 5.0V low power logic signals to the higher voltage and drive levels required for the bus. It also converts the low current (0mA to 11mA typical) loading of the response signal from the slave to logic voltage levels, to allow the response from the slaves to be received.

Each channel contains a CRC generator, that adds a series of bits to each of the transmitted data words sent out on the DBUS. The CRC bits are created from the data pattern and are used by the slave devices to determine if one or more of the data bits sent was in error. The detailed operation and control of this function is covered in the section entitled CRC GENERATION / CHECKING on page 26.

This block also checks the CRC bits that have been added to the end of the response by the slave device. For a given pattern of received data, a new CRC is generated and compared to the CRC bits received. This is performed on the received data from the bus high side, bus low side and bus sum circuits in the bus receiver. The results of these checks, determine if the data are valid, and whether or not the error bit is set as shown in **Table 9**. This bit is read back using the SPI during the same SPI transaction that reads the response, in order to keep them associated with each other. The CRC bits are removed by the IC and not seen by the MCU, when reading the data registers. Operation of the CRC Check is covered in the section entitled CRC GENERATION / CHECKING on page 26.

SPI0 REGISTER AND BIT DESCRIPTIONS

The 33781 has 87 registers associated with the SPI0 interface, shown in Table 8. Each bus channel has its own set of control registers, along with separate command and data registers, for queuing up to four commands. There are also registers containing check pattern data.

Table 9. Register List

Register Address	Register Name	Register Definition	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0000000	D0R0H	DBUS 0 Reg 0 Upper Byte	D15	D14	D13	D12	D11	D10	D9	D8
0000001	D0R0L	DBUS 0 Reg 0 Lower Byte	D7	D6	D5	D4	D3	D2	D1	D0
0000010	D0R0STAT	DBUS 0 Reg 0 Status	ER	TE	SDS	RNE	ICL	0	FIX0	FIX1
0000011	D0R1H	DBUS 0 Reg 1 Upper Byte	D15	D14	D13	D12	D11	D10	D9	D8
0000100	D0R1L	DBUS 0 Reg 1 Lower Byte	D7	D6	D5	D4	D3	D2	D1	D0
0000101	D0R1STAT	DBUS 0 Reg 1 Status	ER	TE	SDS	RNE	ICL	0	FIX0	FIX1
0000110	D0R2H	DBUS 0 Reg 2 Upper Byte	D15	D14	D13	D12	D11	D10	D9	D8
0000111	D0R2L	DBUS 0 Reg 2 Lower Byte	D7	D6	D5	D4	D3	D2	D1	D0
0001000	D0R2STAT	DBUS 0 Reg 2 Status	ER	TE	SDS	RNE	ICL	0	FIX0	FIX1
0001001	D0R3H	DBUS 0 Reg 3 Upper Byte	D15	D14	D13	D12	D11	D10	D9	D8
0001010	D0R3L	DBUS 0 Reg 3 Lower Byte	D7	D6	D5	D4	D3	D2	D1	D0
0001011	D0R3STAT	DBUS 0 Reg 3 Status	ER	TE	SDS	RNE	ICL	0	FIX0	FIX1
0001100	D0CTRL	DBUS 0 Control Register	-	-	DLYB	DLYA	-	LOOP1	LOOP0	MS
0001101	D0EN	DBUS 0 Enable Register	TS	ISDD	-	-	-	BSWH	BSWL	EN
0001110	D0POLY	DBUS 0 Polynomial	CRC POLY7	CRC POLY6	CRC POLY5	CRC POLY4	CRC POLY3	CRC POLY2	CRC POLY1	CRC POLY0
0001111	D0SEED	DBUS 0 CRC Seed	CRC SEED7	CRC SEED6	CRCSEED5	CRCSEED4	CRCSEED3	CRCSEED2	CRCSEED1	CRCSEED0
0010000	D0LENGTH	DBUS 0 Short Word and CRC Lengths	SW LEN3	SW LEN2	SW LEN1	SW LEN0	CRC LEN3	CRC LEN2	CRC LEN1	CRC LEN0
0010001	D0SSCTRL	DBUS 0 Spread Spectrum Control	-	-	-	-	-	DEV2	DEV1	DEV0
0010010	D0FSEL	DBUS 0 Frequency Select	FSEL7	FSEL6	FSEL5	FSEL4	FSEL3	FSEL2	FSEL1	FSEL0
0010011	RESERVED	Writes/reads of this address are ignored	-	-	-	-	-	-	-	-
0010100	RESERVED	Writes/reads of this address are ignored	-	-	-	-	-	-	-	-
0010101	D1R0H	DBUS 1 Reg 0 Upper Byte	D15	D14	D13	D12	D11	D10	D9	D8
0010110	D1R0L	DBUS 1 Reg 0 Lower Byte	D7	D6	D5	D4	D3	D2	D1	D0
0010111	D1R0STAT	DBUS 1 Reg 0 Status	ER	TE	SDS	RNE	ICL	0	FIX0	FIX1
0011000	D1R1H	DBUS 1 Reg 1 Upper Byte	D15	D14	D13	D12	D11	D10	D9	D8
0011001	D1R1L	DBUS 1 Reg 1 Lower Byte	D7	D6	D5	D4	D3	D2	D1	D0
0011010	D1R1STAT	DBUS 1 Reg 1 Status	ER	TE	SDS	RNE	ICL	0	FIX0	FIX1
0011011	D1R2H	DBUS 1 Reg 2 Upper Byte	D15	D14	D13	D12	D11	D10	D9	D8
0011100	D1R2L	DBUS 1 Reg 2 Lower Byte	D7	D6	D5	D4	D3	D2	D1	D0
0011101	D1R2STAT	DBUS 1 Reg 2 Status	ER	TE	SDS	RNE	ICL	0	FIX0	FIX1
0011110	D1R3H	DBUS 1 Reg 3 Upper Byte	D15	D14	D13	D12	D11	D10	D9	D8
0011111	D1R3L	DBUS 1 Reg 3 Lower Byte	D7	D6	D5	D4	D3	D2	D1	D0

Table 9. Register List (continued)

Register Address	Register Name	Register Definition	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0100000	D1R3STAT	DBUS 1 Reg 3 Status	ER	TE	SDS	RNE	ICL	0	FIX0	FIX1
0100001	D1CTRL	DBUS 1 Control Register	-	-	DLYB	DLYA	-	LOOP1	LOOP0	MS
0100010	D1EN	DBUS 1 Enable Register	TS	ISDD	-	-	-	-	-	EN
0100011	D1POLY	DBUS 1 Polynomial	CRC POLY7	CRC POLY6	CRC POLY5	CRC POLY4	CRC POLY3	CRC POLY2	CRC POLY1	CRC POLY0
0100100	D1SEED	DBUS 1 CRC Seed	CRC SEED7	CRC SEED6	CRCSEED5	CRCSEED4	CRCSEED3	CRCSEED2	CRCSEED1	CRCSEED0
0100101	D1LENGTH	DBUS 1 Short Word and CRC Lengths	SW LEN3	SW LEN2	SW LEN1	SW LEN0	CRC LEN3	CRC LEN2	CRC LEN1	CRC LEN0
0100110	D1SSCTRL	DBUS 1 Spread Spectrum Control	-	-	-	-	-	DEV2	DEV1	DEV0
0100111	D1FSEL	DBUS 1 Frequency Select	FSEL7	FSEL6	FSEL5	FSEL4	FSEL3	FSEL2	FSEL1	FSEL0
0101000	RESERVED	Writes/reads of this address are ignored	-	-	-	-	-	-	-	-
0101001	RESERVED	Writes/reads of this address are ignored	-	-	-	-	-	-	-	-
0101010	D2R0H	DBUS 2 Reg 0 Upper Byte	D15	D14	D13	D12	D11	D10	D9	D8
0101011	D2R0L	DBUS 2 Reg 0 Lower Byte	D7	D6	D5	D4	D3	D2	D1	D0
0101100	D2R0STAT	DBUS 2 Reg 0 Status	ER	TE	SDS	RNE	ICL	0	FIX0	FIX1
0101101	D2R1H	DBUS 2 Reg 1 Upper Byte	D15	D14	D13	D12	D11	D10	D9	D8
0101110	D2R1L	DBUS 2 Reg 1 Lower Byte	D7	D6	D5	D4	D3	D2	D1	D0
0101111	D2R1STAT	DBUS 2 Reg 1 Status	ER	TE	SDS	RNE	ICL	0	FIX0	FIX1
0110000	D2R2H	DBUS 2 Reg 2 Upper Byte	D15	D14	D13	D12	D11	D10	D9	D8
0110001	D2R2L	DBUS 2 Reg 2 Lower Byte	D7	D6	D5	D4	D3	D2	D1	D0
0110010	D2R2STAT	DBUS 2 Reg 2 Status	ER	TE	SDS	RNE	ICL	0	FIX0	FIX1
0110011	D2R3H	DBUS 2 Reg 3 Upper Byte	D15	D14	D13	D12	D11	D10	D9	D8
0110100	D2R3L	DBUS 2 Reg 3 Lower Byte	D7	D6	D5	D4	D3	D2	D1	D0
0110101	D2R3STAT	DBUS 2 Reg 3 Status	ER	TE	SDS	RNE	ICL	0	FIX0	FIX1
0110110	D2CTRL	DBUS 2 Control Register	-	-	DLYB	DLYA	-	LOOP1	LOOP0	MS
0110111	D2EN	DBUS 2 Enable Register	TS	ISDD	-	-	-	-	-	EN
0111000	D2POLY	DBUS 2 Polynomial	CRC POLY7	CRC POLY6	CRC POLY5	CRC POLY4	CRC POLY3	CRC POLY2	CRC POLY1	CRC POLY0
0111001	D2SEED	DBUS 2 CRC Seed	CRC SEED7	CRC SEED6	CRCSEED5	CRCSEED4	CRCSEED3	CRCSEED2	CRCSEED1	CRCSEED0
0111010	D2LENGTH	DBUS 2 Short Word and CRC Lengths	SW LEN3	SW LEN2	SW LEN1	SW LEN0	CRC LEN3	CRC LEN2	CRC LEN1	CRC LEN0
0111011	D2SSCTRL	DBUS 2 Spread Spectrum Control	-	-	-	-	-	DEV2	DEV1	DEV0
0111100	D2FSEL	DBUS 2 Frequency Select	FSEL7	FSEL6	FSEL5	FSEL4	FSEL3	FSEL2	FSEL1	FSEL0
0111101	RESERVED	Writes/reads of this address are ignored	-	-	-	-	-	-	-	-
0111110	RESERVED	Writes/reads of this address are ignored	-	-	-	-	-	-	-	-

Table 9. Register List (continued)

Register Address	Register Name	Register Definition	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0111111	D3R0H	DBUS 3 Reg 0 Upper Byte	D15	D14	D13	D12	D11	D10	D9	D8
1000000	D3R0L	DBUS 3 Reg 0 Lower Byte	D7	D6	D5	D4	D3	D2	D1	D0
1000001	D3R0STAT	DBUS 3 Reg 0 Status	ER	TE	SDS	RNE	ICL	0	FIX0	FIX1
1000010	D3R1H	DBUS 3 Reg 1 Upper Byte	D15	D14	D13	D12	D11	D10	D9	D8
1000011	D3R1L	DBUS 3 Reg 1 Lower Byte	D7	D6	D5	D4	D3	D2	D1	D0
1000100	D3R1STAT	DBUS 3 Reg 1 Status	ER	TE	SDS	RNE	ICL	0	FIX0	FIX1
1000101	D3R2H	DBUS 3 Reg 2 Upper Byte	D15	D14	D13	D12	D11	D10	D9	D8
1000110	D3R2L	DBUS 3 Reg 2 Lower Byte	D7	D6	D5	D4	D3	D2	D1	D0
1000111	D3R2STAT	DBUS 3 Reg 2 Status	ER	TE	SDS	RNE	ICL	0	FIX0	FIX1
1001000	D3R3H	DBUS 3 Reg 3 Upper Byte	D15	D14	D13	D12	D11	D10	D9	D8
1001001	D3R3L	DBUS 3 Reg 3 Lower Byte	D7	D6	D5	D4	D3	D2	D1	D0
1001010	D3R3STAT	DBUS 3 Reg 3 Status	ER	TE	SDS	RNE	ICL	0	FIX0	FIX1
1001011	D3CTRL	DBUS 3 Control Register	-	-	DLYB	DLYA	-	LOOP1	LOOP0	MS
1001100	D3EN	DBUS 3 Enable Register	TS	ISDD	-	-	-	-	-	EN
1001101	D3POLY	DBUS 3 Polynomial	CRC POLY7	CRC POLY6	CRC POLY5	CRC POLY4	CRC POLY3	CRC POLY2	CRC POLY1	CRC POLY0
1001110	D3SEED	DBUS 3 CRC Seed	CRC SEED7	CRC SEED6	CRCSEED5	CRCSEED4	CRCSEED3	CRCSEED2	CRCSEED1	CRCSEED0
1001111	D3LENGTH	DBUS 3 Short Word and CRC Lengths	SW LEN3	SW LEN2	SW LEN1	SW LEN0	CRC LEN3	CRC LEN2	CRC LEN1	CRC LEN0
1010000	D3SSCTRL	DBUS 3 Spread Spectrum Control	-	-	-	-	-	DEV2	DEV1	DEV0
1010001	D3FSEL	DBUS 3 Frequency Select	FSEL7	FSEL6	FSEL5	FSEL4	FSEL3	FSEL2	FSEL1	FSEL0
1010010	MASKID	Mask Version ID Code	FPAR	ID6	ID5	ID4	ID3	ID2	ID1	ID0
1010011	CHKCD0	Check Pattern 0	CKPTN23	CKPTN22	CKPTN21	CKPTN20	CKPTN19	CKPTN18	CKPTN17	CKPTN16
1010100	CHKCD1	Check Pattern 1	CKPTN15	CKPTN14	CKPTN13	CKPTN12	CKPTN11	CKPTN10	CKPTN9	CKPTN8
1010101	CHKCD2	Check Pattern 2	CKPTN7	CKPTN6	CKPTN5	CKPTN4	CKPTN3	CKPTN2	CKPTN1	CKPTN0
1010110	NCKCD0	Negative Check Pattern 0	NCKPTN23	NCKPTN22	NCKPTN21	NCKPTN20	NCKPTN19	NCKPTN18	NCKPTN17	NCKPTN16
1010111	NCKCD1	Negative Check Pattern 1	NCKPTN15	NCKPTN14	NCKPTN13	NCKPTN12	NCKPTN11	NCKPTN10	NCKPTN9	NCKPTN8
1011000	NCKCD2	Negative Check Pattern 2	NCKPTN7	NCKPTN6	NCKPTN5	NCKPTN4	NCKPTN3	NCKPTN2	NCKPTN1	NCKPTN0
1011001	RESERVED	Writes/reads of this address are ignored	-	-	-	-	-	-	-	-
1011010	RESERVED	Writes/reads of this address are ignored	-	-	-	-	-	-	-	-

DnRnH REGISTERS

These are read/write registers. There are sixteen of these registers, four for each of the buses, as shown in Table 8. When written to, the data is the high byte of a 9- to16-bit command. When read, it is the high byte of a 9- to 16-bit return on the DBUS. Writing to this register and the low byte register without a framing error schedules a DBUS transaction.

The bit assignments are shown in Figure 24. Even if a short word of 8 bits is selected for this bus (MSn = 1), this register must be written in the SPI burst sequence. When the short word length is set at other than 8 bits, this register will contain the bits above eight, starting with the ninth bit in the least significant bit position of the register. Unused bit positions are *don't care* values.

SPI Data Bit	Bit 7	6	5	4	3	2	1	0
Read/Write	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset	0	0	0	0	0	0	0	0

Figure 24. DnRnH Data Register Bit Assignments

DnRnL REGISTERS

These are read/write registers. There are sixteen of these registers, four for each of the buses. When written to, the data is the low byte of a 16-bit command. When in read, it is the low byte of a 16-bit return on the DBUS. Writing to this register and the high byte register without a framing error, schedules a DBUS transaction. The bit assignments are shown in Figure 25

If this address is pointed to by the first SPI0 byte of a SPI burst transaction, that transaction is ignored.

SPI Data Bit	Bit 7	6	5	4	3	2	1	0
Read/Write	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 25. DnRnL Data Register Bit Assignments

DnRnSTAT REGISTER

There are *read-only* registers. These registers cover the status of their associated DnRnH and DnRnl registers. The values are latched when $\overline{CS0}$ is asserted low. Any changes of status detected by these bits will not update the register until $\overline{CS0}$ is de-asserted. This is done to ensure that partial updates will not occur. If this address is pointed to by the first SPI0 byte of a SPI burst transaction, that transaction is ignored.

The bit assignments are shown in Figure 26.

SPI Data Bit	Bit 7	6	5	4	3	2	1	0
Read	ER	TE	SDS	RNE	ICL	0	FIX0	FIX1
Reset	0	1	0	0	0	0	0	1

Figure 26. DnRnSTAT Register Bit Assignments

ER–CRC Error Bit

- 0 = CRC value for the data in the read buffer was correct.
- 1 = CRC value for the data in the read buffer was not correct (data not valid).

CRC errors are associated with each receive buffer, so that each buffer has a bit to indicate whether the data in that buffer was received correctly. Whenever a received data value is available in the DnRnH and DnRnL registers, the associated CRC error status is available at ERn in the associated DnRnSTAT register. The ER bit is set or cleared whenever data is written from the DBUS into the DnRnH/L receive registers. If Channel Thermal Shutdown or Idle and SIgnal Mode Disable occur, these bits will be reset along with the other channel register bits.

TE–Transmit Register Empty Bit

- 0 = Transmit buffer not empty.
- 1 = Transmit buffer empty.

This bit indicates that data has been written to the associated channel register high and/or low, but has not been read for sending on the DBUS. The bit is set to 0 on the rising

edge of $\overline{CS0}$ after a SPI0 write to the associated DnRnH/L registers. It is set to 1 once the DBUS state machine completes sending the DnRnH/L data in the buffer over the DBUS.

If SPI0 attempts to write to a transmit register that is not empty, the new command will be ignored.

SDS - Signal Mode Shutdown

- 0 = Bus driver is active.
- 1 = High side or low side bus driver had a current shutdown during signal mode in this DBUS transaction.

The bus driver current is independently sensed on both the high side and the low side of the driver during signaling mode. This bit is set if either driver exceeds the over-current detection threshold for greater than the delay time. In that event, the driver is disabled (becomes high-impedance) for the remainder of that DBUS transaction.

The MCU can use this bit along with other fault condition bits to detect that the data in this buffer may be invalid.

RNE–Receive Register Not Empty Bit

- 0 = No new data ready.
- 1 = Data is available to be read.

This bit is set when the DBUS writes to the associated DnRnH and DnRnL registers. The bit is cleared on the rising edge of $\overline{CS0}$ after a read of the DnRn STAT register. This bit is cleared even if a SPI0 framing error occurred during the SPI burst transfer that read the receive register.

This bit will not be set if the V_{SUP} voltage falls below the low voltage detect threshold for longer than the V_{SUP} low mask time during the associated bus transfer.

ICL - Idle Mode Double Current Limit Bit (Idle Mode Shutdown)

- 0 = Idle mode current limit not active.
- 1 = Idle mode current limit active.

During Idle mode, the current limit is independently sensed on both the high side and the low side of the bus driver. An over-current fault condition occurs if either DnH or DnL is within the sourcing or sinking limit (500mA). This is characterized by both DnH and DnL voltage levels being simultaneously at either ground or the bus voltage V_{BUS}.

The ICL bit is set and the drivers are disabled if either of the following conditions are true:

- the fault condition occurs continuously for 2.5µs
- the fault condition occurs four times with 50µs or less between occurrences

Figure 27 shows a representation of the over-current fault condition circuitry.

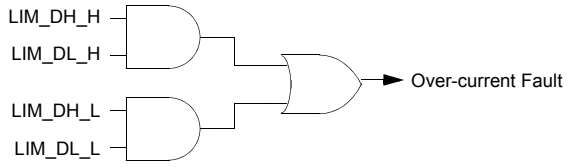


Figure 27. Over-current Fault Condition for ICL Bit

Fix[0:1] - Fixed Bits

These are hard coded bits - FIX0 is always zero and FIX1 is always one. These bits are the last two bits transmitted during the SPI message. Since their values are always fixed, these bits enable the Main MCU software to determine if the SPI data was shifted due to one too many, or one too few SPI clocks.

DnCTRL REGISTER

The read/write DnCTRL register sets up conditions to be used on the DBUS. There are four of these registers, one for each of the buses. The bit assignments are shown in Figure 28.

SPI Data Bit	Bit 7	6	5	4	3	2	1	0
Read/Write	-	-	DLYB	DLYA	-	LOOP1	LOOP0	MS
Reset	0	0	0	0	0	0	0	0

Figure 28. Dn Control Register Bit Assignment

Each bus *n* has an associated DnCTRL register. This register should be written to before data is sent over its bus. A write to the register will abort any current activity on the bus. Any bit changes will take place on the next DBUS transaction following the conclusion of the SPI write to the register. Refer to the Protocol Engine section for more detail.

DLY[B:A]–Interframe Delay for Channel n

These bits specify the minimum delay between transfer frames on the bus as illustrated in Table 10. For example, when DLY[B:A] is set to 00, there is a minimum of four bit times of IDLE voltage level. The time is measured from the end of a DBUS transaction (signaled by the start of the signal high to IDLE voltage transition) to the start of a new DBUS transaction (signaled by the start of the IDLE voltage to signal high transition).

Table 10. DLY[B:A] Frame Spacing

DLY[B:A]	Minimum Delay Between Frames (Bit Times)
00	4
01	5

Table 10. DLY[B:A] Frame Spacing (continued)

10	6
11	8

LOOP[1:0]- LOOP MODE CONTROL

- 00, 01, 10 = Loop Mode disabled.
- 11 = Loop Mode enabled

When loop mode is enabled, the transmitter and receiver circuits are connected within the IC. This allows data to be passed directly through the transmit and receive circuits without going out on the DBUS channel. When LOOP mode is enabled, the DBUS channel is disconnected from the transmitter and receiver circuits, so that any bus fault conditions do not interfere with this test. Setting this bit also disables the bus channel and clears the EN bit in the DnEN register.

MS–Message Size for Channel n

- 0 = Long Word.
- 1 = Short Word

The Long Word will contain 16 bits of data and 0 to 8 bits of CRC. The Short Word can be made to have between 8 and 15 bits of data and 0 to 8 bits of CRC. Long words are generally used for configuration and setup messages. Short words are generally used for DBUS data transactions.

DnEN REGISTER

This read/write register is used to enable or disable each of the buses. It also allows the channel thermal shutdown and bus driver shutdown bits to be read. The bit assignments are shown in Figure 29.

SPI Data Bit	Bit 7	6	5	4	3	2	1	0
Read/Write	TS	ISDD	-	-	-	BSWH (D0EN only)	BSWL (D0EN only)	EN
Reset	0	0	0	0	0	0	0	0

Figure 29. DnEN Register Bits

TS – Indicates a Thermal Shutdown on Channel n

- 0 = No thermal shutdown occurring on the Channel.
- 1 = Thermal shutdown has occurred on the Channel.

If the channel bus thermal limit is reached for either of the channel bus drivers, the channel drivers are disabled and the TS bit is set. There is a 4 µsec filter on Tlim to prevent false triggering. When this bit is set, the channel registers are all reset along with the buffer pointers. Any DBUS transfer that was in progress is stopped.

If the shutdown occurs on channel zero, the pseudo bus switches are also opened and the BSWH and BSWL bits are cleared. If the thermal limit is reached on either of the pseudo bus switches (but not on the channel zero drivers), the bus switches are opened, only the BSWH and BSWL bits are cleared, and no other register bits are changed.

The TS bit is cleared after a zero has been written to the TS bit.

ISDD - Idle and Signal Mode Disable on Channel n

- 0 = Idle and signal mode are active on the Channel.
- 1 = During signaling mode, the bus driver has shut down for sequential transactions on the Channel and the bus drivers are now disabled (high-impedance).

If a channel high side or low side bus driver over-current limit is reached during signaling mode in 2 consecutive frames, the bus drivers are disabled and the ISDD bit is set. If the condition occurs on channel zero, the pseudo bus switches are also opened and the BSWH and BSWL bits are cleared. In addition, the channel buffer registers are reset, the buffer pointers are reset, and the EN bit is cleared. The remainder of the channel registers are not changed. Any DBUS transfer that was in progress is stopped. The ISDD bit is cleared when the MCU writes a zero to this bit.

BSWH - Bus Switch High Enable

- 0 = Channel 0 Bus High Switch Open
- 1 = Channel 0 Bus High Switch Close

Channel 0 of the 33781 has a switch on both the high side and the low side of the bus output driver to allow the channel to drive two separate sets of bus wires. Through this bus switch the bus receiver can also receive data from slaves on both of these buses. When the BSWH bit is written as zero, the high side bus switch will be open. When the bit is written as a 1, the high side bus switch will be closed. Reads of this bit show the current state of the high side bus switch.

The BSWH bit is cleared and the bus switch opened if a channel zero thermal shutdown occurs, if the channel zero EN bit is cleared or ISDD bit is set, or if the high side or low side pseudo bus thermal limit is exceeded. It is necessary to write a one to the BSWH bit to close the switch again.

BSWL - Bus Switch Low Enable

- 0 = Channel 0 Bus Low Switch Open
- 1 = Channel 0 Bus Low Switch Close

When the BSWL bit is written as zero, the low side bus switch will be open. When the bit is written as a 1, the low side bus switch will be closed. Reads of this bit show the current state of the low side bus switch.

The BSWL bit is cleared and the bus switch opened, if a channel 0 thermal shutdown occurs, if the channel zero EN

bit is cleared or the ISDD bit is set, or if the high side or low side pseudo bus thermal limit is exceed. It is necessary to write a one to the BSWL bit to close the switch again.

EN – Controls Enabling and Disabling of Channel

- 0 = The Channel is disabled.
- 1 = The Channel is enabled.

When the channel is disabled, the channel addressed buffer data bits, the status register bits, and the buffer pointers are reset. Any DBUS transfer that was in progress is stopped. If the write is to channel 0, the pseudo bus switches are also opened and the BSWH and BSWL bits are cleared.

The EN bit is also cleared and the channel disabled if a thermal shutdown occurs. It is necessary to write a *1* to the EN bit to turn it back on.

DnPOLY REGISTERS

These read/write registers control the polynomial used for calculating the CRC that is transmitted/received on the DBUS channels. There are four of these registers, one for each DBUS channel. The bit assignments are shown in Figure 30.

SPI Data Bit	Bit 7	6	5	4	3	2	1	0
Read/Write	CRCPOLY7	CRCPOLY6	CRCPOLY5	CRCPOLY4	CRCPOLY3	CRCPOLY2	CRCPOLY1	CRCPOLY0
Reset	0	0	0	1	0	0	0	1

Figure 30. Dn Polynomial Register Bit Assignments

Each bit represents a polynomial term in the CRC equation. Bit 7 represents x^7, bit 6 represents x^6, and so on. Both the short and long word command use the same polynomial. The polynomial bits beyond what is specified in the CRCLEN[3:0] registers are ignored, and the most significant term of each polynomial is assumed to be on. So, for example, to represent a 6-bit CRC with a polynomial of $x^6 + x^3 + 1$, the value in DnPOLY is xx001001. Bits 7 and 6 are ignored in this case. These registers reset to 00010001 ($x^4 + 1$), which is the default DSI value (bit 4 does not need to be on for this case, but is included for readability).

A write to the register will abort any current activity on the bus. Any bit changes will take place on the next DBUS transaction following the conclusion of the SPI write to the register.

DnSEED REGISTERS

These read/write registers control the initial value, or seed, used for calculating the CRC that is transmitted/received on the DBUS channels. There are four of these registers, one for each DBUS channel. The bit assignments are shown in Figure 31.

SPI Data Bit	Bit 7	6	5	4	3	2	1	0
Read/Write	CRCSEED7	CRCEED6	CRCEED5	CRCEED4	CRCEED3	CRCEED2	CRCEED1	CRCEED0
Reset	0	0	0	0	1	0	1	0

Figure 31. Dn CRC Seed Register Bit Assignments

The bits in these registers form a word that is used as the seed for the CRC calculations. Both the short and long word commands use the same seed. The seed bits beyond what is specified in the CRCLEN[3:0] registers are ignored. So, for example, to represent a 6-bit CRC with a seed 010101, the value in DnSEED is xx010101. Bits 7 and 6 are ignored in this case. These registers reset to 00001010, which is the default DSI value.

A write to the register will abort any current activity on the bus. Any bit changes will take place on the next DBUS transaction following the conclusion of the SPI write to the register.

DnLENGTH REGISTERS

These read/write registers control the short word lengths and CRC lengths for data that is transmitted/received on the DBUS channels. There are four of these registers, one for each DBUS channel. The bit assignments are shown in Figure 32.

SPI Data Bit	Bit 7	6	5	4	3	2	1	0
Read/Write	SWLEN3	SWLEN2	SWLEN1	SWLEN0	CRCLEN3	CRCLEN2	CRCLEN1	CRCLEN0
Reset	1	0	0	0	0	1	0	0

Figure 32. Dn Short Word and CRC Length Register Bit Assignments

A write to the register will abort any current activity on the bus. Any bit changes will take place on the next DBUS transaction following the conclusion of the SPI write to the register.

SWLEN[3:0]–Short Word Length in Bits

These bits specify the bit length of the short word command that will be sent onto the specified DBUS channel. The reset value for these bits is 1000 (8 bits), which is the default DSI value. Allowed SWLEN[3:0] values range from 8 bits to 15 bits. If an attempt is made to write a value that is less than 8 bits, a 1 is automatically written to SWLEN3, thereby making the register value greater than or equal to 8 bits.

CRCLEN[3:0]–CRC Length in Bits

These bits specify the bit length of CRCs that are sent out with commands and read back in. The length is valid for both short and long word commands. The reset value for these bits is 0100 (4 bits), which is the default DSI value. Allowed CRCLEN[3:0] values range from 0 bits (no CRC) to 8 bits. If an attempt is made to write a value that is greater than 8 bits, the value 8 (1000) is automatically written into this register. The CRCLEN[3:0] value overrides the CRCPOLY and CRCSEED bit values that are beyond what the CRCLEN[3:0] specifies.

DnSSCTRL REGISTERS

These registers control the operation of the spread spectrum circuits.

A write to the register will abort any current activity on the bus. Any bit changes will take place on the next DBUS transaction following the conclusion of the SPI write to this register. The bit assignments are shown in Figure 33.

SPI Data Bit	Bit 7	6	5	4	3	2	1	0
Read/Write	-	-	-	-	-	DEV2	DEV1	DEV0
Reset	0	0	0	0	0	0	0	0

Figure 33. Dn Spread Spectrum Control Register Bit Assignment

DEV[2:0]–Spread Spectrum Frequency Deviation for Channel n

These bits control the frequency deviation of the spread spectrum signalling.

DEV[2:0] = 000 - No Deviation.

DEV[2:0] = 001 - 16 1/64 MHz periods Max Deviation

DEV[2:0] = 010 - 32 1/64 MHz periods Max Deviation

DEV[2:0] = 011 - 64 1/64 MHz periods Max Deviation

DEV[2:0] = 100 - 78 1/64 MHz periods Max Deviation

The deviation is the max number of 1/64MHz time periods which are randomly added to the base time period to achieve the spread spectrum effect. So for example, if you choose DEV=011, the bit time will randomly vary from the base time period to the base time period plus 1 µsec in 64 equal steps. The mode with deviation disabled may be used to achieve fine control of the bit rate without frequency spreading.

DnFSEL REGISTERS

These read/write registers control the spread spectrum base time period. There are four of these registers, one for each DBUS channel. The bit assignments are shown in Figure 34.

A write to one of these registers will abort any current activity on the bus. Any bit changes will take place on the next DBUS transaction following the conclusion of the SPI write to the register. Refer to the Spread Spectrum section for more detail.

SPI Data Bit	Bit 7	6	5	4	3	2	1	0
Read/Write	FSEL7	FSEL6	FSEL5	FSEL4	FSEL3	FSEL2	FSEL1	FSEL0
Reset	0	0	1	0	1	0	0	0

Figure 34. Dn Frequency Selection Register Bit Assignments

DnFSEL[7:0] - Channel Frequency Selection Bits

These bits select the channel base time period. These bits determine the minimum bit time (maximum bit frequency for a channel. The equation for the minimum bit time is:

$((1/16*f_{CLK}) \times (320 + 2x))$ where x = 0 to 255 (decimal)

The hex value for x in the equation is represented by the FSEL[7:0] bits

With a 4MHz clock and these bits set to zero the max bit rate is 200kbps. Table 8 gives some examples of the max bit rate and minimum bit time for f_{CLK} = 4.0MHz.

MASKID REGISTER

This read-only register contains seven mask ID bits for the silicon. This ID can reflect the version, design change number, or other encoded information. The purpose is for the central module CPU to be able to know what version of silicon

is in the system. The Fuse Parity Error Bit is also included in this register. The bit encoding is shown in Figure 35

SPI Data Bit	Bit 7	6	5	4	3	2	1	0
Read Only	FPAR	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Reset	0	0	0	0	0	0	0	1

Figure 35. Mask ID Register Bit Assignments

FPAR – Fuse Parity Error Bit

- 0 = No fuse parity error.
- 1 = There is a fuse parity error.

Some parameters in the device are trimmed by fuses. Since these parameters can be impacted by the state of the fuses, a fuse parity is calculated and stored during device manufacturing. When the device is powered up, the current fuse parity is checked against the stored parity. If they do not match this bit is set. This bit is also set if the part is untrimmed.

ID[6:0] – Mask ID number

The mask ID that identifies different versions or revisions of the device.

Check Pattern and Negative Check Pattern RegisteRS

These read-only registers are for checking whether there is a stuck bus bit. These registers are read as a 3 byte burst using a standard SPI burst frame The bit encoding is shown in Figure 36 and Figure 37

SPI Data Bit	Bit 7	6	5	4	3	2	1	0
Read	CKPTN23	CKPTN22	CKPTN21	CKPTN20	CKPTN19	CKPTN18	CKPTN17	CKPTN16
Reset	1	0	1	0	1	0	1	0
Read	CKPTN15	CKPTN14	CKPTN13	CKPTN12	CKPTN11	CKPTN10	CKPTN09	CKPTN08
Reset	0	1	0	1	0	1	0	1
Read	CKPTN07	CKPTN06	CKPTN05	CKPTN04	CKPTN03	CKPTN02	CKPTN01	CKPTN00
Reset	1	0	1	0	1	0	1	0

Figure 36. Check Pattern Registers Bit Assignments

SPI Data Bit	Bit 7	6	5	4	3	2	1	0
Read	NCKPTN23	NCKPTN22	NCKPTN21	NCKPTN20	NCKPTN19	NCKPTN18	NCKPTN17	NCKPTN16
Reset	0	1	0	1	0	1	0	1
Read	NCKPTN15	NCKPTN14	NCKPTN13	NCKPTN12	NCKPTN11	NCKPTN10	NCKPTN09	NCKPTN08
Reset	1	0	1	0	1	0	1	0
Read	NCKPTN07	NCKPTN06	NCKPTN05	NCKPTN04	NCKPTN03	NCKPTN02	NCKPTN01	NCKPTN00
Reset	0	1	0	1	0	1	0	1

Figure 37. Negative Check Pattern Registers Bit Assignments

PROTECTION AND DIAGNOSTIC FEATURES

OVER-CURRENT PROTECTION

Current limiters on the outputs prevent damage in the case of shorts. Running in current limit results in high power dissipation of the IC. If the power dissipation becomes high enough, the die temperature will rise above its maximum rating and an over-temperature circuit on the IC will shut down the DBUS Driver/Receiver block.

Each channel high and low side bus drivers have current limits for protection of both this device and slave devices connected on the DBUS. During idle mode, the DnH drivers have a high value current limit when sourcing current to allow the drivers to charge the slave power storage capacitors, and a lower value current limit when sinking current and slewing the load capacitance. Conversely, the DnL drivers have a high value current limit when they are sinking current, and a lower value current limit when they are sourcing current.

In addition, the device monitors the current limit on each channel to see if the channel is in “double current limit” during every idle state. See ICL - Idle Mode Double Current Limit Bit (Idle Mode Shutdown) on page 33. If the idle current limit is detected, the ICL bit is set in the DnSTAT register for the next DBUS transaction.

During signaling mode, the drivers incorporate a gross current limit and an over-current shutdown. The current shutdown is set at a low value, such that the channel high and low side bus driver will shut down if the sourcing or sinking current remains at a value larger than the response current. The over-current shutdown is delayed by a filter to allow the load capacitors to be slewed without causing a shutdown.

The purpose of the gross current limit is to protect the drivers during the filter delay time. This current limit is set higher than the peak current required to slew the load capacitance.

The signals from the sourcing and sinking current detection circuits are connected to a logical OR. The combined signal passes through a common filter before setting the over-current latch. During signaling mode, the over-current shutdown disables both bus drivers and sets the SDS (Signal Driver Shutdown) bit in the appropriate DnSTAT register. The drivers remain high-impedance until the end of Frame, when the bus returns to the Idle state.

The end of Frame clears the over-current shutdown state, allowing the bus drivers to retry in the next Frame. However, if the signal mode over-current shutdown occurs in two sequential frames for the channel, the bus drivers are disabled and can only be re-enabled on command from the MCU. The ISDD bit is also set in the channel DEN register. If the affected channel is channel 0 this set of conditions also disables the pseudo bus switch.

THERMAL PROTECTION

Independent thermal protection is provided for each channel and the Pseudo bus switches. The thermal limit cell is located adjacent to the bus drivers for each channel, such that both drivers are protected. When a thermal fault is detected, the channel drivers are disabled (Hi-Z) until they are re-enabled via the SPI. The thermal protection incorporates hysteresis, preventing the channel bus drivers from being re-enabled until the temperature has decreased. Thermal fault information is reported via the DEN register. See DnEN Register section for a description of the fault reporting and clearing of the EN bits.

LOAD DUMP OPERATION

During an over-voltage condition (e.g., when load dump is applied at the VSUPn pins), the DBUS voltage waveform is modified to ensure that power dissipation is minimized, DBUS timing is not violated, and internal components are protected.

The midpoint of the signalling voltage is clamped at about 13V, such that for V_{SUPn} greater than 26V, the signalling voltage levels do not increase. An over-voltage detection circuit connected to DnH, having a threshold at about 26V, causes the slew rates and driver conditions to be modified. For a Signal-to-Idle transition, this causes the DnH voltage to rise rapidly to the Idle state, and the DnL voltage is maintained close to zero. For an Idle-to-Signal transition, the DnH voltage will decrease rapidly until the over-voltage threshold is reached, when normal operation resumes. During this rapid fall of DnH, the DnL voltage is maintained close to zero by forcing that driver on. See Figure 6.

RESET FUNCTION

A low level on $\overline{RST}$ forces all internal registers to a known (reset) state and the receive and transmit queue pointers are reset. Because the DBUS channels are now disabled (ENn = 0), the DBUS lines are tri-stated.

ABORT FUNCTION

An abort is generated on a channel whenever a control register (DnCTRL, DnPOLY, DnSEED, DnLENGTH, DnSSCTRL or DnFSEL) is addressed while writing, even if the data is unchanged. No other register writes cause an abort, and reads of any register do not cause an abort. The abort is only taken for the channel where the write occurs - all other channels are not effected. The DEN register is not affected by an abort.

The abort occurs as soon as the address of the control register is received on the SPI. Any DBUS transfer that was in progress is stopped, and DBUS lines return to their Idle states. The abort condition remains true throughout the SPI0 write to the DBUS control registers. After the last bit of the DBUS control register is written, the channel addressed buffer data bits and the SPI1 registers are cleared, the status register bits are reset, and the transmit and receive queue pointers are reset for both SPI0 and SPI1. The programmed inter-frame delay is then enforced (using the new values of the delay control bits) to allow reservoir capacitors in remote

nodes to charge. In the case of DLY changing, any partial inter-frame delay based on old control settings is lost.

ENABLE (DISABLE) FUNCTION

When a DBUS channel is disabled, the 33781 device forces its bus output to tri-state. When the channel is disabled the channel addressed buffer data bits are cleared, the status register bits are reset, and the transmit and receive queue reset. Any DBUS transfer that was in progress is stopped.

CHANNEL LOOP FUNCTION

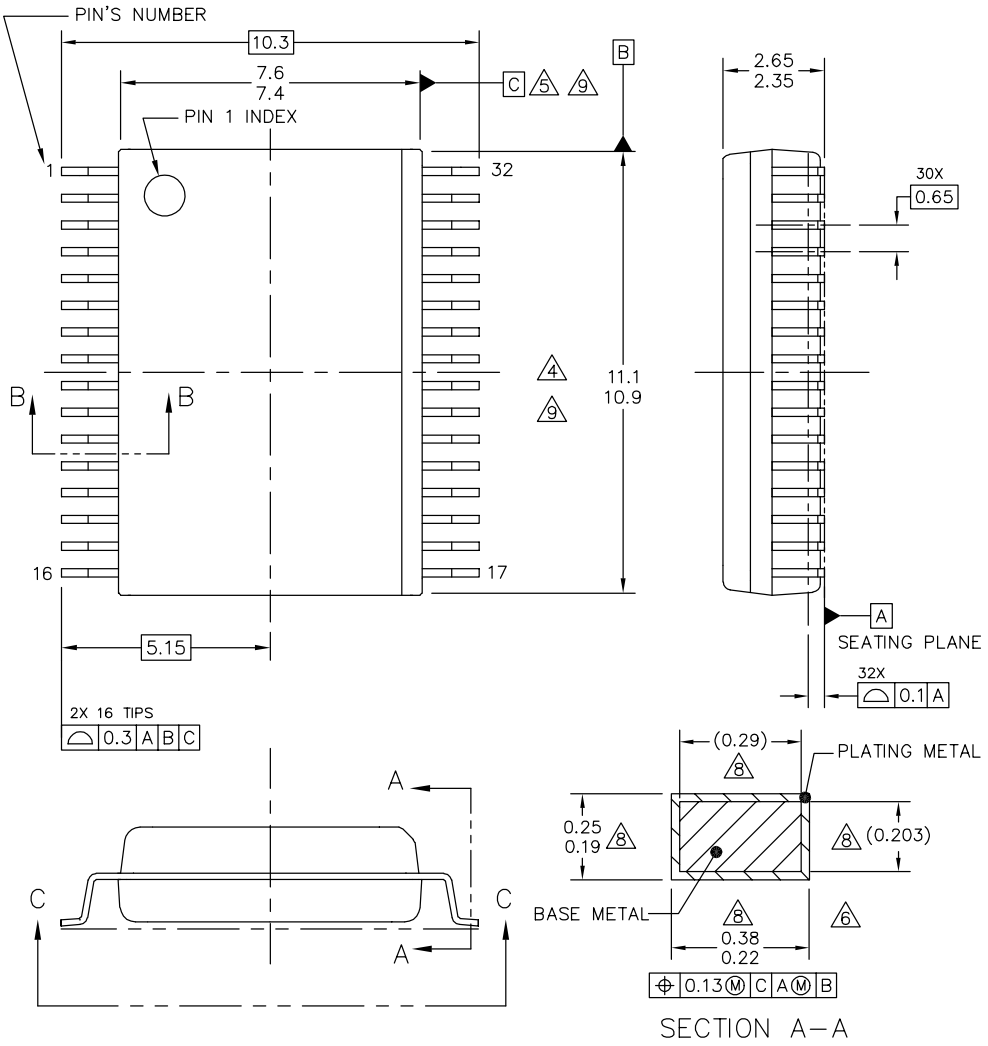
When loop mode is enabled the transmitter and receiver circuits are connected within the IC. This allows data to be passed directly through the transmit and receive circuits without going out on the DBUS channel. When LOOP mode is enabled the DBUS channel is disconnected from the transmitter and receiver circuits so that any bus fault conditions do not interfere with this test. When the loop function is enabled, the EN bit in the DnEN register is cleared, the buffer data bits are cleared, the status register bits are reset, and the transmit and receive queue reset the by the state machine. When the loop mode is exited the state machine sets the registers to their reset state and resets the transmit and receive queue. This allows proper start up of bus transactions.

The channel queue pointers work the same as in non-loop mode.

PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit www.freescale.com and perform a keyword search using the “98A” listed below.



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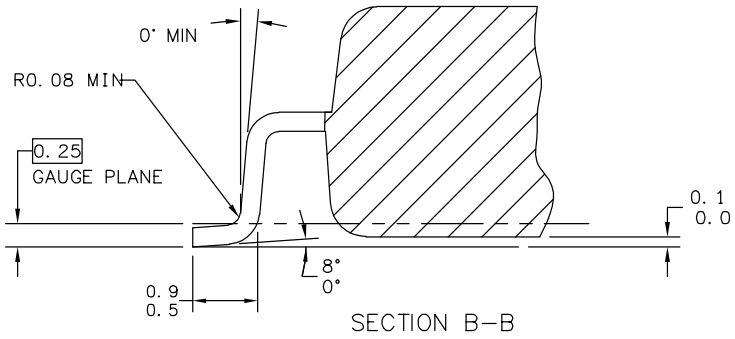
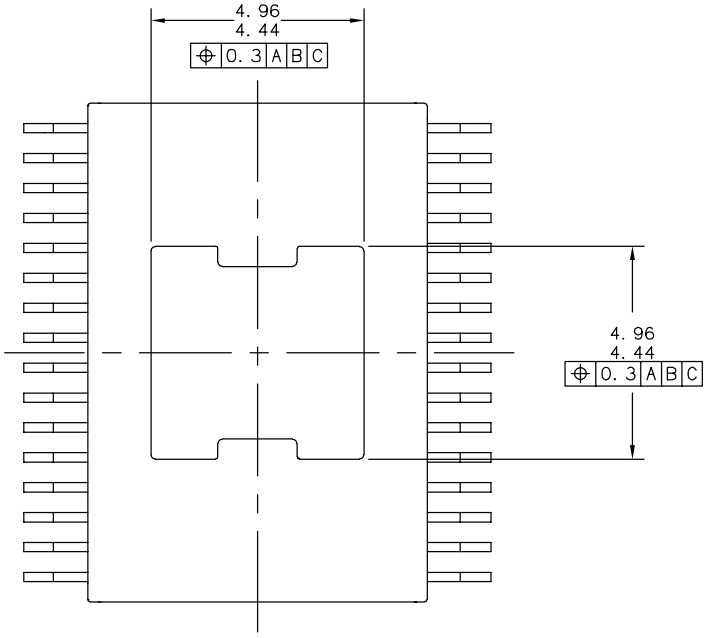
32-PIN
98ASA10556D
ISSUE B

33781



SECTION B–B



VIEW C–C

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TITLE: 32LD SOIC W/B, 0.65 PITCH 4.7 X 4.7 EXPOSED PAD, CASE–OUTLINE	DOCUMENT NO: 98ASA10556D	REV: B
	CASE NUMBER: 1454–02	15 SEP 2005
	STANDARD: NON–JEDEC	

EK SUFFIX (PB-FREE)
32-PIN
98ASA10556D
ISSUE B

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.4 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 mm.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.3 mm FROM THE LEAD TIP.
9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER–LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

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REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
1	3/2008	• Initial Release
2	5/2008	• Deleted rows from Figure 7, Receiver Decision Logic • Corrected several parameter adjustments
3	7/2008	• Numerous minor label and limit changes to Electrical Characteristics • Text corresponding to the changes in the Electrical Characteristics were also made.
4	7/2008	• Changed line to read: In addition, the device monitors the current limit on each channel to see if the channel is in “double current limit” during every idle state. In the OVER-CURRENT Protection
5.0	11/2009	• Changed Part Number from PCZ33781EK/R2 to MCZ33781EK/R2

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