

IRL3402S

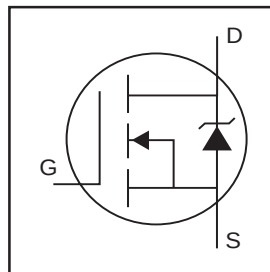
HEXFET® Power MOSFET

- Advanced Process Technology
- Surface Mount
- Optimized for 4.5V-7.0V Gate Drive
- Ideal for CPU Core DC-DC Converters
- Fast Switching

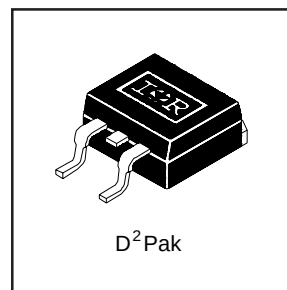
Description

These HEXFET Power MOSFETs were designed specifically to meet the demands of CPU core DC-DC converters in the PC environment. Advanced processing techniques combined with an optimized gate oxide design results in a die sized specifically to offer maximum efficiency at minimum cost.

The D²Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.



$V_{DSS} = 20V$
$R_{DS(on)} = 0.01\Omega$
$I_D = 85A^{\textcircled{6}}$



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^{\circ}C$	Continuous Drain Current, $V_{GS} @ 4.5V^{\textcircled{5}}$	85 ^⑥	A
$I_D @ T_C = 100^{\circ}C$	Continuous Drain Current, $V_{GS} @ 4.5V^{\textcircled{5}}$	54	
I_{DM}	Pulsed Drain Current ^{① ⑤}	340	
$P_D @ T_C = 25^{\circ}C$	Power Dissipation	110	W
	Linear Derating Factor	0.91	W/°C
V_{GS}	Gate-to-Source Voltage	± 10	V
V_{GSM}	Gate-to-Source Voltage (Start Up Transient, $t_p = 100\mu s$)	14	V
E_{AS}	Single Pulse Avalanche Energy ^{② ⑤}	290	mJ
I_{AR}	Avalanche Current ^①	51	A
E_{AR}	Repetitive Avalanche Energy ^①	11	mJ
dv/dt	Peak Diode Recovery dv/dt ^{③ ⑤}	5.0	V/ns
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	---	1.1	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted, steady-state)**	---	40	

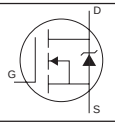
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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	20	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.02	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1\text{mA}$ ⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.010	Ω	$V_{GS} = 4.5V, I_D = 51A$ ④
		—	—	0.008		$V_{GS} = 7.0V, I_D = 51A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	0.70	—	—	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	65	—	—	S	$V_{DS} = 10V, I_D = 51A$ ⑤
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 20V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 16V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 10V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -10V$
Q_g	Total Gate Charge	—	—	78	nC	$I_D = 51A$
Q_{gs}	Gate-to-Source Charge	—	—	18		$V_{DS} = 10V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	30		$V_{GS} = 4.5V$, See Fig. 6 ④⑤
$t_{d(on)}$	Turn-On Delay Time	—	10	—	ns	$V_{DD} = 10V$
t_r	Rise Time	—	140	—		$I_D = 51A$
$t_{d(off)}$	Turn-Off Delay Time	—	80	—		$R_G = 5.0\Omega, V_{GS} = 4.5V$
t_f	Fall Time	—	120	—		$R_D = 0.19\Omega$, ④⑤
L_S	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C_{iss}	Input Capacitance	—	3300	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	1400	—		$V_{DS} = 15V$
C_{rss}	Reverse Transfer Capacitance	—	510	—		$f = 1.0\text{MHz}$, See Fig. 5⑤

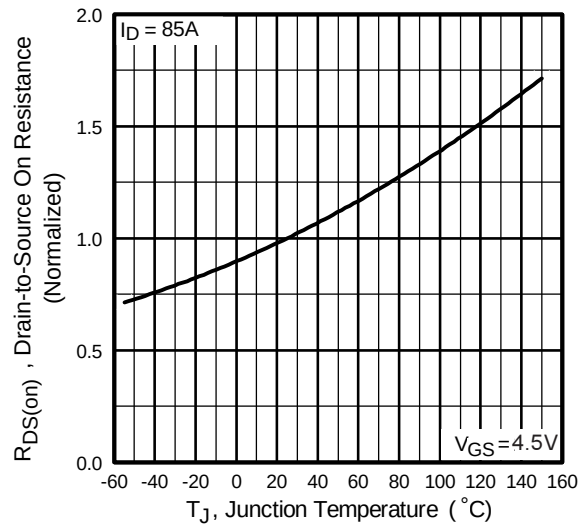
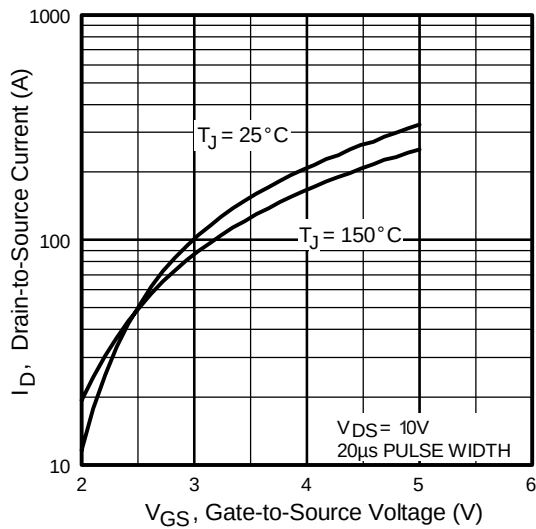
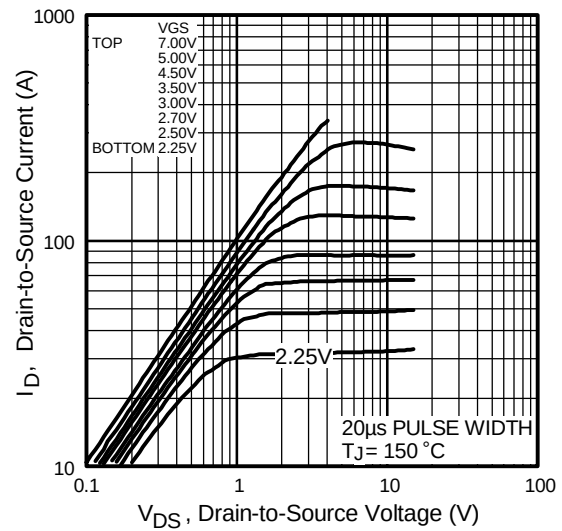
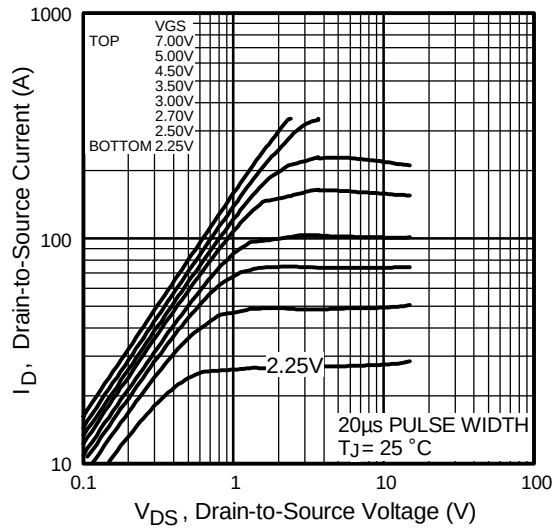
Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	85	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①⑤	—	—	340		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 51A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	72	110	ns	$T_J = 25^\circ\text{C}, I_F = 51A$
Q_{rr}	Reverse Recovery Charge	—	160	240	nC	$di/dt = 100A/\mu s$ ④⑤
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 220\mu H$
 $R_G = 25\Omega$, $I_{AS} = 51A$.
- ③ $I_{SD} \leq 51A$, $di/dt \leq 82A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ⑤ Uses IRL3402 data and test conditions
- ⑥ Calculated continuous current based on maximum allowable junction temperature; for recommended current-handling of the package refer to Design Tip # 93-4

** When mounted on FR-4 board using minimum recommended footprint.
For recommended footprint and soldering techniques refer to application note #AN-994.



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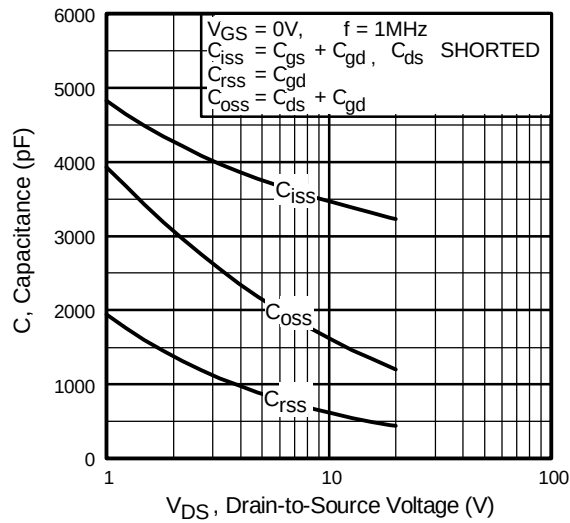


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

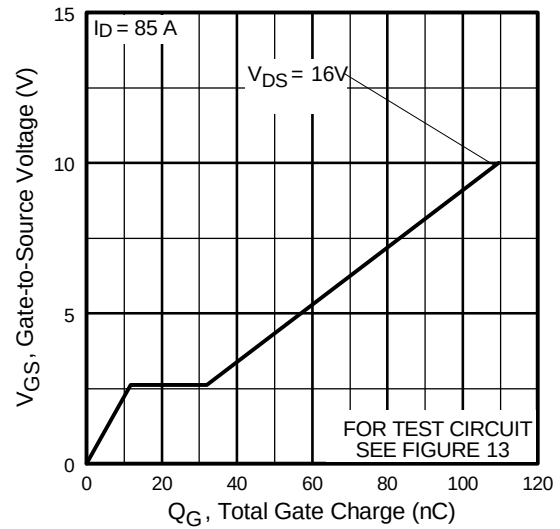


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

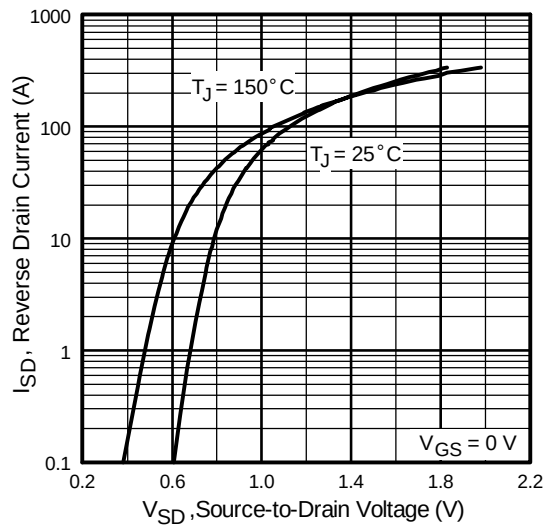


Fig 7. Typical Source-Drain Diode Forward Voltage

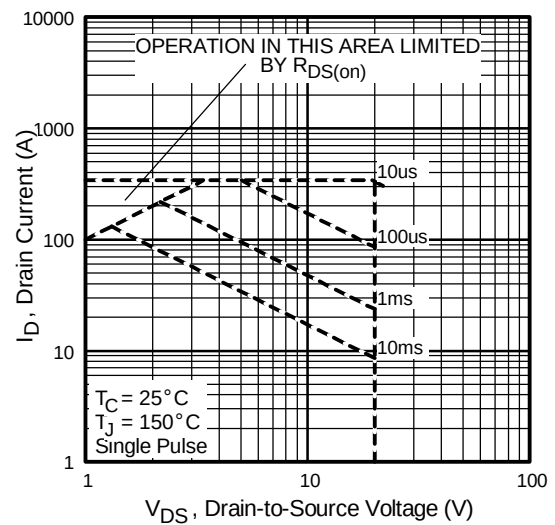
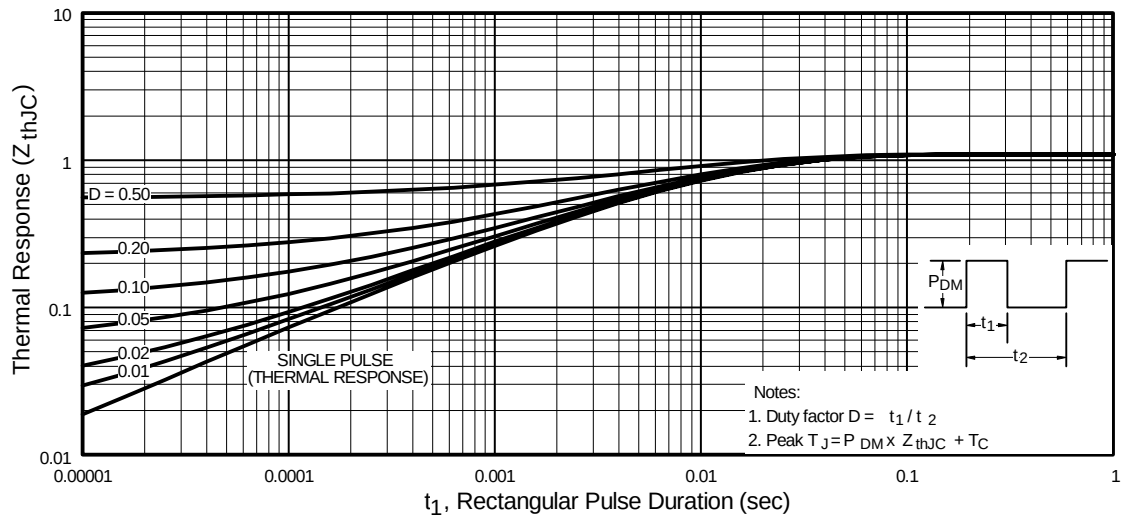
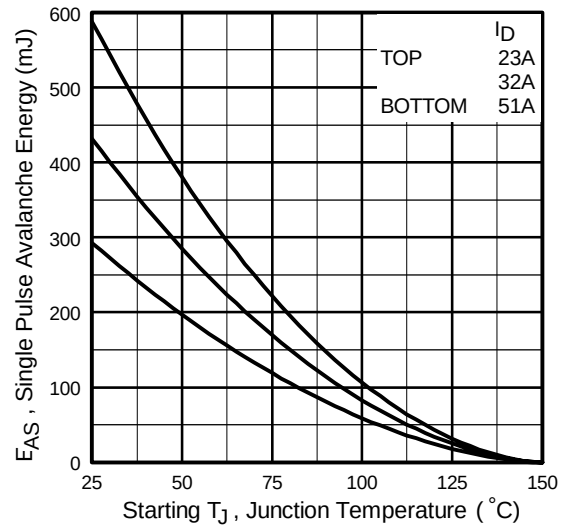
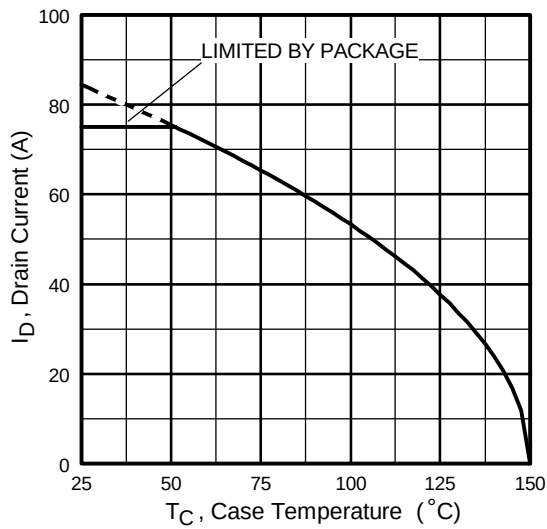


Fig 8. Maximum Safe Operating Area



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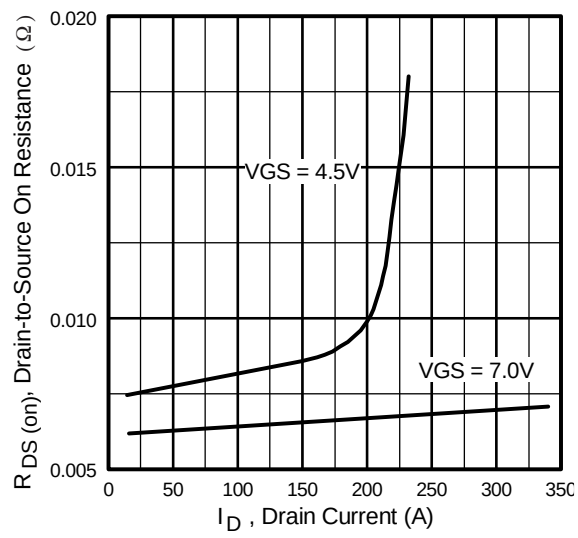


Fig 12. On-Resistance Vs. Drain Current

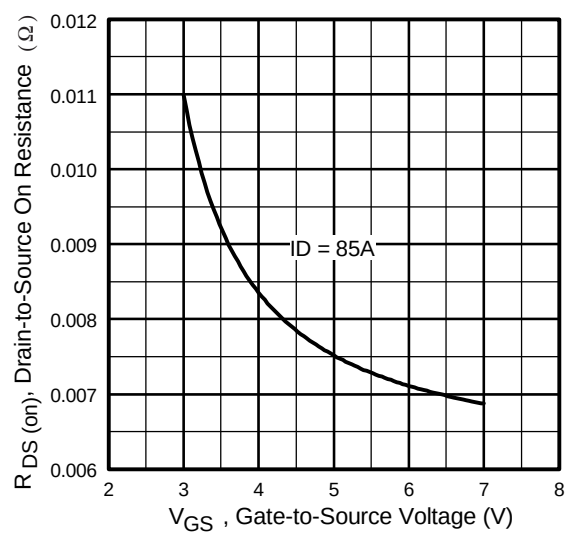
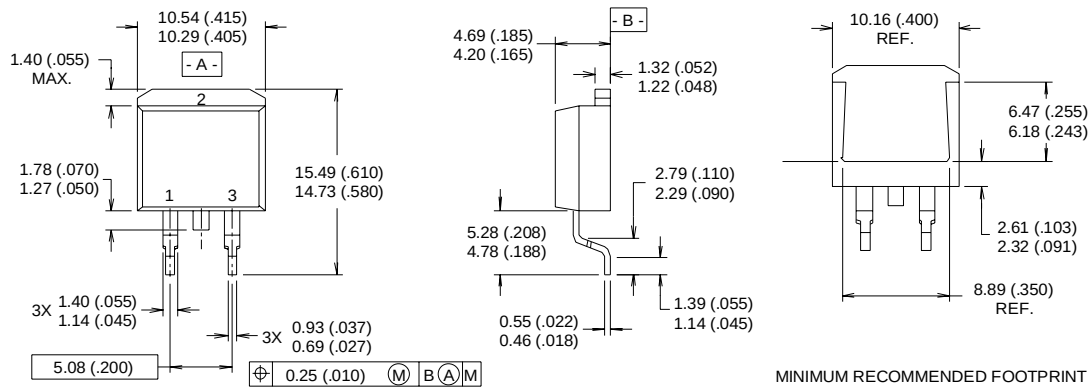


Fig 13. On-Resistance Vs. Gate Voltage

D²Pak Package Outline



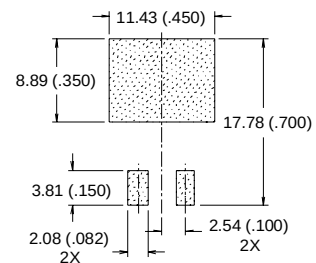
NOTES:

- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS

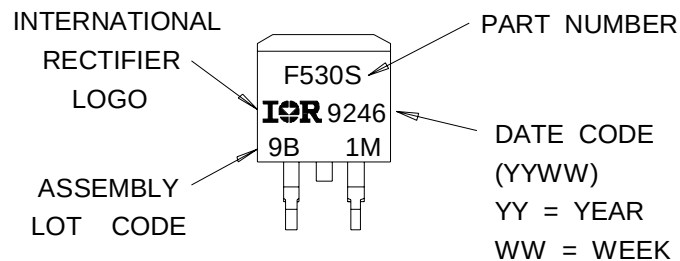
- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

MINIMUM RECOMMENDED FOOTPRINT



Part Marking Information

D²Pak

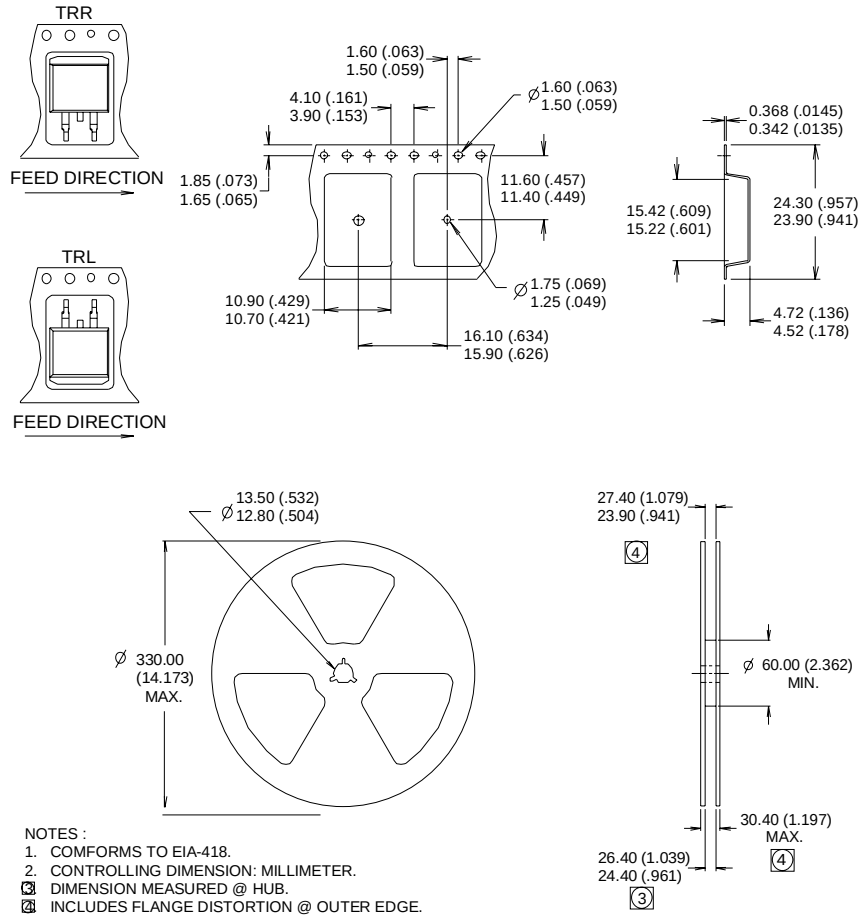


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Tape & Reel Information

D²Pak



Data and specifications subject to change without notice.

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