STEREO AUDIO DAC WITH USB INTERFACE, SINGLE-ENDED HEADPHONE OUTPUT AND S/PDIF OUTPUT

FEATURES

- **On-Chip USB Interface:**
  - **No Need of Dedicated Device Driver**
  - **With Full-Speed Transceivers**
  - **Fully Compliant With USB 1.1 Specification**
  - **Certified by USB-IF**
  - **Partially Programmable Descriptors**
  - **Adaptive Isochronous Transfer for Playback**
  - **Bus-Powered or Self-Powered Operation**
- **Sampling Rate: 32, 44.1, 48 kHz**
- **On-Chip Clock Generator With Single 12-MHz Clock Source**
- **Single Power Supply:**
  - **Bus-Powered: 5 V, Typical (V_{BUS})**
  - **Self-Powered: 3.3 V, Typical**
- **16-Bit Delta-Sigma Stereo DAC**
  - **Analog Performance at 5 V (Bus-Powered), 3.3 V (Self-Powered):**
    - **THD+N: 0.006% R_L > 10 kΩ, Self-Powered**
    - **THD+N: 0.025% R_L = 32 Ω**
    - **SNR = 98 dB**
    - **Dynamic Range: 98 dB**
    - **P_O = 12 mW, R_L = 32 Ω**
  - **Oversampling Digital Filter**
    - **Pass-Band Ripple = ±0.04 dB**
    - **Stop-Band Attenuation = –50 dB**
  - **Single-Ended Voltage Output**
  - **Analog LPF Included**
- **Multiple Functions:**
  - **Up to Eight Human Interface Device (HID) Interfaces (Depending on Model and Settings)**
  - **Suspend Flag**
  - **S/PDIF Out With SCMS**
  - **External ROM Interface (PCM2704/6)**
  - **Serial Programming Interface (PCM2705/7)**
  - **I^2S Interface (Selectable on PCM2706/7)**
- **Package:**
  - **28-Pin SSOP (PCM2704/5)**
  - **32-Pin TQFP (PCM2706/7)**

APPLICATIONS

- **USB Headphones**
- **USB Audio Speaker**
- **USB CRT/LCD Monitor**
- **USB Audio Interface Box**
- **USB-Featured Consumer Audio Product**

DESCRIPTION

The PCM2704/5/6/7 is TI's single-chip USB stereo audio DAC with USB-compliant full-speed protocol controller and S/PDIF. The USB-protocol controller works with no software code, but USB descriptors can be modified in some parts (for example, vendor ID/product ID) through the use of an external ROM (PCM2704/6), SPI (PCM2705/7), or on request. (1) The PCM2704/5/6/7 employs SpAct™ architecture, TI's unique system that recovers the audio clock from USB packet data. On-chip analog PLLs with SpAct enable playback with low clock jitter.

(1) The modification of the USB descriptor through external ROM or SPI must comply with USB-IF guidelines, and the vendor ID must be your own ID as assigned by the USB-IF. The descriptor also can be modified by changing a mask; contact your representative for details.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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I2S is a trademark of NXP Semiconductors.
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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted (1)

Supply voltage	V_{BUS}	–0.3 V to 6.5 V
	V_{CCP}, V_{CCL}, V_{CCR}, V_{DD}	–0.3 V to 4 V
Supply voltage differences	V_{CCP}, V_{CCL}, V_{CCR}, V_{DD}	±0.1 V
Ground voltage differences	PGND, AGNDL, AGNDR, DGND, ZGND	±0.1 V
Digital input voltage	HOST	–0.3 V to 6.5 V
	D+, D–, HID0/MS, HID1/MC, HID2/MD, XTI, XTO, DOUT, $\overline{\text{SSPND}}$, CK, DT, PSEL, FSEL, TEST, TEST0, TEST1, FUNC0, FUNC1, FUNC2, FUNC3	–0.3 V to (V_{DD} + 0.3) V < 4 V
Analog input voltage	V_{COM}	–0.3 V to (V_{CCP} + 0.3) V < 4 V
	V_{OUT}R	–0.3 V to (V_{CCR} + 0.3) V < 4 V
	V_{OUT}L	–0.3 V to (V_{CCL} + 0.3) V < 4 V
Input current (any pins except supplies)		±10 mA
Ambient temperature under bias		–40°C to 125°C
Storage temperature		–55°C to 150°C
Junction temperature		150°C
Lead temperature (soldering)		260°C, 5 s
Package temperature (IR reflow, peak)		260°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range

		MIN	NOM	MAX	UNIT
Supply voltage	V_{BUS}	4.35	5	5.25	V
	V_{CCP}, V_{CCL}, V_{CCR}, V_{DD}	3	3.3	3.6	
Digital input logic level			TTL compatible		
Digital input clock frequency		11.994	12	12.006	MHz
Analog output load resistance		16	32		Ω
Analog output load capacitance				100	pF
Digital output load capacitance				20	pF
Operating free-air temperature, T_A		–25		85	C

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ELECTRICAL CHARACTERISTICS

all specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz,16-bit data (unless otherwise noted)

PARAMETER			TEST CONDITIONS	PCM2704DB, PCM2705DB, PCM2706PJT, PCM2707PJT			UNIT
				MIN	TYP	MAX	
DIGITAL INPUT/OUTPUT							
	Host interface			Apply USB revision 1.1, full-speed			
	Audio data format			USB isochronous data format			
INPUT LOGIC							
V_{IH}	Input logic level			2		3.3	Vdc
V_{IL}				–0.3		0.8	
V_{IH} (1)				2		5.5	
V_{IL} (1)				–0.3		0.8	
I_{IH} (2)	Input logic current		V_{IN} = 3.3 V			±10	µA
I_{IL} (2)			V_{IN} = 0 V			±10	
I_{IH}			V_{IN} = 3.3 V		65	100	
I_{IL}			V_{IN} = 0 V			±10	
OUTPUT LOGIC							
V_{OH} (3)	Output logic level		I_{OH} = –2 mA	2.8			Vdc
V_{OL} (3)			I_{OL} = 2 mA			0.3	
V_{OH}			I_{OH} = –2 mA	2.4			
V_{OL}			I_{OL} = 2 mA			0.4	
CLOCK FREQUENCY							
	Input clock frequency, XTI			11.994	12	12.006	MHz
f_S	Sampling frequency				32, 44.1, 48		kHz
DAC CHARACTERISTICS							
	Resolution				16		Bits
	Audio data channel				1, 2		Channel
DC ACCURACY							
	Gain mismatch, channel-to-channel				±2	±8	% of FSR
	Gain error				±2	±8	% of FSR
	Bipolar zero error				±3	±6	% of FSR
DYNAMIC PERFORMANCE (4)							
THD+N	Total harmonic distortion + noise	Line (5)	R_L > 10 kΩ, self-powered, V_{OUT} = 0 dB		0.006%	0.01%	
			R_L > 10 kΩ, bus-powered, V_{OUT} = 0 dB		0.012%	0.02%	
		Headphone	R_L = 32 Ω, self-/ bus-powered, V_{OUT} = 0 dB		0.025%		
THD+N	Total harmonic distortion + noise		V_{OUT} = –60 dB		2%		
	Dynamic range		EIAJ, A-weighted	90	98		dB
S/N	Signal-to-noise ratio		EIAJ, A-weighted	90	98		dB
	Channel separation			60	70		dB

(1) HOST
(2) D+, D–, HOST, TEST, TEST0, TEST1, DT, PSEL, FSEL, XTI
(3) FUNC0, FUNC1, FUNC2
(4) f_{IN} = 1 kHz, using the System Two™ Cascade audio measurement system by Audio Precision™ in the RMS mode with a 20-kHz LPF and 400-Hz HPF.
(5) THD+N performance varies slightly, depending on the effective output load, including dummy load R7, R8 in Figure 32.

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ELECTRICAL CHARACTERISTICS (continued)

all specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz,16-bit data (unless otherwise noted)

PARAMETER			TEST CONDITIONS	PCM2704DB, PCM2705DB, PCM2706PJT, PCM2707PJT			UNIT
				MIN	TYP	MAX	
ANALOG OUTPUT							
	Output voltage				0.55 V_{CCL}, 0.55 V_{CCR}		Vp-p
	Center voltage				0.5 V_{CCP}		V
	Load impedance	Line	AC coupling	10			kΩ
		Headphone	AC coupling	16	32		Ω
	LPF frequency response		–3 dB		140		kHz
			f = 20 kHz		–0.1		dB
DIGITAL FILTER PERFORMANCE							
	Pass band					0.454 f_S	Hz
	Stop band			0.546 f_S			Hz
	Pass-band ripple					±0.04	dB
	Stop-band attenuation			–50			dB
	Delay time				20/f_S		s
POWER SUPPLY REQUIREMENTS							
	Voltage range	V_{BUS}	Bus-powered	4.35	5	5.25	Vdc
		V_{CCP}, V_{CCL}, V_{CCR}, V_{DD}	Self-powered	3	3.3	3.6	
	Supply current	Line	DAC operation		23	30	mA
		Headphone	DAC operation R_L = 32 Ω)		35	46	
		Line/headphone	Suspend mode (6)		150	190	µA
	Power dissipation (self-powered)	Line	DAC operation		76	108	mW
		Headphone	DAC operation R_L = 32 Ω)		116	166	
		Line/headphone	Suspend mode (6)		495	684	µW
	Power dissipation (bus-powered)	Line	DAC operation		115	158	mW
		Headphone	DAC operation R_L = 32 Ω)		175	242	
		Line/headphone	Suspend mode (6)		750	998	µW
	Internal power-supply voltage (7)	V_{CCP}, V_{CCL}, V_{CCR}, V_{DD}	Bus-powered	3.2	3.35	3.5	Vdc
TEMPERATURE RANGE							
	Operating temperature			–25		85	°C
θ_{JA}	Thermal resistance	28-pin SSOP (PCM2704/5)			100		°C/W
		32-pin TQFP (PCM2706/7)			80		

(6) Under USB suspend state.
(7) V_{DD}, V_{CCP}, V_{CCL}, V_{CCR}. These pins work as output pins of internal power supply for bus-powered operation.

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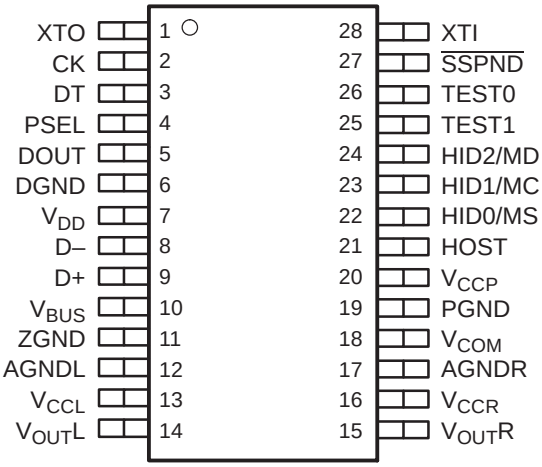
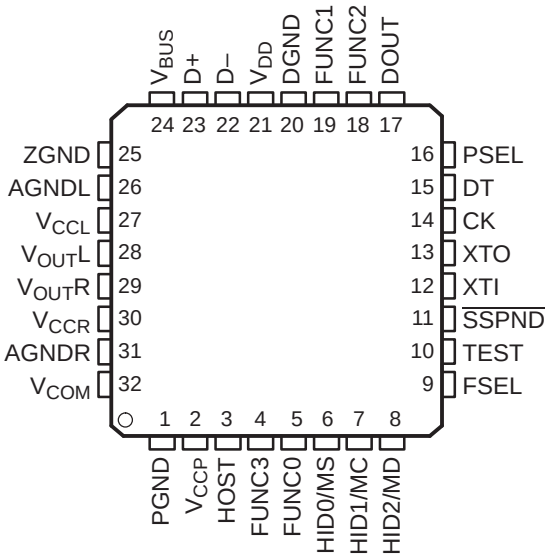
PIN ASSIGNMENTS

PCM2704/PCM2705
DB PACKAGE
(TOP VIEW)



PCM2706/PCM2707
PJT PACKAGE
(TOP VIEW)



P0020-01

Terminal Functions (PCM2704DB/PCM2705DB)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGNDL	12	—	Analog ground for headphone amplifier of L-channel
AGNDR	17	—	Analog ground for headphone amplifier of R-channel
CK	2	O	Clock output for external ROM (PCM2704). Must be left open (PCM2705).
D+	9	I/O	USB differential input/output plus (1)
D–	8	I/O	USB differential input/output minus (1)
DGND	6	—	Digital ground
DOUT	5	O	S/PDIF output
DT	3	I/O	Data input/output for external ROM (PCM 2704). Must be left open with pullup resistor (PCM2705). (1)
HID0/MS	22	I	HID key state input (mute), active HIGH (PCM2704). MS input (PCM2705). (2)
HID1/MC	23	I	HID key state input (volume up), active HIGH (PCM2704). MC input (PCM2705). (2)
HID2/MD	24	I	HID key state input (volume down), active HIGH (PCM2704). MD input (PCM2705). (2)
HOST	21	I	Host detection during self-powered operation (connect to V_{BUS}). Max power select during bus-powered operation (LOW: 100 mA, HIGH: 500 mA). (3)
PGND	19	—	Analog ground for DAC, OSC, and PLL
PSEL	4	I	Power source select (LOW: self-power, HIGH: bus-power) (1)
$\overline{SSPND}$	27	O	Suspend flag, active LOW (LOW: suspend, HIGH: operational)
TEST0	26	I	Test pin. Must be set HIGH (1)
TEST1	25	I	Test pin. Must be set HIGH (1)
V_{BUS}	10	—	Connect to USB power (V_{BUS}) for bus-powered operation. Connect to V_{DD} for self-powered operation.
V_{CCL}	13	—	Analog power supply for headphone amplifier of L-channel (4)
V_{CCP}	20	—	Analog power supply for DAC, OSC, and PLL (4)
V_{CCR}	16	—	Analog power supply for headphone amplifier of R-channel (4)
V_{COM}	18	—	Common voltage for DAC (V_{CCP}/2). Connect decoupling capacitor to PGND.
V_{DD}	7	—	Digital power supply (4)
V_{OUT}L	14	O	DAC analog output for L-channel
V_{OUT}R	15	O	DAC analog output for R-channel
XTI	28	I	Crystal oscillator input (1)
XTO	1	O	Crystal oscillator output
ZGND	11	—	Ground for internal regulator

(1) LV-TTL level
(2) LV-TTL level with internal pulldown
(3) LV-TTL level, 5-V tolerant
(4) Connect decoupling capacitor to GND. Supply 3.3 V for self-powered applications.

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Terminal Functions (PCM2706PJT/PCM2707PJT)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGNDL	26	—	Analog ground for headphone amplifier of L-channel
AGNDR	31	—	Analog ground for headphone amplifier of R-channel
CK	14	O	Clock output for external ROM (PCM2706). Must be left open (PCM2707).
D+	23	I/O	USB differential input/output plus (1)
D–	22	I/O	USB differential input/output minus (1)
DGND	20	—	Digital ground
DOUT	17	O	S/PDIF output/I^2S™ data output
DT	15	I/O	Data input/output for external ROM (PCM2706). Must be left open with pullup resistor (PCM2707). (1)
FSEL	9	I	Function select (LOW: I^2S DATA output, HIGH: S/PDIF output) (1)
FUNC0	5	I/O	HID key state input (next track), active HIGH (FSEL = 1). I^2S LR clock output (FSEL = 0). (2)
FUNC1	19	I/O	HID key state input (previous track), active HIGH (FSEL = 1). I^2S bit clock output (FSEL = 0). (2)
FUNC2	18	I/O	HID key state input (stop), active HIGH (FSEL = 1). I^2S system clock output (FSEL = 0). (2)
FUNC3	4	I	HID key state input (play/pause), active HIGH (FSEL = 1). I^2S data input (FSEL = 0). (2)
HID0/MS	6	I	HID key state input (mute), active HIGH (PCM2706). MS input (PCM2707) (2)
HID1/MC	7	I	HID key state input (volume up), active HIGH (PCM2706). MC input (PCM2707) (2)
HID2/MD	8	I	HID key state input (volume down), active HIGH (PCM2706). MD input (PCM2707) (2)
HOST	3	I	Host detection during self-powered operation (connect to V_{BUS}). Max power select during bus-powered operation. (LOW: 100 mA, HIGH: 500 mA). (3)
PGND	1	—	Analog ground for DAC, OSC, and PLL
PSEL	16	I	Power source select (LOW: self-power, HIGH: bus-power) (1)
$\overline{SSPND}$	11	O	Suspend flag, active LOW (LOW: suspend, HIGH: operational)
TEST	10	I	Test pin. Must be set HIGH (1)
V_{BUS}	24	—	Connect to USB power (V_{BUS}) for bus-powered operation. Connect to V_{DD} for self-powered operation.
V_{CCL}	27	—	Analog power supply for headphone amplifier of L-channel (4)
V_{CCP}	2	—	Analog power supply for DAC, OSC, and PLL (4)
V_{CCR}	30	—	Analog power supply for headphone amplifier of R-channel (4)
V_{COM}	32	—	Common voltage for DAC (V_{CCP}/2). Connect decoupling capacitor to PGND.
V_{DD}	21	—	Digital power supply (4)
$V_{OUT}L$	28	O	DAC analog output for L-channel
$V_{OUT}R$	29	O	DAC analog output for R-channel
XTI	12	I	Crystal oscillator input (1)
XTO	13	O	Crystal oscillator output
ZGND	25	—	Ground for internal regulator

(1) LV-TTL level
(2) LV-TTL level with internal pulldown
(3) LV-TTL level, 5-V tolerant
(4) Connect decoupling capacitor to GND. Supply 3.3 V for self-powered applications.

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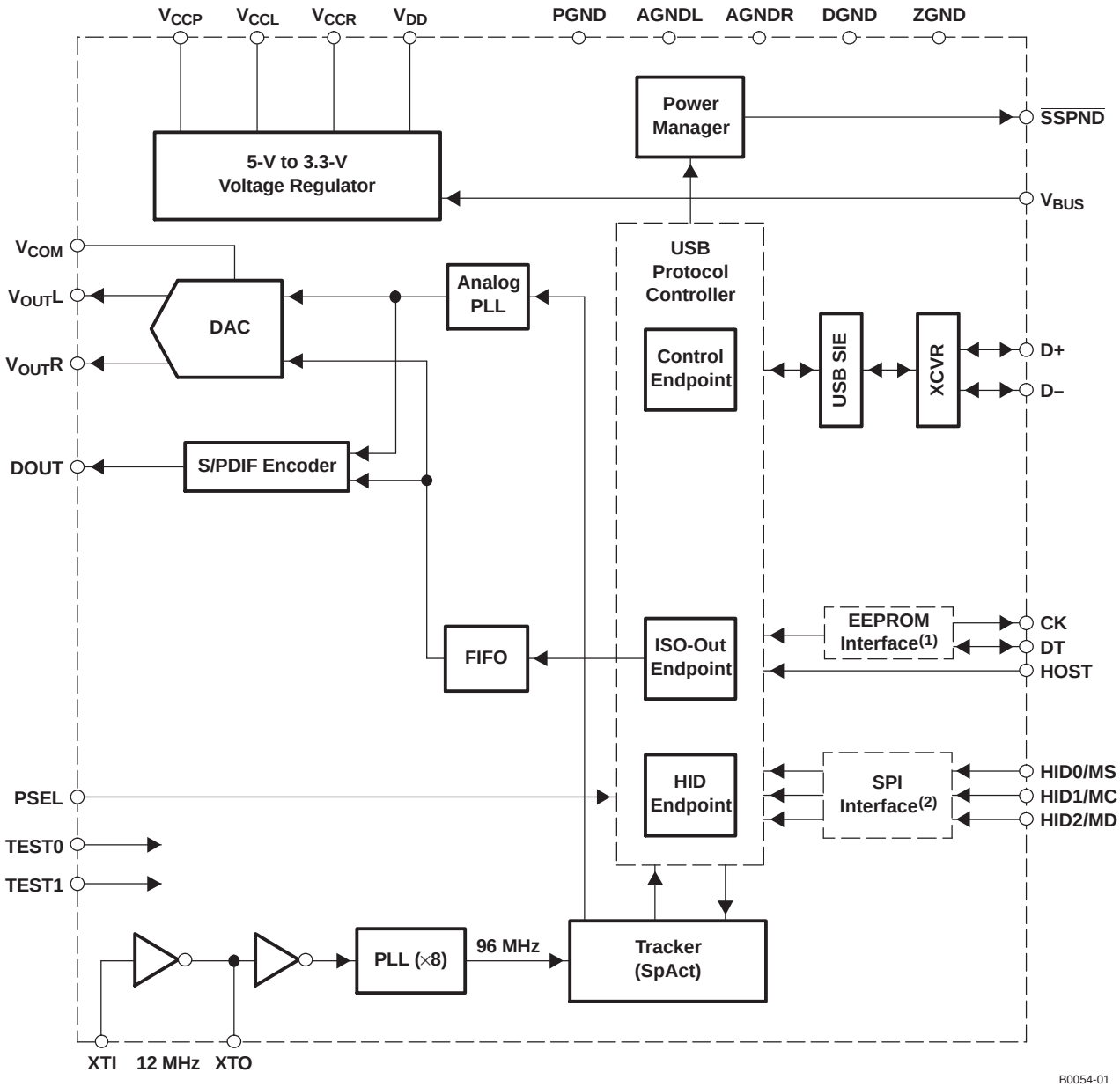
BLOCK DIAGRAM (PCM2704DB/PCM2705DB)



(1) Applies to PCM2704DB

(2) Applies to PCM2705DB

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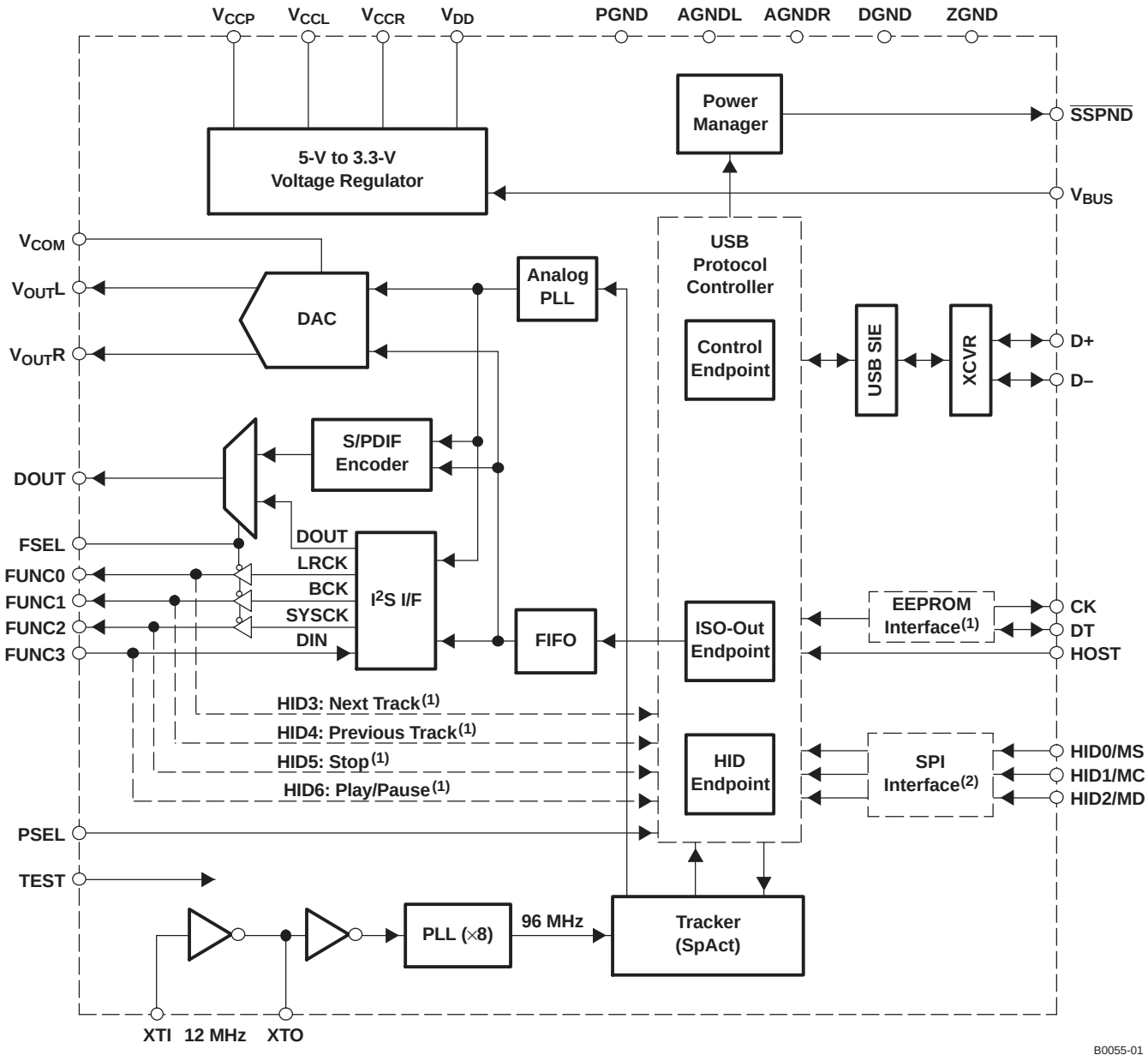
BLOCK DIAGRAM (PCM2706PJT/PCM2707PJT)



(1) Applies to PCM2706PJT

(2) Applies to PCM2707PJT

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTER

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data (unless otherwise noted).

DAC Digital Interpolation Filter Frequency Response

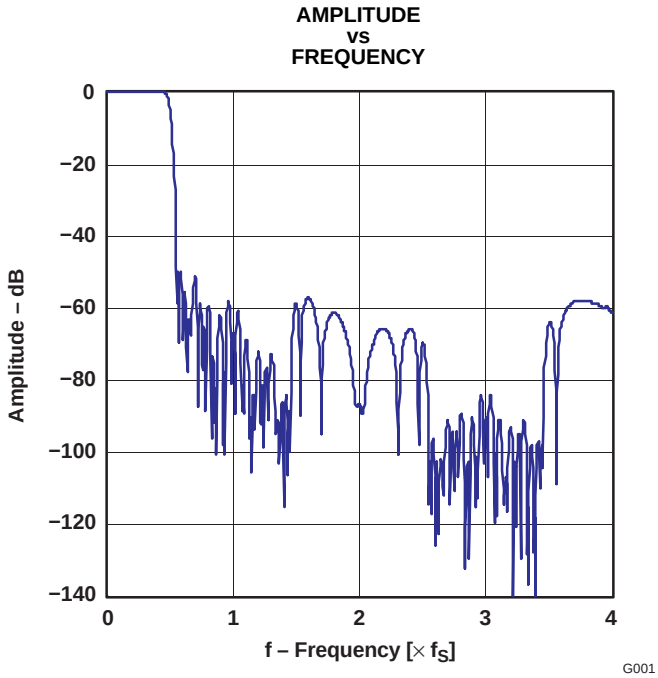


Figure 1. Frequency Response

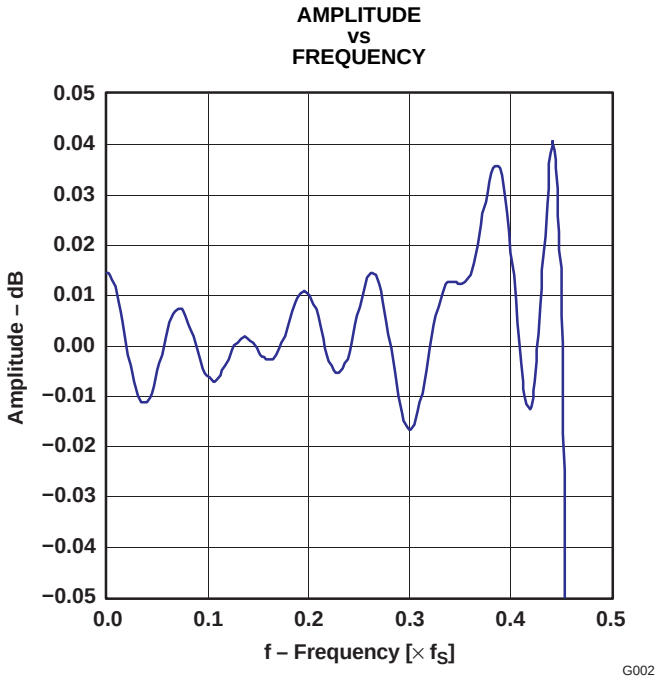


Figure 2. Pass-Band Ripple

DAC Analog Low-Pass Filter Frequency Response

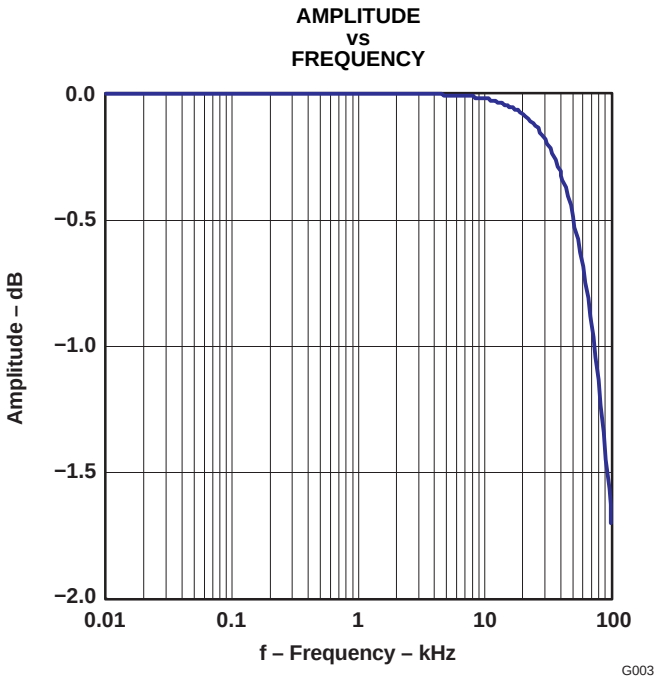


Figure 3. Pass-Band Characteristics

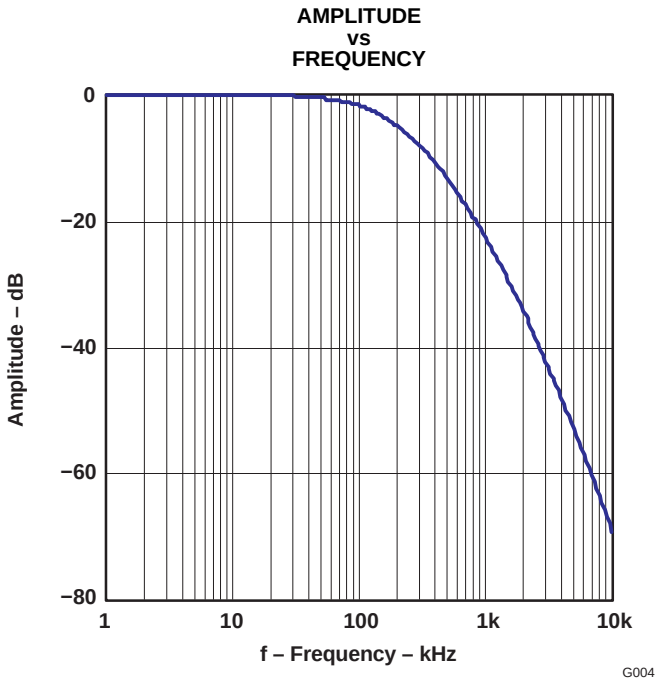


Figure 4. Stop-Band Characteristics

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TYPICAL PERFORMANCE CURVES

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data (unless otherwise noted).

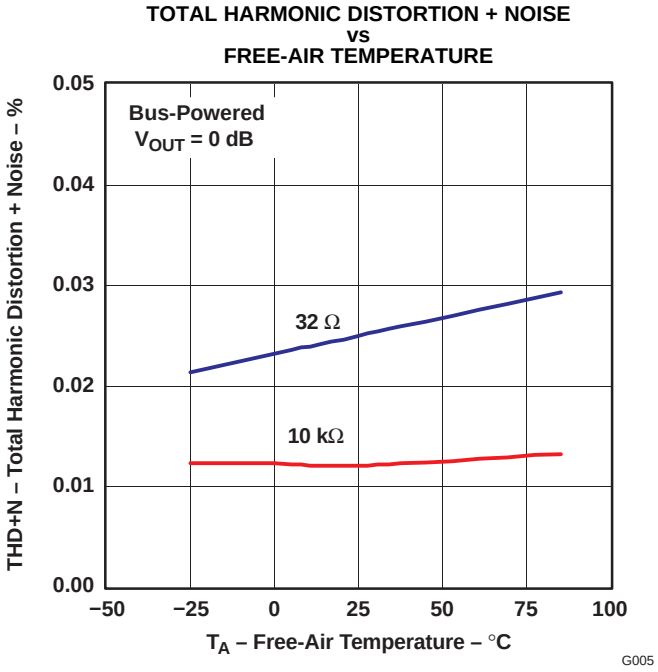


Figure 5.

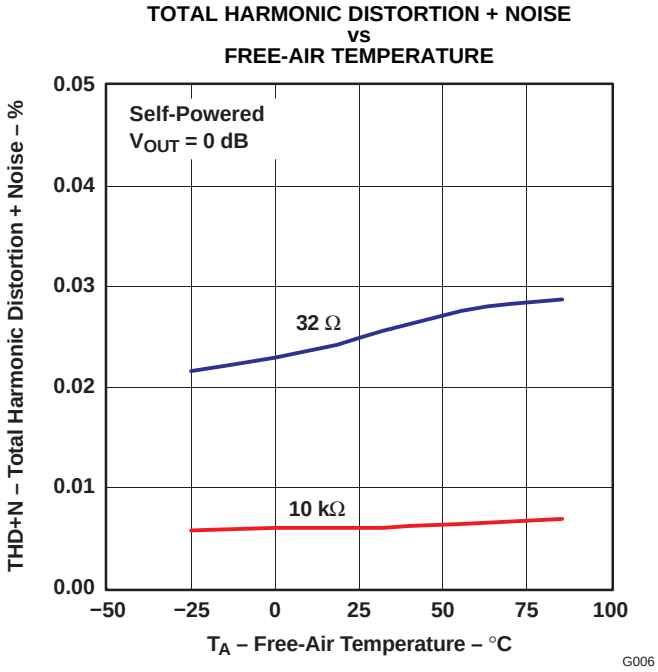
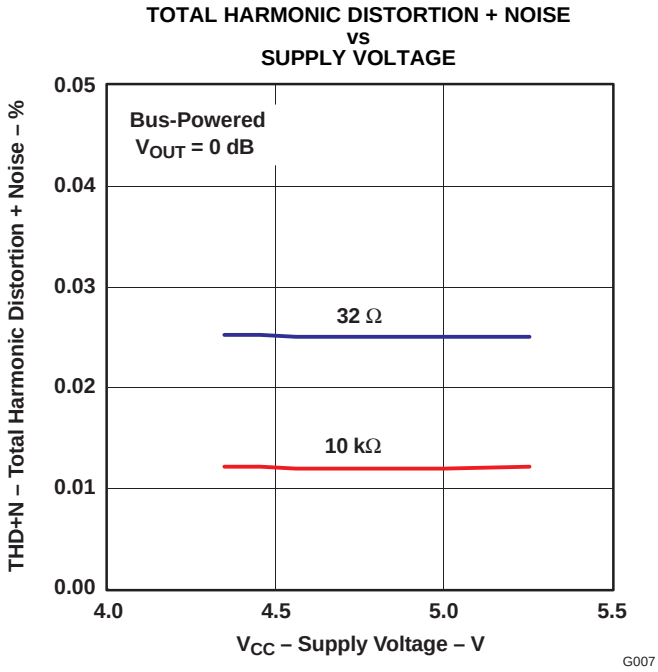


Figure 6.



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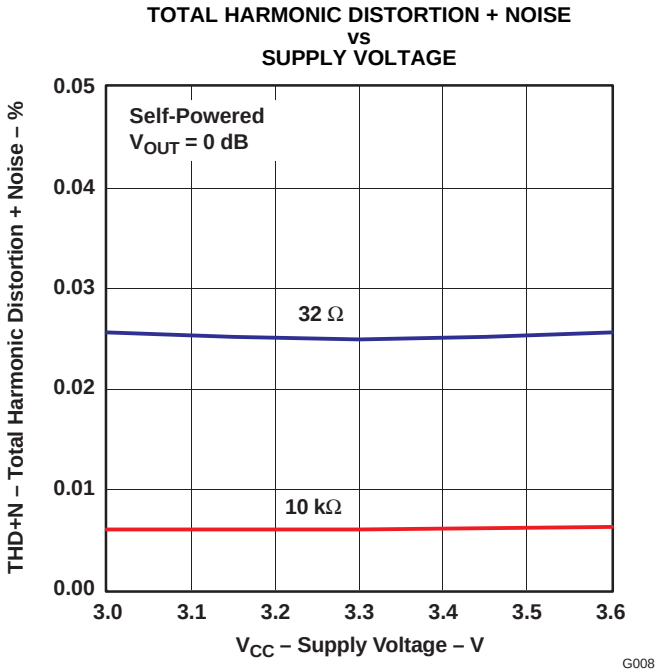

Figure 8.

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TYPICAL PERFORMANCE CURVES (continued)

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data (unless otherwise noted).

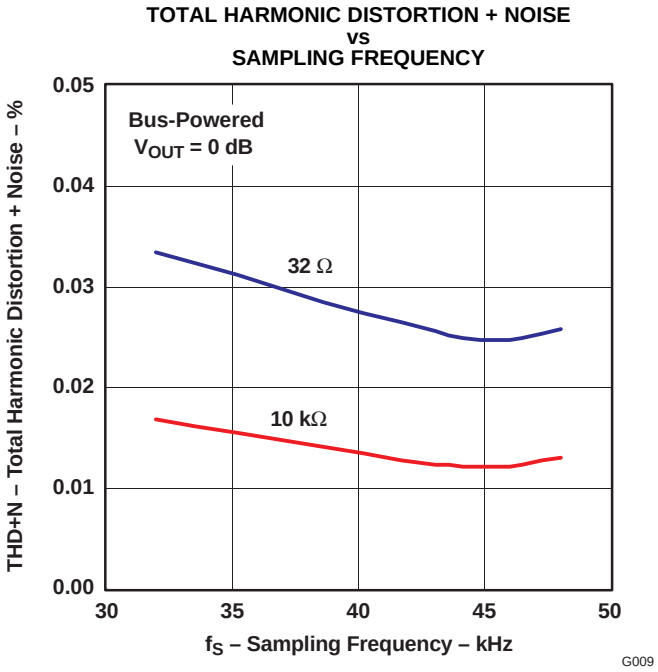

Figure 9.

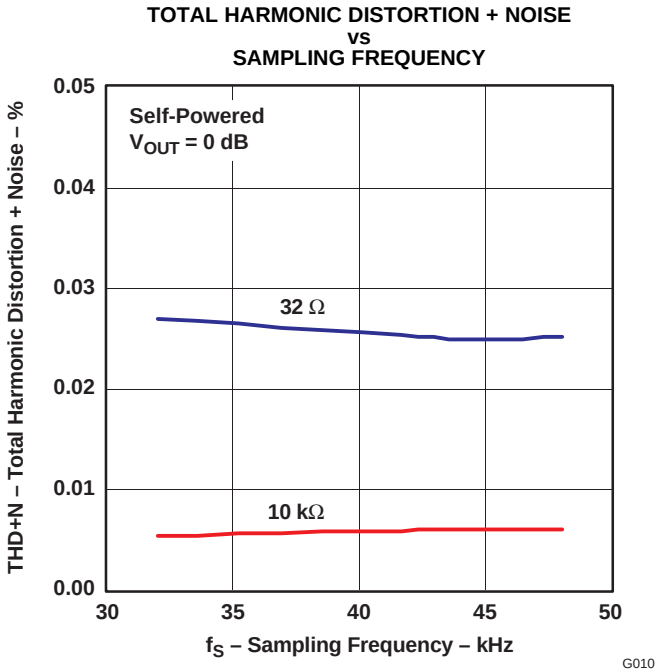

Figure 10.

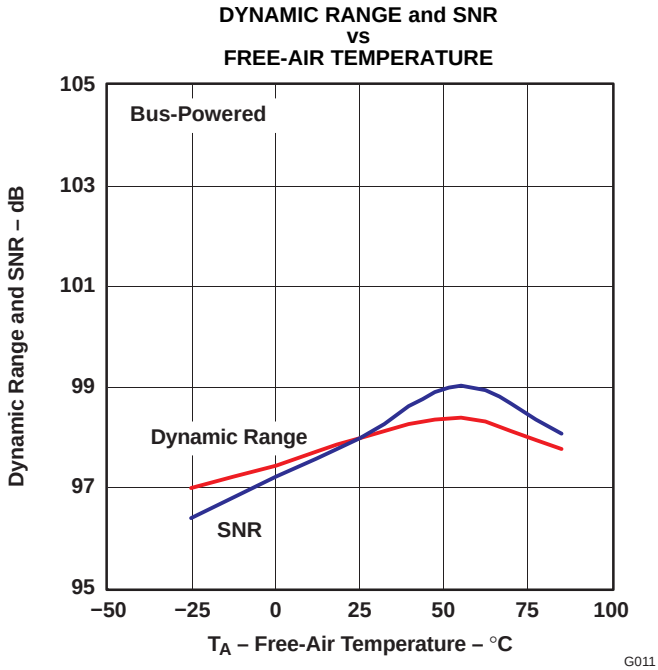

Figure 11.

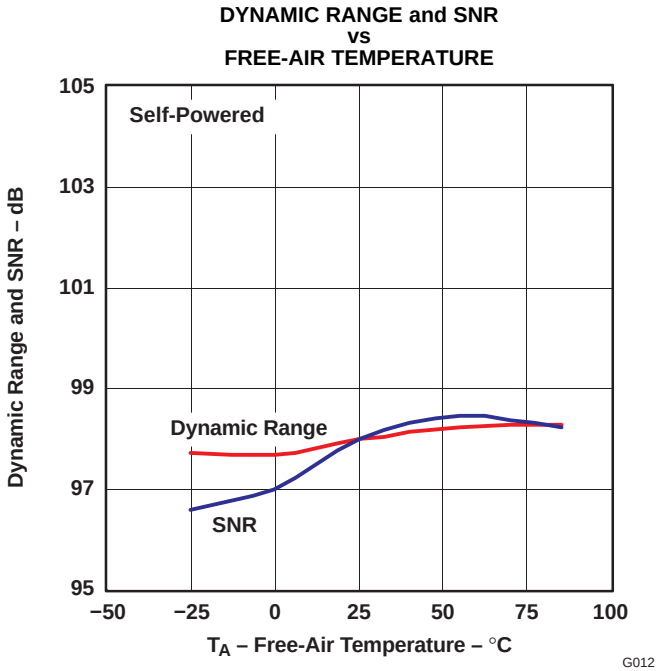

Figure 12.

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TYPICAL PERFORMANCE CURVES (continued)

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data (unless otherwise noted).

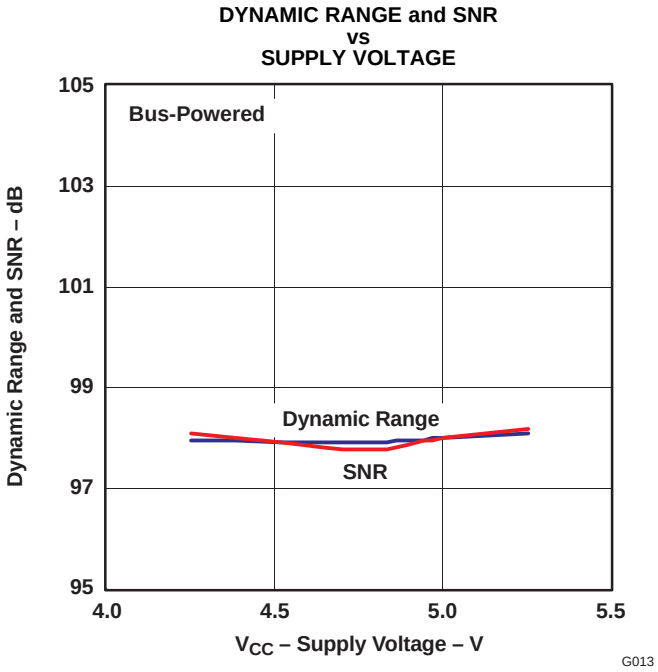

Figure 13.

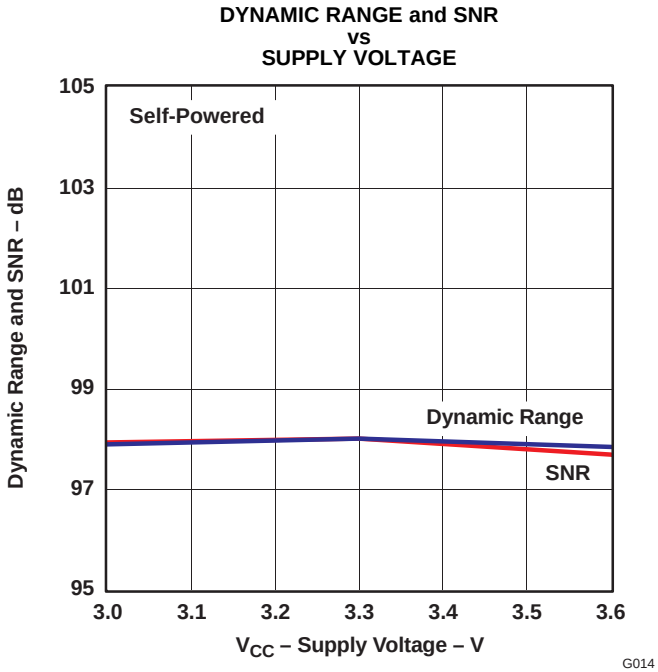

Figure 14.

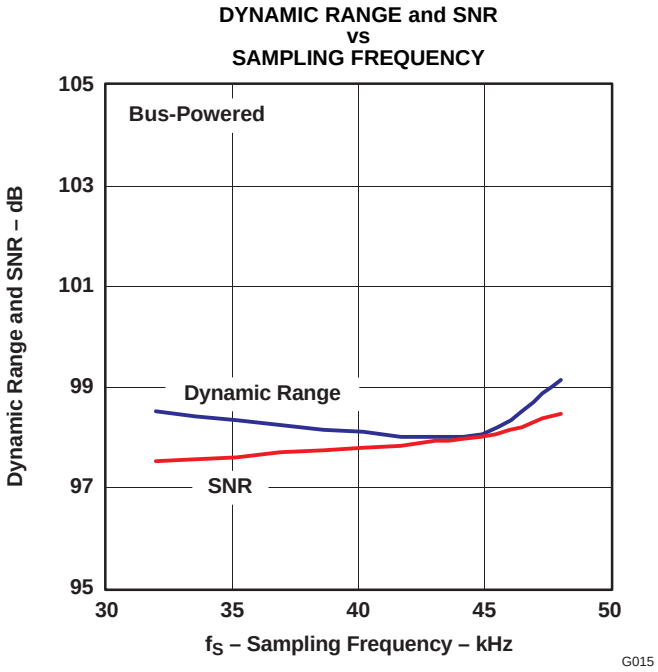

Figure 15.

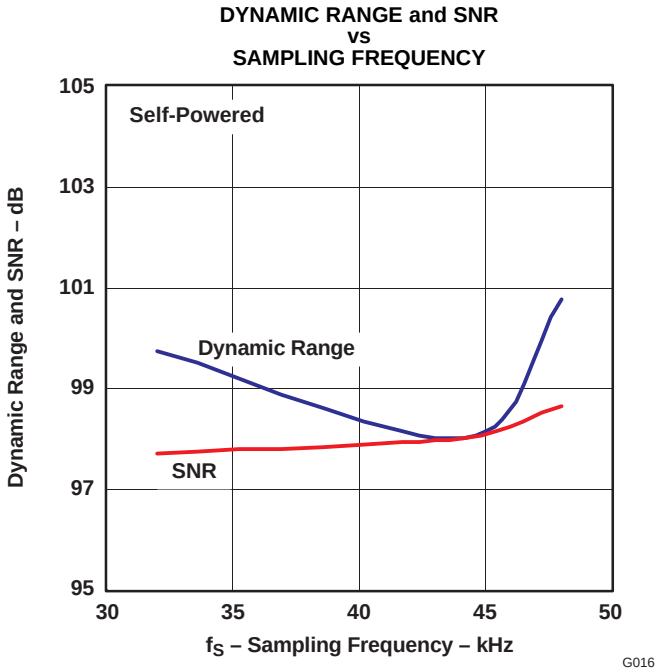

Figure 16.

TYPICAL PERFORMANCE CURVES (continued)

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data (unless otherwise noted).

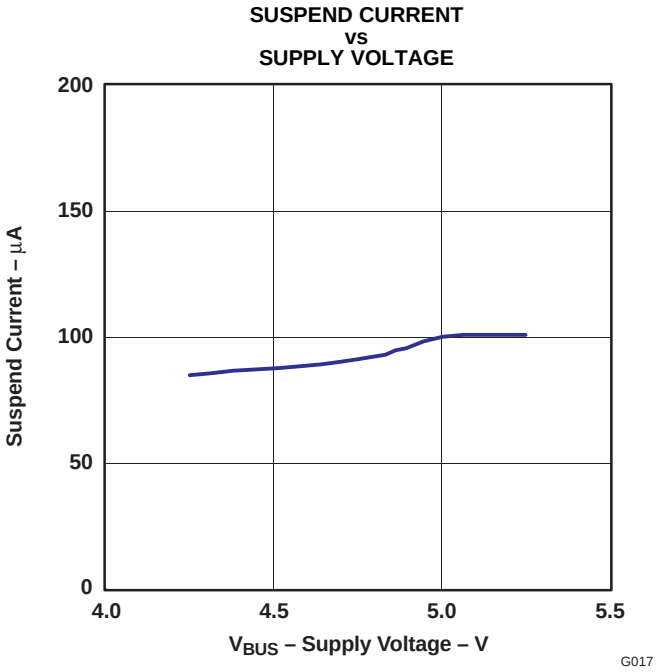

Figure 17.

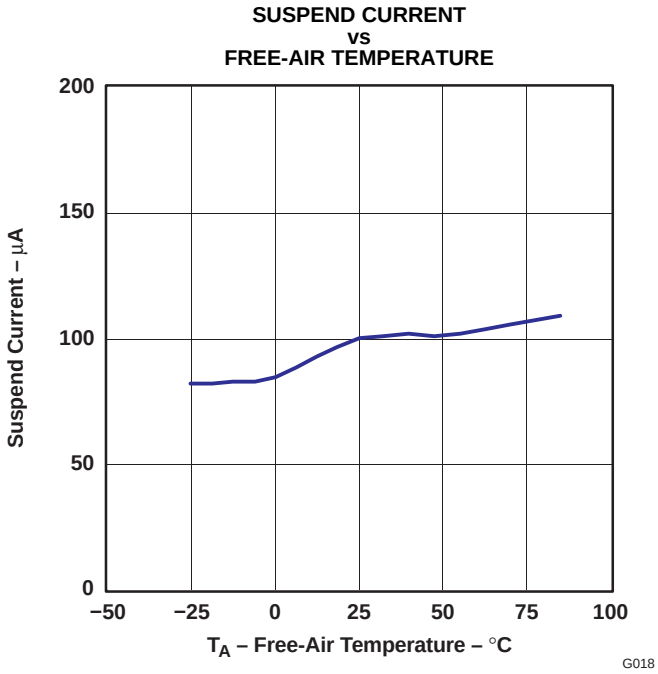

Figure 18.

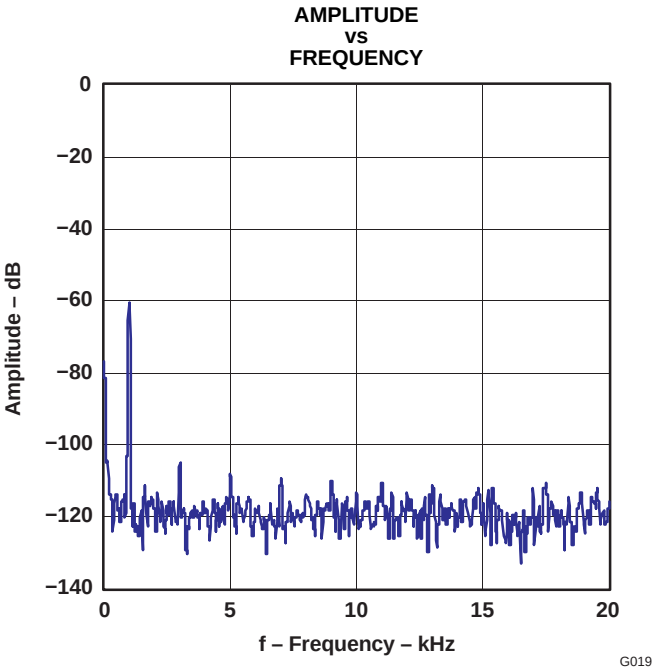

Figure 19. Output Spectrum (–60 dB, N = 8192)

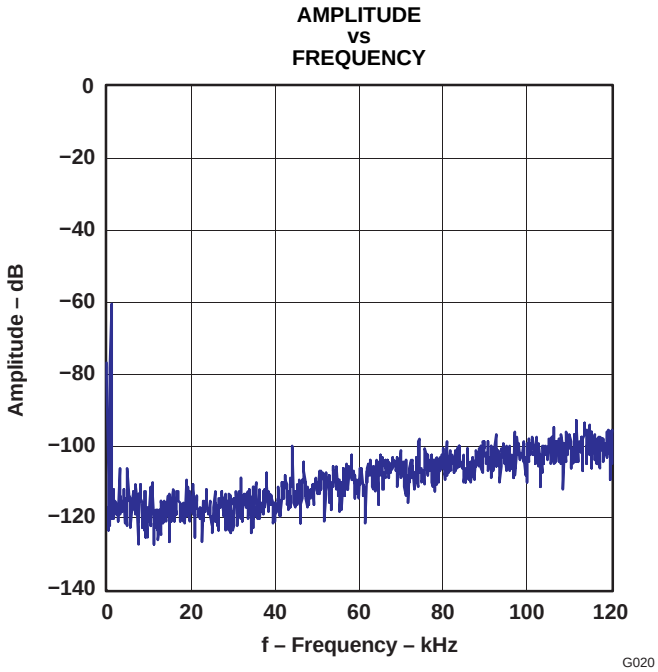

Figure 20. Output Spectrum (–60 dB, N = 8192)

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DETAILED DESCRIPTION

Clock and Reset

For both USB and audio functions, the PCM2704/5/6/7 requires a 12-MHz (±500 ppm) clock, which can be generated by the built-in oscillator using a 12-MHz crystal resonator. The 12-MHz crystal resonator must be connected to XTI (pin 28 for PCM2704/5, pin 12 for PCM2706/7) and XTO (pin 1 for PCM2704/5, pin 13 for PCM2706/7) with one large (1-MΩ) resistor and two small capacitors, the capacitance of which depends on the specified load capacitance of the crystal resonator. An external clock can be supplied from XTI (pin 28 for PCM2704/5, pin 12 for PCM2706/7). If an external clock is supplied, XTO (pin 1 for PCM2704/5, pin 13 for PCM2706/7) must be left open. Because no clock disabling pin is provided, it is not recommended to use the external clock supply. $\overline{\text{SSPND}}$ (pin 27 for PCM2704/5, pin 11 for PCM2706/7) is unable to use clock disabling.

The PCM2704/5/6/7 has an internal power-on reset circuit, and it works automatically when V_{DD} (pin 7 for PCM2704/5, pin 21 for PCM2706/7) exceeds 2 V typical (1.6 V–2.4 V), which is equivalent to V_{BUS} (pin 10 for PCM2704/5, pin 24 for PCM2706/7) exceeding 3 V typical for bus-powered applications. Approximately 700 µs is required until internal reset release.

Operation Mode Selection

The PCM2704/5/6/7 has the following mode-select pins.

Power Configuration Select/Host Detection

PSEL (pin 4 for PCM2704/5, pin 16 for PCM2706/7) is dedicated to selecting the power source. This selection affects the configuration descriptor. While in bus-powered operation, maximum power consumption from V_{BUS} is determined by HOST (pin 21 for PCM2704/5, pin 3 for PCM2706/7). For self-powered operation, HOST must be connected to V_{BUS} of the USB bus with a pulldown resistor to detect attach and detach. (To avoid excessive suspend current, the pulldown should be a high-value resistor.)

Table 1. Power Configuration Select

PSEL	DESCRIPTION
0	Self-powered
1	Bus-powered
HOST	**DESCRIPTION**
0	Detached from USB (self-powered)/100 mA (bus-powered)
1	Attached to USB (self-powered)/500 mA (bus-powered)

Function Select (PCM2706/7)

FSEL (pin 9) determines the function of FUNC0–FUNC3 (pins 4, 5, 18, and 19) and DOUT (pin17). When the I^2S interface is required, FSEL must be set to LOW. Otherwise, FSEL must be set to HIGH.

Table 2. Function Select

FSEL	DOUT	FUNC0	FUNC1	FUNC2	FUNC3
0	Data out (I^2S)	LRCK (I^2S)	BCK (I^2S)	SYSCK (I^2S)	Data in (I^2S)
1	S/PDIF data	Next track (HID) (1)	Previous track (HID) (1)	Stop (HID) (1)	Play/pause (HID) (1)

(1) Valid on the PCM2706; no function assigned on the PCM2707.

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USB Interface

Control data and audio data are transferred to the PCM2704/5/6/7 via D+ (pin 9 for PCM2704/5, pin 23 for PCM2706/7) and D– (pin 8 for PCM2704/5, pin 22 for PCM2706/7). D+ should be pulled up with a 1.5-kΩ (±5%) resistor. To avoid back voltage in self-powered operation, the device must not provide power to the pullup resistor on D+ while V_{BUS} of the USB port is inactive.

All data to/from the PCM2704/5/6/7 are transferred at full speed. The following information is provided in the device descriptor. Some parts of the device descriptor can be modified through external ROM (PCM2704/6), SPI (PCM2705/7), or internal mask ROM on request.

Table 3. Device Descriptor

DEVICE DESCRIPTOR	DESCRIPTION
USB revision	1.1 compliant
Device class	0x00 (device defined interface level)
Device subclass	0x00 (not specified)
Device protocol	0x00 (not specified)
Max packet size for endpoint 0	8 bytes
Vendor ID	0x08BB (default value, can be modified)
Product ID	0x2704/0x2705/0x2706/0x2707 (These values correspond to the model number, and the value can be modified.)
Device release number	1.0 (0x0100)
Number of configurations	1
Vendor strings	Burr-Brown from TI (default value, can be modified)
Product strings	USB Audio DAC (default value, can be modified)
Serial number	Not supported

The following information is contained in the configuration descriptor. Some parts of the configuration descriptor can be modified through external ROM (PCM2704/6), SPI (PCM2705/7), or internal mask ROM on request.

Table 4. Configuration Descriptor

CONFIGURATION DESCRIPTOR	DESCRIPTION
Interface	Three interfaces
Power attribute	0x80 or 0xC0 (bus-powered or self-powered, depending on PSEL; no remote wake up. This value can be modified.)
Max power	0x0A, 0x32 or 0xFA (20 mA for self-powered, 100 mA or 500 mA for bus-powered, depending on PSEL and HOST. This value can be modified.)

The following information is contained in the string descriptor. Some parts of the string descriptor can be modified through external ROM (PCM2704/6), SPI (PCM2705/7), or internal mask ROM on request.

Table 5. String Descriptor

STRING DESCRIPTOR	DESCRIPTION
#0	0x0409
#1	Burr-Brown from TI (default value, can be modified)
#2	USB Audio DAC (default value, can be modified)

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Device Configuration

Figure 21 illustrates the USB audio function topology. The PCM2704/5/6/7 has three interfaces. Each interface is enabled by some alternative settings.

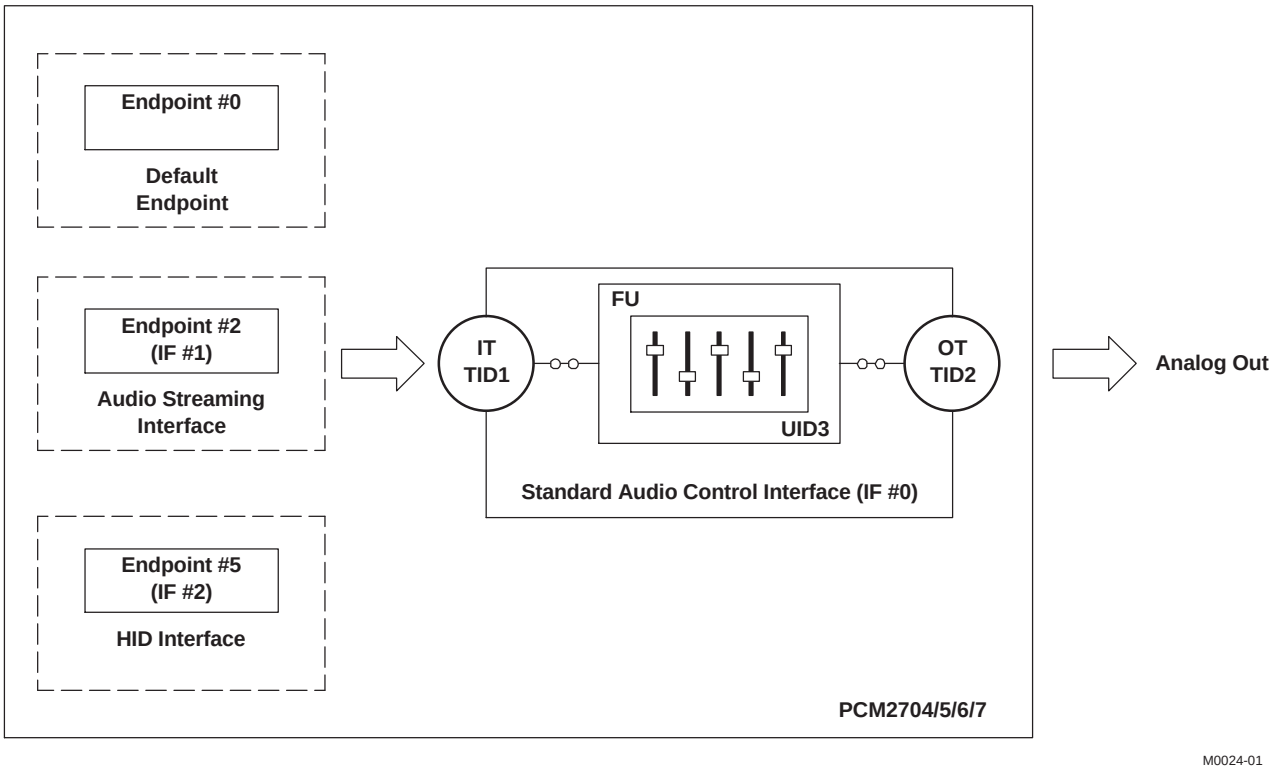

Figure 21. USB Audio Function Topology

Interface #0 (Default/Control Interface)

Interface #0 is the control interface. Setting #0 is the only possible setting for interface #0. Setting #0 describes the standard audio control interface. Audio control interface consists of a terminal. The PCM2704/5/6/7 has three terminals:

- Input terminal (IT #1) for isochronous-out stream
- Output terminal (OT #2) for audio analog output
- Feature unit (FU #3) for DAC digital attenuator

Input terminal #1 is defined as a USB stream (terminal type 0x0101). Input terminal #1 can accept two-channel audio streams constructed of left and right channels. Output terminal #2 is defined as a speaker (terminal type 0x0301). Feature unit #3 supports the following sound control features:

- Volume control
- Mute control

The built-in digital volume controller can be manipulated by an audio-class-specific request from 0 dB to –64 dB in steps of 1 dB. Changes are made by incrementing or decrementing one step (1 dB) for every $1/f_S$ time interval, until the volume level reaches the requested value. Each channel can be set to a separate value. The master volume control is not supported. A request to the master volume is stalled and ignored. The built-in digital mute controller can be manipulated by an audio-class-specific request. A master mute control request is acceptable. A mute control request to an individual channel is stalled and ignored. The digital volume control does not affect the S/PDIF and I^2S outputs (PCM2706/7).

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Interface #1 (Isochronous-Out Interface)

Interface #1 is for the audio-streaming data-out interface. Interface #1 has the following three alternative settings. Alternative setting #0 is the zero-bandwidth setting. All other alternative settings are operational settings.

ALTERNATIVE SETTING	DATA FORMAT			TRANSFER MODE	SAMPLING RATE (kHz)
00	Zero bandwidth				
01	16-bit	Stereo	2s complement (PCM)	Adaptive	32, 44.1, 48
02	16-bit	Mono	2s complement (PCM)	Adaptive	32, 44.1, 48

Interface #2 (HID Interface)

Interface #2 is the interrupt-data-in interface. Interface #2 comprises the HID consumer control device. Alternative setting #0 is the only possible setting for interface #2.

On the HID device descriptor, eight HID items are reported as follows for any model, in any configuration.

Basic HID Operation

Interface #2 can report the following three key statuses for any model. These statuses can be set by the HID0–HID2 pins (PCM2704/6) or the SPI port (PCM2705/7).

- Mute (0xE2)
- Volume up (0xE9)
- Volume down (0xEA)

Extended HID Operation (PCM2705/6/7)

By using the FUNC0–FUNC3 pins (PCM2706) or the SPI port (PCM2705/7), the following additional conditions can be reported to the host.

- Play/Pause (0xCD)
- Stop (0xB7)
- Previous (0xB6)
- Next (0xB5)

Auxiliary HID Status Report (PCM2705/7)

One additional HID status can be reported to the host though the SPI port. This status flag is defined by SPI command or external ROM. This definition must be described as on the report descriptor with a three-byte usage ID. *AL A/V Capture* (0x0193) is assigned as the default for this status flag.

Endpoints

The PCM2704/5/6/7 has three endpoints:

- Control endpoint (EP #0)
- Isochronous-out audio data-stream endpoint (EP #2)
- HID endpoint (EP #5)

The control endpoint is a default endpoint. The control endpoint is used to control all functions of the PCM2704/5/6/7 by standard USB request and USB audio-class-specific request from the host. The isochronous-out audio data-stream endpoint is an audio sink endpoint that receives the PCM audio data. The isochronous-out audio data-stream endpoint accepts the adaptive transfer mode. The HID endpoint is an interrupt-in endpoint. The HID endpoint reports HID status every 10 ms.

The HID endpoint is defined as a consumer-control device. The HID function is designed as an independent endpoint from the isochronous-out endpoint. This means that the effect of HID operation depends on host software. Typically, the HID function is used to control the primary audio-out device.

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DAC

The PCM2704/5/6/7 has a DAC that uses an oversampling technique with 128-f_S second-order multibit noise shaping. This technique provides extremely low quantization noise in the audio band, and the built-in analog low-pass filter removes the high-frequency components of the noise-shaping signal. DAC outputs through the headphone amplifier $V_{OUT}L$ and $V_{OUT}R$ can provide 12 mW at 32 Ω, as well as 1.8 V_{PP} into a 10-kΩ load.

Digital Audio Interface—S/PDIF Output

The PCM2704/5/6/7 employs S/PDIF output. Isochronous-out data from the host are encoded to S/PDIF output DOUT, as well as to DAC analog outputs $V_{OUT}L$ and $V_{OUT}R$. Interface format and timing follow the IEC-60958 standard. Monaural data are converted to the stereo format at the same data rate. S/PDIF output is not supported in the I^2S I/F enable mode. The implementation of this feature is optional. Note that it is your responsibility to determin whether to implement this feature in your product or not.

Channel Status Information

The channel status information is fixed as consumer application, PCM mode, copyright, and digital/digital converter. All other bits are fixed as 0s, except for the sample frequency, which is set automatically according to the data received through the USB.

Copyright Management

Digital audio data output always is encoded as original with SCMS control. Only one generation of digital duplication is allowed.

Digital Audio Interface—I^2S Interface Output (PCM2706/7)

The PCM2706 and PCM2707 can support the I^2S interface, which is enabled by FSEL (pin 9). In the I^2S interface enabled mode, pins 4, 18, 19, 5, and 17 are assigned as DIN, SYSCK, BCK, LRCK, and DOUT, respectively. They provide digital output/input data in the 16-bit I^2S format, which also is accepted by the internal DAC. I^2S interface format and timing are shown in Figure 22, Figure 23, and Figure 24.

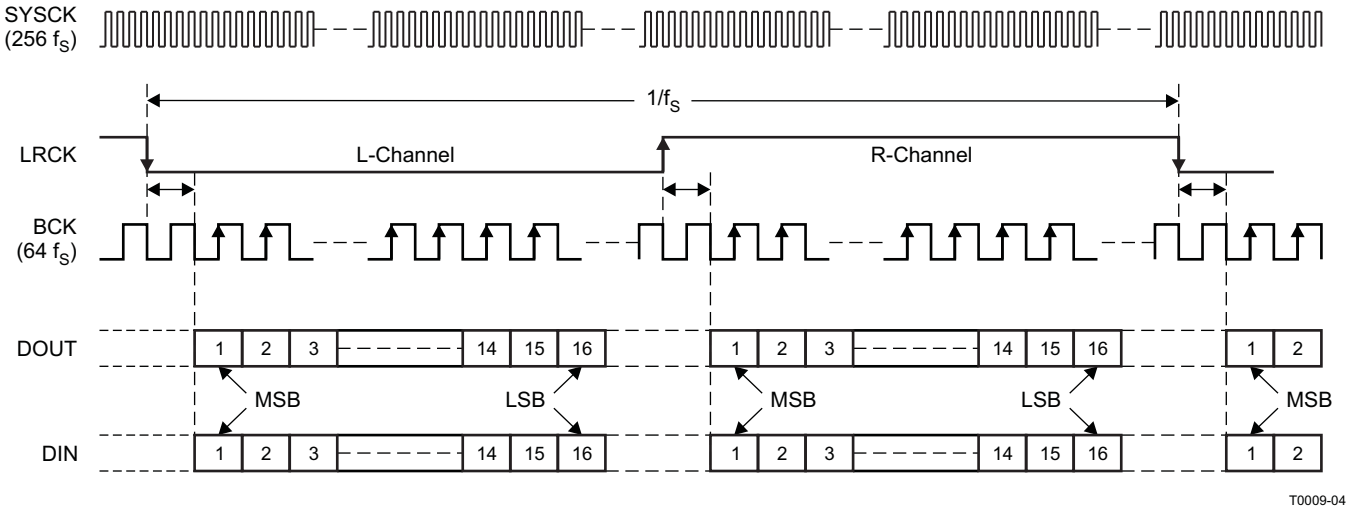
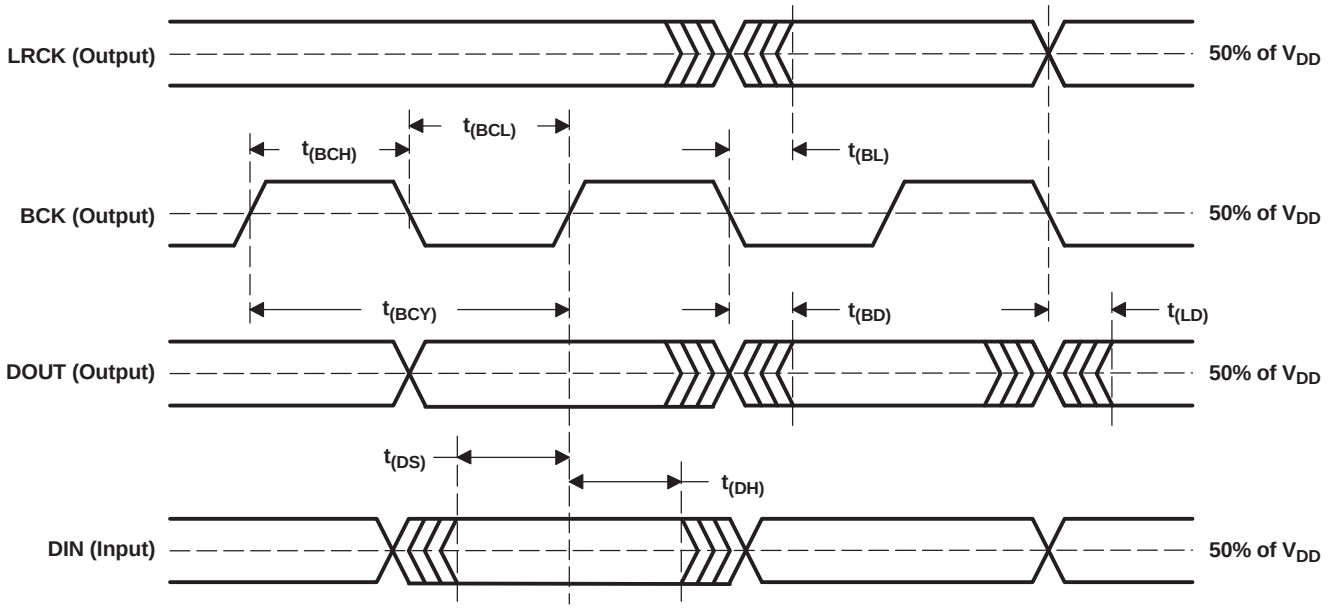


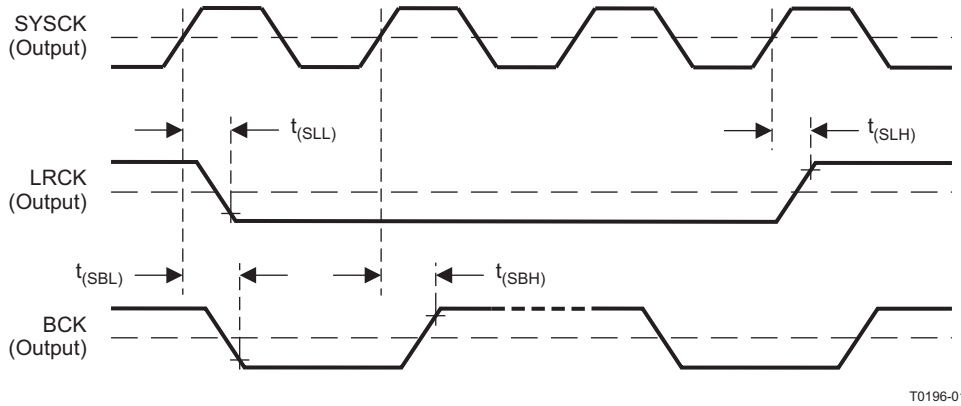
Figure 22. Audio Data Interface Format



SYMBOL	PARAMETER	MIN	MAX	UNIT
$t_{(BCY)}$	BCK pulse cycle time	300		ns
$t_{(BCH)}$	BCK pulse duration, HIGH	100		ns
$t_{(BCL)}$	BCK pulse duration, LOW	100		ns
$t_{(BL)}$	LRCK delay time from BCK falling edge	–20	40	ns
$t_{(BD)}$	DOUT delay time from BCK falling edge	–20	40	ns
$t_{(LD)}$	DOUT delay time from LRCK edge	–20	40	ns
$t_{(DS)}$	DIN setup time	20		ns
$t_{(DH)}$	DIN hold time	20		ns

NOTE: Load capacitance of LRCK, BCK, and DOUT is 20 pF.

Figure 23. Audio Interface Timing



SYMBOL	PARAMETER	MIN	MAX	UNIT
$t_{(SLL)}$, $t_{(SLH)}$	LRCK delay time from SYSCK rising edge	–5	10	ns
$t_{(SBL)}$, $t_{(SBH)}$	BCK delay time from SYSCK rising edge	–5	10	ns

NOTE: Load capacitance is 20 pF.

Figure 24. Audio Clock Timing

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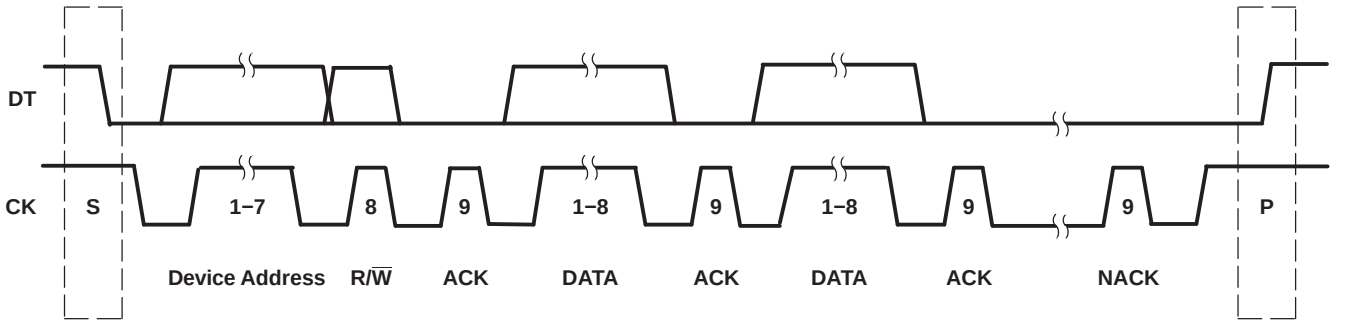
DESCRIPTOR DATA MODIFICATION

The descriptor data can be modified through I^2C port by external ROM (PCM2704/6) or through our SPI port by an SPI host such as an MCU (PCM2705/7) under a particular condition of PSEL pin and HOST pin. A condition of PSEL pin = High and HOST pin = High is needed to modify the descriptor data, and D+ pull-up must not be activated before completion of programming the descriptor data through external ROM or SPI port. The descriptor data have to be sent from external ROM to PCM2704/6 or or from SPI host to PCM2705/7 in LSB first with specified byte order. Also, the content of the power attribute and max power must be consistent with PSEL setting and power usage from USB VBUS of actual application. Therefore, the descriptor data modification in self-powered configuration (PSEL = Low) is not supported.

External ROM Descriptor (PCM2704/6)

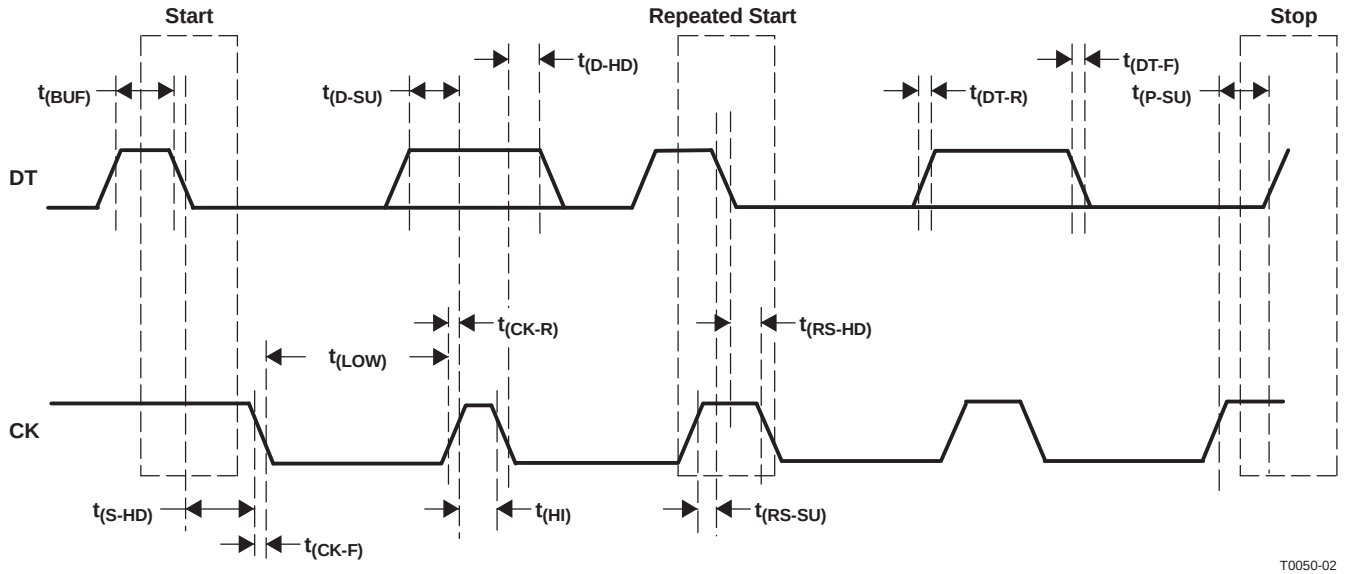
The PCM2704/6 supports an external ROM interface to override internal descriptors. Pin 3 (for PCM2704)/pin 15 (for PCM2706) is assigned as DT (serial data) and pin 2 (for PCM2704)/pin 14 (for PCM2706) is assigned as CK (serial clock) of the I^2C interface when using the external ROM descriptor. Descriptor data is transferred from the external ROM to the PCM2704/6 through the I^2C interface the first time when the device activates after power-on reset. Before completing a read of the external ROM, the PCM2704/6 replies with NACK for any USB command request from the host to the device itself. The descriptor data, which can be in external ROM, are as follows. String descriptors must be described in ANSI ASCII code (1 byte for each character). String descriptors are converted automatically to unicode strings for transmission to the host. The device address of the external ROM is fixed as 0xA0. The data must be stored from address 0x00 and must consist of 57 bytes, as described in the following items. The data bits must be sent from LSB to MSB on the I^2C bus. This means that each byte of data must be stored with its bits in reverse order. Read operation is performed at a frequency of XTI/384 (approximately 30 kHz). The content of power attribute and max power must be consistent with actual application circuit configuration (PSEL setting and actual power usage from VBUS of USB connector); otherwise, it may cause improper or unexpected PCM2704/6 operation.

- Vendor ID (2 bytes)
- Product ID (2 bytes)
- Product string (16 bytes in ANSI ASCII code)
- Vendor string (32 bytes in ANSI ASCII code)
- Power attribute (1 byte)
- Max power (1 byte)
- Auxiliary HID usage ID in report descriptor (3 bytes)



M	*M*	*M*	*S*	*S*	*M*	*S*	*M*	*S*	*M*	*M*
S	Device address	R/W	ACK	DATA	ACK	DATA	ACK	...	NACK	P

Figure 25. External ROM Read Operation



SYMBOL	PARAMETER	MIN	MAX	UNIT
$f_{(CK)}$	CK clock frequency		100	kHz
$t_{(BUF)}$	Bus free time between a STOP and a START condition	4.7		µs
$t_{(LOW)}$	Low period of the CK clock	4.7		µs
$t_{(HI)}$	High period of the CK clock	4		µs
$t_{(RS-SU)}$	Setup time for START/repeated START condition	4.7		µs
$t_{(S-HD)}$ $t_{(RS-HD)}$	Hold time for START/repeated START condition	4		µs
$t_{(D-SU)}$	Data setup time	250		ns
$t_{(D-HD)}$	Data hold time	0	900	ns
$t_{(CK-R)}$	Rise time of CK signal	20 + 0.1 C_B	1000	ns
$t_{(CK-F)}$	Fall time of CK signal	20 + 0.1 C_B	1000	ns
$t_{(DT-R)}$	Rise time of DT signal	20 + 0.1 C_B	1000	ns
$t_{(DT-F)}$	Fall time of DT signal	20 + 0.1 C_B	1000	ns
$t_{(P-SU)}$	Setup time for STOP condition	4		µs
C_B	Capacitive load for DT and CK lines		400	pF
V_{NH}	Noise margin at HIGH level for each connected device (including hysteresis)	0.2 V_{DD}		V

Figure 26. External ROM Read Interface Timing Requirements

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External ROM Example

Here is an example of external ROM data, with an explanation of the example following the data.

```
0xBB, 0x08, 0x04, 0x27,
0x50, 0x72, 0x6F, 0x64, 0x75, 0x63, 0x74, 0x20, 0x73, 0x74, 0x72, 0x69, 0x6E, 0x67, 0x73, 0x2E,
0x56, 0x65, 0x6E, 0x64, 0x6F, 0x72, 0x20, 0x73, 0x74, 0x72, 0x69, 0x6E, 0x67, 0x73, 0x20, 0x61,
0x72, 0x65, 0x20, 0x70, 0x6C, 0x61, 0x63, 0x65, 0x64, 0x20, 0x68, 0x65, 0x72, 0x65, 0x2E, 0x20,
0x80,
0x7D,
0x0A, 0x93, 0x01
```

The data are stored beginning at address 0x00.

Vendor ID: 0x08BB

Product ID: 0x2704

Product string: Product strings (16 bytes).

Vendor string: Vendor strings are placed here (32 bytes, 31 visible characters are followed by 1 space).

Power attribute (bmAttribute): 0x80 (Bus-powered).

Max power (maxPower): 0x7D (250 mA).

Auxiliary HID usage ID: 0x0A, 0x93, 0x01 (AL A/V capture).

Note that the data bits must be sent from LSB to MSB on the I^2C bus. This means that each data byte must be stored with its bits in reverse order.

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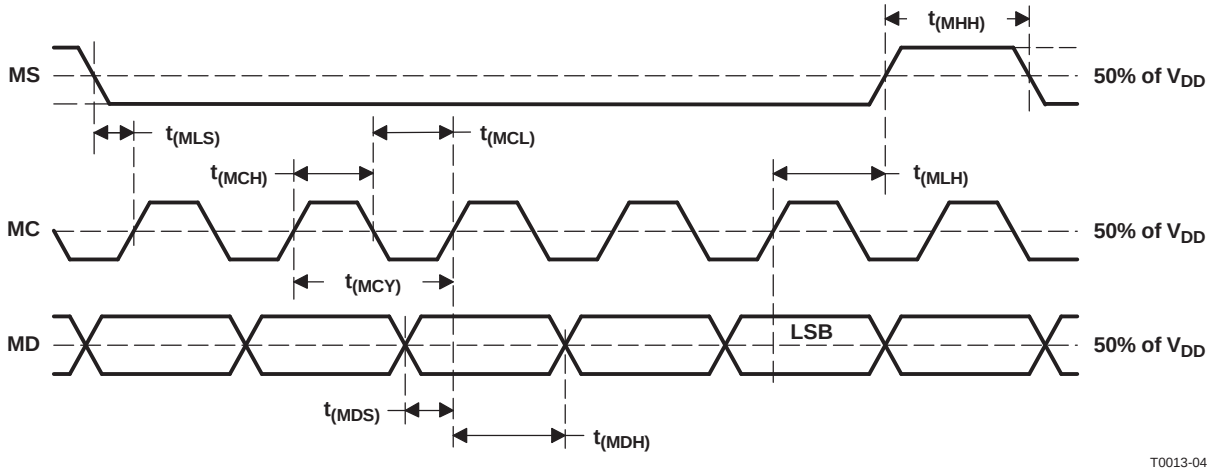
Serial Programming Interface (PCM2705/7)

The PCM2705/7 supports the serial programming interface (SPI) to program the descriptor and to set the HID state. Descriptor data are described in the *SubSec1 8.8External ROM Descriptor* section.



SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
$t_{(MCY)}$	MC pulse cycle time	100			ns
$t_{(MCL)}$	MC low-level time	50			ns
$t_{(MCH)}$	MC high-level time	50			ns
$t_{(MHH)}$	MS high-level time	100			ns
$t_{(MLS)}$	MS falling edge to MC rising edge	20			ns
$t_{(MLH)}$	MS hold time	20			ns
$t_{(MDH)}$	MD hold time	15			ns
$t_{(MDS)}$	MD setup time	20			ns

Figure 27. SPI Timing Diagram

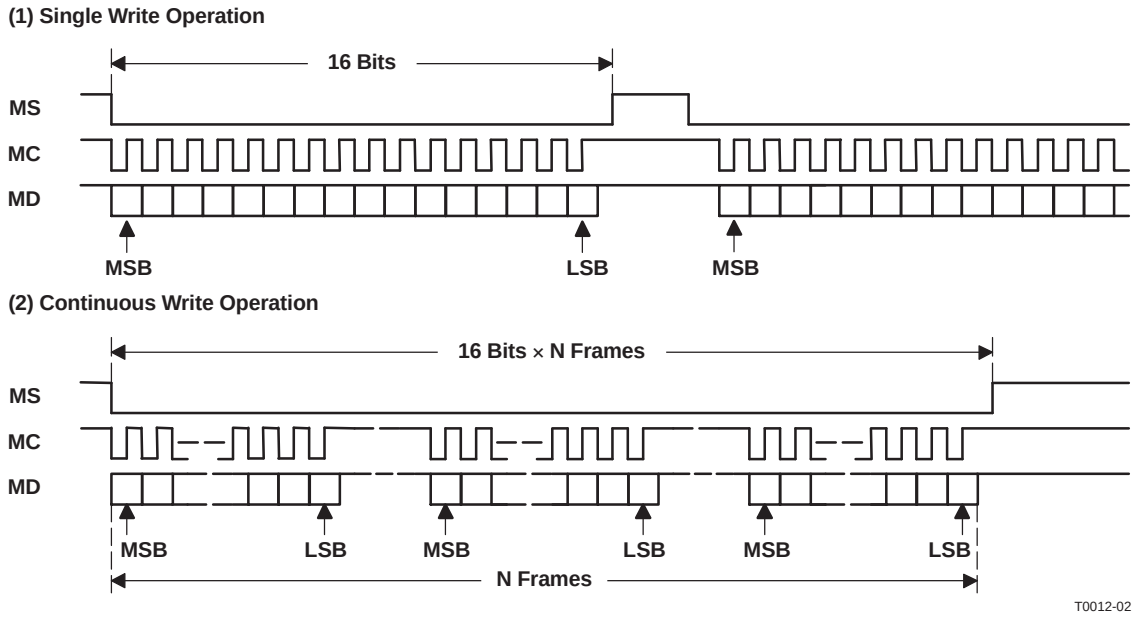


Figure 28. SPI Write Operation

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SPI Register (PCM2705/7)

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	ST	0	ADDR	0	D0	D1	D2	D3	D4	D5	D6	D7

D[7:0] Function of the lower 8 bits depends on the value of the ST (B11) bit.

ST = 0 (HID status write)

- D7 Reports MUTE HID status to the host (active high)
- D6 Reports volume-up HID status to the host (active high)
- D5 Reports volume-down HID status to the host (active high)
- D4 Reports next-track HID status to the host (active high)
- D3 Reports previous-track HID status to the host (active high)
- D2 Reports stop HID status to the host (active high)
- D1 Reports play/pause HID status to the host (active high)
- D0 Reports extended command status to the host (active high)

ST = 1 (ROM data write)

- D[7:0] Internal descriptor ROM data, D0:LSB, D7:MSB

The content of power attribute and max power must be consistent with the actual application circuit configuration (PSEL setting and actual power usage from VBUS of USB connector); otherwise, it may cause improper or unexpected PCM2705/7 operation.

ADDR Starts write operation for internal descriptor reprogramming (active high)

This bit resets descriptor ROM address counter and indicates following words should be ROM data (described in the *External ROM Example* section). 456 bits of ROM data must be continuously followed after this bit has been asserted. The data bits must be sent from LSB (D0) to MSB (D7).

To set ADDR high, ST must be set low. Note that the lower 8 bits are still active as an HID status write when ST is set low.

ST Determines the function of the lower 8-bit data as follows:

0: HID status write

1: Descriptor ROM data write

Table 6. Functionality of ST and ADDR Bit Combinations

ST	ADDR	FUNCTION
0	0	HID status write
0	1	HID status write and descriptor ROM address reset
1	0	Descriptor ROM data write
1	1	Reserved

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USB Host Interface Sequence

Power-On, Attach, and Playback Sequence

The PCM2704/5/6/7 is ready for setup when the reset sequence has finished and the USB bus is attached. After a connection has been established by setup, the PCM2704/5/6/7 is ready to accept USB audio data. While waiting for the audio data (idle state), the analog output is set to bipolar zero (BPZ).

When receiving the audio data, the PCM2704/5/6/7 stores the first audio packet, which contains 1 ms of audio data, into the internal storage buffer. The PCM2704/5/6/7 starts playing the audio data after detecting the next subsequent start-of-frame (SOF) packet.

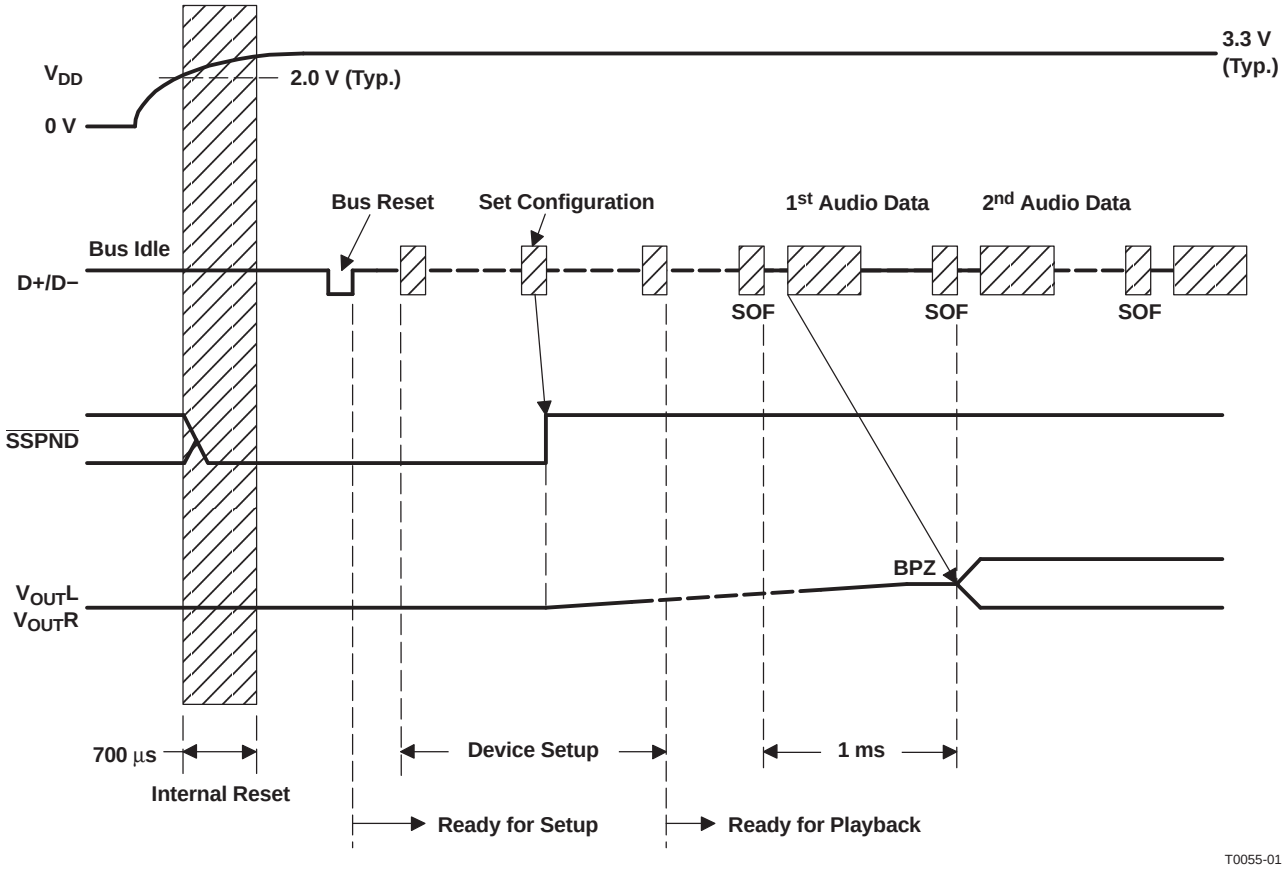

Figure 29. Initial Sequence

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Play, Stop, and Detach Sequence

When the host finishes or aborts the playback, the PCM2704/5/6/7 stops playing after completing the output of the last audio data.

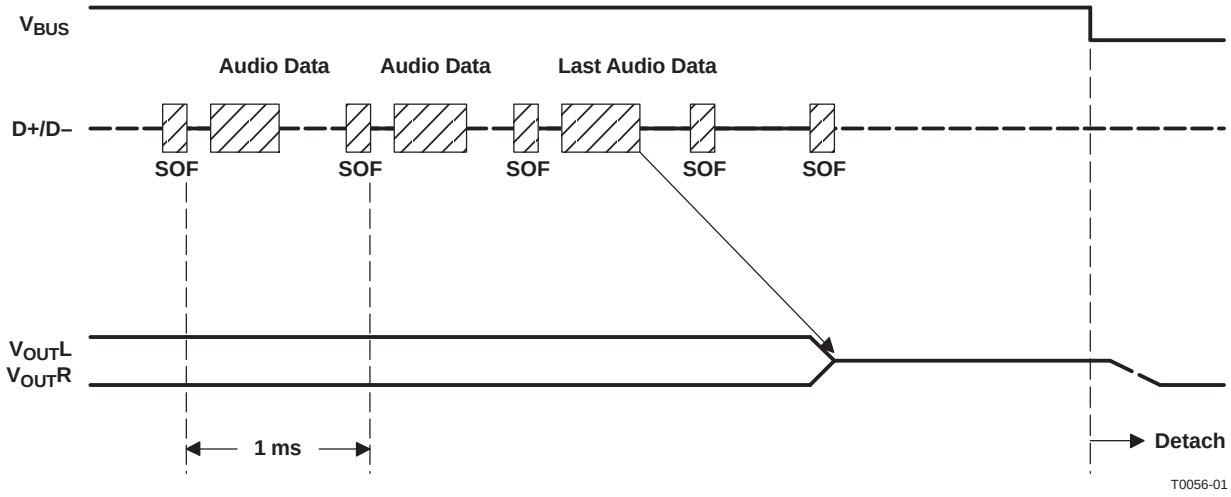


Figure 30. Play, Stop, and Detach

Suspend and Resume Sequence

The PCM2704/5/6/7 enters the suspend state after the USB bus has been in a constant idle state for approximately 5 ms. While the PCM2704/5/6/7 is in the suspend state, $\overline{\text{SSPND}}$ flag (pin 27 for PCM2704/5, pin 11 for PCM2706/7) is asserted. The PCM2704/5/6/7 wakes up immediately when detecting the non-idle state on the USB bus.

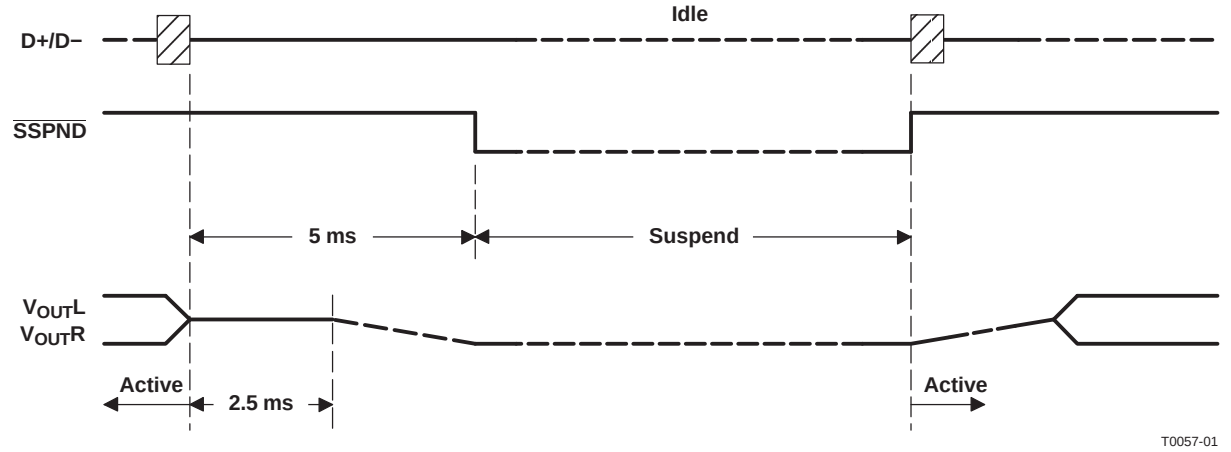
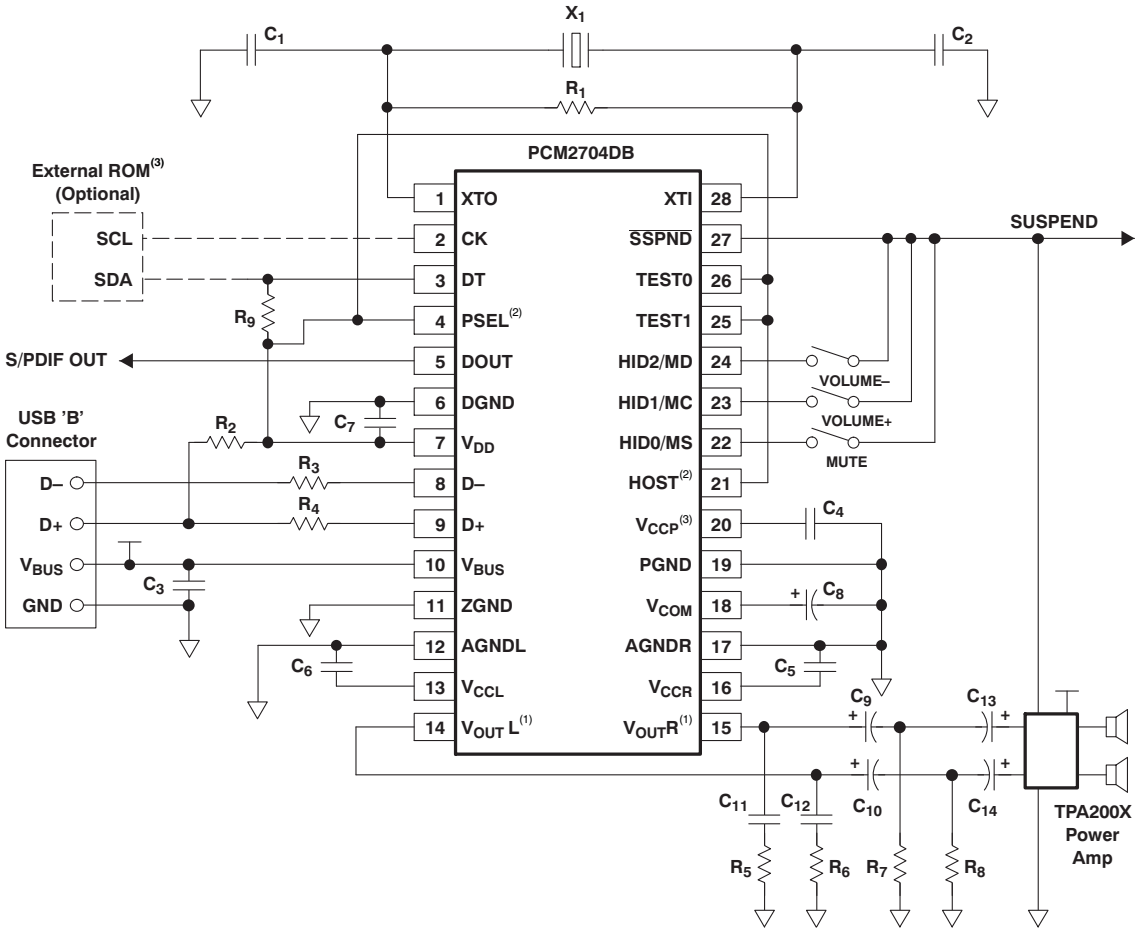


Figure 31. Suspend and Resume

Typical Circuit Connection 1 (Example of USB Speaker)

Figure 32 illustrates a typical circuit connection for an internal-descriptor, bus-powered, 500-mA application.



NOTE: X_1: 12-MHz crystal resonator. C_1, C_2: 10-pF to 33-pF capacitor (depending on load capacitance of crystal resonator). C_3-C_7: 1-µF ceramic capacitor. C_8: 10-µF electrolytic capacitor. C_9, C_{10}: 100-µF electrolytic capacitor (depending on tradeoff between required frequency response and discharge time for resume). C_{11}, C_{12}: 0.022-µF ceramic capacitor. C_{13}, C_{14}: 1-µF electrolytic capacitor. R_1: 1 MΩ resistor. R_2, R_9: 1.5 kΩ resistors. R_3, R_4: 22 Ω resistors. R_5, R_6: 16 Ω resistors. R_7, R_8: 330 Ω resistors (depending on tradeoff between required THD performance and pop-noise level for suspend).

(1) Output impedance of $V_{OUT}L$ and $V_{OUT}R$ during suspend mode or lack of power supply is 26 kΩ ±20%, which is the discharge path for C_9 and C_{10}.

(2) Descriptor programming through external ROM is only available when PSEL and HOST are high.

(3) External ROM power can be supplied from $V_{CC}P$, but any other active component must not use V_{CCP}, V_{CCL}, V_{CCR}, or V_{DD} as a power source.

Figure 32. Bus-Powered Application

NOTE:

The circuit illustrated in Figure 32 is for information only. The entire board design should be considered to meet the USB specification as a USB-compliant product.

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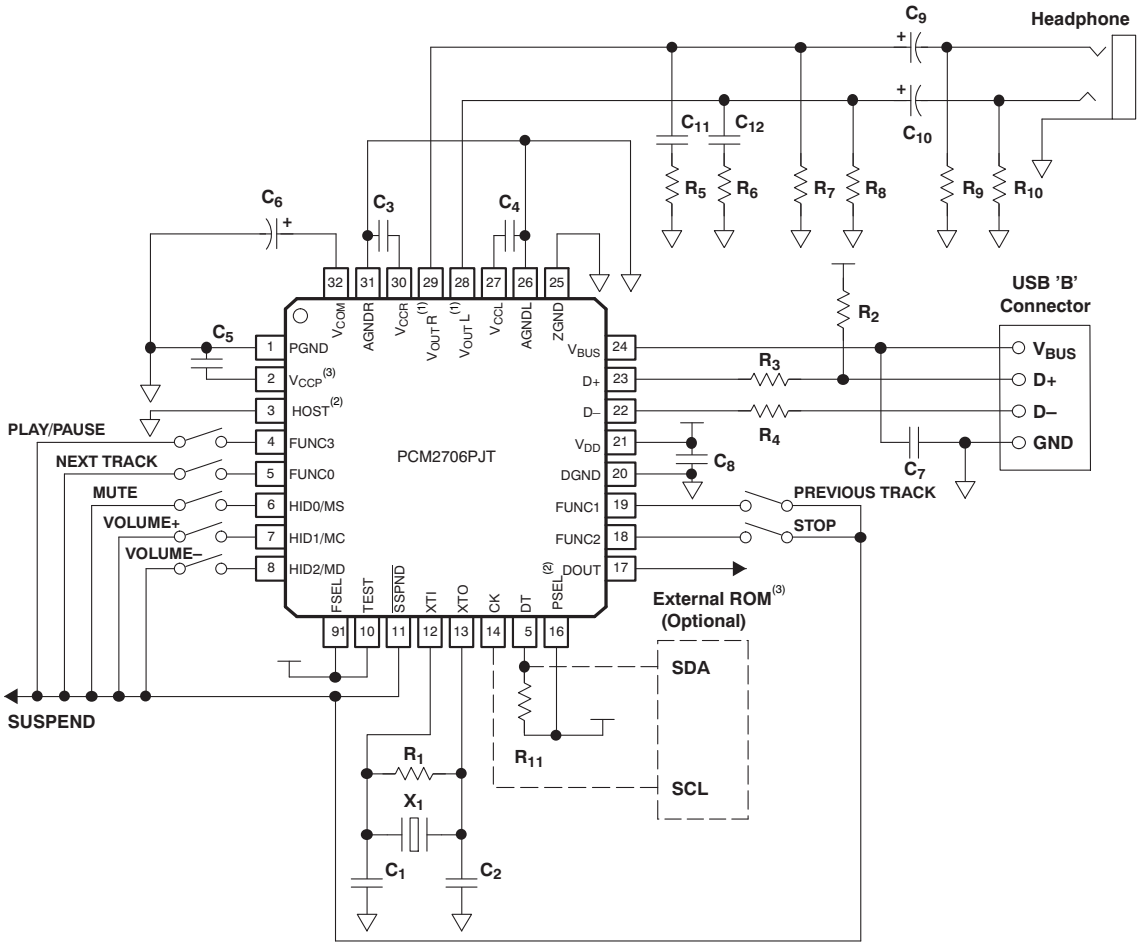
Typical Circuit Connection 2 (Example of Remote Headphone)

Figure 33 illustrates a typical circuit connection for a bus-powered, 100-mA headphone with seven HIDs.



NOTE: X_1: 12-MHz crystal resonator. C_1, C_2: 10-pF to 33-pF capacitors (depending on load capacitance of crystal resonator). C_3-C_5, C_7, C_8: 1-µF ceramic capacitors. C_6: 10-µF electrolytic capacitor. C_9, C_{10}: 100-µF electrolytic capacitors (depending on required frequency response). C_{11}, C_{12}: 0.022-µF ceramic capacitors. R_1: 1 MΩ resistor. R_2, R_{11}: 1.5 kΩ resistors. R_3, R_4: 22 Ω resistors. R_5, R_6: 16 Ω resistors. R_7-R_{10}: 3.3 kΩ resistors.

(1) Output impedance of $V_{OUT}L$ and $V_{OUT}R$ during suspend mode or lack of power supply is 26 kΩ ±20%, which is the discharge path for C_9 and C_{10}.

(2) Descriptor programming through external ROM is only available when PSEL and HOST are high.

(3) External ROM power can be supplied from V_{CCP}, but any other active component must not use V_{CCP}, V_{CCL}, V_{CCR}, or V_{DD} as a power source.

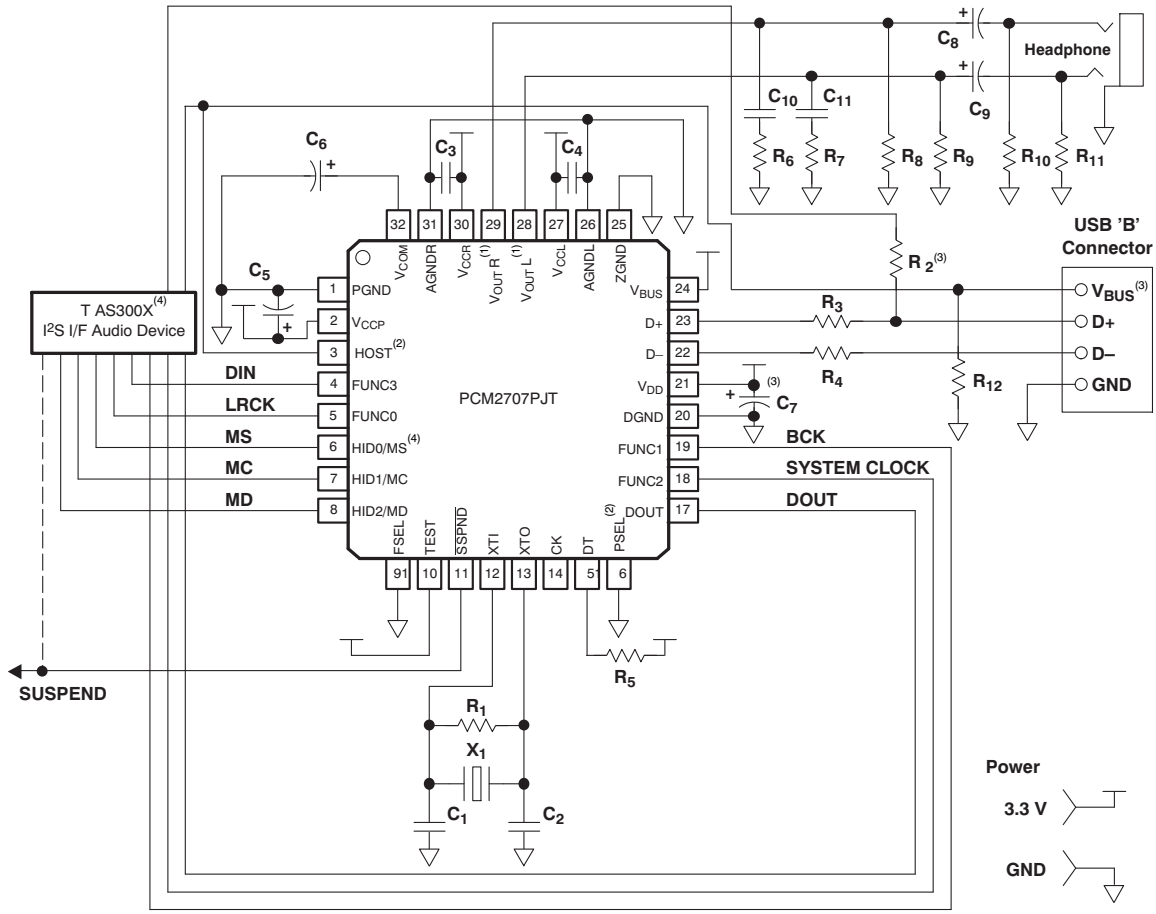
Figure 33. Bus-Powered Application

NOTE:

The circuit illustrated in Figure 33 is for information only. The entire board design should be considered to meet the USB specification as a USB-compliant product.

Typical Circuit Connection 3 (Example of DSP Surround Processing Amp)

Figure 34 illustrates a typical circuit connection for an I²S- and SPI-enabled self-powered application.



NOTE: X_1: 12-MHz crystal resonator. C_1, C_2: 10-pF to 33-pF capacitors (depending on load capacitance of crystal resonator). C_3, C_4: 1-µF ceramic capacitors. C_5, C_7: 0.1-µF ceramic capacitor and 10-µF electrolytic capacitor. C_6: 10-µF electrolytic capacitors. C_8, C_9: 100-µF electrolytic capacitors (depending on required frequency response). C_{10}, C_{11}: 0.022-µF ceramic capacitors. R_1, R_{12}: 1 MΩ resistors. R_2, R_5: 1.5 kΩ resistors. R_3, R_4: 22 Ω resistors. R_6, R_7: 16 Ω resistors. R_8-R_{11}: 3.3 kΩ resistors.

(1) Output impedance of $V_{OUT}L$ and $V_{OUT}R$ during suspend mode or lack of power supply is 26 kΩ ±20%, which is the discharge path for C_8 and C_9.

(2) Descriptor programming through SPI is only available when PSEL and HOST are high.

(3) D+ pull-up must not be activated (HIGH: 3.3V) while the device is detached from USB or power supply is not applied on V_{DD} and $V_{CC}X$. VBUS of USB (5V) can be used to detect USB power status.

(4) MS must be high until the PCM2707 power supply is ready and the SPI host (DSP) is ready to send data. Also, the SPI host must handle the D+ pull-up if the descriptor is programmed through the SPI. D+ pull-up must not be activated (HIGH = 3.3 V) before programming of the PCM2707 through the SPI is complete.

Figure 34. Self-Powered Application

NOTE:

The circuit illustrated in Figure 34 is for information only. The entire board design should be considered to meet the USB specification as a USB-compliant product.

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APPENDIX

Operating Environment

For current information on the PCM2704/2705/2706/2707 operating environment, see the *Updated Operating Environments for PCM270X, PCM290X Applications* application report, SLAA374, available through the TI web site at www.ti.com.

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (November 2007) to Revision F **Page**

- Added new feature 1
- Moved text to end of Digital Audio Interface-S/PDIF Output section 19
- Added Descriptor Data Modification paragraph 21
- Deleted *HOST* from list of circuit configuration terms 21
- Deleted *HOST* from list of circuit configuration terms 25
- Added notes to Figure 32, Figure 33, and Figure 34 for clarifying requirement of descriptor programing. 28

Changes from Revision D (December 2006) to Revision E **Page**

- Deleted operating environment information from data sheet and added reference to application report 31

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PCM2704DB	Active	Production	SSOP (DB) | 28	47 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM2704
PCM2704DB.B	Active	Production	SSOP (DB) | 28	47 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM2704
PCM2704DBG4	Active	Production	SSOP (DB) | 28	47 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM2704
PCM2704DBG4.B	Active	Production	SSOP (DB) | 28	47 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM2704
PCM2704DBR	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM2704
PCM2704DBR.B	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM2704
PCM2705DB	Active	Production	SSOP (DB) | 28	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM2705
PCM2705DB.B	Active	Production	SSOP (DB) | 28	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM2705
PCM2705DBG4	Active	Production	SSOP (DB) | 28	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM2705
PCM2705DBR	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM2705
PCM2705DBR.B	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM2705
PCM2706PJT	Active	Production	TQFP (PJT) | 32	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM2706
PCM2706PJT.B	Active	Production	TQFP (PJT) | 32	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM2706
PCM2706PJTR	Active	Production	TQFP (PJT) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM2706
PCM2706PJTR.B	Active	Production	TQFP (PJT) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM2706

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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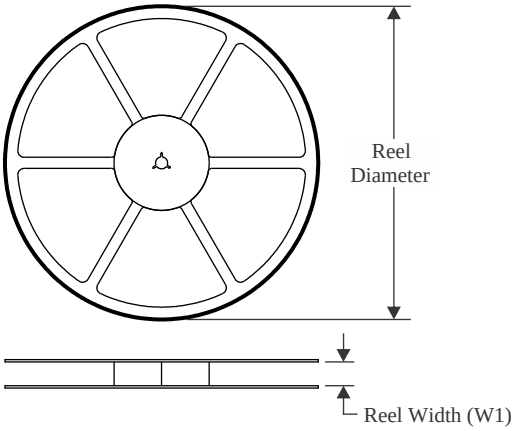
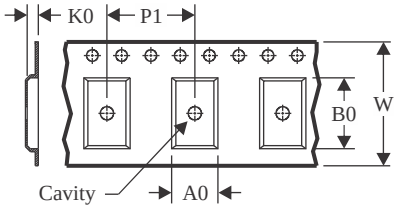
TAPE AND REEL INFORMATION

REEL DIMENSIONS

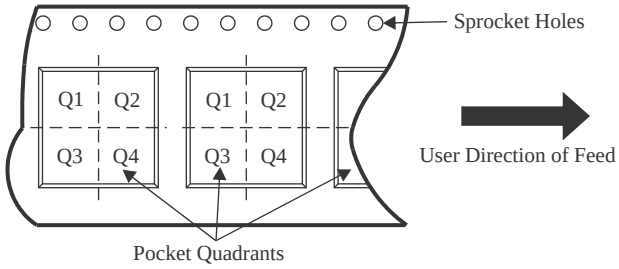


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

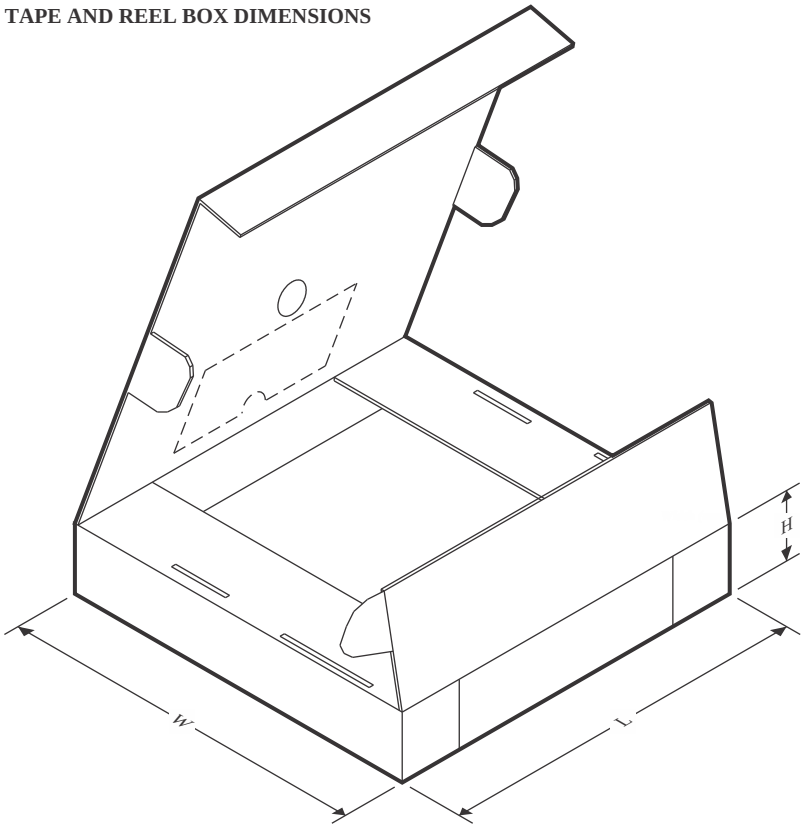
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM2704DBR	SSOP	DB	28	2000	330.0	17.4	8.5	10.8	2.4	12.0	16.0	Q1
PCM2704DBR	SSOP	DB	28	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
PCM2705DBR	SSOP	DB	28	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
PCM2706PJTR	TQFP	PJT	32	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

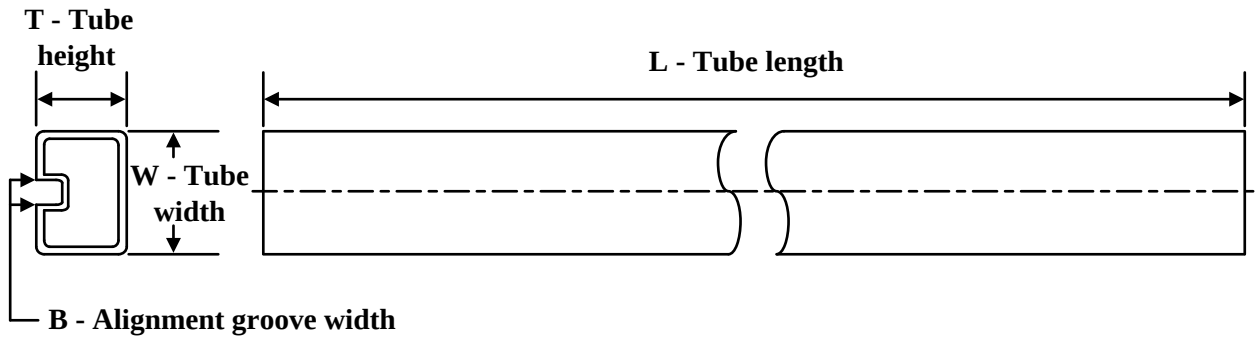
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM2704DBR	SSOP	DB	28	2000	336.6	336.6	28.6
PCM2704DBR	SSOP	DB	28	2000	353.0	353.0	32.0
PCM2705DBR	SSOP	DB	28	2000	353.0	353.0	32.0
PCM2706PJTR	TQFP	PJT	32	1000	350.0	350.0	43.0

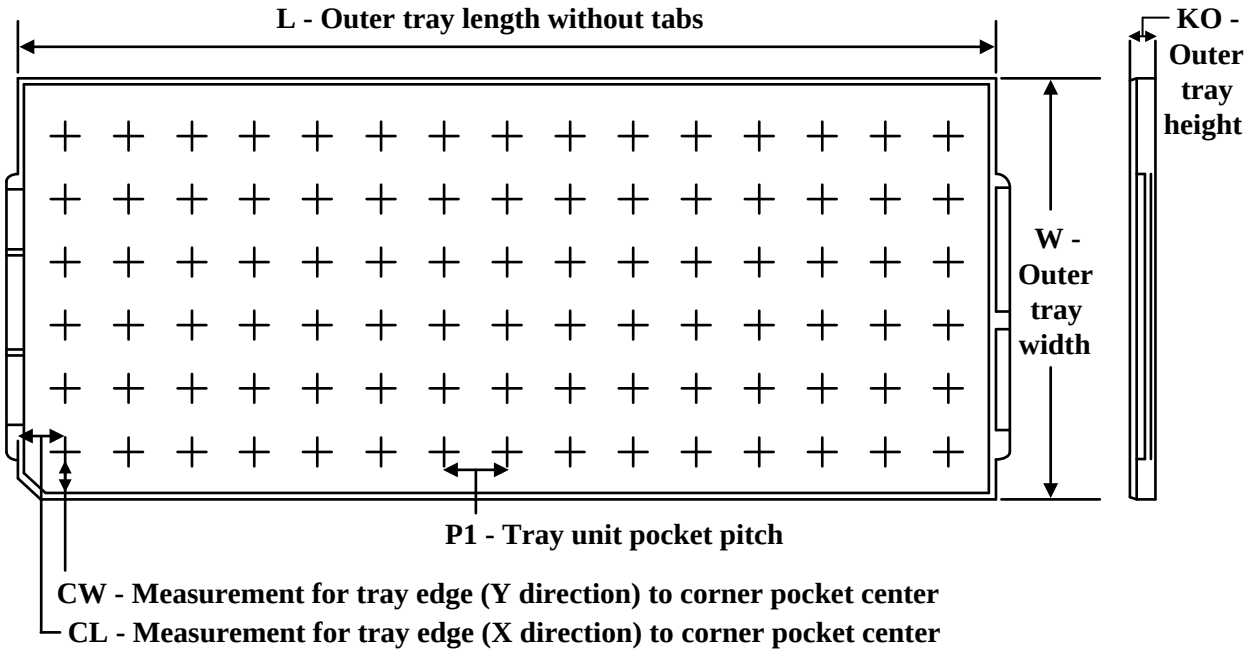
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
PCM2704DB	DB	SSOP	28	47	500	10.6	500	9.6
PCM2704DB	DB	SSOP	28	47	530	10.5	4000	4.1
PCM2704DB.B	DB	SSOP	28	47	500	10.6	500	9.6
PCM2704DB.B	DB	SSOP	28	47	530	10.5	4000	4.1
PCM2704DBG4	DB	SSOP	28	47	530	10.5	4000	4.1
PCM2704DBG4.B	DB	SSOP	28	47	530	10.5	4000	4.1
PCM2705DB	DB	SSOP	28	50	530	10.5	4000	4.1
PCM2705DB.B	DB	SSOP	28	50	530	10.5	4000	4.1
PCM2705DBG4	DB	SSOP	28	50	530	10.5	4000	4.1

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

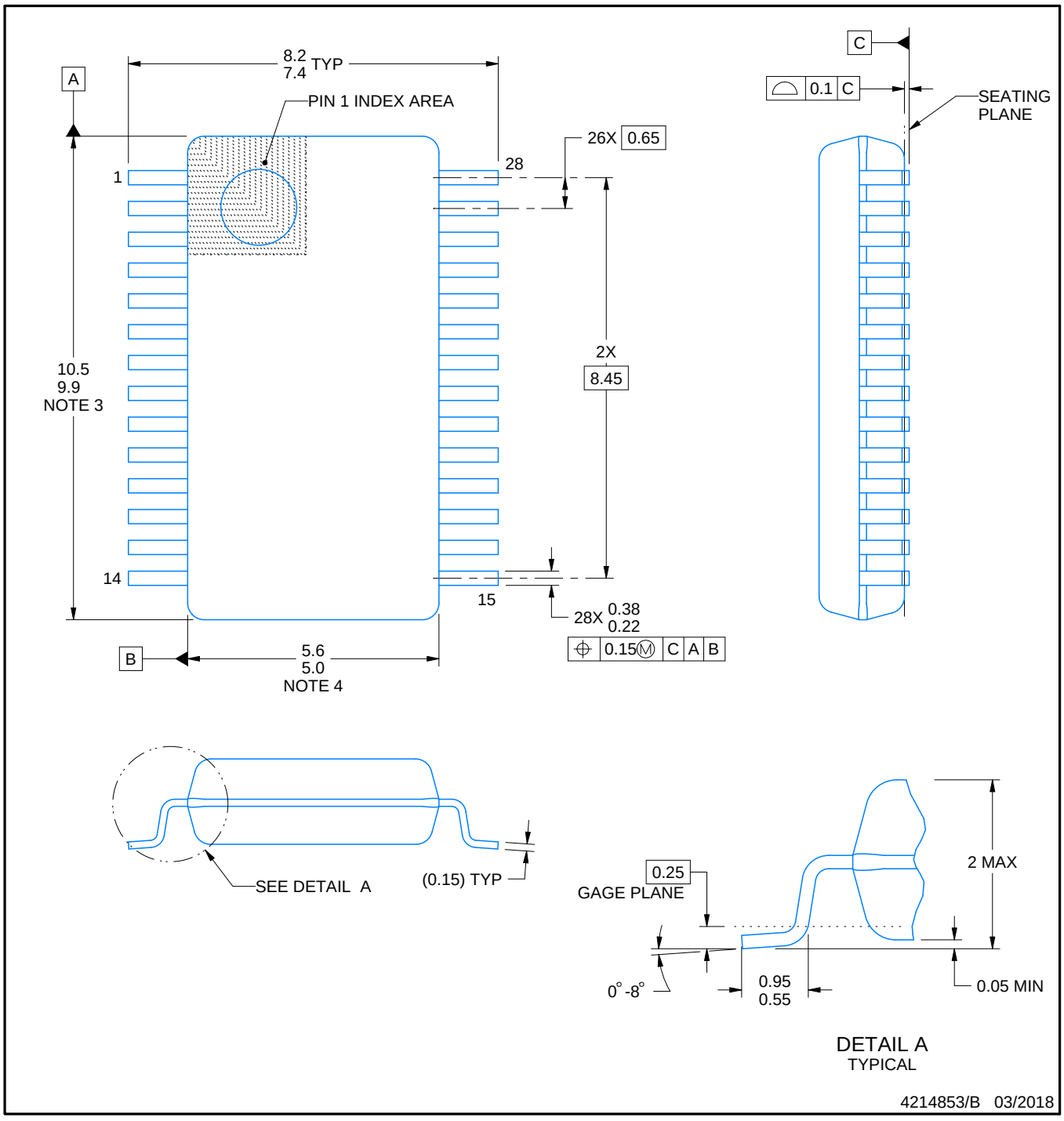
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
PCM2706PJT	PJT	TQFP	32	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
PCM2706PJT	PJT	TQFP	32	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
PCM2706PJT.B	PJT	TQFP	32	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
PCM2706PJT.B	PJT	TQFP	32	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
PCM2706PJTR	PJT	TQFP	32	1000	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
PCM2706PJTR	PJT	TQFP	32	1000	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
PCM2706PJTR.B	PJT	TQFP	32	1000	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
PCM2706PJTR.B	PJT	TQFP	32	1000	10 x 25	150	315	135.9	7620	12.2	11.1	11.25

PACKAGE OUTLINE

DB0028A

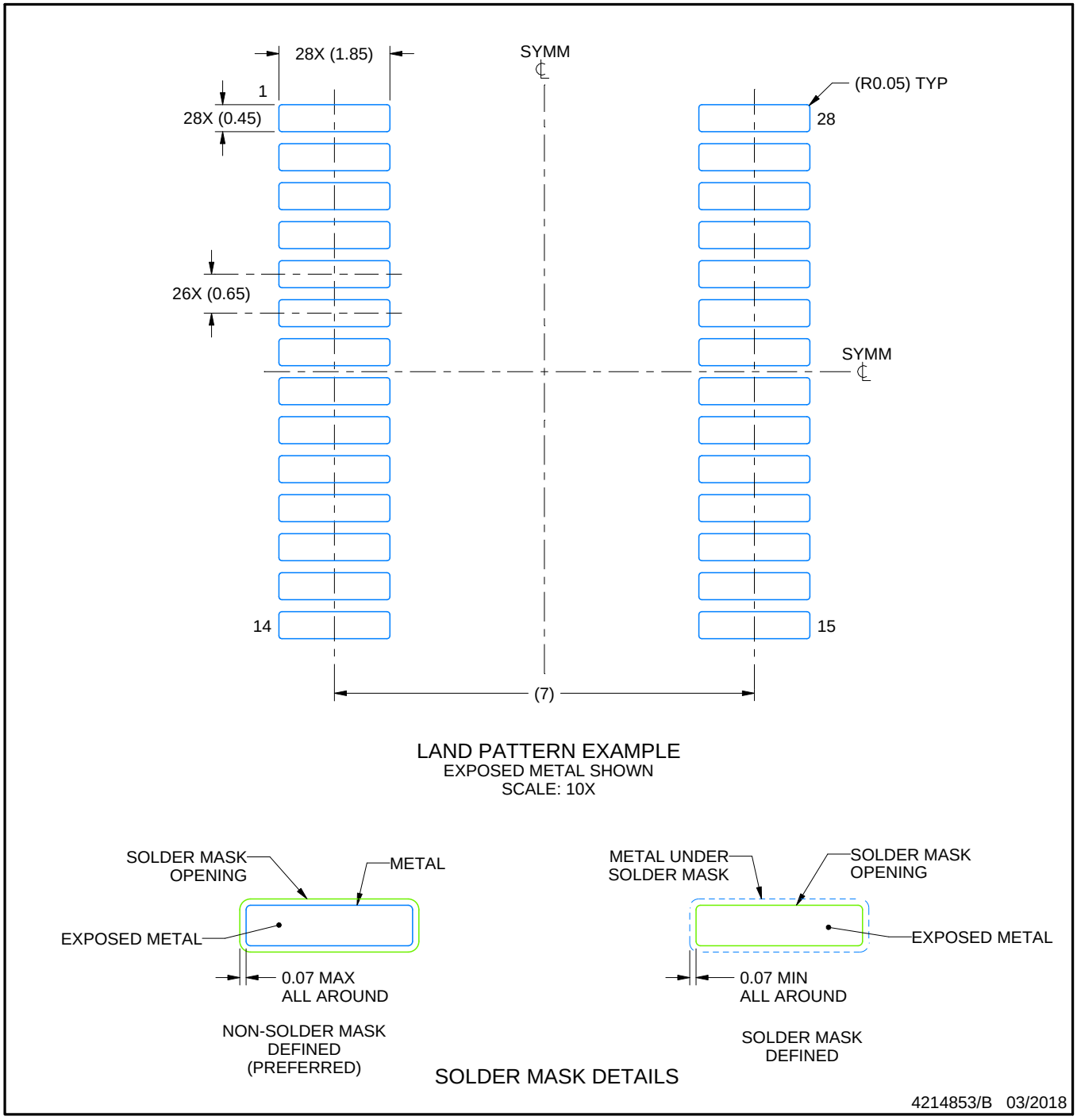
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



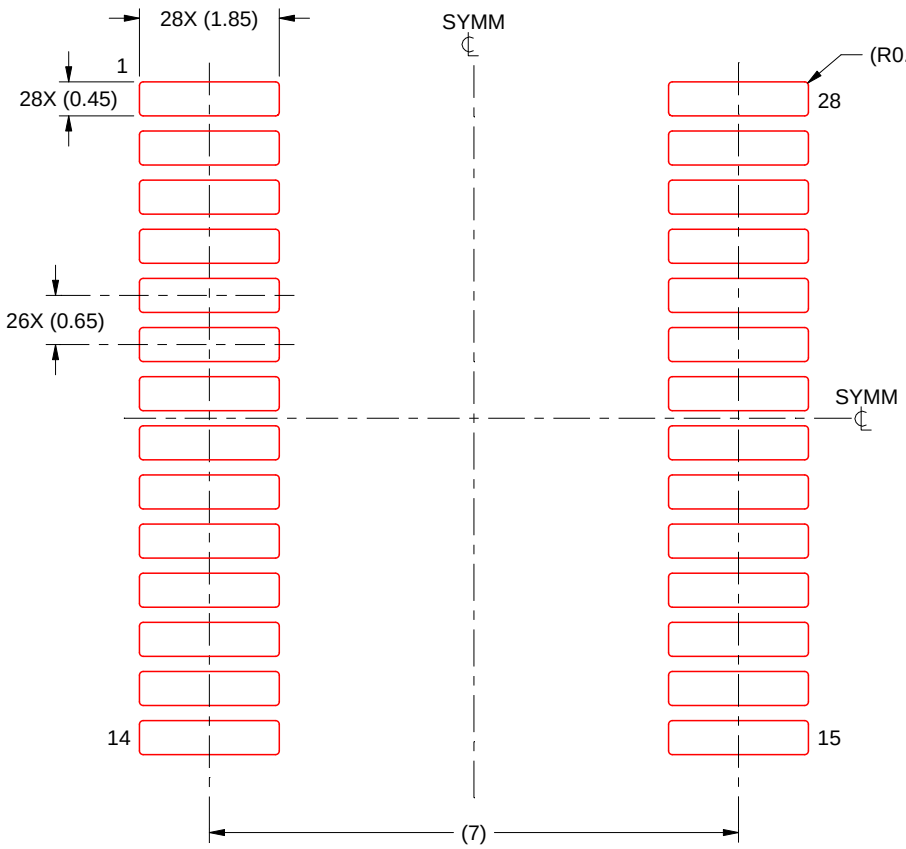
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214853/B 03/2018

NOTES: (continued)

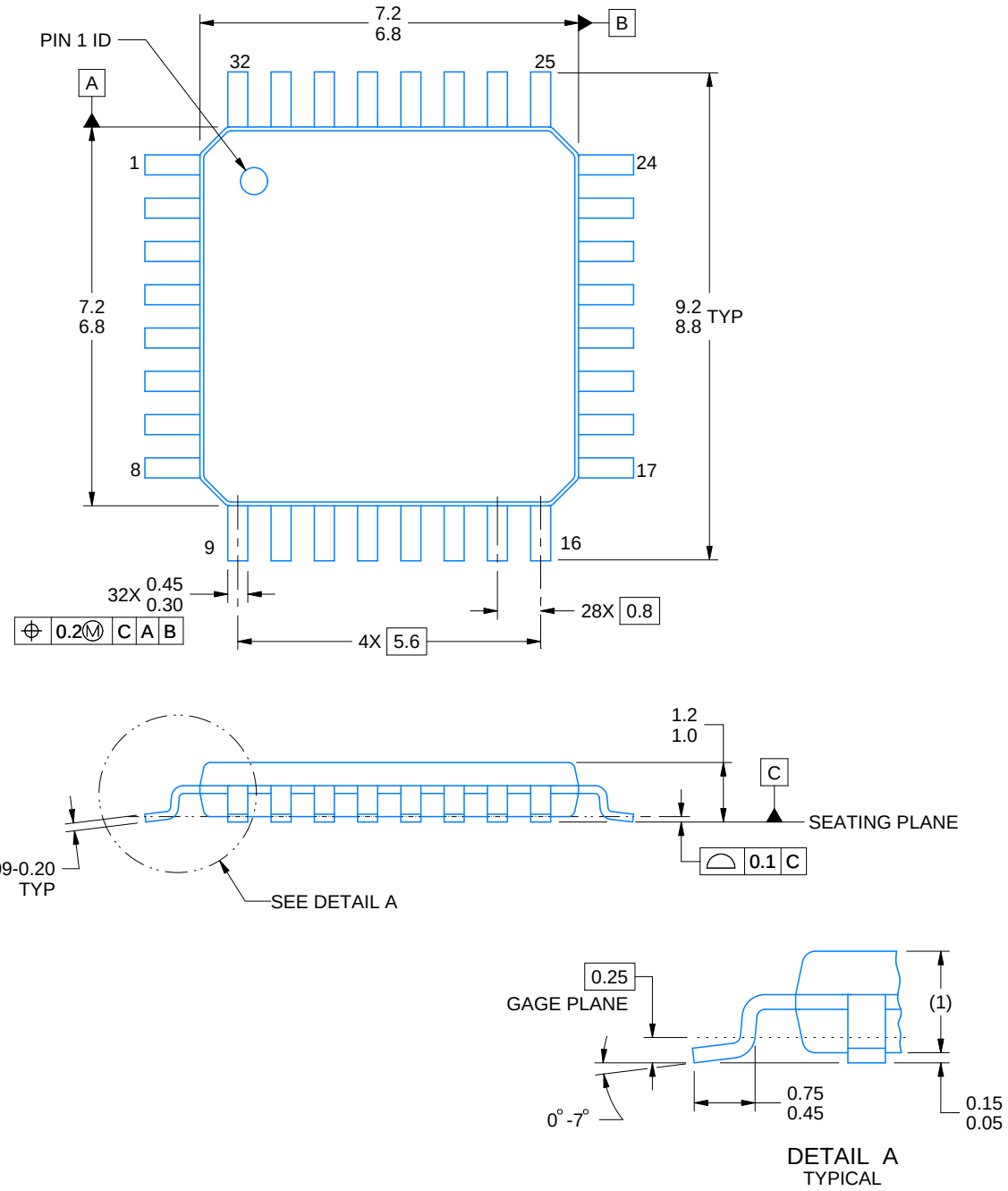
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PJT0032A

TQFP - 1.2 mm max height

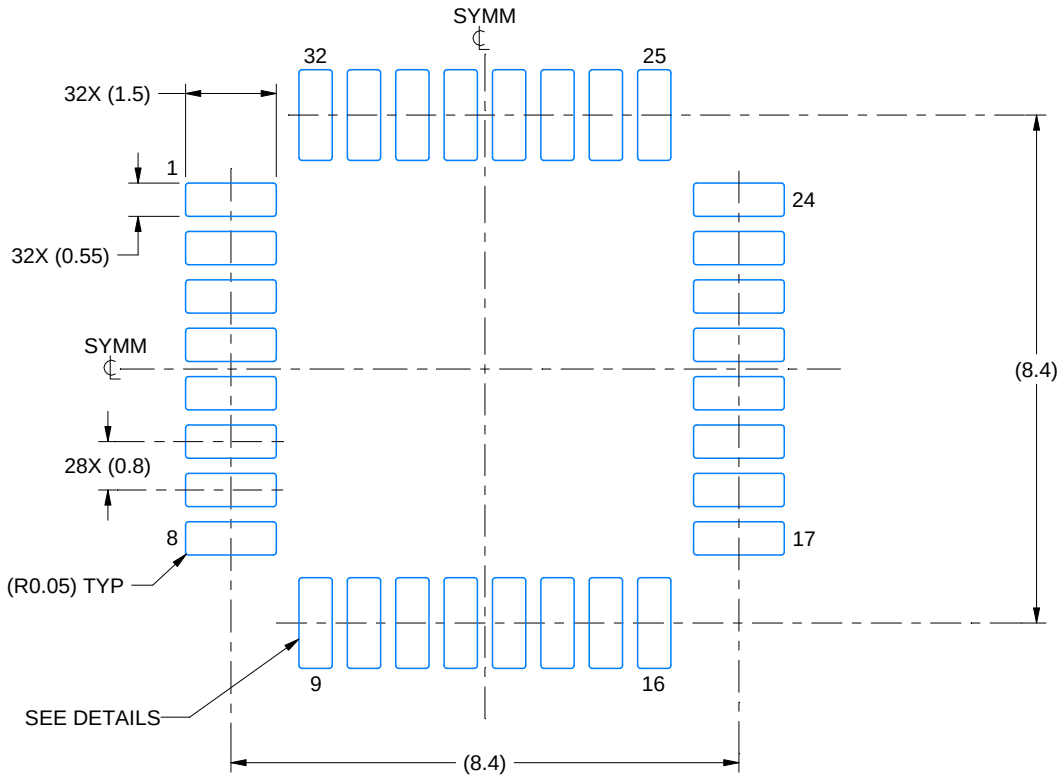
PLASTIC QUAD FLATPACK



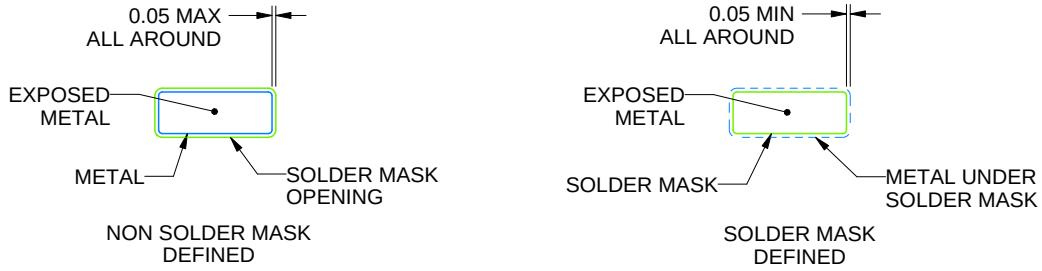
4220861/A 07/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

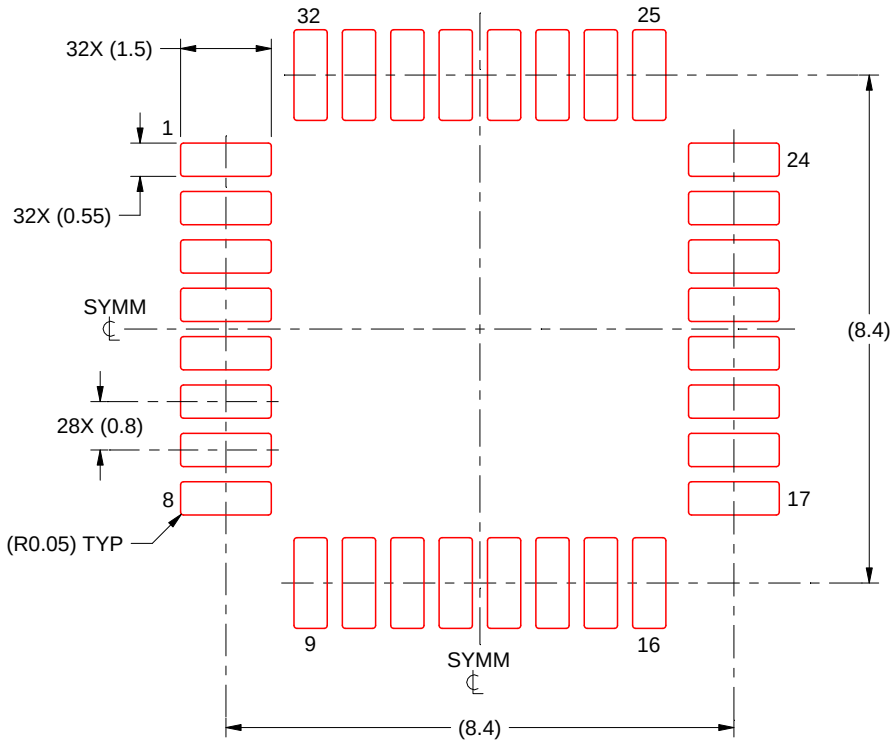


SOLDER MASK DETAILS

4220861/A 07/2023

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220861/A 07/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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