Doc No. TT4-EA-12100

Revision. 2

Panasonic

MOS FET

MTMC8E2A0LBF

MTMC8E2A0LBF

Gate Resistor installed Dual N-Channel MOS Typ

For lithium-ion secondary battery protection circuit

■ Features

- Low drain-source On-state Resistance RDS(on) typ. = 15 m Ω (VGS =4.5 V)
- Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL:Level 1 compliant)
- Marking Symbol: 4B

■ Packaging

Embossed type (Thermo-compression sealing): 3 000 pcs / reel (standard)

	Unit: mm		
2. 9			
8 7	0.3 0.16		
	2. 4		
0.65	3 4 (0.81)		
1. Source	5. Drain		
2. Gate	6. Drain		
Source	7. Drain		
4. Gate	8. Drain		
Panasonic	WMini8-F1		
JEITA	SC-115		
Code			

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	Absolute	Maximum	Raimus	1a - 25	٠.

Parameter		Symbol	Rating	Unit
	Drain-source Voltage	VDS	20	V
	Gate-source Voltage	VGS	±12	V
	Drain current	ID	7.0	Α
	Peak drain current	IDp	42	Α
Overall		PD1 *1	1.0	
	Total power dissipation	PD2 *1,2	1.2	W
		PD3 *3	0.4	
	Channel temperature	Tch	150	°C
	Operating ambient temperature	Topr	-40 to + 85	°C
	Storage temperature	Tstg	-55 to +150	°C

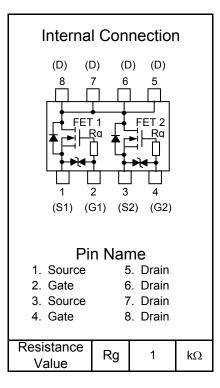
- Note) *1 Glass epoxy board: 25.4 mm × 25.4 mm × 0.8 mm Copper foil of the drain portion should have a area of 300 mm² or more PD absolute maximum rating without a heat shink: 400 mW
 - *2 t = 10 s

Established: 2010-01-06

: 2013-09-02

Revised

*3 Stand-alone (without the board)



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■ Electrical Characteristics Ta = 25°C ± 3°C

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Drain-source surrender voltage	VDSS	ID = 1.0 mA, VGS = 0	20			V
Drain-source cutoff current	IDSS	VDS = 20 V, VGS = 0			1.0	μA
Gate-source cutoff current	IGSS	$VGS = \pm 8.0 \text{ V}, VDS = 0$			±10	μA
Gate threshold voltage	Vth	ID = 1.0 mA, VDS = 10 V	0.40	0.85	1.30	V
	RDS(ON)1	ID = 2.0 A, VGS = 4.5 V		15	21	mΩ
Drain-source ON resistance	RDS(ON)2	ID = 2.0 A, VGS = 3.7 V		18	25	mΩ
	RDS(ON)3	ID = 2.0 A, VGS = 2.5 V		22	33	mΩ
Forward transfer admittance	Yfs	ID = 1.0 A, VDS = 10 V	3.0			S
Short-circuit input capacitance (Common source)	Ciss			1450		pF
Short-circuit output capacitance (Common source)	Coss	VDS = 10 V, VGS = 0, f = 1 MHz		100		pF
Reverse transfer capacitance (Common source)	Crss			90		pF
Turn-on delay time *1	td(on)	VDD = 10 V, VGS = 0 V to 4 V		0.33		μs
Rise time *1	tr	ID = 1.0 A		0.70		μs
Turn-off delay time *1	td(off)	VDD = 10 V, VGS = 4 V to 0 V		4.0		μs
Fall time *1	tf	ID = 1.0 A		2.0		μs

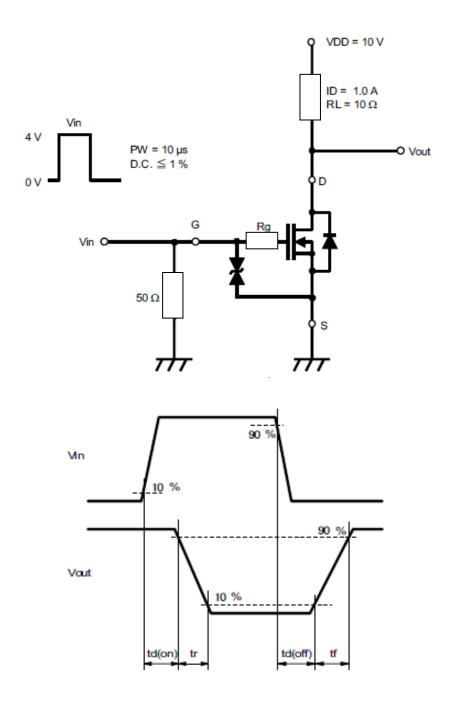
Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

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^{2. *1} Measurement circuit for Turn-on Delay Time/Rise Time/Turn-off Delay Time/Fall Time

*1 Measurement circuit for Turn-on Delay Time/Rise Time/Turn-off Delay Time/Fall Time

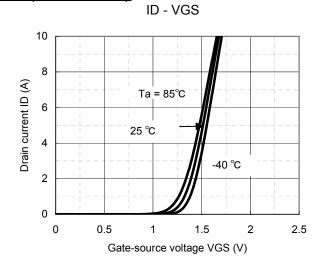


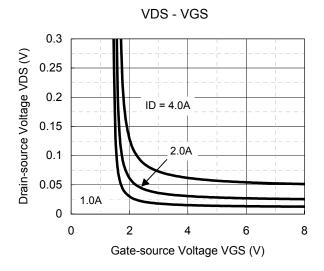
MOS FET

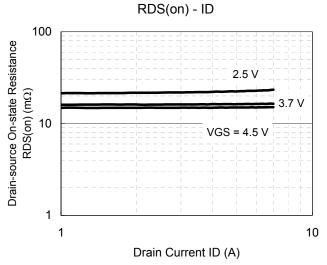
MTMC8E2A0LBF

Technical Data (reference)

ID - VDS 6 /GS = 4.5 V 5 Drain Current ID (A) 2.5 V 3 2.0 V 2 1.5 V 0 0 0.1 0.2 0.3 Drain-source Voltage VDS (V)



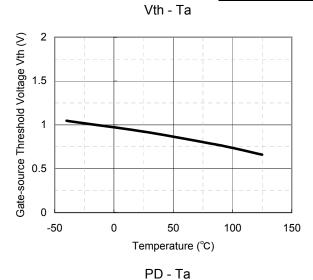


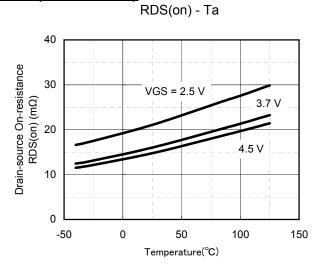


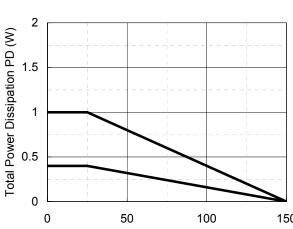
Established: 2010-01-06 Revised: 2013-09-02

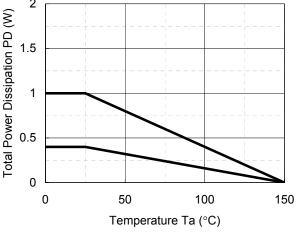
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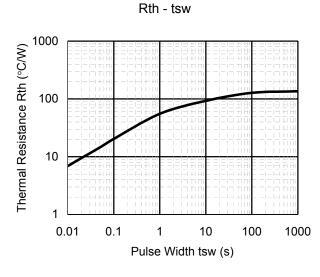
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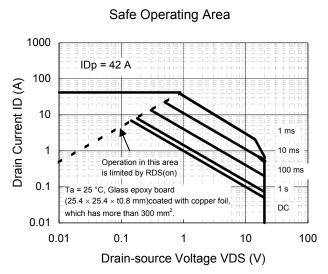












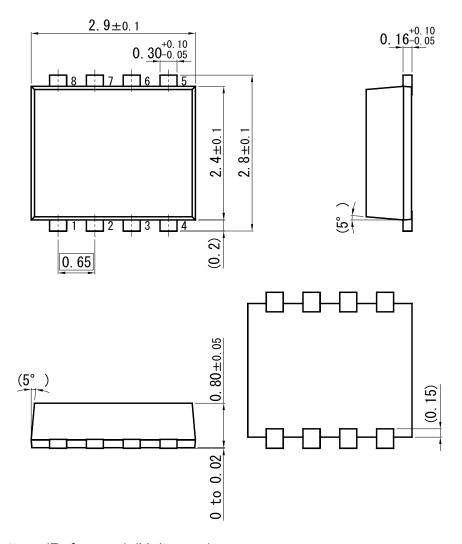
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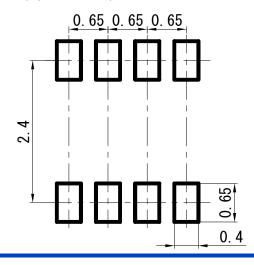
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WMini8-F1

Unit: mm



Land Pattern (Reference) (Unit: mm)



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