

FTXL 3190 Free Topology Transceiver Models 14260R-800, 14240R, and 14250R-300



Description

The FTXL 3190 Free Topology Transceiver is a high-performance free topology transceiver and media access controller for developing high-performance devices based on the LonTalk Platform. The LonTalk® Platform for the FTXL transceiver combines development tools, an application programming interface (API), and a high-performance ANSI/CEA-709.1-B (EN 14908.1) protocol stack with the FTXL transceiver providing unparalleled performance coupled with ease-of-development, reliability, and stability. The LonTalk Platform for FTXL transceivers is ideally suited for high-value controllers required for system and area level applications. It removes restrictions associated with address table size and transaction control and address table limitations that existed with earlier solutions. The LonTalk Platform is also available for the shortsack® Micro server—providing a scalable solution from any shortsack application and host processor to an FTXL application with an Altera host processor.

For maximum performance, reliability, and flexibility, Echelon has ported its widely used LonTalk protocol stack to the nios II embedded processor supported by the Altera FPGA devices. Echelon's FTXL LonTalk protocol stack is a complete implementation of the ANSI/CEA-709.1-B (EN 14908.1) Control Networking Protocol, including support for the ANSI/CEA-709.1-B (EN 14908.1) Enhanced Command set providing higher performance for controller applications. The rich mix of pin and logic element configurations offered by the Cyclone II/III family of FPGA devices combined with the high-performance FTXL LonTalk protocol stack provides developers with the options to exactly fit their application requirements for controller devices connected directly to a TP/FT-10 LonWorks® control network segment. Used in conjunction with the FTXL transceiver, the nios II embedded processor on the Cyclone II/III FPGA provides a powerful and scaleable platform for system controller applications in LonWorks networks.

The foundation code base for the FTXL LonTalk protocol stack has already been widely deployed in Echelon's iLon® and Lns® product platforms for proven reliability and performance.

- ▼ Provides a high-performance control networking solution for free topology twisted pair applications
- ▼ Drives down development and part costs while maximizing customized solutions
- ▼ Highest performance ANSI/CEA-709.1-B and EN 14908.1 solution
- ▼ Supports up to 4,096 static and dynamic network variables
- ▼ Supports LonMark® standard changeable-network-variable types
- ▼ Supports up to 4096 address table entries
- ▼ Supports up to 200 concurrent receive and 2500 send transactions
- ▼ Supports up to 8192 alias table entries
- ▼ Leverages flexible and scaleable nios® II embedded processor technology of the Altera® Cyclone® II/III FPGA device families
- ▼ Shares a common platform and API with shortsack® applications
- ▼ Supports polarity-insensitive free topology star, daisy chain, bus, loop, or mixed topology wiring
- ▼ 78 kilobits-per-second bit rate for distances up to 500 meters in free topology or 2700 meters in bus topology with double terminations
- ▼ Unique 48-bit neuron® ID in every device for network installation and management
- ▼ Compact external transformer with patent-pending architecture providing exceptional immunity from magnetic interference and high frequency common mode noise
- ▼ Compatible with TP/FT-10 channels using devices based on FT 3120 / 3150 smart Transceivers, FTT-10 and/or FTT-10A Free Topology Transceivers, and, with suitable DC blocking capacitors, LPT-10 Link Power Transceivers
- ▼ Communications parameters preprogrammed for the TP/FT-10 channel at 10MHz
- ▼ Developer's kit available as a free download
- ▼ No runtime royalties
- ▼ 5V operation with low power consumption
- ▼ -40 to +85°C operating temperature range [1,2]

The LonTalk Platform is a compatible family of development tools, an API, firmware, and chips that can be used to implement a wide variety of LonWorks devices, from simple sensors and actuators to complex system- and area-controllers. The LonTalk Platform for the FTXL transceiver provides an Altera FPGA-hosted solution with unparalleled performance for applications requiring up to 4096 network variables. The LonTalk Platform is also available for the shortsack Micro server—providing a solution that can be used with any host processor that requires up to 254 network vari-

Notes:

¹ EEPROM programming must be limited to -25 to 85°C for a 10-year data retention over the -40 to 85°C operating temperature range.

² Maximum junction temperature should not exceed 105°C. T_{junction} can be calculated as follows: T_{junction} = T_{ambient} + V_I•q_{JA} where q_{JA} for 32-pin SOIC = 51°C/W, q_{JA} for 44-pin TQFP = 43°C/W, and q_{JA} for 64-pin TQFP =

ables. Both solutions share compatible application programming interfaces (APIs) and interface builder tools, lowering the learning time for developers using both frameworks, and simplifying the use of common code for both FTXL transceivers and shortstack Micro servers.

The FTXL 3190 transceiver is fully compatible with the LonMark TP/FT-10 channel and can communicate with devices implemented with Echelon's FT 3120 and 3150 smart Transceivers, FTT-10A Free Topology Transceiver, and when used with suitable DC blocking capacitors, the FTXL transceiver is also fully compatible with the LPT-10 and LPT-11 Link Power Transceivers.

The FTXL 3190 transceiver is offered in a compact 44-lead TQFP package. It supports input clock rates of 5, 10, 20, and 40 MHz (20 MHz recommended). An FT-X1 or FT-X2 communication transformer must be used with the FTXL 3190 transceiver. The FT-X1 Communication Transformer is a through-hole component while FT-X2 is a surface-mount component. The FT-X1 and FT-X2 transformers have similar noise immunity and performance characteristics.

The FTXL 3190 transceiver and communication transformers (Models 14260r -800, 14240r , and 14250r -300) are compliant with the European Directive 2002/95/EC on the restriction of the use of certain hazardous substances (roHS) in electrical and electronic equipment.

Solution Architecture

A device implemented with an FTXL transceiver includes the following components (see Figure 1):

- ▼ Application and FTXL nios II library for a 32-bit nios II embedded processor implemented on an Altera FPGA device
- ▼ FTXL 3190 transceiver
- ▼ FT-X1 or FT-X2 Communication Transformer

The interface between the nios II host processor and FTXL 3190 transceiver uses a high-speed 8-bit parallel interface that includes support of an uplink interrupt as packets from the network are received and moved up the LonTalk protocol stack running on the nios II host. The FTXL 3190 transceiver implements layers 1 and 2 of the ANSI/CEA-709.1-B (En 14908.1) protocol to free the nios II processor from media access processing. The default buffer configuration on the FTXL transceiver provides support for the maximum ANSI/CEA-709.1-B (En 14908.1) packet size of 255 bytes. The device driver uses the Altera Hardware Abstraction Layer (HAL) to implement a portable interface that may be effortlessly incorporated in your design, even if your final FPGA hardware solution does not match that of the development board.

Altera Nios II FPGA Benefits

The Altera family of FPGA devices provides a rich mix of pin and logic element configurations, and the nios II embedded processor comes in three performance-levels (economy, standard and fast) to choose from, allowing trade-offs of logic element count vs. performance. The 32-bit nios II embedded processor may also be config-

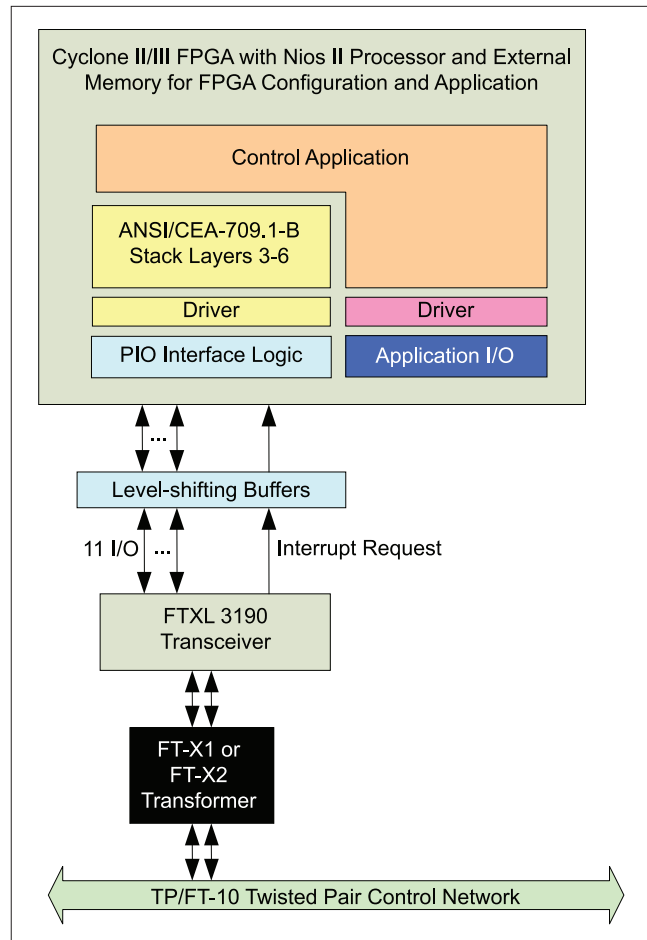


Figure 1: FTXL Solution Architecture

ured to support different memory and cache configurations to provide the performance necessary for the application. Together, Altera FPGA and nios II embedded processor technology allow system designers to customize the peripherals and hardware resources to exactly match the application needs. Altera C to hardware compilation technology can dramatically improve system performance by implementing algorithms normally handled in software as custom instructions in hardware. Math intensive applications can benefit with the addition of hardware multipliers to the nios II embedded processor. Altera FPGA and nios II embedded processor technology allow system designers to customize the peripherals and hardware resources to exactly match the application needs. Altera system-on-a-Programmable-Chip (SoPC) technology allows for rapid and flexible hardware design.

Development Platform

The FTXL Developer's Kit is required to develop applications for the FTXL transceiver. The developer's kit is available as a free download from www.echelon.com and includes the following:

- ▼ FTXL nios II library supporting layers 3-6 of the ANSI/CEA-709.1-B (En 14908.1) protocol, and interfacing with the FTXL transceiver
- ▼ nios II HAL-compliant drivers targeting custom hardware peripherals provided with the reference design

- ▼ A utility, called the *LonTalk Interface Builder*, creates C declarations for a specified *LonWorks* interface, and also creates LonTalk protocol stack structures and data tables
- ▼ Example FTXL applications built using the Altera *nios II Embedded Development suite (EDs)*
- ▼ *s*chematics providing reference implementations for the level-shifting interface required to connect the FTXL transceiver to the Cyclone II FPGA
- ▼ Quartus® 7.2 compatible design files to execute the examples on the DBC2C20 development board and easy migration to your own hardware design
- ▼ *s*ource files providing an *o*s compatibility layer (*o*s CL) to allow developers to target a real-time kernel other than Micrium μ C/*o*s-2

Design and development tools for an Altera FPGA and the *nios II* soft processor are required to develop applications using the FTXL transceiver. The FTXL solution has been tested with Altera's Quartus 7.2 release with *s*o PC Builder and the Altera *nios II Embedded Development suite (EDs)*. This software is available from Altera, and is subject to Altera licenses. For more information on these tools, see www.altera.com.

Your application development is accelerated by using development hardware from Devboards (www.devboards.de). The FTXL Developer's Kit includes example applications and Cyclone II design files that target the Devboards DBC2C20 Cyclone II development board. The DBE-FT-Par and DBE-ADAP add-on boards and the

DBC2C20 development board are available from Devboards.

With the FTXL Developer's Kit, a Devboards DBC2C20 Cyclone II development board, and the FTXL Developer's Kit add-on boards, you can quickly prototype a working *Ansi/CEA-709.1-B (En 14908.1)* solution for your controller design with no hardware development effort.

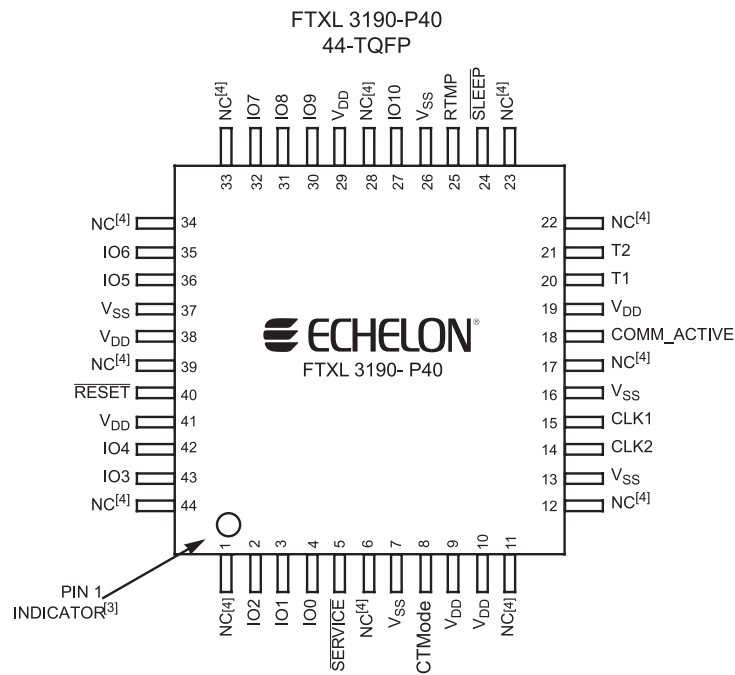
For more information on the developer's kit, see the *Model 10050-10 FTXL Developer's Kit Datasheet*.

Network Noise Protection

The communication transformer enables operation in the presence of high frequency common mode noise on unshielded twisted pair networks. Properly designed devices can meet the rigorous Level 3 requirements of *En 61000-4-6* without the need for a network isolation choke. The transformer also offers outstanding immunity from magnetic noise, eliminating the need for protective magnetic shields in most applications.

FT-X1/FT-X2 Communication Transformers must be ordered separately. see FTXL 3190 Transceiver ordering Information for product offerings and descriptions. The FTXL 3190 Free Topology Transceiver and the FT-X1/FT-X2 Communication Transformer are designed to be used as a pair and therefore must be implemented together in all designs. *n*o transformer other than the FT-X1 or FT-X2 Communication Transformer may be used with the FTXL 3190 Free Topology Transceiver, or the transceiver warranty will be void.

FTXL 3190 Transceiver IC Pin Configurations



Notes:

³ The small dimple at the bottom left of the marking indicates pin 1.

⁴ NC (No Connect) — Should not be used. (These pins are reserved for internal testing.)

FTXL 3190 Transceiver IC Pin Descriptions

| Pin Name | Type | Pin Functions | FTXL 31190-P40 TQFP-44 Pin Number |
|-----------------------------|--|---|--|
| CLK1 | Input | oscillator connection or external clock input. | 15 |
| CLK2 | output | oscillator connection. Leave open when external clock is input to CLK1. Maximum of one external HCMOS equivalent load. | 14 |
| $\overline{\text{rEsET}}$ | I/o (Built-in Pull-up) | reset pin (active Low). <i>Note:</i> The allowable external capacitance connected to the $\overline{\text{rEsET}}$ pin is 100pF-1000pF. | 40 |
| $\overline{\text{sErVICE}}$ | I/o (Built-in Configurable Pull-up) | service pin (active Low). Alternates between input and output at a 76Hz rate. | 5 |
| Io 0-Io 3 | I/o | Large current-sink capacity (20mA). General I/o port. The output of timer/counter 1 may be routed to Io 0. The output of timer/counter 2 may be routed to Io 1. | 4, 3, 2, 43 |
| Io 4-Io 7 | I/o (Built-in Configurable Pull-up) | General I/o port. The input of timer/counter 1 may be derived from one of Io 4-Io 7. The input to timer/counter 2 may be derived from Io 4. | 42, 36, 35, 32 |
| Io 8-Io 10 | I/o | General I/o port. May be used for serial communication under firmware control. | 31, 30, 27 |
| V _{DD} | Power | Power input (5V nom). All V _{DD} pins must be connected together externally. | 9, 10, 19, 29, 38, 41 |
| V _{ss} | Power | Power input (0V, GND). All V _{ss} pins must be connected together externally. | 7, 13, 16, 26, 37 |
| ICTMode | Input | In-circuit test mode control. Driving the ICTMode high and $\overline{\text{rEsET}}$ low will put the device in the In-Circuit Test mode (all pins are placed in a high impedance state). | 8 |
| T1 | I/o | Analog pin to be interfaced with T1 of the external transformer. Corresponds to CP0 on Toshiba and Cypress neuron Chips. | 20 |
| T2 | I/o | Analog pin to be interfaced with T2 of the external transformer. Corresponds to CP1 on Toshiba and Cypress neuron Chips. | 21 |
| CoMM_ACTIVE | output | May be used to monitor, transmit/receive activity. Driven high during data transmissions, driven low when receiving data and kept at high impedance otherwise. | 18 |
| $\overline{\text{sLEEP}}$ | output | $\overline{\text{sLEEP}}$. May be configured as an output to indicate when the FT 3120 / FT 3150 is in sleep mode. Corresponds to CP3 on Toshiba and Cypress neuron Chips. | 24 |
| $\overline{\text{rTMP}}$ | Input | reserved for future use. Must be pulled up to 5V. Corresponds to CP4 on Toshiba and Cypress neuron Chips. | 25 |
| n C | — | no connect. Must be left open. | 1, 6, 11, 12, 17, 22, 23, 28, 33, 34, 39, 44 |

FT-X1 Communication Transformer Pin Configuration

6-pin through-hole transformer (top view)

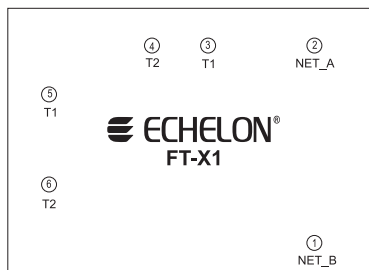


Figure 3a

FT-X2 Communication Transformer Pin Configuration

4-pin surface mount transformer (top view)



Figure 3b

FT-X1/FT-X2 Communication Transformer Pin Descriptions

| Pin Name | Pin Function | Transformer Pin Number |
|----------|--|---------------------------|
| n ET_B | n etwork Port, polarity Insensitive | 1 |
| n ET_A | n etwork Port, polarity Insensitive | 2 |
| T1 | Internally connects to pin 5. Alternate connection to T1 pin on the FTXL 3190 IC. | 3 (n ot used on FT-X2) |
| T2 | Internally connects to pin 6. Alternate connection to T2 pin on the FTXL 3190 IC. | 4 (n ot used on FT-X2) |
| T1 | Connects to the Es D/transient protection circuitry and T1 pin on the FTXL 3190 IC. Internally connects to pin 3 of the FT-X1. | 5 |
| T2 | Connects to the Es D/transient protection circuitry and T2 pin on the FTXL 3190 IC. Internally connects to pin 4 of the FT-X1. | 6 |

Electrical Characteristics (VDD = 4.75-5.25V)

| Parameter | Description | Min. | Max. | Unit |
|------------------|---|---|--|------|
| V _{IL} | Input Low Voltage Io 0-Io 10, sEr VICE, D0-D7, r Es ET | | 0.8 | V |
| V _{IH} | Input High Voltage Io 0-Io 10, sEr VICE, D0-D7, r Es ET | 2.0 | | V |
| V _{oL} | Low-Level o utput Voltage I _{out} < 20μA s tandard o utputs (Io L = 1.4 mA) ^[5] High s ink (Io 0-Io 3), sEr VICE, r Es ET (Io L = 20 mA) High s ink (Io 0-Io 3), sEr VICE, r Es ET (Io L = 10 mA) Maximum s ink (Co MM_ACTIVE) (Io L = 40 mA) Maximum s ink (Co MM_ACTIVE) (Io L = 15 mA) | | 0.1 0.4 0.8 0.4 1.0 0.4 | V |
| V _{oH} | High-Level o utput Voltage I _{out} < 20μA s tandard o utputs (Io H = -1.4 mA) ^[5] High s ink (Io 0-Io 3), sEr VICE (Io H = -1.4 mA) Maximum s ink (Co MM_ACTIVE) (Io L = -40 mA) Maximum s ink (Co MM_ACTIVE) (Io L = -15 mA) | V _{DD} - 0.1 V _{DD} - 0.4 V _{DD} - 0.4 V _{DD} - 1.0 V _{DD} - 0.4 | | V |
| V _{hys} | Hysteresis (Excluding CLK1) | 175 | | mV |
| I _{in} | Input Current (Excluding Pull-ups) (V _{ss} to V _{DD}) ^[6] | | +/- 10 | μA |
| I _{pu} | Pull-up s ource Current (V _{out} = 0 V, o utput = High-Z) ^[6] | 60 | 260 | μA |
| I _{DD} | o perating Mode s upply Current ^[7,8] 40MHz Clock | I _{DD} (receive) | 60 | mA |
| | | I _{DD} (transmit) | 75 | mA |
| | | I _{DD} (receive) | 42 | mA |
| | | I _{DD} (transmit) | 57 | mA |
| | | I _{DD} (receive) | 35 | mA |
| | | I _{DD} (transmit) | 50 | mA |
| | | I _{DD} (receive) | 20 | mA |
| | | I _{DD} (transmit) | 35 | mA |

LVI Trip Point (VDD)

| Part Number | Min. | Typ. | Max. | Unit |
|-------------|------|------|------|------|
| FTXL 3190 | 3.8 | 4.1 | 4.4 | V |

Notes:

¹ Standard outputs are I04-I010. (RESET is an open drain input/output. CLK2 must have 15pF load.) For FT 3150, standard outputs also include A0-A15, D0-D7, E, and R/W.

² I04-I07 and SERVICE have configurable pull-ups. RESET has a permanent pull-up.

⁷ Supply current measurement conditions: all outputs under no-load conditions, all inputs 0.2V or (VDD - 0.2V), configurable pull-ups off and crystal oscillator clock input disabled.

⁸ Maximum supply current values are at midpoint of supply voltage range.

Recommended FTXL 3190 Transceiver IC Pad Layout

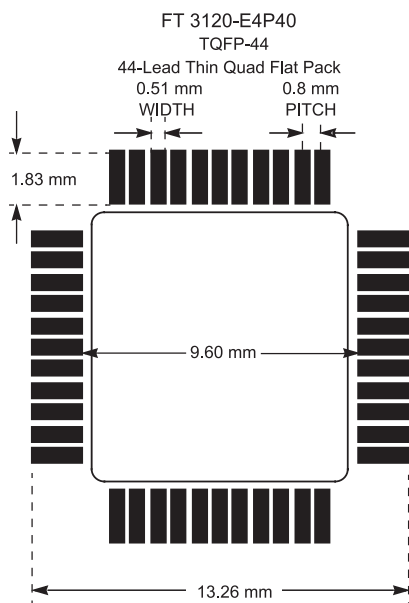


Figure 4

Recommended FT-X2 Pad Layout (4 pins)

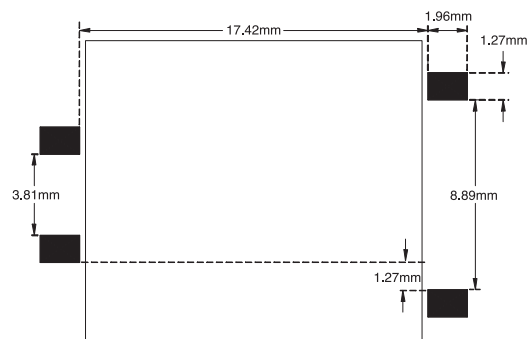


Figure 5

FTXL 3190 Transceiver IC Package Diagrams

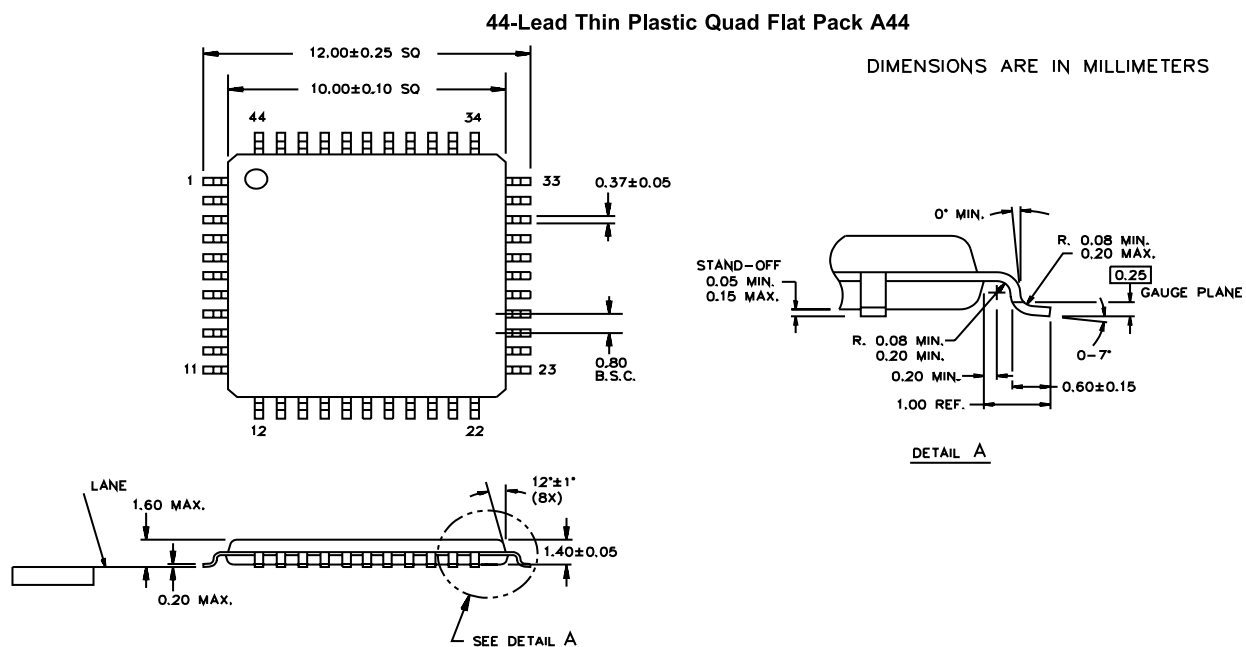


Figure 6

(Dimensions in mm)



(Dimensions in mm)



DETAIL A

Figure 8

General Specifications

| | |
|--|---|
| Data Communications Type | Differential Manchester coding |
| Network Polarity | Polarity insensitive |
| Isolation Between Network and | |
| 0-60Hz, 60 seconds | 1000Vrms |
| 0-60Hz, continuous | 277Vrms ^[9] |
| EMI | Designed to comply with FCC Part 15 Level B and En 55022 Level B |
| Es D | Designed to comply with En 61000-4-2, Level 4 |
| Radiated Electromagnetic Susceptibility | Designed to comply with En 61000-4-3, Level 3 |
| Fast Transient/Burst Immunity | Designed to comply with En 61000-4-4, Level 4 |
| Surge Immunity | Designed to comply with En 61000-4-5, Level 3 |
| Conducted RF Immunity | Designed to comply with En 61000-4-6, Level 3 |
| Safety Approvals (FT-X1/FT-X2 Communication Transformer) | Recognized by UL to UL standards 60950, 2000; Cs A C22.2 no. 60950, 2000; and TÜV En 60950 |
| Transmission Speed | 78 kilobits per second |
| Number of Transceivers Per Segment | Up to 64 |
| Network Wiring | 24 to 16AWG twisted pair; see user's guide or <i>Junction Box and Wiring Guidelines</i> application note for qualified cable types |
| Network Length in Free Topology ^[10] | 1000m (3,280 feet) maximum total wire with one repeater 500m (1,640 feet) maximum total wire with no repeaters 500m (1,640 feet) maximum device-to-device distance |
| Network Length in Doubly Terminated Bus Topology ^[10] | 5400m (17,710 feet) with one repeater 2700m (8,850 feet) with no repeaters |
| Maximum Sub Length in Doubly-Terminated Bus Topology | 3m (9.8 feet) |
| Network Termination | One terminator in free topology; two terminators in bus topology |
| Power-down Network Protection | High impedance when unpowered |
| Physical Layer Repeater | The FTXL 3190 transceiver cannot be used to implement a physical layer repeater. In the event that the limits on the number of transceivers or total wire distance are exceeded, FTT-10A transceivers may be used to create physical layer repeaters. See the <i>FTT-10A Free Topology Transceiver User's Guide</i> for more details. |
| Operating Temperature | -40 to 85°C ^[11] |
| Operating Humidity | 25-90% RH @50°C, non-condensing |
| Non-operating Humidity | 95% RH @ 50°C, non-condensing |
| Vibration | 1.5g peak-to-peak, 8Hz-2kHz |
| Mechanical Shock | 100g (peak) |
| Reflow Soldering Temperature Profile | Refer to Joint Industry standard document <i>IPC/JEDEC J-STD-020C</i> (July 2004) |
| Peak Reflow Soldering Temperature | 260°C (Model 14260r -800) 245°C (FT-X2 Model 14250r -300) |

Notes:

⁹ Safety agency hazardous voltage barrier requirements are not supported.

¹⁰ Network segment length varies depending on wire type. See *Junction Box and Wiring Guidelines* application note for detailed specifications.

Documentation

The following documentation is included with the FTXL Developer's Kit. The documentation provides an overview of the development of LonWorks applications using an FTXL transceiver.

| Document | Echelon Part Number |
|---------------------|---------------------|
| FTXL User's Guide | 078-0363-01 |
| FTXL Hardware Guide | 078-0364-01 |

Ordering Information (note: The FTXL 3190 Transceiver IC and the FT-X1/FT-X2 Communication Transformer must be ordered in the same quantities.)

The FTXL Developer's Kit is available for free download from www.echelon.com/ftxl. Contact your local Echelon representative or distributor for details on ordering the FTXL transceiver and transformer.

| Product | Model Number |
|---------------------------------|--------------|
| FTXL Developer's Kit | 10050-10 |
| FTXL 3190-P40 Transceiver Chip | 14260r -800 |
| FT-X1 Communication Transformer | 14240r |
| FT-X2 Communication Transformer | 14250r -300 |

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003-0441-01a