TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC7MB3125CFT, TC7MB3125CFK, TC7MB3125CFTG
TC7MB3126CFT, TC7MB3126CFK, TC7MB3126CFTG

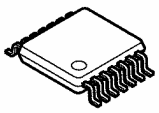
Low Capacitance Quad Bus Switch

The TC7MB3125C, TC7MB3126C is a Low ON-resistance / Low Capacitance CMOS 4bit Bus Switch. The low on-resistance of the switch allows connections to be made with minimal propagation delay time.

The TC7MB3125C requires the output enable ($\overline{OE}$) input to be set high to place the output into the high impedance state,whereas the TC7MB3126C requires the output enable (OE) input to be set low to place the output into the high impedance.

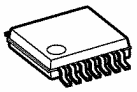
All inputs are equipped with protection circuits against static discharge.

TC7MB3125CFT, TC7MB3126CFT



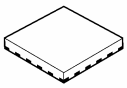
TSSOP14-P-0044-0.65A

TC7MB3125CFK, TC7MB3126CFK



VSSOP14-P-0030-0.50

TC7MB3125CFTG, TC7MB3126CFTG



VQON16-P-0303-0.50

Weight

TSSOP14-P-0044-0.65A	: 0.06 g (typ.)
VSSOP14-P-0030-0.50	: 0.02 g (typ.)
VQON16-P-0303-0.50	: 0.013 g(typ.)

Features

- Operating voltage: V_{CC} = 4.0 to 5.5 V
- On-capacitance: $C_{I/O}$ = 7 pF Switch On (typ.) @ V_{CC} = 5 V
- On-resistance: R_{ON} = 3 Ω (typ.) @ V_{CC}=4.5 V, V_{IS} = 0 V
- ESD performance: Machine model ≥ ±200 V
  Human body model ≥ ±2000 V
- Compatible with TTL outputs (control inputs)
- Power-down protection for inputs ($\overline{OE}$, OE and I/O)
- Package: TSSOP14,VSSOP14 (US14), VQON16

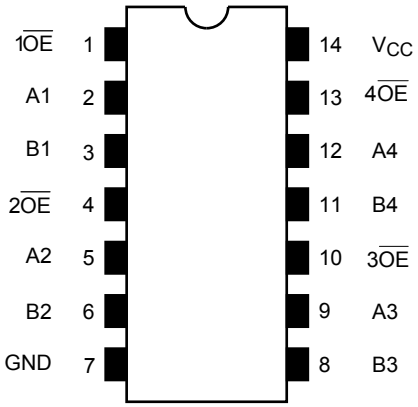
Note: When mounting VQON package, the type of recommended flux is RA or RMA.

Start of commercial production
2010-10

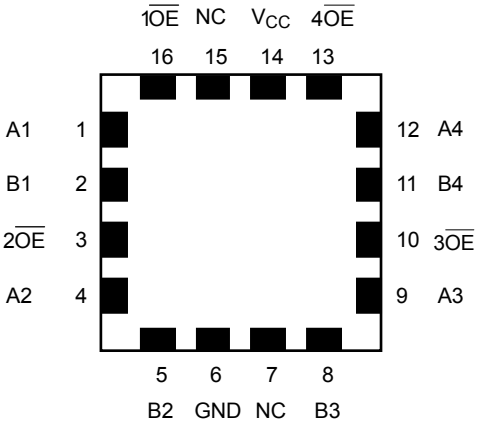
Pin Assignment (top view)

TC7MB3125C

FT (TSSOP14-P-0044-0.65A)
FK (VSSOP14-P-0030-0.50)

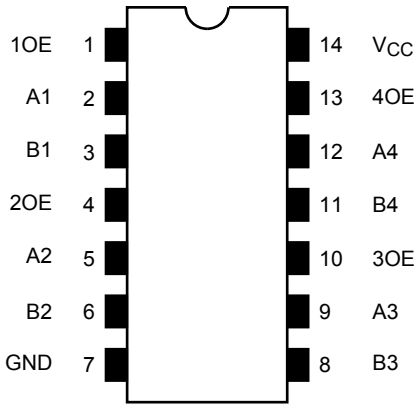


FTG (VQON16-P-0303-0.50)

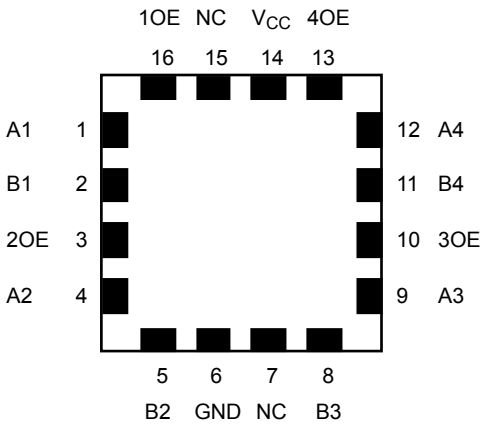


TC7MB3126C

FT (TSSOP14-P-0044-0.65A)
FK (VSSOP14-P-0030-0.50)



FTG (VQON16-P-0303-0.50)

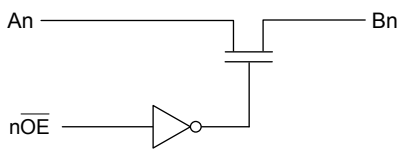


Truth Table

Inputs (3125C)	Inputs (3126C)	Function
$\overline{OE}$	OE	
L	H	A port = B port
H	L	Disconnect

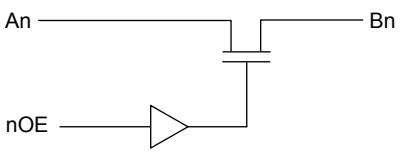
System Diagram

TC7MB3125C



(n=1,2,3,4)

TC7MB3126C



(n=1,2,3,4)

Absolute Maximum Ratings (Note)

Characteristic	Symbol	Rating	Unit
Power supply range	V_{CC}	−0.5 to 7	V
Control pin input voltage ($\overline{OE}$,OE)	V_{IN}	−0.5 to 7	V
Switch terminal I/O voltage	V_S	−0.5 to 7	V
Clump diode current	I_{IK}	−50	mA
Switch I/O current	I_S	50	mA
Power dissipation	P_D	180	mW
DC V_{CC}/GND current	I_{CC}/I_{GND}	±100	mA
Storage temperature	T_{stg}	−65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristic	Symbol	Rating	Unit
Power supply voltage	V_{CC}	4.0 to 5.5	V
Control pin input voltage ($\overline{OE}$,OE)	V_{IN}	0 to 5.5	V
Switch I/O voltage	V_S	0 to 5.5	V
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	dt/dv	0 to 10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused control pin inputs must be tied to either V_{CC} or GND.
Leave unused switch I/O pins open.

Electrical Characteristics

DC Characteristics (Ta = –40 to 85°C)

Characteristics		Symbol	Test Condition		V_{CC} (V)	Min	Typ.	Max	Unit
Input voltage ($\overline{OE}$, OE)	"H" level	V_{IH}	—		4.0 to 5.5	2.0	—	—	V
	"L" level	V_{IL}	—		4.0 to 5.5	—	—	0.8	
Input leakage current ($\overline{OE}$, OE)		I_{IN}	V_{IN} = 0 to 5.5 V		4.0 to 5.5	—	—	±1.0	μA
Power-off leakage current		I_{OFF}	$\overline{OE}$, OE, A, B = 0 to 5.5 V		0	—	—	10	μA
Off-state leakage current (switch off)		I_{SZ}	A, B = 0 to 5.5 V, $\overline{OE}$ = V_{CC}(3125C), OE=GND(3126C)		4.0 to 5.5	—	—	±1.0	μA
On resistance (Note2)		R_{ON}	V_{IS} = 0 V	I_{IS} = 30 mA (Note1)	4.5	—	3	7	Ω
			V_{IS} = 2.4 V	I_{IS} = 15 mA (Note1)	4.5	—	5	15	
					4.0	—	9	20	
Quiescent supply current		I_{CC}	V_{IN} = V_{CC} or GND, I_{OUT} = 0 A		5.5	—	—	10	μA
		ΔI_{CC}	V_{IN} = 3.4V (one input)		5.5	—	—	500	μA

Note1: All typical values are at Ta=25°C.

Note2: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Characteristics (Ta = –40 to 85°C)

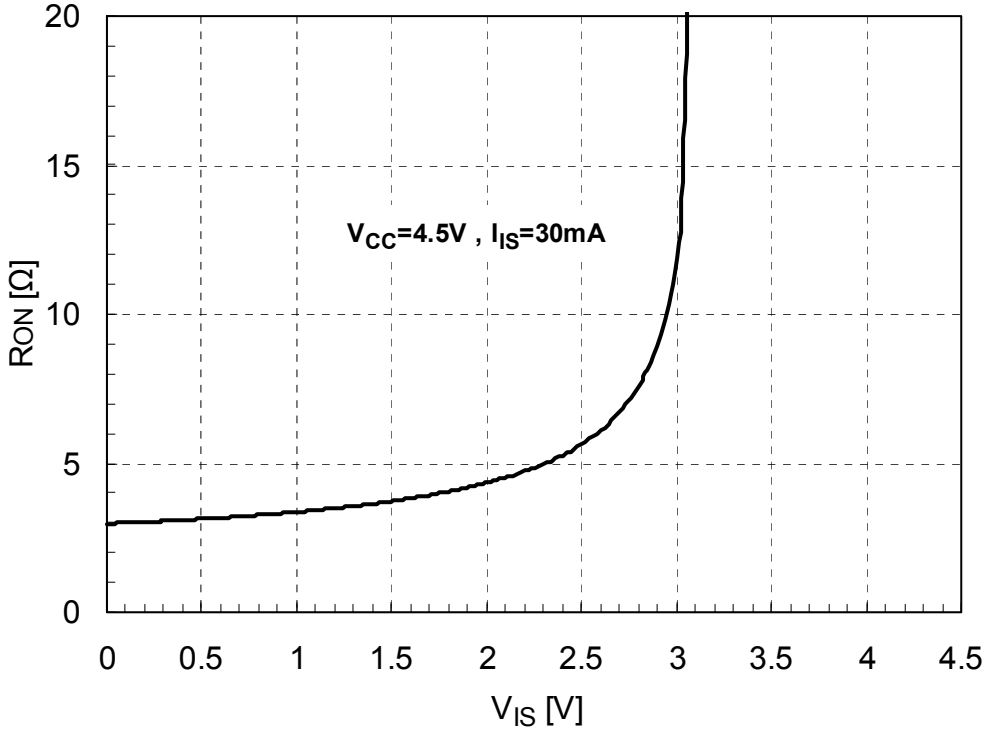
Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Max	Unit
Output enable time	t_{pZL} t_{pZH}	Figure 1, Figure 2	4.5	—	6	ns
Output disable time	t_{pLZ} t_{pHZ}	Figure 1, Figure 2	4.5	—	6	ns

Capacitive Characteristics (Ta = 25°C)

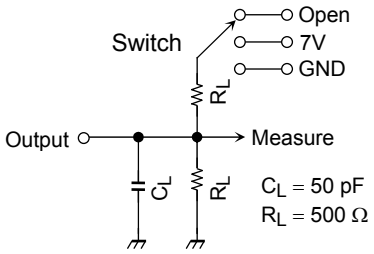
Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Unit
Control pin input capacitance	C_{IN}	V_{IN} =0 V (Note)	5.0	5	pF
Switch OFF terminal capacitance	$C_{I/O}$	$V_{I/O}$=0V, $\overline{OE}$ =V_{CC}(3125C), OE=GND(3126C) (Note)	5.0	4	pF
Switch ON terminal capacitance	$C_{I/O}$	$V_{I/O}$=0V, $\overline{OE}$ =GND(3125C),OE=V_{CC}(3126C) (Note)	5.0	7	pF

Note: This parameter is guaranteed by design

R_{ON} - V_{IS} Curve（Typ.）Ta = 25℃



AC Test Circuit



Parameter	Switch
t_{pLZ}, t_{pZL}	7V
t_{pHZ}, t_{pZH}	Open

Figure 1

AC Waveform

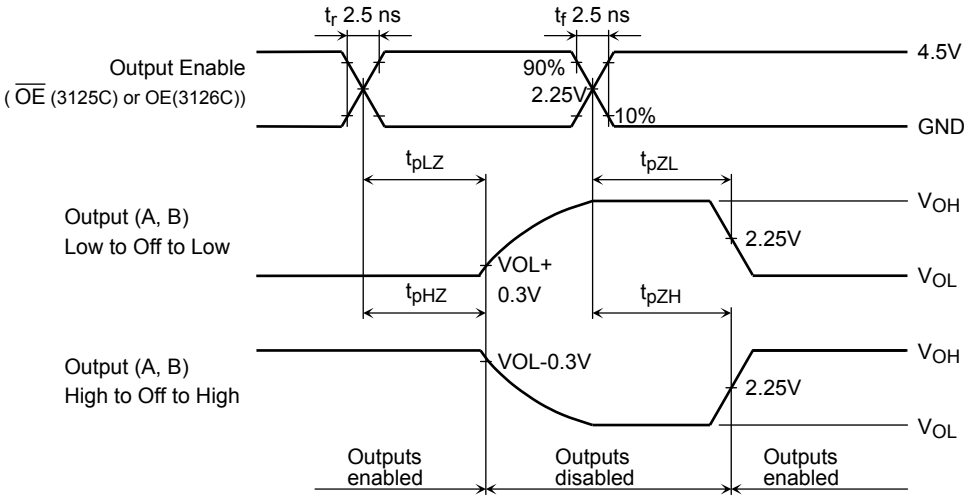


Figure 2 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

Rise and Fall Times (tr / tf) of the TC7MB3125C，3126C I/O Signals

The tr(out) and tf(out) values of the output signals are affected by the CR time constant of the input, which consists of the switch terminal capacitance ($C_{I/O}$) and the on-resistance (R_{ON}) of the input.

In practice, the tr(out) and tf(out) values are also affected by the circuit's capacitance and resistance components other than those of the TC7MB3125C, 3126C.

The tr / tf (out) values can be approximated as follows. (Figure 3 shows the test circuit.)

$$tr / tf\ out\ (approx) = -(C_{I/O} + C_L) \cdot (R_{DRIVE+} R_{ON}) \cdot \ln(((V_{OH} - V_{OL}) - V_M) / (V_{OH} - V_{OL}))$$

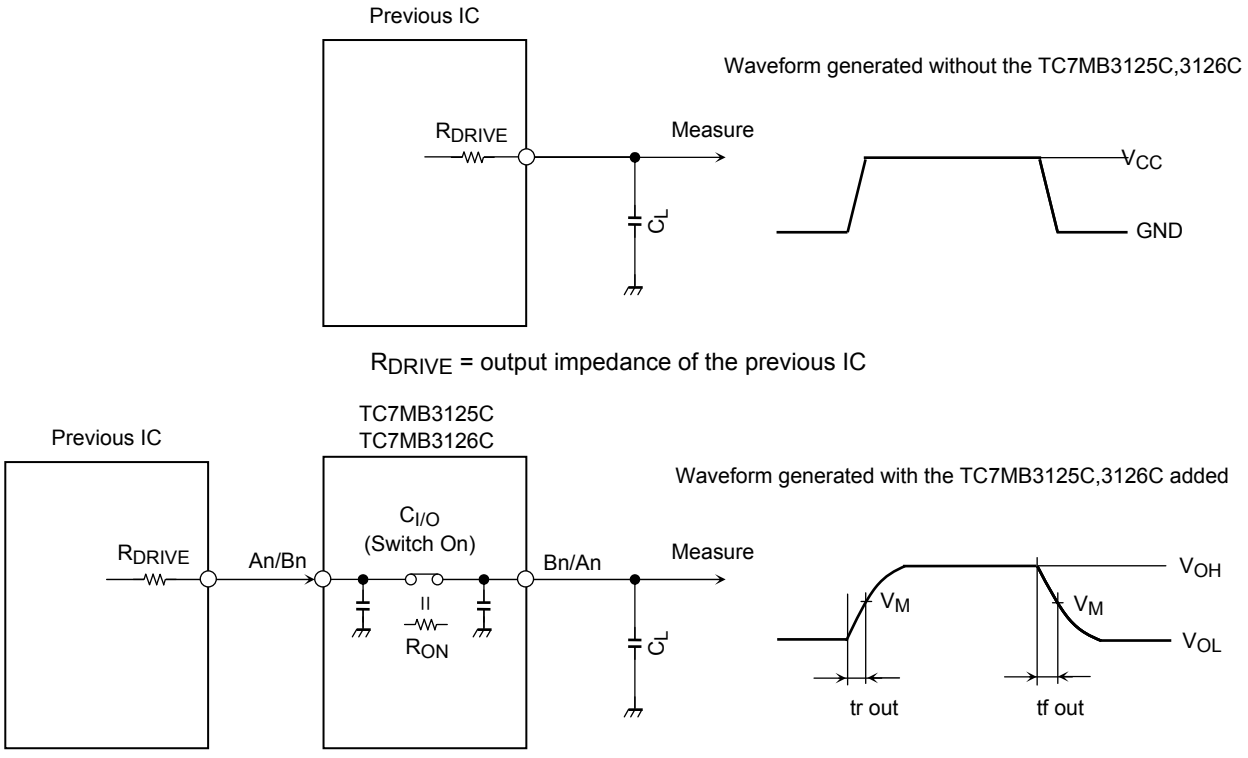
where, R_{DRIVE} is the output impedance of the previous-stage circuit.

Calculation example:

$$tr\ out\ (approx) = -(8 + 15)E\text{-}12 \cdot (120 + 3) \cdot \ln(((4.5 - 0) - 2.25) / (4.5 - 0))$$
$$\approx 2.0\ ns$$

Calculation conditions:

V_{CC} = 4.5V , C_L = 15pF , R_{DRIVE} = 120Ω(output impedance of the previous IC), V_M = 2.25V (V_{CC} / 2)
Output of the previous IC = digital (i.e., high-level voltage = V_{CC}; low-level voltage = GND)

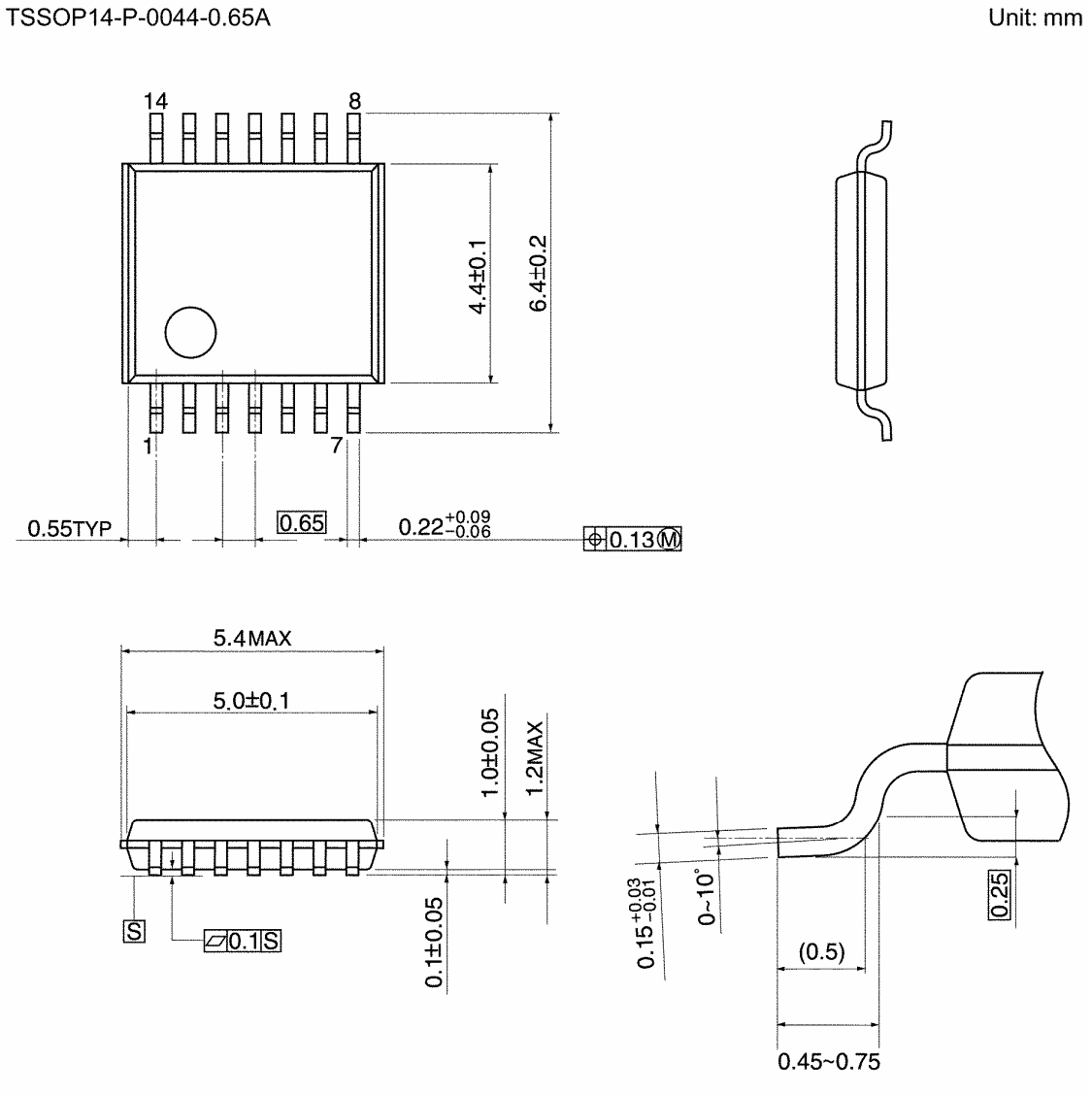


Parameter	V_{CC}
	5.0 ± 0.5 V
V_M	V_{CC} / 2

Figure 3 Test Circuit

Package Dimensions

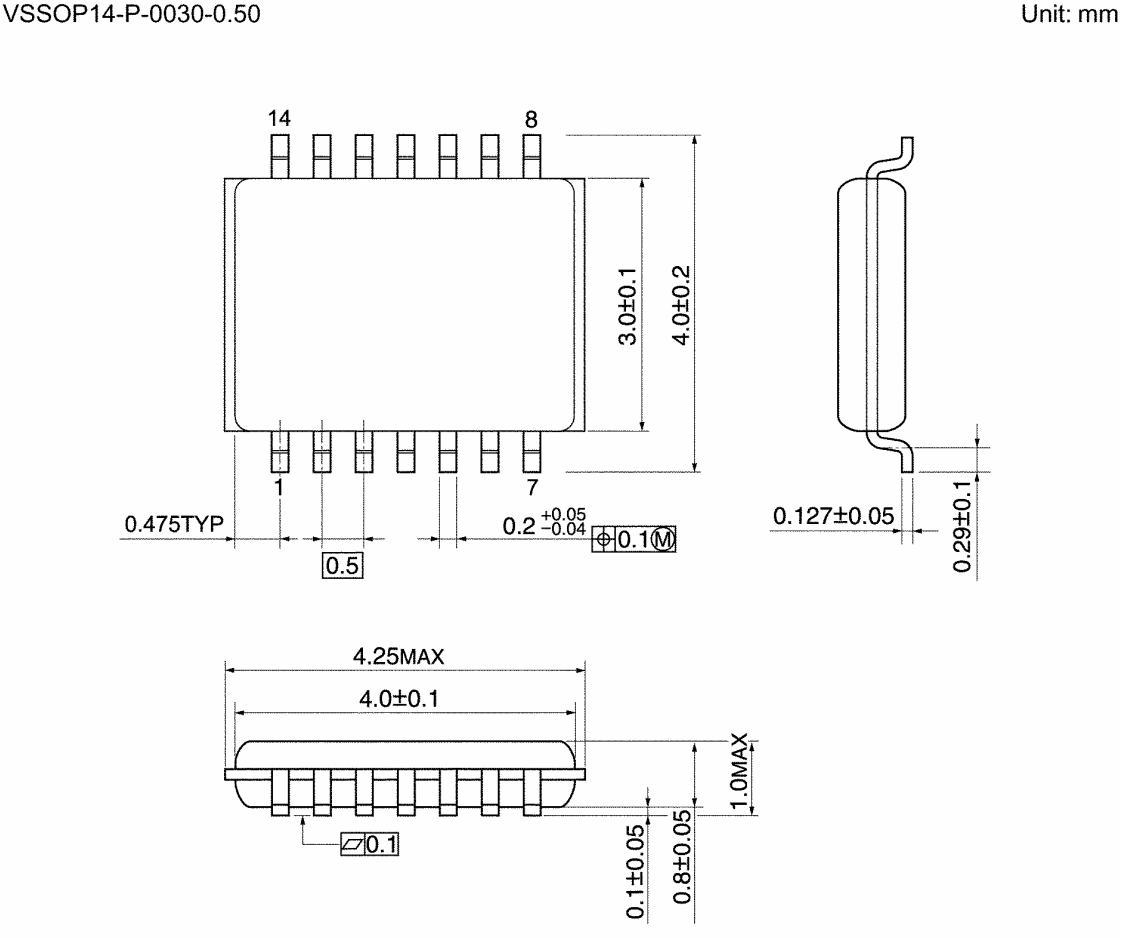
TSSOP14-P-0044-0.65A Unit: mm



Weight: 0.06 g (typ.)

Package Dimensions

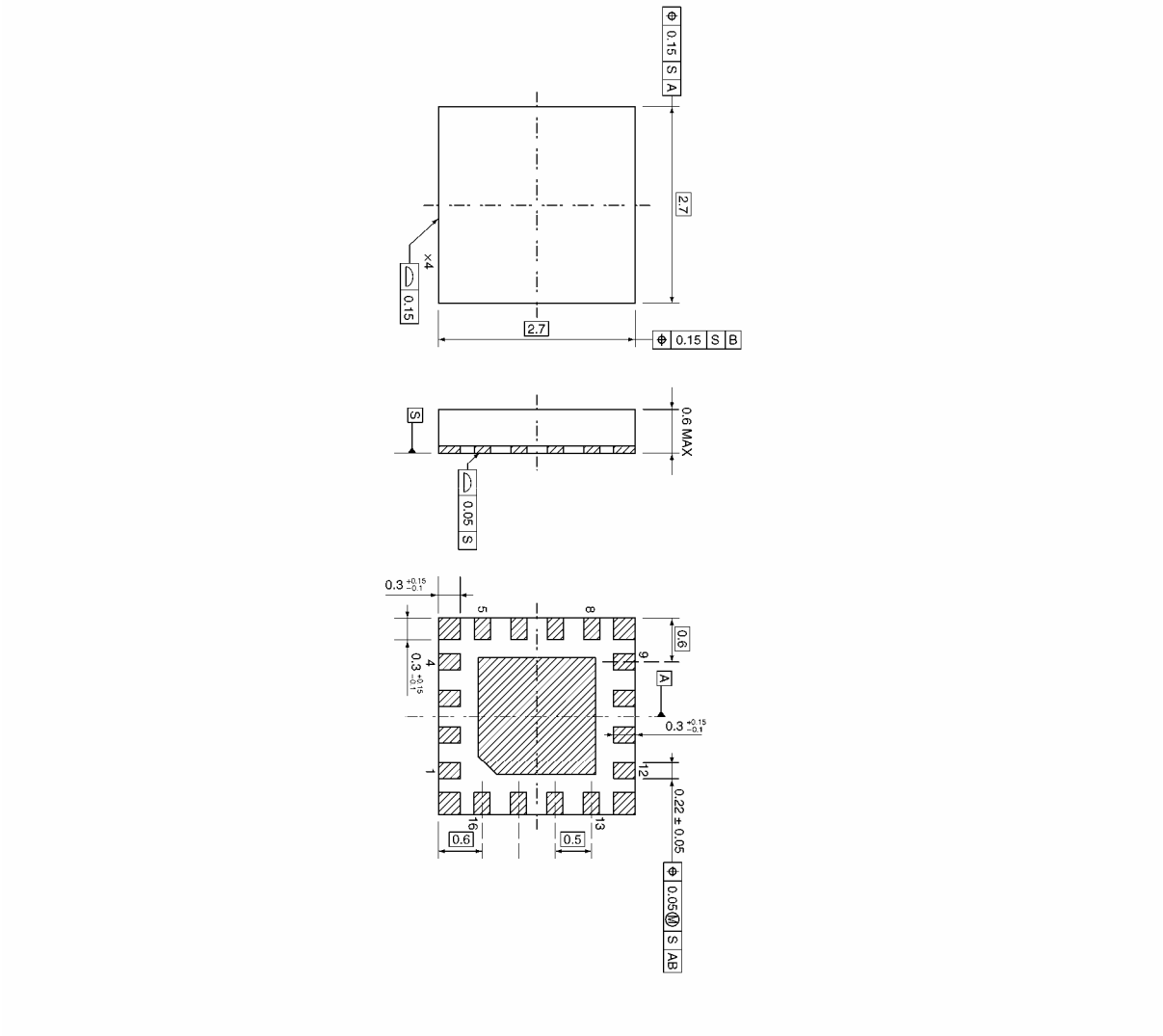
VSSOP14-P-0030-0.50 Unit: mm



Weight: 0.02 g (typ.)

Package Dimensions

VQON16-P-0303-0.50 Unit: mm



Weight: 0.013 g (typ.)

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