



## 32K ´ 8 CMOS STATIC RAM

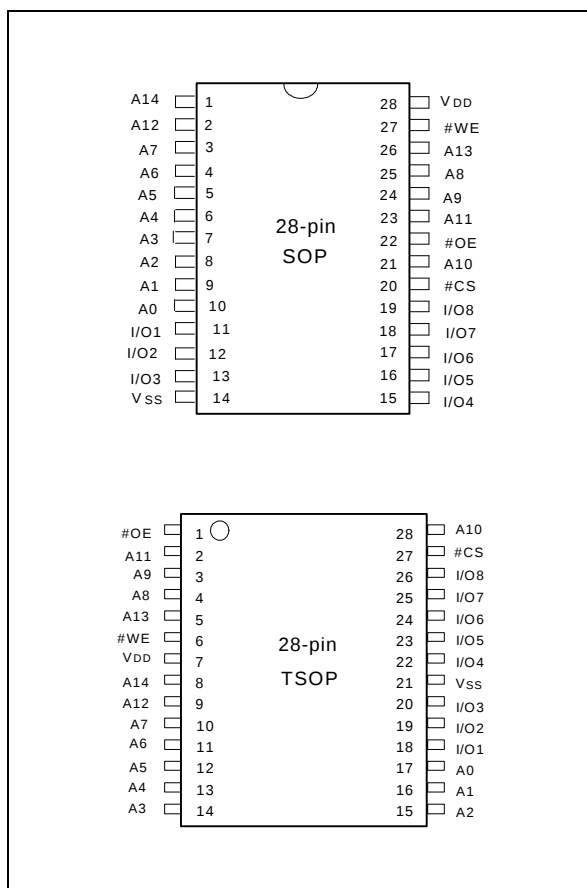
### GENERAL DESCRIPTION

The W24257 is a slow speed, low power CMOS static RAM organized as  $32768 \times 8$  bits that operates on a single 5-volt power supply. This device is manufactured using Winbond's high performance CMOS technology.

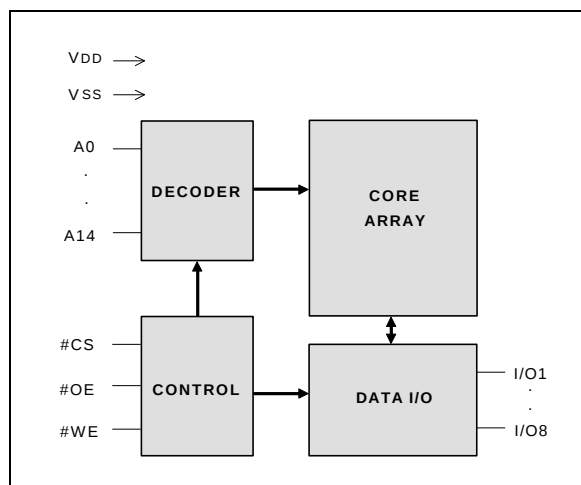
### FEATURES

- Low power consumption:
  - Active: 325 mW (max.)
  - Standby: 75  $\mu$ W (max.) (LL-version)  
150  $\mu$ W (max.) (L-version)
- Access time: 70 nS (max.)
- Single +5V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Battery back-up operation capability
- Data retention voltage: 2V (min.)
- Packaged in 28-pin 330 mil SOP,  
standard type one TSOP (8 mm x 13.4 mm )

### PIN CONFIGURATIONS



### BLOCK DIAGRAM



### PIN DESCRIPTION

| SYMBOL    | DESCRIPTION         |
|-----------|---------------------|
| A0–A14    | Address Inputs      |
| I/O1–I/O8 | Data Inputs/Outputs |
| #CS       | Chip Select Input   |
| #WE       | Write Enable Input  |
| #OE       | Output Enable Input |
| VDD       | Power Supply        |
| VSS       | Ground              |

## TRUTH TABLE

| #CS | #OE | #WE | MODE           | I/O1 - I/O8 | V <sub>DD</sub> CURRENT            |
|-----|-----|-----|----------------|-------------|------------------------------------|
| H   | X   | X   | Not Selected   | High Z      | I <sub>SB</sub> , I <sub>SB1</sub> |
| L   | H   | H   | Output Disable | High Z      | I <sub>DD</sub>                    |
| L   | L   | H   | Read           | Data Out    | I <sub>DD</sub>                    |
| L   | X   | L   | Write          | Data In     | I <sub>DD</sub>                    |

## DC CHARACTERISTICS

### Absolute Maximum Ratings

| PARAMETER                                   | RATING                       | UNIT |
|---------------------------------------------|------------------------------|------|
| Supply Voltage to V <sub>SS</sub> Potential | -0.5 to +7.0                 | V    |
| Input/Output to V <sub>SS</sub> Potential   | -0.5 to V <sub>DD</sub> +0.5 | V    |
| Allowable Power Dissipation                 | 1.0                          | W    |
| Storage Temperature                         | -65 to +150                  | °C   |
| Operating Temperature                       | 0 to +70                     | °C   |

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

### Operating Characteristics

(V<sub>DD</sub> = 5V ±10%, V<sub>SS</sub> = 0V, T<sub>A</sub> = 0 to 70° C for LL/L; -20 to 85° C for LE)

| PARAMETER                      | SYM.             | TEST CONDITIONS                                                                                                                                      | MIN.  | TYP. | MAX.                 | UNIT |    |
|--------------------------------|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|-------|------|----------------------|------|----|
| Input Low Voltage              | V <sub>IL</sub>  | -                                                                                                                                                    | -0.5  | -    | +0.8                 | V    |    |
| Input High Voltage             | V <sub>IH</sub>  | -                                                                                                                                                    | +2.2  | -    | V <sub>DD</sub> +0.5 | V    |    |
| Input Leakage Current          | I <sub>LI</sub>  | V <sub>IN</sub> = V <sub>SS</sub> to V <sub>DD</sub>                                                                                                 | -2    | -    | +2                   | μA   |    |
| Output Leakage Current         | I <sub>LO</sub>  | V <sub>I/O</sub> = V <sub>SS</sub> to V <sub>DD</sub> , #CS = V <sub>IH</sub> (min.) or #OE = V <sub>IH</sub> (min.) or #WE = V <sub>IL</sub> (max.) | -2    | -    | + 2                  | μA   |    |
| Output Low Voltage             | V <sub>OL</sub>  | I <sub>OL</sub> = +4.0 mA                                                                                                                            | -     | -    | 0.4                  | V    |    |
| Output High Voltage            | V <sub>OH</sub>  | I <sub>OH</sub> = -1.0 mA                                                                                                                            | 2.4   | -    | -                    | V    |    |
| Operating Power Supply Current | I <sub>DD</sub>  | #CS = V <sub>IL</sub> (min.),<br>I/O = 0 mA Cycle = min.,<br>Duty = 100%                                                                             | -     | -    | 70                   | mA   |    |
| Standby Power Supply Current   | I <sub>SB</sub>  | #CS = V <sub>IH</sub> (min.)<br>Cycle = min., Duty = 100%                                                                                            | -     | -    | 3                    | mA   |    |
|                                | I <sub>SB1</sub> | #CS ≥ V <sub>DD</sub> -0.2V                                                                                                                          | LL/LE | -    | -                    | 15   | μA |
|                                |                  |                                                                                                                                                      | L     | -    | -                    | 30   | μA |

Note: Typical characteristics are at V<sub>DD</sub> = 5V, T<sub>A</sub> = 25° C.



## CAPACITANCE

( $V_{DD} = 5V$ ,  $T_A = 25^\circ C$ ,  $f = 1\text{ MHz}$ )

| PARAMETER                | SYM.      | CONDITIONS     | MAX. | UNIT |
|--------------------------|-----------|----------------|------|------|
| Input Capacitance        | $C_{IN}$  | $V_{IN} = 0V$  | 6    | pF   |
| Input/Output Capacitance | $C_{I/O}$ | $V_{OUT} = 0V$ | 8    | pF   |

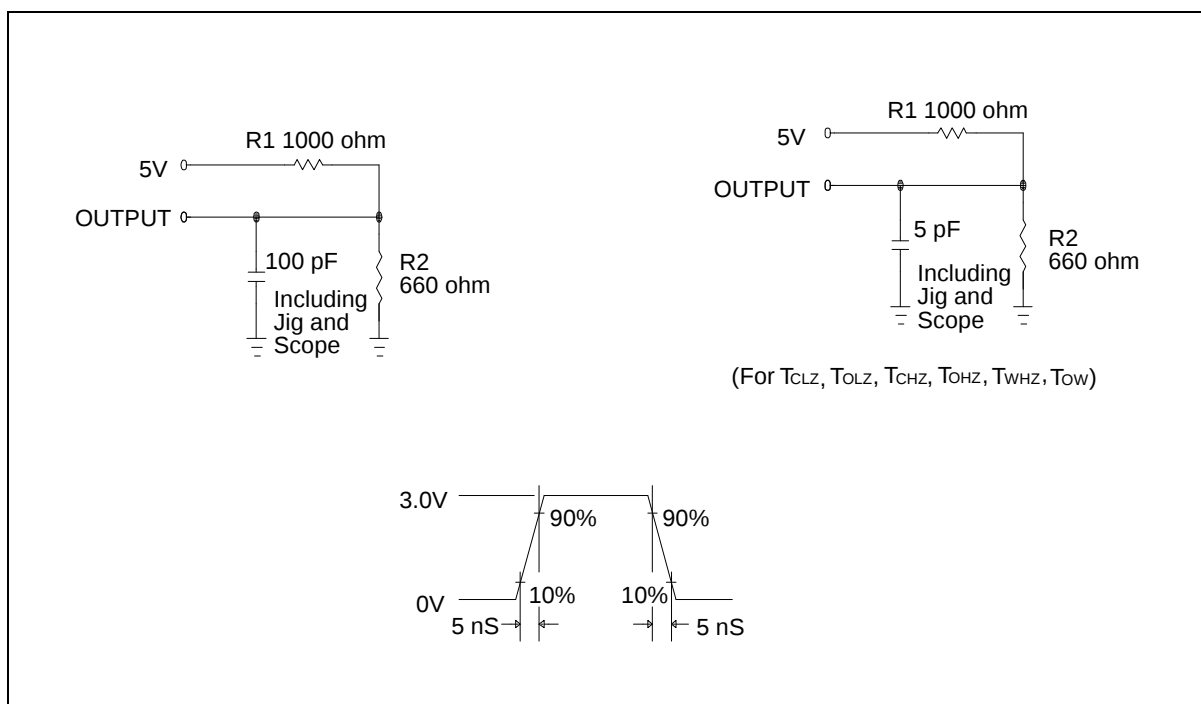
Note: These parameters are sampled but not 100% tested.

## AC CHARACTERISTICS

### AC Test Conditions

| PARAMETER                               | CONDITIONS                                                         |
|-----------------------------------------|--------------------------------------------------------------------|
| Input Pulse Levels                      | 0.6V to 2.4V                                                       |
| Input Rise and Fall Times               | 5 nS                                                               |
| Input and Output Timing Reference Level | 1.5V                                                               |
| Output Load                             | $C_L = 100\text{ pF}$ , $I_{OH}/I_{OL} = -1\text{ mA}/4\text{ mA}$ |

### AC Test Loads and Waveform





AC Characteristics, continued

(V<sub>DD</sub> = 5V ±10%, V<sub>SS</sub> = 0V, T<sub>A</sub> = 0 to 70° C for LL/L; -20 to 85° C for LE)**Read Cycle**

| PARAMETER                            | SYMBOL | W24257-70 |      | UNIT |
|--------------------------------------|--------|-----------|------|------|
|                                      |        | MIN.      | MAX. |      |
| Read Cycle Time                      | TRC    | 70        | -    | nS   |
| Address Access Time                  | TAA    | -         | 70   | nS   |
| Chip Select Access Time              | TACS   | -         | 70   | nS   |
| Output Enable to Output Valid        | TAOE   | -         | 35   | nS   |
| Chip Selection to Output in Low Z    | TCLZ*  | 10        | -    | nS   |
| Output Enable to Output in Low Z     | TOLZ*  | 5         | -    | nS   |
| Chip Deselection to Output in High Z | TCHZ*  | -         | 30   | nS   |
| Output Disable to Output in High Z   | TOHZ*  | -         | 30   | nS   |
| Output Hold from Address Change      | TOH    | 10        | -    | nS   |

\* These parameters are sampled but not 100% tested

**Write Cycle**

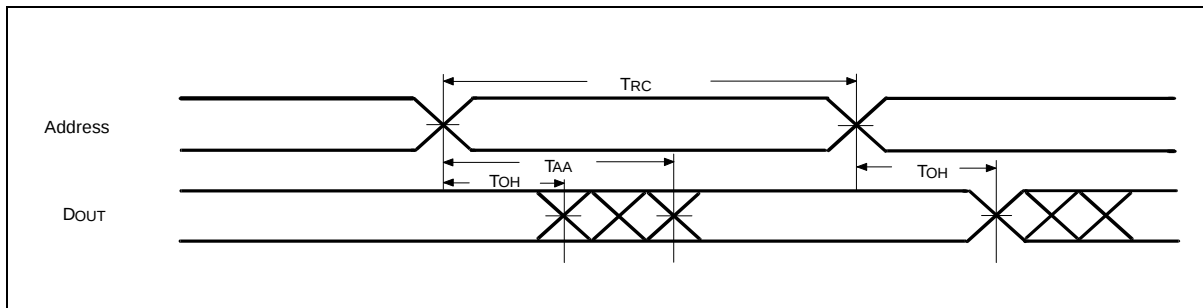
| PARAMETER                          |          | SYMBOL | W24257-70 |      | UNIT |
|------------------------------------|----------|--------|-----------|------|------|
|                                    |          |        | MIN.      | MAX. |      |
| Write Cycle Time                   |          | TWC    | 70        | -    | nS   |
| Chip Selection to End of Write     |          | TCW    | 60        | -    | nS   |
| Address Valid to End of Write      |          | TAW    | 60        | -    | nS   |
| Address Setup Time                 |          | TAS    | 0         | -    | nS   |
| Write Pulse Width                  |          | TWP    | 45        | -    | nS   |
| Write Recovery Time                | #CS, #WE | TWR    | 0         | -    | nS   |
| Data Valid to End of Write         |          | TDW    | 30        | -    | nS   |
| Data Hold from End of Write        |          | TDH    | 0         | -    | nS   |
| Write to Output in High Z          |          | TWHZ*  | -         | 30   | nS   |
| Output Disable to Output in High Z |          | TOHZ*  | -         | 30   | nS   |
| Output Active from End of Write    |          | TOW    | 0         | -    | nS   |

\* These parameters are sampled but not 100% tested

## TIMING WAVEFORMS

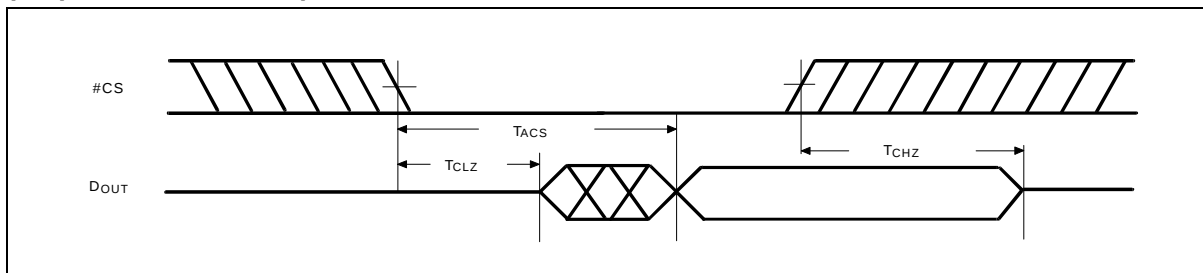
### Read Cycle 1

(Address Controlled)



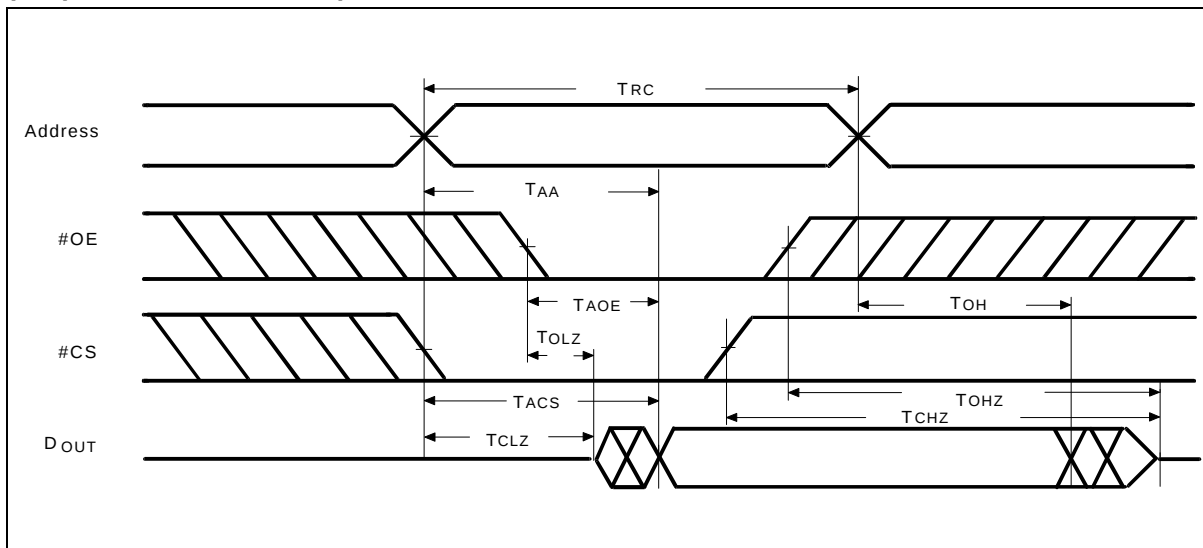
### Read Cycle 2

(Chip Select Controlled)



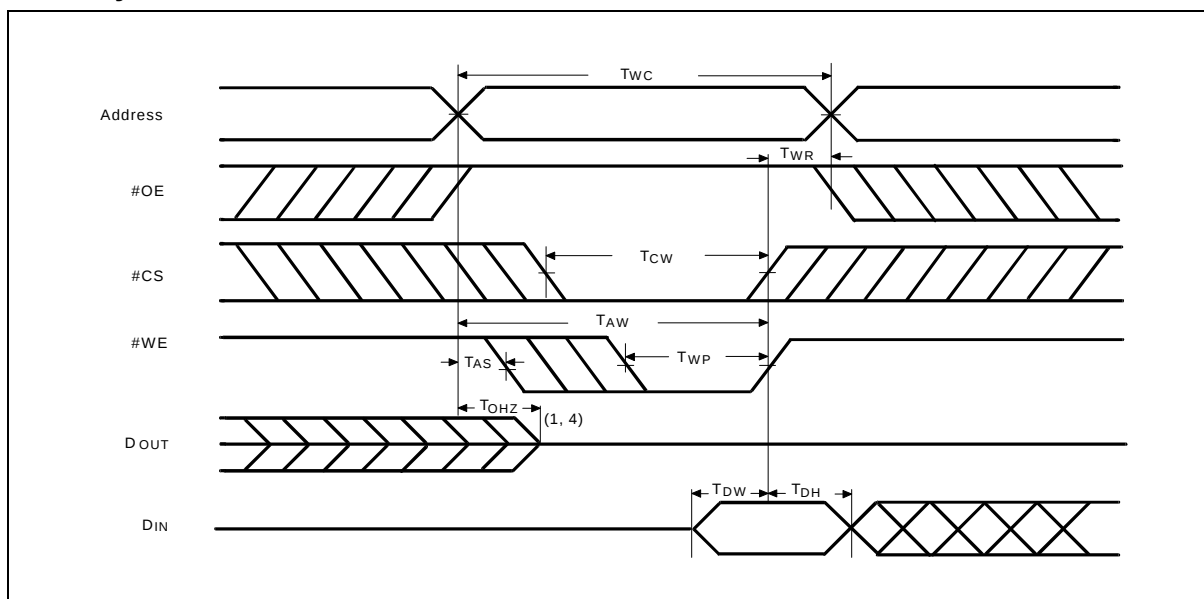
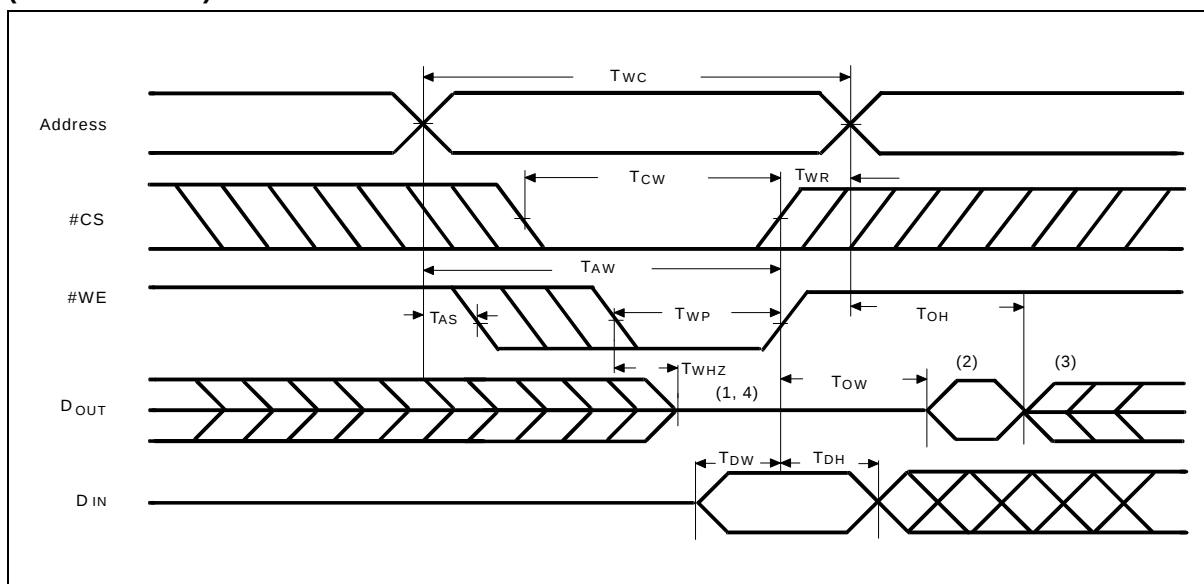
### Read Cycle 3

(Output Enable Controlled)





Timing Waveforms, continued

**Write Cycle 1****Write Cycle 2****( $\overline{\text{OE}} = \text{VIL}$  Fixed)**

Notes:

- During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
- The data output from D<sub>OUT</sub> are the same as the data written to D<sub>IN</sub> during the write cycle.
- D<sub>OUT</sub> provides the read data for the next address.
- Transition is measured  $\pm 500$  mV from steady state with  $C_L = 5$  pF. This parameter is guaranteed but not 100% tested.



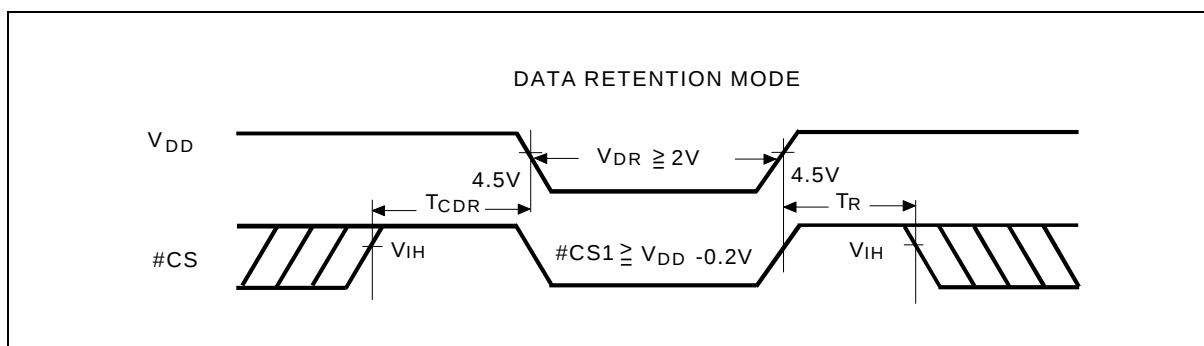
## DATA RETENTION CHARACTERISTICS

( $T_A = 0$  to  $70^\circ\text{C}$  for LL/L;  $-20$  to  $85^\circ\text{C}$  for LE)

| PARAMETER                            | SYM.              | TEST CONDITIONS          | MIN.              | TYP. | MAX. | UNIT             |
|--------------------------------------|-------------------|--------------------------|-------------------|------|------|------------------|
| V <sub>DD</sub> for Data Retention   | V <sub>DR</sub>   | #CS $\geq V_{DD} - 0.2V$ | 2.0               | -    | -    | V                |
| Data Retention Current               | I <sub>DDDR</sub> | #CS $\geq V_{DD} - 0.2V$ | LL/LE             | -    | -    | 15 $\mu\text{A}$ |
|                                      |                   | V <sub>DD</sub> = 3V     | L                 | -    | -    | 30 $\mu\text{A}$ |
| Chip Deselect to Data Retention Time | T <sub>CDR</sub>  | See data retention       | 0                 | -    | -    | nS               |
| Operation Recovery Time              | T <sub>R</sub>    | Waveform                 | T <sub>RC</sub> * | -    | -    | nS               |

T<sub>RC</sub>\* = Read Cycle Time

## DATA RETENTION WAVEFORM



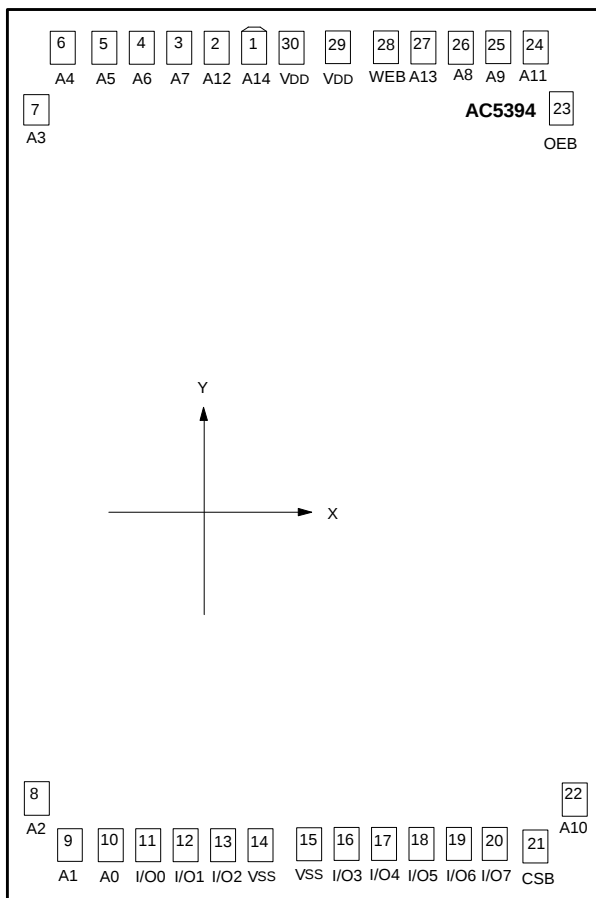
## ORDERING INFORMATION

| PART NO.     | ACCESS TIME (nS) | OPERATING CURRENT MAX. (mA) | STANDBY CURRENT MAX. (mA) | OPERATING TEMP. (°C) | PACKAGE                |
|--------------|------------------|-----------------------------|---------------------------|----------------------|------------------------|
| W24257S-70LL | 70               | 70                          | 15                        | 0 to 70              | 330 mil SOP            |
| W24257S-70L  | 70               | 70                          | 30                        | 0 to 70              | 330 mil SOP            |
| W24257S-70LE | 70               | 70                          | 15                        | -20 to 85            | 330 mil SOP            |
| W24257Q-70LL | 70               | 70                          | 15                        | 0 to 70              | Standard type one TSOP |
| W24257Q-70L  | 70               | 70                          | 30                        | 0 to 70              | Standard type one TSOP |
| W24257Q-70LE | 70               | 70                          | 15                        | -20 to 85            | Standard type one TSOP |

Notes:

- Winbond reserves the right to make changes to its products without prior notice.
- Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

## BONDING PAD DIAGRAM

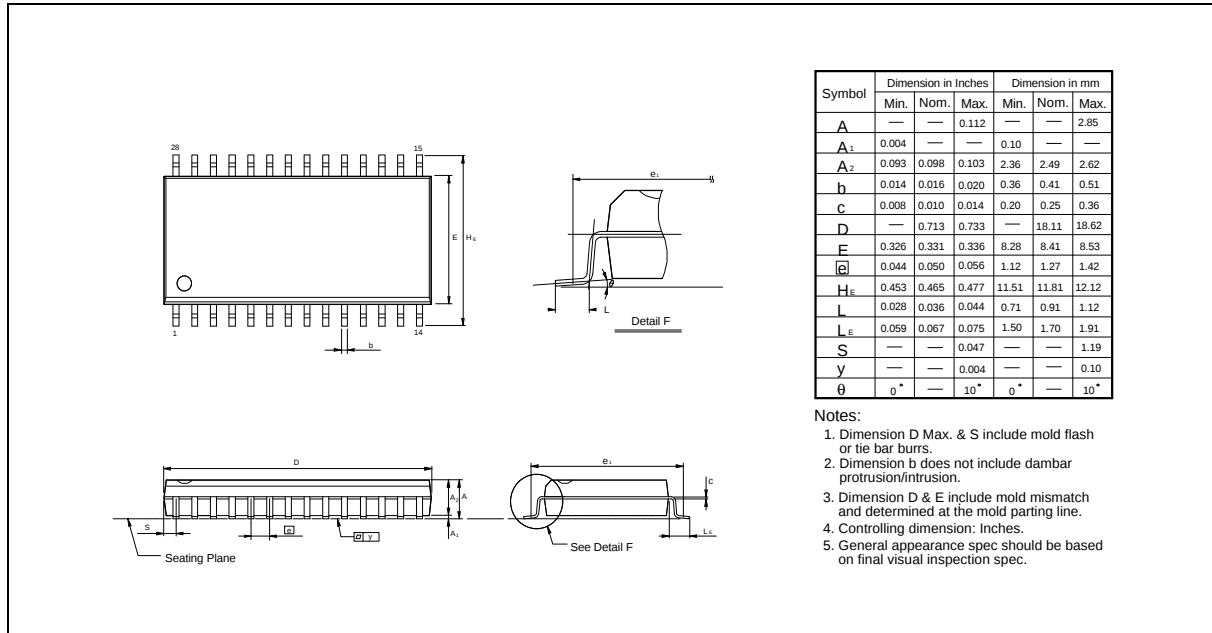


| PAD NO. | X       | Y        |
|---------|---------|----------|
| 1       | -232.25 | 1445.22  |
| 2       | -351.70 | 1445.22  |
| 3       | -471.15 | 1445.22  |
| 4       | -590.60 | 1445.22  |
| 5       | -710.05 | 1445.22  |
| 6       | -829.50 | 1445.22  |
| 7       | -992.79 | 1362.24  |
| 8       | -992.79 | -1306.11 |
| 9       | -857.86 | -1452.79 |
| 10      | -738.41 | -1452.79 |
| 11      | -594.84 | -1414.13 |
| 12      | -451.06 | -1414.13 |
| 13      | -310.67 | -1414.13 |
| 14      | -171.78 | -1405.28 |
| 15      | 24.45   | -1405.28 |
| 16      | 151.80  | -1414.13 |
| 17      | 298.07  | -1414.13 |
| 18      | 443.28  | -1414.13 |
| 19      | 588.20  | -1414.13 |
| 20      | 732.84  | -1414.13 |
| 21      | 871.11  | -1452.79 |
| 22      | 992.75  | -1312.15 |
| 23      | 992.75  | 1373.67  |
| 24      | 810.09  | 1445.22  |
| 25      | 690.64  | 1445.22  |
| 26      | 571.19  | 1445.22  |
| 27      | 451.74  | 1445.22  |
| 28      | 332.29  | 1445.22  |
| 29      | 120.25  | 1444.65  |
| 30      | -93.23  | 1444.65  |

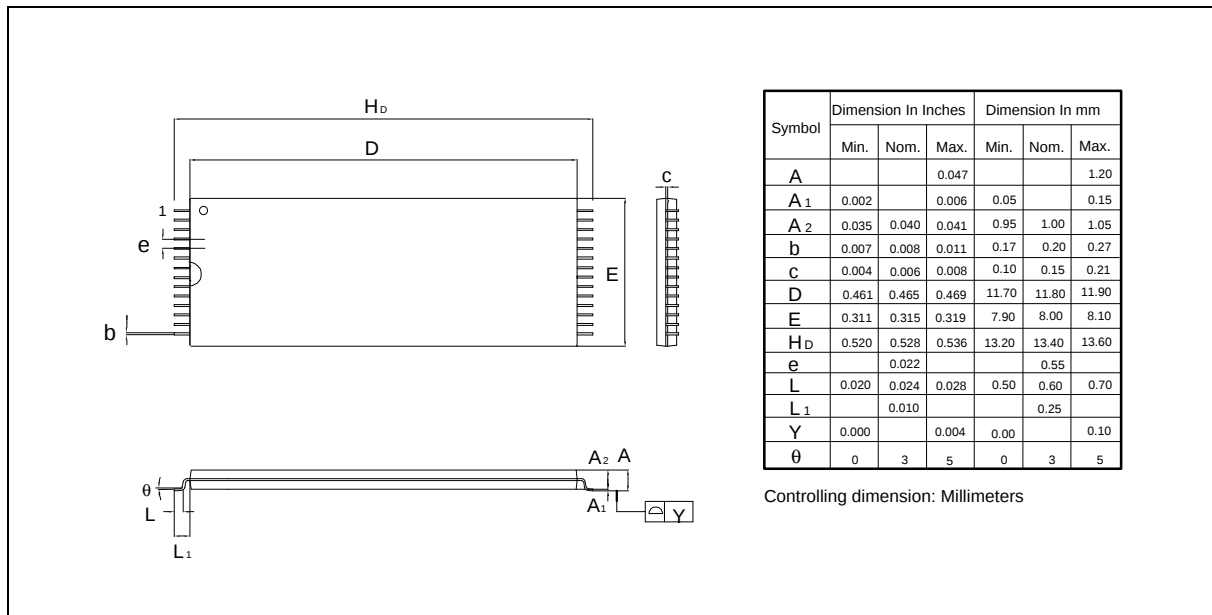
Note: For bare chip form (C.O.B.) applications, the substrate must be connected to VDD or left floating in the PCB layout.

## PACKAGE DIMENSIONS

### 28-pin SO Wide Body



### 28-pin Standard Type One TSOP





## VERSION HISTORY

| VERSION | DATE      | PAGE    | DESCRIPTION                                          |
|---------|-----------|---------|------------------------------------------------------|
| A12     | Nov. 1999 | 1, 2, 7 | Change the IDD, ISB, ISB1                            |
|         |           | 4, 7    | Remove the W24257-10 spc.                            |
| A13     | Apr. 2000 | 7       | Typo correction in Standby Current Max.: mA->μA      |
| A14     | May 2000  | 1, 7, 8 | Delete 28-pin DIP Package                            |
|         |           | 8       | Add in Bonding Pad Diagram                           |
| A15     | Nov. 2000 | 2       | Modify Operating Power Supply Current (IDD) as 70 mA |
|         |           | 1       | Add in TSOP Pin Configuration                        |
| A16     | Feb. 2001 | 2, 4, 7 | Add in LE grade                                      |



### Headquarters

No. 4, Creation Rd. III,  
Science-Based Industrial Park,  
Hsinchu, Taiwan  
TEL: 886-3-5770066  
FAX: 886-3-5796096  
<http://www.winbond.com.tw/>  
Voice & Fax-on-demand: 886-2-27197006

### Taipei Office

11F, No. 115, Sec. 3, Min-Sheng East Rd.,  
Taipei, Taiwan  
TEL: 886-2-27190505  
FAX: 886-2-27197502

### Winbond Electronics (H.K.) Ltd.

Unit 9-15, 22F, Millennium City,  
No. 378 Kwun Tong Rd;  
Kowloon, Hong Kong  
TEL: 852-27513100  
FAX: 852-27552064

### Winbond Electronics North America Corp

**Winbond Memory Lab.**  
**Winbond Microelectronics Corp.**  
**Winbond Systems Lab.**  
2727 N. First Street, San Jose,  
CA 95134, U.S.A.  
TEL: 408-9436666  
FAX: 408-5441798

Note: All data and specifications are subject to change without notice.