

Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D $T_A = 25^\circ C$
40V	30m Ω @ $V_{GS} = 10V$	13.8A
	54m Ω @ $V_{GS} = 4.5V$	10.3A

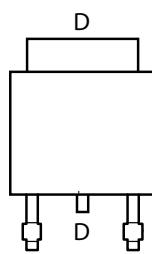
Description and Applications

This new generation MOSFET has been designed to minimize the on-state resistance ($R_{DS(on)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

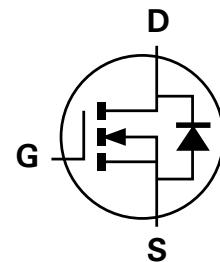
- Backlighting
- DC-DC Converters
- Power management functions



Top View



Top View
Pin-Out



Equivalent Circuit

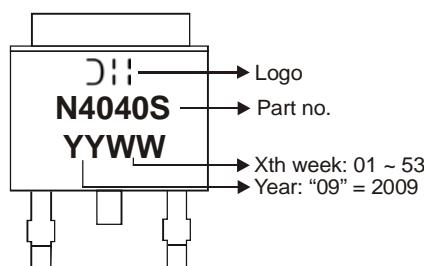
Ordering Information (Note 3)

Part Number	Case	Packaging
DMN4040SK3-13	TO252-3L	2500 / Tape & Reel

Notes:

1. No purposefully added lead.
2. Diodes Inc.'s "Green" policy can be found on our website at <http://www.diodes.com>.
3. For packaging details, go to our website at <http://www.diodes.com>.

Marking Information



Maximum Ratings @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	40	V
Gate-Source Voltage			V_{GSS}	± 20	V
Continuous Drain Current (Note 4) $V_{GS} = 10\text{V}$	Steady State	$T_A = 25^\circ\text{C}$ $T_A = 70^\circ\text{C}$	I_D	6.0 4.8	A
Continuous Drain Current (Note 5) $V_{GS} = 10\text{V}$	Steady State	$T_A = 25^\circ\text{C}$ $T_A = 70^\circ\text{C}$	I_D	9.3 7.4	A
Continuous Drain Current (Note 5) $V_{GS} = 10\text{V}$	$t \leq 10\text{s}$	$T_A = 25^\circ\text{C}$ $T_A = 70^\circ\text{C}$	I_D	13.8 11.0	A
Continuous Drain Current (Note 5) $V_{GS} = 4.5\text{V}$	Steady State	$T_A = 25^\circ\text{C}$ $T_A = 70^\circ\text{C}$	I_D	6.9 5.5	A
Continuous Drain Current (Note 5) $V_{GS} = 4.5\text{V}$	$t \leq 10\text{s}$	$T_A = 25^\circ\text{C}$ $T_A = 70^\circ\text{C}$	I_D	10.3 8.2	A
Pulsed Drain Current (Note 6)			I_{DM}	50	A

Thermal Characteristics

Characteristic	Symbol	Max	Unit
Power Dissipation (Note 4)	P_D	1.71	W
Thermal Resistance, Junction to Ambient @ $T_A = 25^\circ\text{C}$ (Note 4)	$R_{\theta JA}$	72.9	°C/W
Power Dissipation (Note 5)	P_D	4.1	W
Thermal Resistance, Junction to Ambient @ $T_A = 25^\circ\text{C}$ (Note 5)	$R_{\theta JA}$	30.8	°C/W
Power Dissipation (Note 5) $t \leq 10\text{s}$	P_D	8.9	W
Thermal Resistance, Junction to Ambient @ $T_A = 25^\circ\text{C}$ (Note 5) $t \leq 10\text{s}$	$R_{\theta JA}$	14	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics @ $T_A = 25^\circ\text{C}$ unless otherwise stated

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	40	-	-	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
Zero Gate Voltage Drain Current $T_J = 25^\circ\text{C}$	I_{DSS}	-	-	1.0	μA	$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	-	-	± 100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.3	3.0	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(\text{ON})}$	-	20	30	$\text{m}\Omega$	$V_{GS} = 10\text{V}, I_D = 12\text{A}$
		-	43	54		$V_{GS} = 4.5\text{V}, I_D = 6\text{A}$
Forward Transfer Admittance	$ Y_{fs} $	-	11	-	S	$V_{DS} = 5\text{V}, I_D = 12\text{A}$
Diode Forward Voltage	V_{SD}	-	0.76	1.0	V	$V_{GS} = 0\text{V}, I_S = 1\text{A}$
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	-	945	-	pF	$V_{DS} = 20\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	-	69	-		
Reverse Transfer Capacitance	C_{rss}	-	58	-		
Gate Resistance	R_g	-	1.45	-	Ω	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$
Total Gate Charge $V_{GS} = 4.5\text{V}$	Q_g	-	8.4	-	nC	$V_{GS} = 4.5\text{V}, V_{DS} = 20\text{V}, I_D = 12\text{A}$
Total Gate Charge $V_{GS} = 10\text{V}$	Q_g	-	18.6	-		
Gate-Source Charge	Q_{gs}	-	3.3	-		
Gate-Drain Charge	Q_{gd}	-	2.2	-	ns	$V_{GS} = 10\text{V}, V_{DS} = 20\text{V}, I_D = 12\text{A}$
Turn-On Delay Time	$t_{D(on)}$	-	6.4	-		
Turn-On Rise Time	t_r	-	9.7	-		
Turn-Off Delay Time	$t_{D(off)}$	-	19.8	-		
Turn-Off Fall Time	t_f	-	3.1	-		

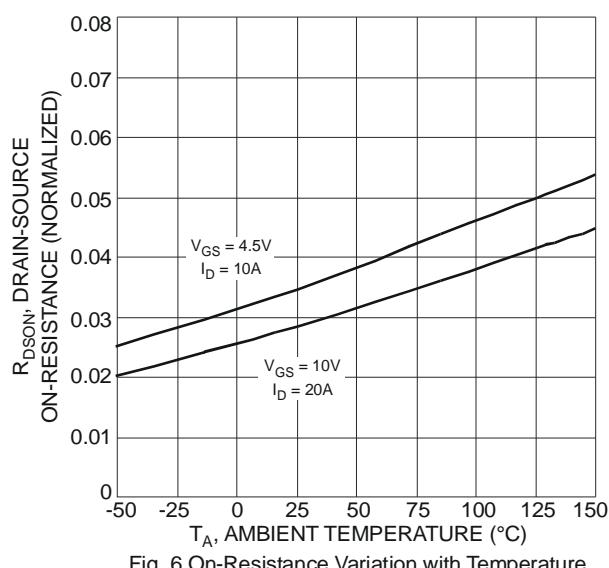
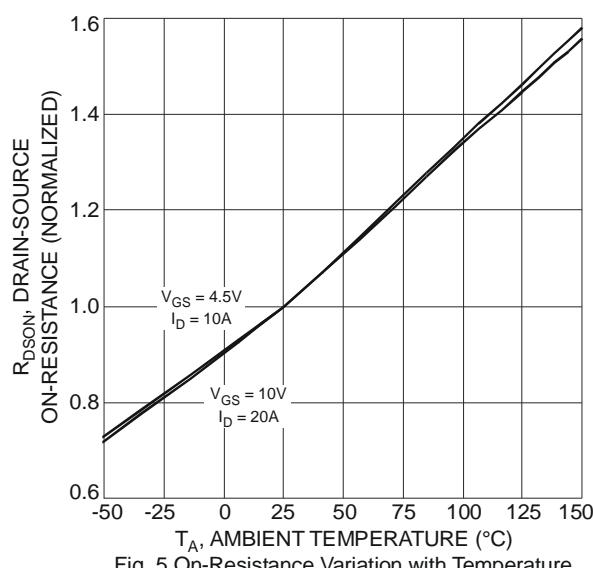
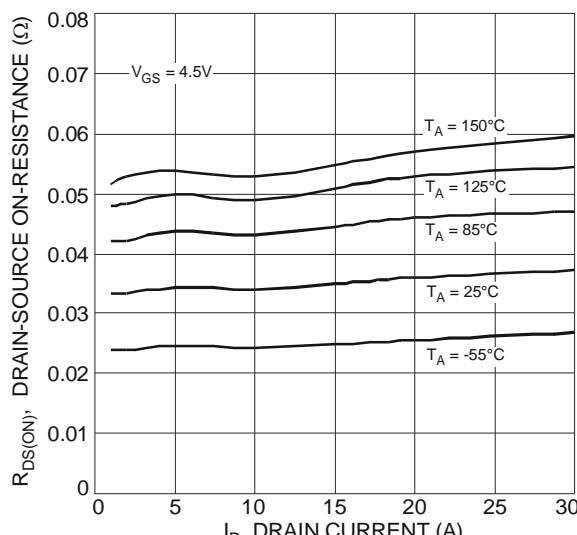
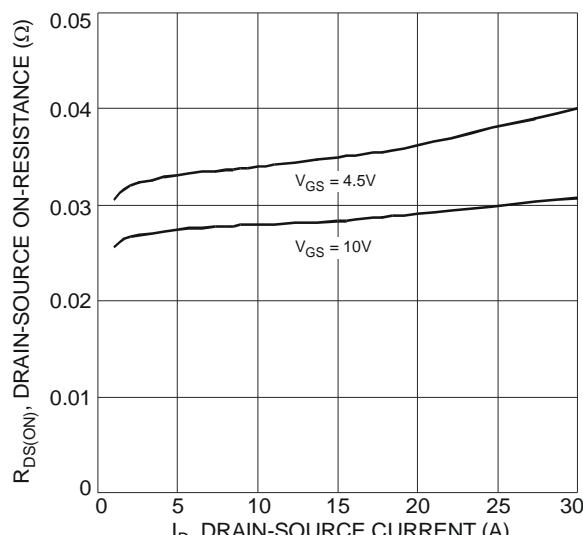
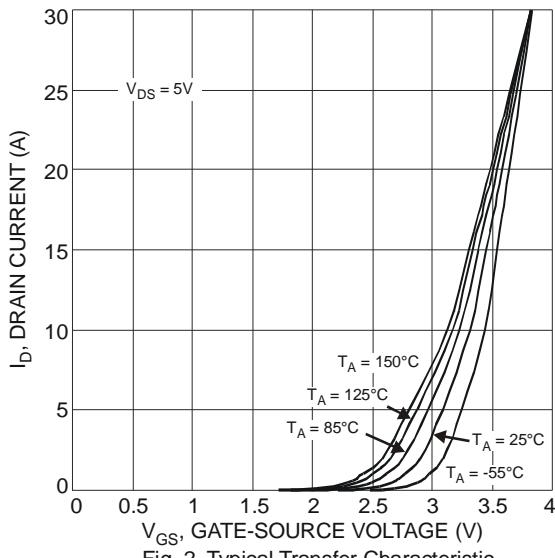
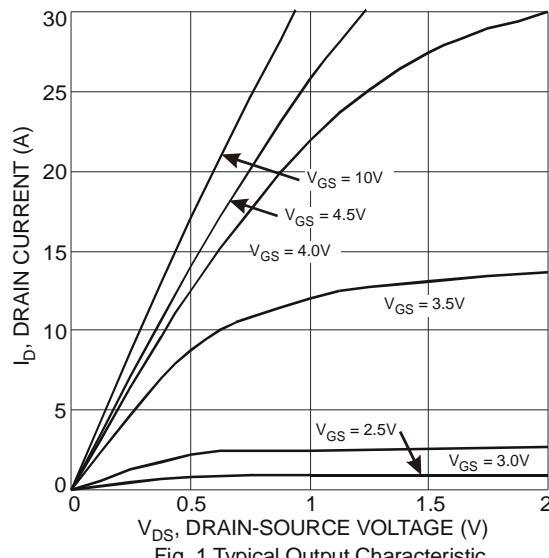
Notes: 4. Device mounted on FR-4 PCB with minimum recommended pad layout, single sided.

5. Device mounted on 2" x 2" FR-4 PCB with high coverage 2 oz. Copper, single sided.

6. Repetitive rating, pulse width limited by junction temperature.

7. Short duration pulse test used to minimize self-heating effect.

8. Guaranteed by design. Not subject to production testing.



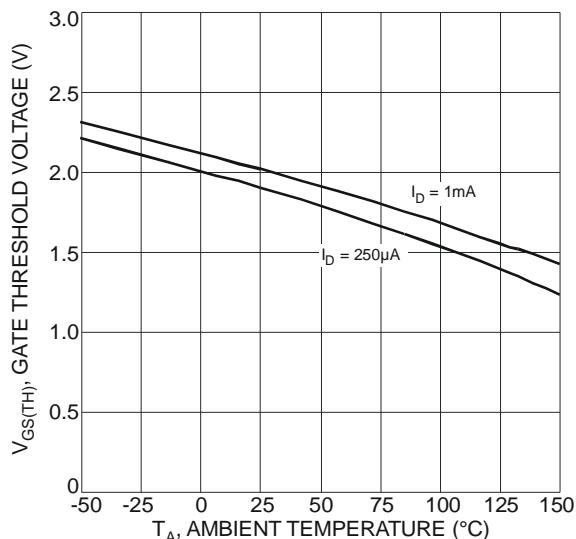


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

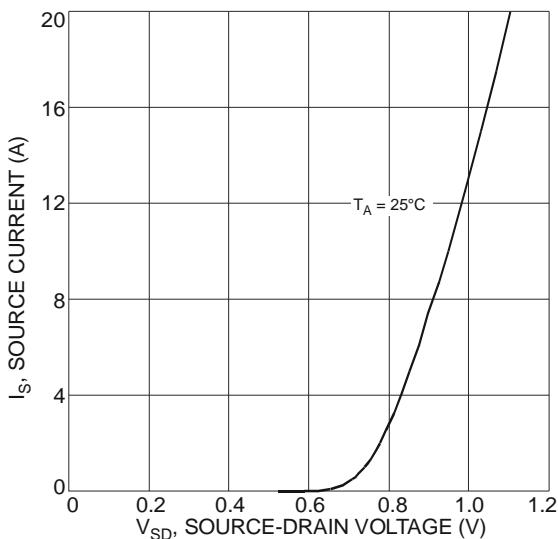


Fig. 8 Diode Forward Voltage vs. Current

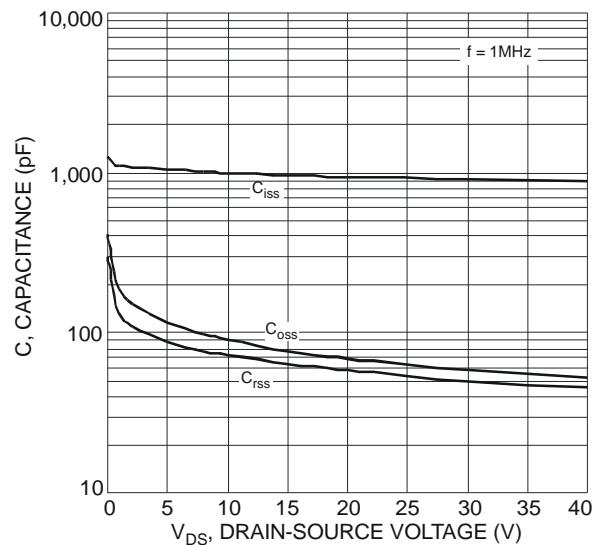


Fig. 9 Typical Total Capacitance

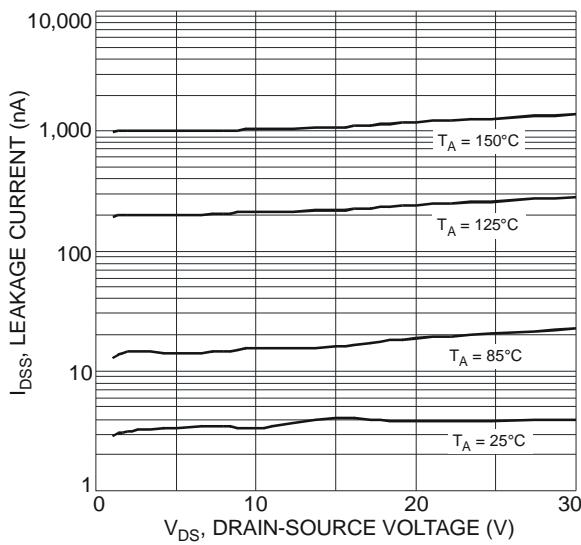


Fig. 10 Typical Leakage Current
vs. Drain-Source Voltage

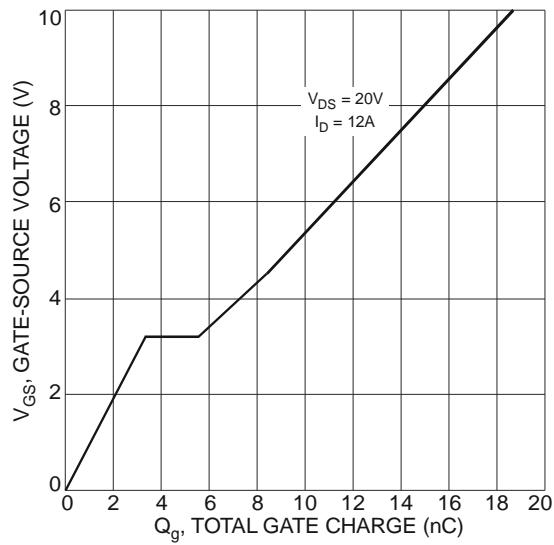
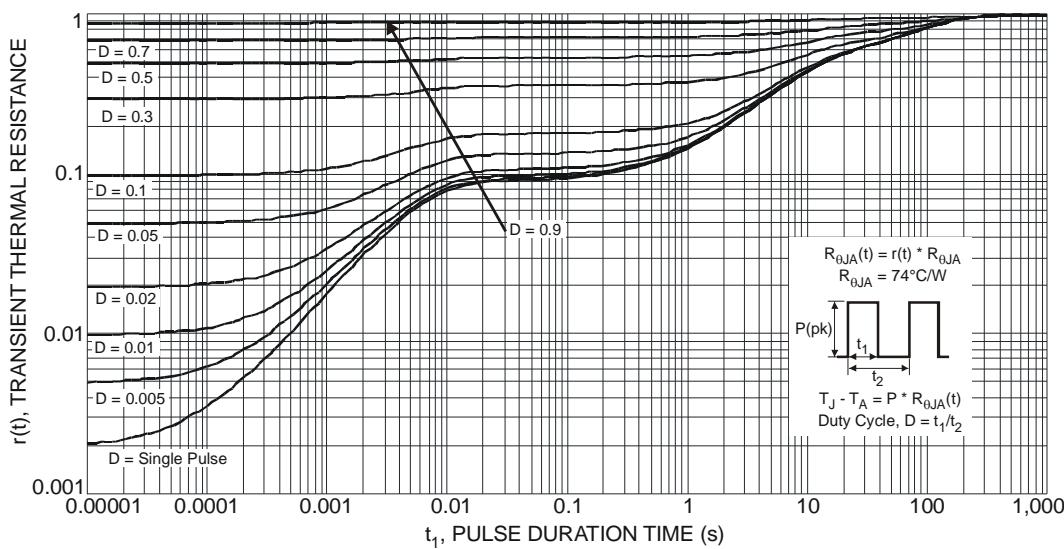
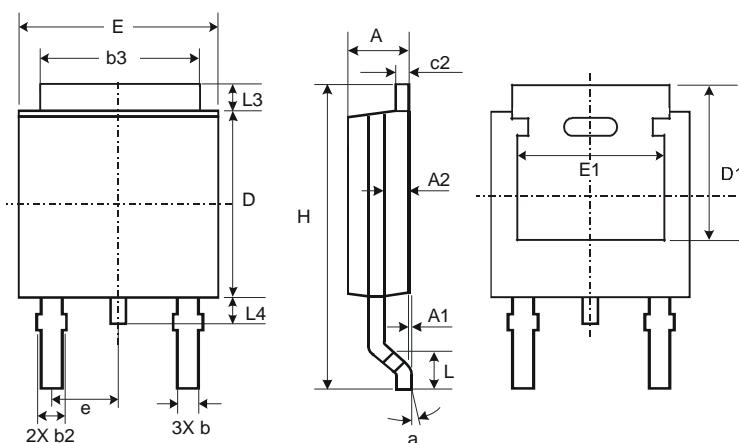


Fig. 11 Gate-Charge Characteristics



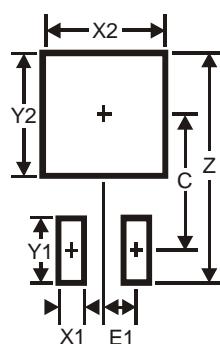
Package Outline Dimensions



TO252-3L			
Dim	Min	Max	Typ
A	2.19	2.39	2.29
A1	0.00	0.13	0.08
A2	0.97	1.17	1.07
b	0.64	0.88	0.783
b2	0.76	1.14	0.95
b3	5.21	5.46	5.33
c2	0.45	0.58	0.531
D	6.00	6.20	6.10
D1	5.21	—	—
e	—	—	2.286
E	6.45	6.70	6.58
E1	4.32	—	—
H	9.40	10.41	9.91
L	1.40	1.78	1.59
L3	0.88	1.27	1.08
L4	0.64	1.02	0.83
a	0°	10°	—

All Dimensions in mm

Suggested Pad Layout



Dimensions	Value (in mm)
Z	11.6
X1	1.5
X2	7.0
Y1	2.5
Y2	7.0
C	6.9
E1	2.3

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