



3.3V CMOS DUAL J- \bar{K} FLIP-FLOP WITH SET AND RESET, POSITIVE-EDGE TRIG- GER, AND 5 VOLT TOLERANT I/O

IDT74LVC109A

FEATURES:

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- 1.27mm pitch SOIC, 0.635mm pitch QSOP,
0.65mm pitch SSOP, 0.65mm pitch TSSOP packages
- Extended commercial range of - 40°C to +85°C
- V_{CC} = 3.3V \pm 0.3V, Normal Range
- V_{CC} = 2.3V to 3.6V, Extended Range
- CMOS power levels (0.4 μ W typ. static)
- Rail-to-Rail output swing for increased noise margin
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

Drive Features for LVC109A:

- High Output Drivers: \pm 24mA
- Reduced system switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

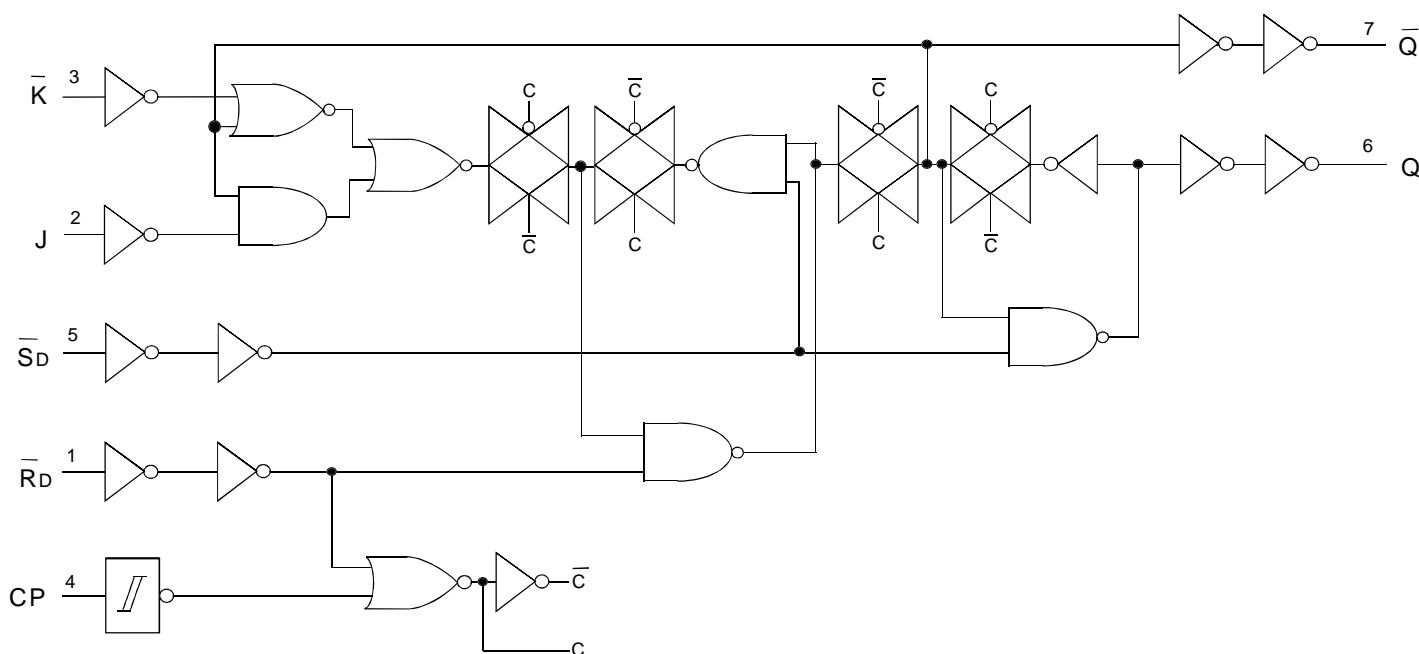
DESCRIPTION:

The LVC109A dual J- \bar{K} flip-flop with set and reset, positive-edge trigger is built using advanced dual metal CMOS technology. This device features individual J, \bar{K} inputs, clock (CP) inputs, set (\bar{S}_D) and reset (\bar{R}_D) inputs; also complementary Q and \bar{Q} outputs. The set and reset are asynchronous active low inputs and operate independently of the clock input. The J and \bar{K} inputs control the state changes of the flip-flops as described in the function table. The J and \bar{K} inputs must be stable one setup time prior to the low-to-high clock transition for predictable operation. The J- \bar{K} design allows operation as a D-type flip-flop by tying the J and \bar{K} inputs together.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

The LVC109A has been designed with a \pm 24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

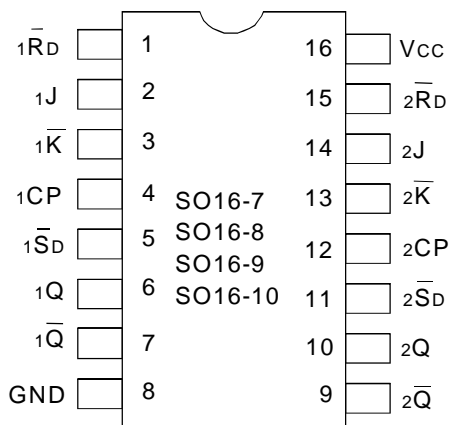
FUNCTIONAL BLOCK DIAGRAM



NOTE:

Pin numbers are for section 1. Refer to pin configuration for section 2 pin numbers.

PIN CONFIGURATION



QSOP/ SOIC/ SSOP/ TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

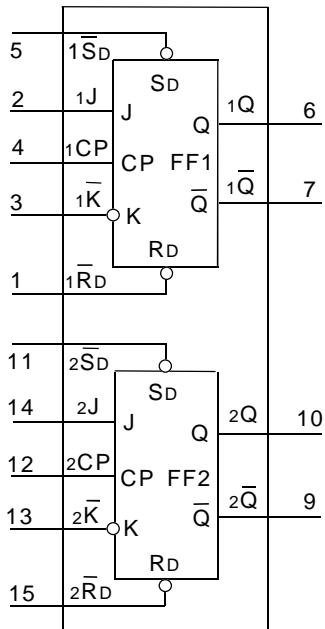
Symbol	Description	Max.	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	- 0.5 to +6.5	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	- 0.5 to +6.5	V
T _{STG}	Storage Temperature	- 65 to +150	°C
I _{OUT}	DC Output Current	- 50 to +50	mA
I _{IK} I _{OK}	Continuous Clamp Current, V _I < 0 or V _O < 0	- 50	mA
I _{CC} I _{SS}	Continuous Current through each V _{CC} or GND	±100	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC}.

FUNCTIONAL DIAGRAM



CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	6.5	8	pF

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NOTE:

- As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
xCP	Clock Inputs, LOW-to-HIGH, edge-triggered
xRD	Asynchronous Reset Input (Active LOW)
xSD	Asynchronous Set Inputs (Active LOW)
xJ, xK	Synchronous Inputs
xQ	True Flip-Flop Outputs
xQ-bar	Complement Flip-Flop Outputs

FUNCTION TABLE (1)

Operating Modes	Inputs					Outputs	
	\overline{xSD}	\overline{xRD}	xCP	xJ	\overline{xK}	xQ	\overline{xQ}
Asynchronous set	L	H	X	X	X	H	L
Asynchronous reset	H	L	X	X	X	L	H
Undetermined	L	L	X	X	X	H	H
Toggle	H	H	↑	h	l	$\overline{Q_0}$	Q_0
Load "0" (reset)	H	H	↑	l	l	L	H
Load "1" (set)	H	H	↑	h	h	H	L
Hold "no change"	H	H	↑	l	h	Q_0	$\overline{Q_0}$

NOTE:

- H = HIGH voltage level
h = HIGH voltage level of input set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level of input set-up time prior to LOW-to-HIGH CP transition
X = Don't care
↑ = LOW-to-HIGH CP Transition
 Q_0 = Level of Q before the indicated steady-state input conditions were established.
 $\overline{Q_0}$ = Complement of Q_0 or level of \overline{Q} before the indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = - 40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V_{IH}	Input HIGH Voltage Level	$V_{CC} = 2.3V$ to $2.7V$		1.7	—	—	V
		$V_{CC} = 2.7V$ to $3.6V$		2	—	—	
V_{IL}	Input LOW Voltage Level	$V_{CC} = 2.3V$ to $2.7V$		—	—	0.7	V
		$V_{CC} = 2.7V$ to $3.6V$		—	—	0.8	
I_{IH} I_{IL}	Input Leakage Current	$V_{CC} = 3.6V$	$V_I = 0$ to $5.5V$	—	—	±5	μA
I_{OZH} I_{OZL}	High Impedance Output Current (3-State Output pins)	$V_{CC} = 3.6V$	$V_O = 0$ to $5.5V$	—	—	±10	μA
I_{OFF}	Input/Output Power Off Leakage	$V_{CC} = 0V$, V_{IN} or $V_O \leq 5.5V$		—	—	±50	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = 2.3V$, $I_{IN} = -18mA$		—	-0.7	-1.2	V
V_H	Input Hysteresis	$V_{CC} = 3.3V$		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = 3.6V$	$V_{IN} = GND$ or V_{CC}	—	—	10	μA
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at $V_{CC} - 0.6V$ other inputs at V_{CC} or GND		—	—	500	μA

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NOTE:

- Typical values are at $V_{CC} = 3.3V$, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = – 0.1mA	VCC – 0.2	—	V
		VCC = 2.3V	IOH = – 6mA	2	—	
		VCC = 2.3V	IOH = – 12mA	1.7	—	
		VCC = 2.7V		2.2	—	
		VCC = 3.0V		2.4	—	
		VCC = 3.0V	IOH = – 24mA	2.2	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IOL = 0.1mA	—	0.2	V
		VCC = 2.3V	IOL = 6mA	—	0.4	
			IOL = 12mA	—	0.7	
		VCC = 2.7V	IOL = 12mA	—	0.4	
		VCC = 3.0V	IOL = 24mA	—	0.55	

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NOTE:

1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range. TA = – 40°C to +85°C.

OPERATING CHARACTERISTICS, TA = 25°C

Symbol	Parameter	Test Conditions	VCC = 2.5V±0.2V	VCC = 3.3V±0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance per flip-flop	CL = 0pF, f = 10Mhz	—	—	pF

SWITCHING CHARACTERISTICS ⁽¹⁾

Symbol	Parameter	VCC = 2.5V±0.2V		VCC = 2.7V		VCC = 3.3V±0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
tPLH	Propagation Delay	—	9	—	8.5	—	7.5	ns
tPHL	xCP to xQ or xQ̄	—	—	—	—	—	—	
tPLH	Propagation Delay	—	11	—	9	—	8	ns
	xSD̄ to xQ or xRD̄ to Q̄	—	—	—	—	—	—	
tPHL	Propagation Delay	—	10	—	10	—	9	ns
	xSD̄ to xQ or xRD̄ to Q̄	—	—	—	—	—	—	
tsu	Set-up Time, xJ, xK̄ to xCP	2.5	—	2.5	—	2.5	—	ns
th	Hold Time, xJ, xK̄ to xCP	2	—	2	—	2	—	ns
trem	Removal Time, xSD̄, xRD̄ to xCP	3	—	3	—	3	—	ns
tw	Pulse Width	3.3	—	3.3	—	3.3	—	ns
	CLK HIGH or LOW	—	—	—	—	—	—	
tw	Set or Reset Pulse Width,	3	—	3	—	3	—	ns
	HIGH or LOW	—	—	—	—	—	—	
tSK(0)	Output Skew ⁽²⁾	—	—	—	—	—	500	ps

NOTES:

1. See test circuits and waveforms. TA = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

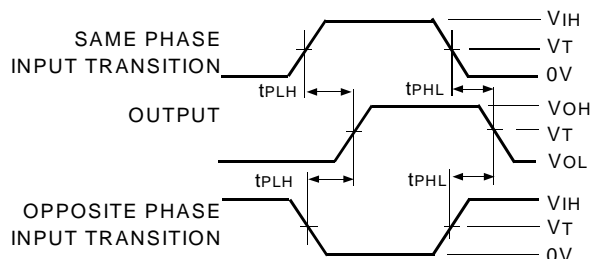
TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC(1)} = 2.5V \pm 0.2V$	$V_{CC(2)} = 3.3V \pm 0.3V \text{ \& } 2.7V$	Unit
V_{LOAD}	$2 \times V_{CC}$	6	V
V_{IH}	V_{CC}	2.7	V
V_T	$V_{CC} / 2$	1.5	V
V_{LZ}	150	300	mV
V_{HZ}	150	300	mV
C_L	30	50	pF

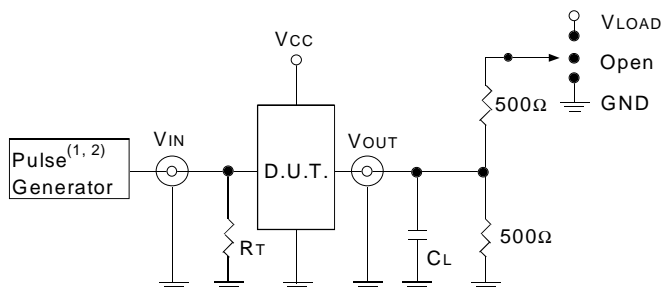
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PROPAGATION DELAY



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TEST CIRCUITS FOR ALL OUTPUTS



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DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

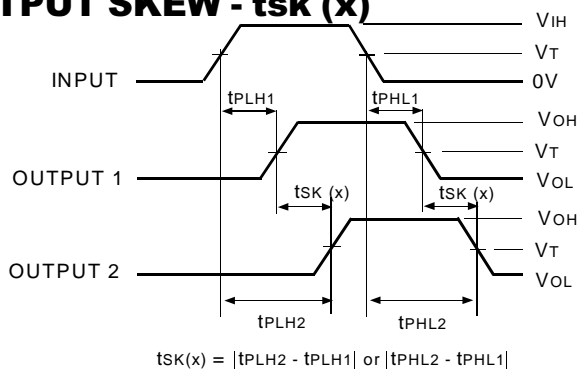
1. Pulse Generator for All Pulses: Rate $\leq 10\text{MHz}$; $t_F \leq 2\text{ns}$; $t_R \leq 2\text{ns}$.
2. Pulse Generator for All Pulses: Rate $\leq 10\text{MHz}$; $t_F \leq 2.5\text{ns}$; $t_R \leq 2.5\text{ns}$.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other tests	Open

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OUTPUT SKEW - $t_{SK}(x)$



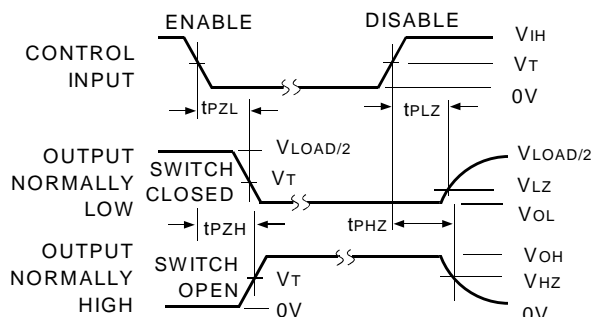
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

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NOTES:

1. For $t_{SK}(o)$ OUTPUT1 and OUTPUT2 are any two outputs.
2. For $t_{SK}(b)$ OUTPUT1 and OUTPUT2 are in the same bank.

ENABLE AND DISABLE TIMES

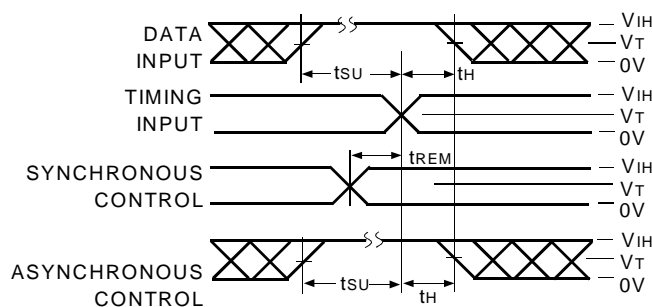


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NOTE:

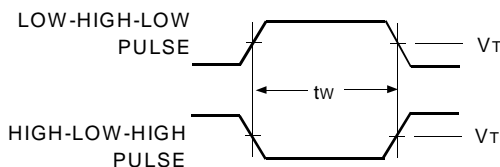
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



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PULSE WIDTH



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ORDERING INFORMATION

IDT	XX	LVC	XXXX	XX	
Temp. Range			Device Type	Package	
				Q	Quarter Size Outline Package (SO16-7)
				DC	Small Outline IC (SO16-8)
				PY	Shrink Small Outline Package (SO16-9)
				PG	Thin Shrink Small Outline Package (SO16-10)
				109A	Dual J-K Flip-Flop with Set and Reset, Positive-Edge Trigger, $\pm 24\text{mA}$
				74	-40°C to +85°C



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