Structure Silicon Monolithic Integrated Circuit

Product Name Compound LED Driver for cellular phone

Type **BD6081GU**

Features Charge Pump DC/DC
LCD Back Light LED Driver /RGB LED Driver

○Absolute Maximum Ratings (Ta=25 °C)

Parameter	Symbol	Limits	Unit	Condition
Maximum Applied voltage	VMAX	7	V	
Power Dissipation	Pd	1725	mW	
Operating Temperature Range	Topr	-25 ~ +85	°C	
Storage Temperature Range	Tstg	-55 ~ +150	°C	

note) Power dissipation deleting is 13.8mW/ °C, when it's used in over 25 °C.
(It's deleting is on the board that is ROHM's standard)

○Operating conditions (VBAT≥VIO, Ta=-25~85 °C)

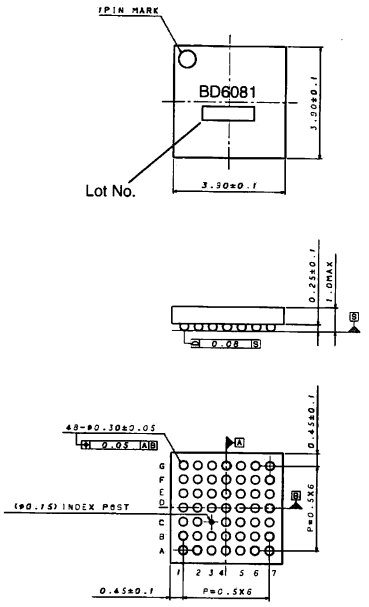
Parameter	Symbol	Limits	Unit	Condition
VBAT input voltage	VBAT	2.7~5.5	V	
VIO pin voltage	VIO	1.65~3.3	V	

*This chip is not designed to protect itself against radioactive rays.

○Electrical Characteristics (Unless otherwise specified, Ta=25°C, VBAT=3.6V, VIO=1.8V)

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Circuit Current						
VBAT Circuit current 1	IBAT1	-	0.1	3.0	μA	RESET=0V, VIO=0V
VBAT Circuit current 2	IBAT2	-	0.5	3.0	μA	RESET=0V, VIO=1.8V
VBAT Circuit current 3	IBAT3	-	6.2	9.5	μA	REG2 energy save mode, Io=0mA
VBAT Circuit current 4	IBAT4	-	100	150	μA	REG2 normal mode, Io=0mA
VBAT Circuit current 5	IBAT5	-	140	210	μA	REG1, REG2 normal mode Io=0mA
VBAT Circuit current 6	IBAT6	-	63	95	mA	DC/DC x1 mode, Io=60mA VBAT=4.0V
VBAT Circuit current 7	IBAT7	-	95	143	mA	DC/DC x1.5 mode, Io=60mA VBAT=3.6V
VBAT Circuit current 8	IBAT8	-	125	188	mA	DC/DC x2 mode, Io=60mA VBAT=2.7V
LED Driver						
LED current Step 1	ILEDSTP1		32		Step	MLED1~4, SLED1~2
LED current Step 2	ILEDSTP2		64		Step	R1LED, G1LED, B1LED R2LED, G2LED, B2LED (with 0mA setting)
LED Maximum setup current 1	IMAX1	-	-	32	mA	MLED1~4, SLED1~2, ISET=120kΩ
LED Maximum setup current 2	IMAX2	-	-	31.5	mA	R1LED, G1LED, B1LED R2LED, G2LED, B2LED, ISET=120kΩ
LED current accurate	ILED	18	20	22	mA	ILED=20mA, ISET=120kΩ
LED current Matching	ILEDMT	-	5	10	%	Between MLED1~4 Between SLED1~2 Between R1LED, G1LED and B1LED Between R2LED, G2LED and B2LED
LED OFF Leak current	ILKLED	-	-	1.0	μA	
DC/DC(Charge Pump)						
Output voltage	VoCP	Vf+0.15	Vf+0.2	-	V	Vf is LED forward voltage
Current Load	IOUT	-	-	255	mA	VBAT≥3.2V, VOUT=4V
Oscillator frequency	fosc	0.8	1.0	1.2	MHz	
Over voltage protection detect	OVP	-	6.0	6.5	V	
Over current protection detect	OCP	-	250	375	mA	VOUT=0V
REG1						
Output voltage	Vo1	2.716	2.80	2.884	V	Io=150mA, VBAT≥3.1V
I/O voltage difference	Vsat1	-	0.2	0.3	V	VBAT=2.5V, Io=150mA
Load stability	ΔVo11	-	10	60	mV	Io=1~150mA
Input stability	ΔVo12	-	10	60	mV	VBAT=3.2~5.5V, Io=150mA
Ripple rejection ratio	RR1	30	40	-	dB	f=100Hz, Vin=200mVp-p
Short circuit current limit	Ilim01	-	225	450	mA	Vo=0V
Discharge resister at OFF	ROFF1	-	1.0	1.5	kΩ	
REG2						
Output voltage1	Vo21	1.74	1.8	1.86	V	Io=150mA (Normal mode)
Output voltage2	Vo22	1.71	1.8	1.89	V	Io=100μA (Energy save mode)
Load stability	ΔVo21	-	10	60	mV	Io=1~150mA
Input stability	ΔVo22	-	10	60	mV	VBAT=3.2~5.5V, Io=150mA
Ripple rejection ratio	RR2	30	40	-	dB	f=100Hz, Vin=200mVp-p
Short circuit current limit	Ilim02	-	225	450	mA	Vo=0V
Discharge resister at OFF	ROFF2	-	1.0	1.5	kΩ	

○External dimensions

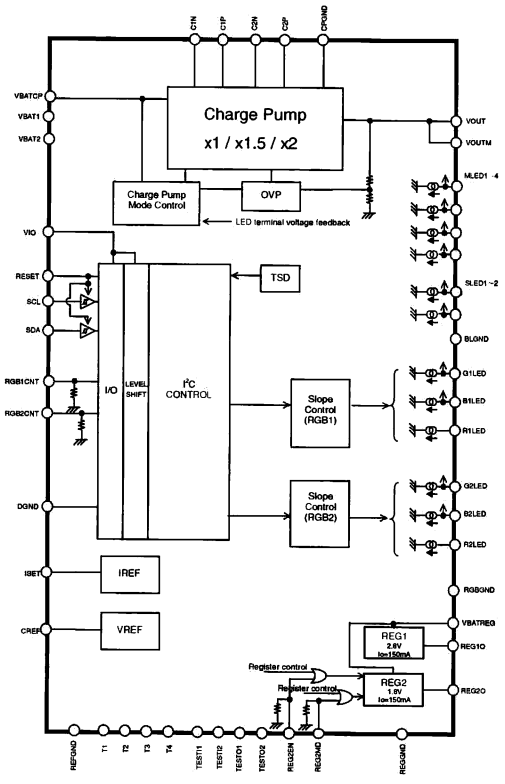


VCSP85H3 (48pins) (Unit : mm)

○Terminals

PIN	PIN Name	PIN	PIN Name	PIN	PIN Name
B7	VBATCP	A6	C2N	E4	REG2EN
G2	VBAT1	C7	C2P	F5	REG2MD
A5	VBAT2	D7	VOUT	D3	TESTI1
G4	VBATREG	D6	VOUTM	D4	TESTI2
A1	T1	E3	ISET	C5	TESTO1
A7	T2	F4	REG1O	C4	TESTO2
G7	T3	G3	REG2O	–	–
G1	T4	A3	MLED1	–	–
F3	CREF	B3	MLED2	–	–
G6	VIO	A4	MLED3	–	–
F7	RESET	B4	MLED4	–	–
E6	SDA	B1	SLED1	–	–
D5	SCL	A2	SLED2	–	–
B5	CPGND	F2	R1LED	–	–
F1	REFGND	E1	G1LED	–	–
G5	REGGND	E2	B1LED	–	–
B2	BLGND	D2	R2LED	–	–
D1	RGBGND	C1	G2LED	–	–
E7	DGND	C2	B2LED	–	–
B6	C1N	F6	RGB1CNT	–	–
C6	C1P	E5	RGB2CNT	–	–

○Block diagram



○Cautions on use

(1) Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Power supply and GND line
Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. Pay attention to the interference by common impedance of layout pattern when there are plural power supplies and GND lines. Especially, when there are GND pattern for small signal and GND pattern for large current included the external circuits, please separate each GND pattern. Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use a capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(3) GND voltage
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(4) Short circuit between terminals and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(5) Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

(6) Input terminals
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(7) External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(8) Thermal shutdown circuit (TSD)
This LSI builds in a thermal shutdown (TSD) circuit. When junction temperatures become detection temperature or higher, the thermal shutdown circuit operates and turns a switch OFF. The thermal shutdown circuit, which is aimed at isolating the LSI from thermal runaway as much as possible, is not aimed at the protection or guarantee of the LSI. Therefore, do not continuously use the LSI with this circuit operating or use the LSI assuming its operation.

(9) Thermal design
Perform thermal design in which there are adequate margins by taking into account the permissible dissipation (Pd) in actual states of use.

(10) LDO
Use each output of LDO by the independence. Don't use under the condition that each output is short-circuited because it has the possibility that a operation becomes unstable.

(11) Other cautions on use
Please consult supplementary documents such as function description of this LSI.

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