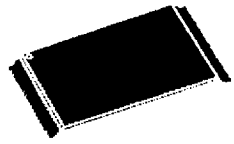
SGS-THOMSON MICROELECTRONICS

M28F411
M28F421

4 Megabit (x 8, Block Erase) FLASH MEMORY

PRELIMINARY DATA

- SMALL SIZE PLASTIC PACKAGE TSOP40
- MEMORY ERASE in BLOCKS
  - One 16K Byte Boot Block (top or bottom location) with hardware write and erase protection
  - Two 8K Byte Key Parameter Blocks
  - One 96K Byte Main Block
  - Three 128K Byte Main Blocks
- 5V ± 10% SUPPLY VOLTAGE
- 12V ± 5% PROGRAMMING VOLTAGE
- 100,000 PROGRAM/ERASE CYCLES
- PROGRAM/ERASE CONTROLLER
- AUTOMATIC STATIC MODE
- LOW POWER CONSUMPTION
  - 60µA Typical in Standby
  - 0.2µA Typical in Deep Power Down
  - 20/25mA Typical Operating Consumption
- HIGH SPEED ACCESS TIME: 70ns
- EXTENDED TEMPERATURE RANGES



TSOP40 (N)
10 x 20mm

DESCRIPTION

The M28F411 and M28F421 FLASH MEMORIES are non-volatile memories that may be erased electrically at the block level and programmed by byte.

Figure 1. Logic Diagram

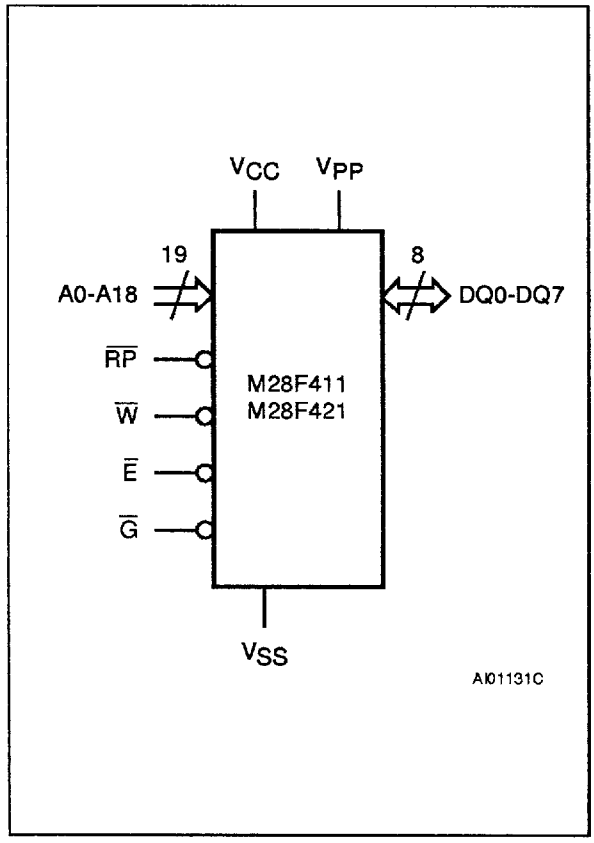


Table 1. Signal Names

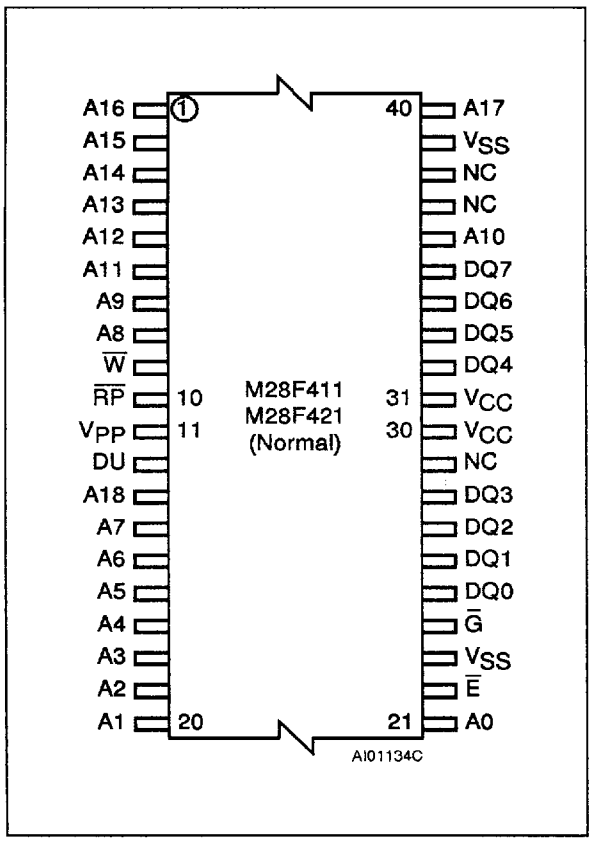
A0-A18	Address Inputs
DQ0-DQ7	Data Input / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset/Power Down/Boot Block Unlock
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 3 grade 5 grade 6	0 to 70 –40 to 125 –20 to 85 –40 to 85	°C
T_{BIAS}	Temperature Under Bias		–50 to 125	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO} (2, 3)	Input or Output Voltages		–0.6 to 7	V
V_{CC}	Supply Voltage		–0.6 to 7	V
V_{A9} (2)	A9 Voltage		–0.6 to 13.5	V
V_{PP} (2)	Program Supply Voltage, during Erase or Programming		–0.6 to 14	V
V_{RP} (2)	$\overline{RP}$ Voltage		–0.6 to 13.5	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Minimum Voltage may undershoot to –2V during transition and for less than 20ns.
3. Maximum DC voltage on I/O is V_{CC} + 0.5V, overshoot to 7V allowed for less than 20ns.

Figure 2. TSOP Pin Connections



Warning: NC = Not Connected, DU = Don't Use

DEVICE OPERATION (cont'd)

The interface is directly compatible with most microprocessors. TSOP40 (10 x 20mm) package is used.

Organization

The M28F411 and M28F421 are organized as 512K x 8. Memory control is provided by Chip Enable, Output Enable and Write Enable inputs. A Reset/Power Down/Boot block unlock, tri-level input, places the memory in deep power down, normal operation or enables programming and erasure of the Boot block.

Blocks

Erasure of the memories is in blocks. There are 7 blocks in the memory address space, one Boot Block of 16K Bytes, two 'Key Parameter Blocks' of 8K Bytes, one 'Main Block' of 96K Bytes, and three 'Main Blocks' of 128K Bytes. The M28F411 memory has the Boot Block at the top of the memory address space (7FFFFh) and the M28F421 locates the Boot Block starting at the bottom (00000h). Erasure of each block takes typically 1 second and each block can be programmed and erased over 100,000 cycles.

The Boot Block is hardware protected from accidental programming or erasure depending on the $\overline{RP}$ signal. Program/Erase commands in the Boot Block are executed only when $\overline{RP}$ is at 12V.

Block erasure may be suspended while data is read from other blocks of the memory, then resumed.

Table 3. Operations

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	DQ0 - DQ7
Read Byte	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Data Output
Write Byte	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Data Input
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Hi-Z
Standby	V_{IH}	X	X	V_{IH}	Hi-Z
Power Down	X	X	X	V_{IL}	Hi-Z

Note: X = V_{IL} or V_{IH}, V_{PP} = V_{PPL} or V_{PPH}

Table 4. Electronic Signature

Code	Device	$\overline{E}$	$\overline{G}$	$\overline{W}$	A0	A9	A1-A8 & A10-A18	DQ0 - DQ7
Manufact. Code		V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{ID}	Don't Care	20h
Device Code	M28F411	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	Don't Care	0F6h
	M28F421	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	Don't Care	0FEh

Note: $\overline{RP}$ = V_{IH}

Bus Operations

Six operations can be performed by the appropriate bus cycles, Read Byte from the Array, Read Electronic Signature, Output Disable, Standby, Power Down and Write the Command of an Instruction.

Command Interface

Commands can be written to a Command Interface (C.I.) latch to perform read, programming, erasure and to monitor the memory's status. When power is first applied, on exit from power down or if V_{CC} falls below V_{LKO}, the command interface is reset to Read Memory Array.

Instructions and Commands

Eight Instructions are defined to perform Read Memory Array, Read Status Register, Read Electronic Signature, Erase, Program, Clear Status Register, Erase Suspend and Erase Resume. An internal Program/Erase Controller (P/E.C.) handles all timing and verification of the Program and Erase instructions and provides status bits to indicate its operation and exit status. Instructions are composed of a first command write operation followed by either second command write, to confirm the commands for programming or erase, or a read operation to read data from the array, the Electronic Signature or the Status Register.

For added data protection, the instructions for byte program and block erase consist of two commands that are written to the memory and which start the automatic P/E.C. operation. Byte programming takes typically 9µs, block erase typically 1 second. Erasure of a memory block may be suspended in order to read data from another block and then resumed. A Status Register may be read at any time, including during the programming or erase cycles, to monitor the progress of the operation.

Power Saving

The M28F411 and M28F421 have a number of power saving features. A CMOS standby mode is entered when the Chip Enable $\overline{E}$ and the Reset/Power Down ($\overline{RP}$) signals are at V_{CC}, when the supply current drops to typically 60µA. A deep power down mode is enabled when the Reset/Power Down ($\overline{RP}$) signal is at V_{SS}, when the supply current drops to typically 0.2µA. The time required to awake from the deep power down mode is 300ns maximum, with instructions to the C.I. recognised after only 210ns.

DEVICE OPERATION

Signal Descriptions

A0-A18 Address Inputs. The address signals, inputs for the memory array, are latched during a write operation.

A9 Address Input is also used for the Electronic Signature Operation. When A9 is raised to 12V the Electronic Signature may be read. The A0 signal is used to read two bytes, when A0 is Low the Manufacturer code is read and when A0 is High the Device code.

Table 5. Instructions

Mnemonic	Instruction	Cycles	1st Cycle			2nd Cycle		
			Operation	Address (1)	Data	Operation	Address (1)	Data
RD	Read Memory Array	1+	Write	X	0FFh	Read (2)	Read Address	Data
RSR	Read Status Register	1+	Write	X	70h	Read (2)	X	Status Register
RSIG	Read Electronic Signature	3	Write	X	90h	Read (2)	Signature Adress (3)	Signature
EE	Erase	2	Write	X	20h	Write	Block Address	0D0h
PG	Program	2	Write	X	40h or 10h	Write	Address	Data Input
CLRS	Clear Status Register	1	Write	X	50h			
ES	Erase Suspend	1	Write	X	0B0h			
ER	Erase Resume	1	Write	X	0D0h			

Notes: 1. X = Don't Care.
2. The first cycle of the RD, RSR or RSIG instruction is followed by read operations to read memory array, Status Register or Electronic Signature codes. Any number of Read cycle can occur after one command cycle.
3. Signature address bit A0=V_{IL} will output Manufacturer code. Address bit A0=V_{IH} will output Device code. Other address bits are ignored.

Table 6. Commands

Hex Code	Command
00h	Invalid/Reserved
10h	Alternative Program Set-up
20h	Erase Set-up
40h	Program Set-up
50h	Clear Status Register
70h	Read Status Register
90h	Read Electronic Signature
0B0h	Erase Suspend
0D0h	Erase Resume/Erase Confirm
0FFh	Read Array

DQ0-DQ7 Data Input/Outputs. The data inputs, a byte to be programmed or a command to the C.I., are latched when both Chip Enable $\overline{E}$ and Write Enable $\overline{W}$ are active. The data output from the memory Array, the Electronic Signature or Status Register is valid when Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ are active. The output is high impedance when the chip is deselected or the outputs are disabled.

$\overline{E}$ Chip Enable. The Chip Enable activates the memory control logic, input buffers, decoders and sense amplifiers. $\overline{E}$ High de-selects the memory and reduces the power consumption to the standby level. $\overline{E}$ can also be used to control writing to the command register and to the memory array, while $\overline{W}$ remains at a low level. Both addresses and data inputs are then latched on the rising edge of $\overline{E}$.

$\overline{RP}$ Reset/Power Down. This is a tri-level input which locks the Boot Block from programming and erasure, and allows the memory to be put in deep power down.

When $\overline{RP}$ is High (up to 6.5V maximum) the Boot Block is locked and cannot be programmed or erased. When $\overline{RP}$ is above 11.4V the Boot Block is unlocked for programming or erasure.

With $\overline{RP}$ Low the memory is in deep power down, and if $\overline{RP}$ is within V_{SS}+0.2V the lowest supply current is absorbed.

Table 7. Status Register

Mnemonic	Bit	Name	Logic Level	Definition	Note
P/ECS	7	P/E.C. Status	'1'	Ready	Indicates the P/E.C. status, check during Program or Erase, and on completion before checking bits b4 or b5 for Program or Erase Success
			'0'	Busy	
ESS	6	Erase Suspend Status	'1'	Suspended	On an Erase Suspend instruction P/ECS and ESS bits are set to '1'. ESS bit remains '1' until an Erase Resume instruction is given.
			'0'	In progress or Completed	
ES	5	Erase Status	'1'	Erase Error	ES bit is set to '1' if P/E.C. has applied the maximum number of erase pulses to the block without achieving an erase verify.
			'0'	Erase Success	
PS	4	Program Status	'1'	Program Error	PS bit set to '1' if the P/E.C. has failed to program a byte.
			'0'	Program Success	
VPPS	3	V_{PP} Status	'1'	V_{PP} Low, Abort	VPPS bit is set if the V_{PP} voltage is below V_{PPH}(min) when a Program or Erase instruction has been executed.
			'0'	V_{PP} OK	
	2	Reserved			
	1	Reserved			
	0	Reserved			

Notes: Logic level '1' is High, '0' is Low.

$\overline{G}$ Output Enable. The Output Enable gates the outputs through the data buffers during a read operation.

$\overline{W}$ Write Enable. It controls writing to the Command Register and Input Address and Data latches. Both Addresses and Data Inputs are latched on the rising edge of $\overline{W}$.

V_{PP} Program Supply Voltage. This supply voltage is used for memory Programming and Erase.

V_{PP} ±10% tolerance option is provided for application requiring maximum 100 write and erase cycles.

V_{CC} Supply Voltage. It is the main circuit supply.

V_{SS} Ground. It is the reference for all voltage measurements.

Memory Blocks

The memory blocks of the M28F411 and M28F421 are shown in Figure 8. The difference between the two products is simply an inversion of the block map to position the Boot Block at the top or bottom of the memory. The selection of the Boot Block at the top or bottom of the memory depends on the microprocessor needs.

Each block of the memory can be erased separately, but only by one block at a time. The erase operation is managed by the P/E.C. but can be suspended in order to read from another block and then resumed.

Programming and erasure of the memory is disabled when the program supply is at V_{PPL}. For successful programming and erasure the program supply must be at V_{PPH}.

The Boot Block provides additional hardware security by use of the $\overline{RP}$ signal which must be at V_{HH} before any program or erase operation will be executed by the P/E.C. on the Boot Block.

Table 8. AC Measurement Conditions

	SRAM Interface Levels	EPROM Interface Levels
Input Rise and Fall Times	≤ 10ns	≤ 10ns
Input Pulse Voltages	0 to 3V	0.45V to 2.4V
Input and Output Timing Ref. Voltages	1.5V	0.8V and 2V

Figure 3. AC Testing Input Output Waveform

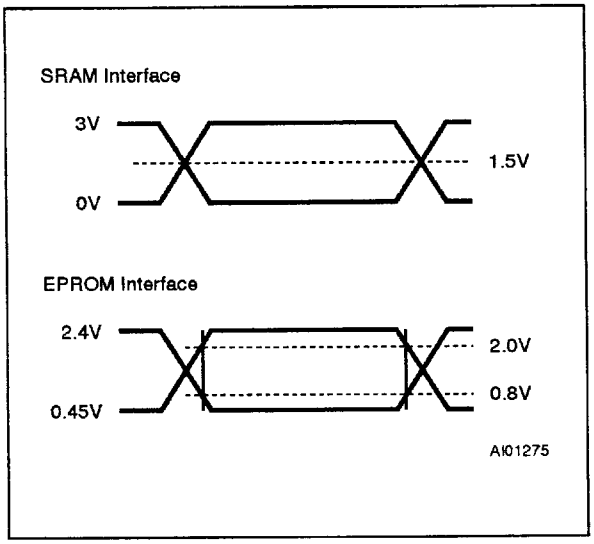


Figure 4. AC Testing Load Circuit

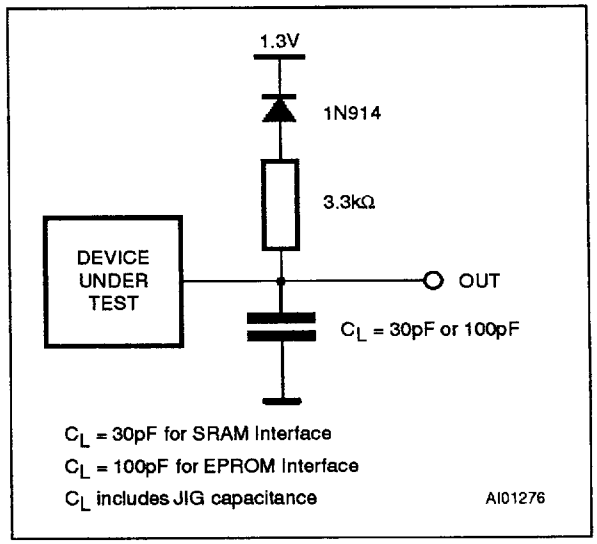


Table 9. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Operations

Operations are defined as specific bus cycles and signals which allow memory Read, Command Write, Output Disable, Standby, Power Down, and Electronic Signature Read. They are shown in Table 3.

Read. Read operations are used to output the contents of the Memory Array, the Status Register or the Electronic Signature. Both Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ must be low in order to read the output of the memory. The Chip Enable input also provides power control and should be used for device selection. Output Enable should be used to gate data onto the output independent of the device selection. The data read depends on the previous command written to the memory (see instructions RD, RSR and RSIG).

Write. Write operations are used to give Instruction Commands to the memory or to latch input data to be programmed. A write operation is initiated when Chip Enable $\overline{E}$ is Low and Write Enable $\overline{W}$ is Low with Output Enable $\overline{G}$ High. Commands, Input Data and Addresses are latched on the rising edge of $\overline{W}$ or $\overline{E}$.

Table 10. DC Characteristics
(T_A = 0 to 70°C; V_{CC} = 5V±5% or 5V±10%; V_{PP} = 12V±5%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC} (1,3)	Supply Current (Read) TTL	$\overline{E} = V_{IL}$, f = 10MHz, I_{OUT} = 0mA		50	mA
	Supply Current (Read) CMOS	$\overline{E} = V_{SS}$, f = 10MHz, I_{OUT} = 0mA		45	mA
I_{CC1} (3)	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$, $\overline{RP} = V_{IH}$		3	mA
	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$, $\overline{RP} = V_{CC} \pm 0.2V$		100	µA
I_{CC2} (3)	Supply Current (Power Down) CMOS	$\overline{RP} = V_{SS} \pm 0.2V$		5	µA
I_{CC3}	Supply Current (Program)	Program in progress		50	mA
I_{CC4}	Supply Current (Erase)	Erase in progress		30	mA
I_{CC5} (2)	Supply Current (Erase Suspend)	$\overline{E} = V_{IH}$, Erase suspended		10	mA
I_{PP}	Program Leakage Current (Read or Standby)	$V_{PP} > V_{CC}$		200	µA
I_{PP1}	Program Current (Read or Standby)	$V_{PP} \le V_{CC}$		±10	µA
I_{PP2}	Program Current (Power Down)	$\overline{RP} = V_{SS} \pm 0.2V$		5	µA
I_{PP3}	Program Current (Program)	Program in progress		30	mA
I_{PP4}	Program Current (Erase)	Erase in progress		30	mA
I_{PP5}	Program Current (Erase Suspend)	Erase suspended		200	µA
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = -2.5mA	2.4		V
V_{PPL}	Program Voltage (Normal operation)		0	6.5	V
V_{PPH}	Program Voltage (Program or Erase operations)		11.4	12.6	V
V_{ID}	A9 Voltage (Electronic Signature)		11.4	13	V
I_{ID}	A9 Current (Electronic Signature)	A9 = V_{ID}		500	µA
V_{LKO}	Supply Voltage (Erase and Program lock-out)		2		V
V_{HH}	Input Voltage ($\overline{RP}$, Boot unlock)	Boot Block Program or Erase	11.4	13	V

Notes: 1. Automatic Power Saving reduces I_{CC} to ≤ 8mA typical in static operation.
2. Current increases to I_{CC} + I_{CC5} during a read operation.
3. CMOS levels V_{CC} ± 0.2V and V_{SS} ± 0.2V. TTL levels V_{IH} and V_{IL}.

Table 11. DC Characteristics
(T_A = -20 to 85°C or -40 to 85°C ; V_{CC} = 5V±5% or 5V±10%; V_{PP} = 12V±5%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC} (1, 3)	Supply Current (Read) TTL	$\overline{E} = V_{IL}$, f = 10MHz, I_{OUT} = 0mA		65	mA
	Supply Current (Read) CMOS	$\overline{E} = V_{SS}$, f = 10MHz, I_{OUT} = 0mA		60	mA
I_{CC1} (3)	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$, $\overline{RP} = V_{IH}$		3	mA
	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$, $\overline{RP} = V_{CC} \pm 0.2V$		100	µA
I_{CC2} (3)	Supply Current (Power Down) CMOS	$\overline{RP} = V_{SS} \pm 0.2V$		8	µA
I_{CC3}	Supply Current (Program)	Program in progress		50	mA
I_{CC4}	Supply Current (Erase)	Erase in progress		30	mA
I_{CC5} (2)	Supply Current (Erase Suspend)	$\overline{E} = V_{IH}$, Erase suspended		10	mA
I_{PP}	Program Leakage Current (Read or Standby)	$V_{PP} > V_{CC}$		200	µA
I_{PP1}	Program Current (Read or Standby)	$V_{PP} \le V_{CC}$		±15	µA
I_{PP2}	Program Current (Power Down)	$\overline{RP} = V_{SS} \pm 0.2V$		5	µA
I_{PP3}	Program Current (Program)	Program in progress		30	mA
I_{PP4}	Program Current (Erase)	Erase in progress		30	mA
I_{PP5}	Program Current (Erase Suspend)	Erase suspended		200	µA
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = -2.5mA	2.4		V
V_{PPL}	Program Voltage (Normal operation)		0	6.5	V
V_{PPH}	Program Voltage (Program or Erase operations)		11.4	12.6	V
V_{ID}	A9 Voltage (Electronic Signature)		11.4	13	V
I_{ID}	A9 Current (Electronic Signature)	A9 = V_{ID}		500	µA
V_{LKO}	Supply Voltage (Erase and Program lock-out)		2		V
V_{HH}	Input Voltage ($\overline{RP}$, Boot unlock)	Boot Block Program or Erase	11.4	13	V

Notes: 1. Automatic Power Saving reduces I_{CC} to ≤ 8mA typical in static operation.
2. Current increases to $I_{CC} + I_{CC5}$ during a read operation.
3. CMOS levels $V_{CC} \pm 0.2V$ and $V_{SS} \pm 0.2V$. TTL levels V_{IH} and V_{IL}.

Table 12. DC Characteristics
(T_A = −40 to 125°C; V_{CC} = 5V±5% or 5V±10%; V_{PP} = 12V±5%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC} (1, 3)	Supply Current (Read) TTL	$\overline{E} = V_{IL}$, f = 10MHz, I_{OUT} = 0mA		65	mA
	Supply Current (Read) CMOS	$\overline{E} = V_{SS}$, f = 10MHz, I_{OUT} = 0mA		60	mA
I_{CC1} (3)	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$, $\overline{RP} = V_{IH}$		3	mA
	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$, $\overline{RP} = V_{CC} \pm 0.2V$		130	µA
I_{CC2} (3)	Supply Current (Power Down) CMOS	$\overline{RP} = V_{SS} \pm 0.2V$		80	µA
I_{CC3}	Supply Current (Program)	Program in progress		50	mA
I_{CC4}	Supply Current (Erase)	Erase in progress		30	mA
I_{CC5} (2)	Supply Current (Erase Suspend)	$\overline{E} = V_{IH}$, Erase suspended		10	mA
I_{PP}	Program Leakage Current (Read or Standby)	$V_{PP} > V_{CC}$		200	µA
I_{PP1}	Program Current (Read or Standby)	$V_{PP} \le V_{CC}$		±15	µA
I_{PP2}	Program Current (Power Down)	$\overline{RP} = V_{SS} \pm 0.2V$		5	µA
I_{PP3}	Program Current (Program)	Program in progress		30	mA
I_{PP4}	Program Current (Erase)	Erase in progress		30	mA
I_{PP5}	Program Current (Erase Suspend)	Erase suspended		200	µA
V_{IL}	Input Low Voltage		−0.5	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = −2.5mA	2.4		V
V_{PPL}	Program Voltage (Normal operation)		0	6.5	V
V_{PPH}	Program Voltage (Program or Erase operations)		11.4	12.6	V
V_{ID}	A9 Voltage (Electronic Signature)		11.4	13	V
I_{ID}	A9 Current (Electronic Signature)	A9 = V_{ID}		500	µA
V_{LKO}	Supply Voltage (Erase and Program lock-out)		2		V
V_{HH}	Input Voltage ($\overline{RP}$, Boot unlock)	Boot Block Program or Erase	11.4	13	V

Notes: 1. Automatic Power Saving reduces I_{CC} to ≤ 8mA typical in static operation.
2. Current increases to I_{CC} + I_{CC5} during a read operation.
3. CMOS levels V_{CC} ± 0.2V and V_{SS} ± 0.2V. TTL levels V_{IH} and V_{IL}.

Table 13. Read AC Characteristics (1)
(T_A = 0 to 70°C, −20 to 85°C or −40 to 85°C; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28F411 / 421								Unit
			-70		-80		-100		-120		
			V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			SRAM Interface		EPROM Interface		EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	70		80		100		120		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid		70		80		100		120	ns
t_{PHQV}	t_{PWH}	Power Down High to Output Valid		300		300		300		300	ns
t_{ELQX} (2)	t_{LZ}	Chip Enable Low to Output Transition	0		0		0		0		ns
t_{ELQV} (3)	t_{CE}	Chip Enable Low to Output Valid		70		80		100		120	ns
t_{GLQX} (2)	t_{OLZ}	Output Enable Low to Output Transition	0		0		0		0		ns
t_{GLQV} (3)	t_{OE}	Output Enable Low to Output Valid		35		40		45		50	ns
t_{EHQX} (2)	t_{OH}	Chip Enable High to Output Transition	0		0		0		0		ns
t_{EHQZ} (2)	t_{HZ}	Chip Enable High to Output Hi-Z		25		30		35		35	ns
t_{GHQX} (2)	t_{OH}	Output Enable High to Output Transition	0		0		0		0		ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z		25		30		35		35	ns
t_{AXQX} (2)	t_{OH}	Address Transition to Output Transition	0		0		0		0		ns

Notes: 1. See Figure 3 and Table 8 for timing measurements.
2. Sampled only, not 100% tested.
3. $\overline{G}$ may be delayed by up to $t_{ELQV} - t_{GLQV}$ after the falling edge of $\overline{E}$ without increasing t_{ELQV}.

Table 14. Read AC Characteristics (1)
(T_A = -40 to 125°C; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28F411 / 421								Unit
			-80		-90		-100		-120		
			V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			SRAM Interface		EPROM Interface		EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	80		90		100		120		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid		80		90		100		120	ns
t_{PHQV}	t_{PWH}	Power Down High to Output Valid		300		300		300		300	ns
t_{ELQX} (2)	t_{LZ}	Chip Enable Low to Output Transition	0		0		0		0		ns
t_{ELQV} (3)	t_{CE}	Chip Enable Low to Output Valid		80		90		100		120	ns
t_{GLQX} (2)	t_{OLZ}	Output Enable Low to Output Transition	0		0		0		0		ns
t_{GLQV} (3)	t_{OE}	Output Enable Low to Output Valid		40		45		50		55	ns
t_{EHQX} (2)	t_{OH}	Chip Enable High to Output Transition	0		0		0		0		ns
t_{EHQZ} (2)	t_{HZ}	Chip Enable High to Output Hi-Z		30		35		40		45	ns
t_{GHQX} (2)	t_{OH}	Output Enable High to Output Transition	0		0		0		0		ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z		30		35		40		45	ns
t_{AXQX} (2)	t_{OH}	Address Transition to Output Transition	0		0		0		0		ns

Notes: 1. See Figure 3 and Table 8 for timing measurements.
2. Sampled only, not 100% tested.
3. $\overline{G}$ may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ without increasing t_{ELQV}.

Figure 5. Read Mode AC Waveforms

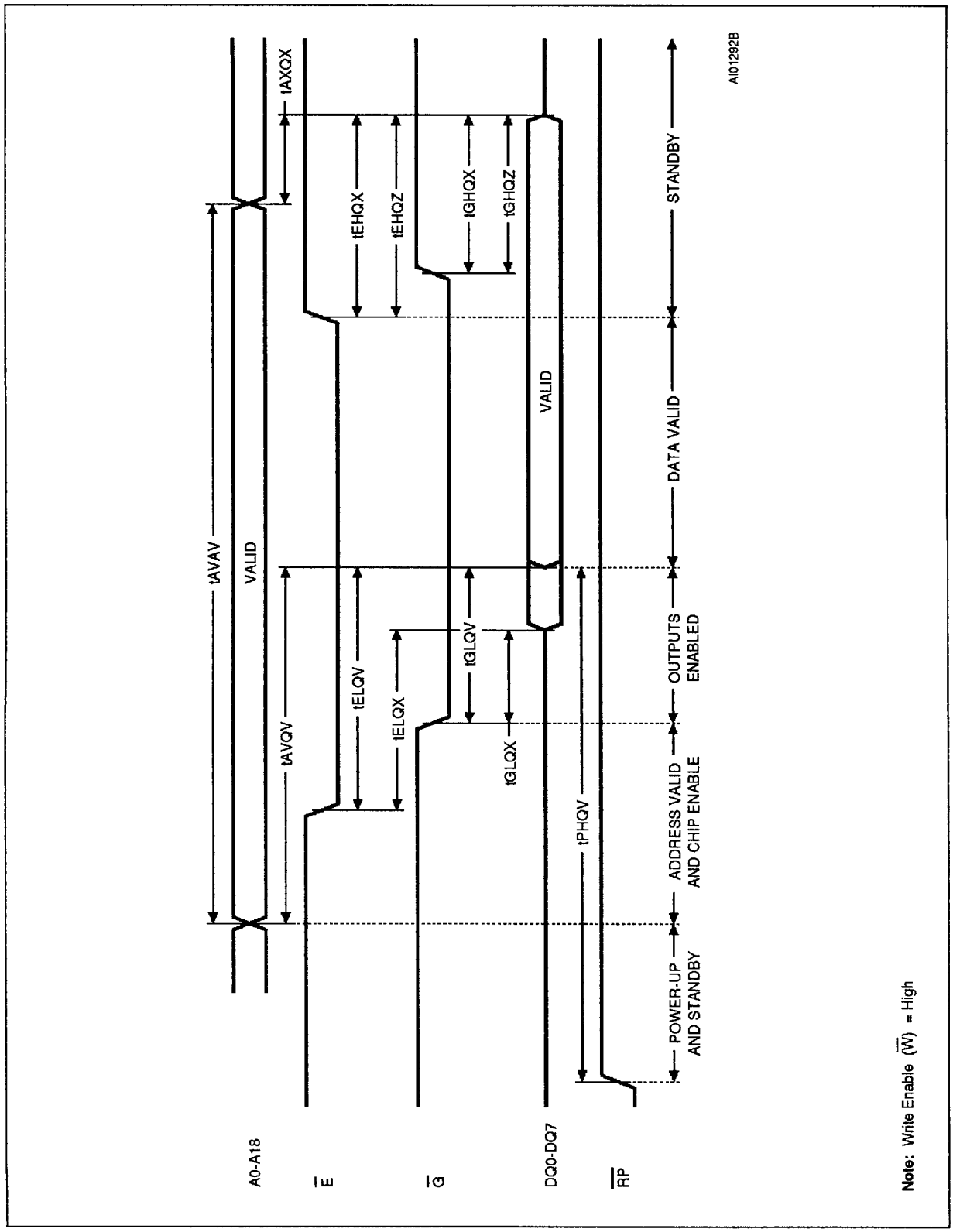


Table 15A. Write AC Characteristics, Write Enable Controlled (1)
(T_A = 0 to 70°C, −20 to 85°C or −40 to 85°C; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28F411 / 421				Unit
			-70		-80		
			V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		
			SRAM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	70		80		ns
t_{PHWL}	t_{PS}	Power Down High to Write Enable Low	210		210		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	50		50		ns
t_{DVWH}	t_{DS}	Data Valid to Write Enable High	50		50		ns
t_{WHDX}	t_{DH}	Write Enable High to Data Transition	0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	10		10		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		30		ns
t_{AVWH}	t_{AS}	Address Valid to Write Enable High	50		50		ns
t_{PHHWH} (5)	t_{PHS}	Power Down V_{HH} (Boot Block Unlock) to Write Enable High	100		100		ns
t_{VPHWH} (5)	t_{VPS}	V_{PP} High to Write Enable High	100		100		ns
t_{WHAX}	t_{AH}	Write Enable High to Address Transition	10		10		ns
t_{WHQV1} (2, 3)		Write Enable High to Output Valid	6		6		µs
t_{WHQV2} (2, 3)		Write Enable High to Output Valid (Boot Block Erase)	0.3		0.3		sec
t_{WHQV3} (2)		Write Enable High to Output Valid (Parameter Block Erase)	0.3		0.3		sec
t_{WHQV4} (2)		Write Enable High to Output Valid (Main Block Erase)	0.6		0.6		sec
t_{QVPH} (5)	t_{PHH}	Output Valid to Reset/Power Down High	0		0		ns
t_{QVVPL} (5)		Output Valid to V_{PP} Low	0		0		ns
t_{PHBR} (4, 5)		Reset/Power Down High to Boot Block Relock		100		100	ns

Notes: 1. See Figure 3 and Table 8 for timing measurements.
2. Time is measured to Status Register Read giving bit b7 = '1'.
3. For Program or Erase of the Boot Block $\overline{RP}$ must be at V_{HH}.
4. Time required for Relocking the Boot Block.
5. Sampled only, not 100% tested.

Table 15B. Write AC Characteristics, Write Enable Controlled (1)
(T_A = 0 to 70°C, −20 to 85°C or −40 to 85°C; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28F411 / 421				Unit
			-100		-120		
			V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	100		120		ns
t_{PHWL}	t_{PS}	Power Down High to Write Enable Low	210		210		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	60		70		ns
t_{DVWH}	t_{DS}	Data Valid to Write Enable High	60		60		ns
t_{WHDX}	t_{DH}	Write Enable High to Data Transition	0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	10		10		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	40		50		ns
t_{AVWH}	t_{AS}	Address Valid to Write Enable High	60		60		ns
t_{PHHWH} (5)	t_{PHS}	Power Down V_{HH} (Boot Block Unlock) to Write Enable High	100		100		ns
t_{VPHWH} (5)	t_{VPS}	V_{PP} High to Write Enable High	100		100		ns
t_{WHAX}	t_{AH}	Write Enable High to Address Transition	10		10		ns
t_{WHQV1} (2, 3)		Write Enable High to Output Valid	7		7		µs
t_{WHQV2} (2, 3)		Write Enable High to Output Valid (Boot Block Erase)	0.4		0.4		sec
t_{WHQV3} (2)		Write Enable High to Output Valid (Parameter Block Erase)	0.4		0.4		sec
t_{WHQV4} (2)		Write Enable High to Output Valid (Main Block Erase)	0.7		0.7		sec
t_{QVPH} (5)	t_{PHH}	Output Valid to Reset/Power Down High	0		0		ns
t_{QVVPL} (5)		Output Valid to V_{PP} Low	0		0		ns
t_{PHBR} (4, 5)		Reset/Power Down High to Boot Block Relock		100		100	ns

Notes: 1. See Figure 3 and Table 8 for timing measurements.
2. Time is measured to Status Register Read giving bit b7 = '1'.
3. For Program or Erase of the Boot Block RP must be at V_{HH}.
4. Time required for Relocking the Boot Block.
5. Sampled only, not 100% tested.

Table 16A. Write AC Characteristics, Write Enable Controlled (1)
(T_A = –40 to 125°C; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28F411 / 421				Unit
			-80		-90		
			V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		
			SRAM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	80		90		ns
t_{PHWL}	t_{PS}	Power Down High to Write Enable Low	210		210		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	50		60		ns
t_{DVWH}	t_{DS}	Data Valid to Write Enable High	50		60		ns
t_{WHDX}	t_{DH}	Write Enable High to Data Transition	0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	10		10		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	30		40		ns
t_{AVWH}	t_{AS}	Address Valid to Write Enable High	50		60		ns
t_{PHHWH} (5)	t_{PHS}	Power Down V_{HH} (Boot Block Unlock) to Write Enable High	100		100		ns
t_{VPHWH} (5)	t_{VPS}	V_{PP} High to Write Enable High	100		100		ns
t_{WHAX}	t_{AH}	Write Enable High to Address Transition	10		10		ns
t_{WHQV1} (2, 3)		Write Enable High to Output Valid	6		7		µs
t_{WHQV2} (2, 3)		Write Enable High to Output Valid (Boot Block Erase)	0.3		0.4		sec
t_{WHQV3} (2)		Write Enable High to Output Valid (Parameter Block Erase)	0.3		0.4		sec
t_{WHQV4} (2)		Write Enable High to Output Valid (Main Block Erase)	0.6		0.7		sec
t_{QVPH} (5)	t_{PHH}	Output Valid to Reset/Power Down High	0		0		ns
t_{QVVPL} (5)		Output Valid to V_{PP} Low	0		0		ns
t_{PHBR} (4, 5)		Reset/Power Down High to Boot Block Relock		100		100	ns

Notes: 1. See Figure 3 and Table 8 for timing measurements.
2. Time is measured to Status Register Read giving bit b7 = '1'.
3. For Program or Erase of the Boot Block RP must be at V_{HH}.
4. Time required for Relocking the Boot Block.
5. Sampled only, not 100% tested.

Table 16B. Write AC Characteristics, Write Enable Controlled (1)
(T_A = -40 to 125°C; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28F411 / 421				Unit
			-100		-120		
			V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	100		120		ns
t_{PHWL}	t_{PS}	Power Down High to Write Enable Low	210		210		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	60		70		ns
t_{DVWH}	t_{DS}	Data Valid to Write Enable High	60		60		ns
t_{WHDX}	t_{DH}	Write Enable High to Data Transition	0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	10		10		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	40		50		ns
t_{AVWH}	t_{AS}	Address Valid to Write Enable High	60		60		ns
t_{PHHWH} (5)	t_{PHS}	Power Down V_{HH} (Boot Block Unlock) to Write Enable High	100		100		ns
t_{VPHWH} (5)	t_{VPS}	V_{PP} High to Write Enable High	100		100		ns
t_{WHAX}	t_{AH}	Write Enable High to Address Transition	10		10		ns
t_{WHQV1} (2, 3)		Write Enable High to Output Valid	7		7		µs
t_{WHQV2} (2, 3)		Write Enable High to Output Valid (Boot Block Erase)	0.4		0.4		sec
t_{WHQV3} (2)		Write Enable High to Output Valid (Parameter Block Erase)	0.4		0.4		sec
t_{WHQV4} (2)		Write Enable High to Output Valid (Main Block Erase)	0.7		0.7		sec
t_{QVPH} (5)	t_{PHH}	Output Valid to Reset/Power Down High	0		0		ns
t_{QVVPL} (5)		Output Valid to V_{PP} Low	0		0		ns
t_{PHBR} (4, 5)		Reset/Power Down High to Boot Block Relock		100		100	ns

Notes: 1. See Figure 3 and Table 8 for timing measurements.
2. Time is measured to Status Register Read giving bit b7 = '1'.
3. For Program or Erase of the Boot Block RP must be at V_{HH}.
4. Time required for Relocking the Boot Block.
5. Sampled only, not 100% tested.

Figure 6. Program & Erase AC Waveforms, $\overline{W}$ Controlled

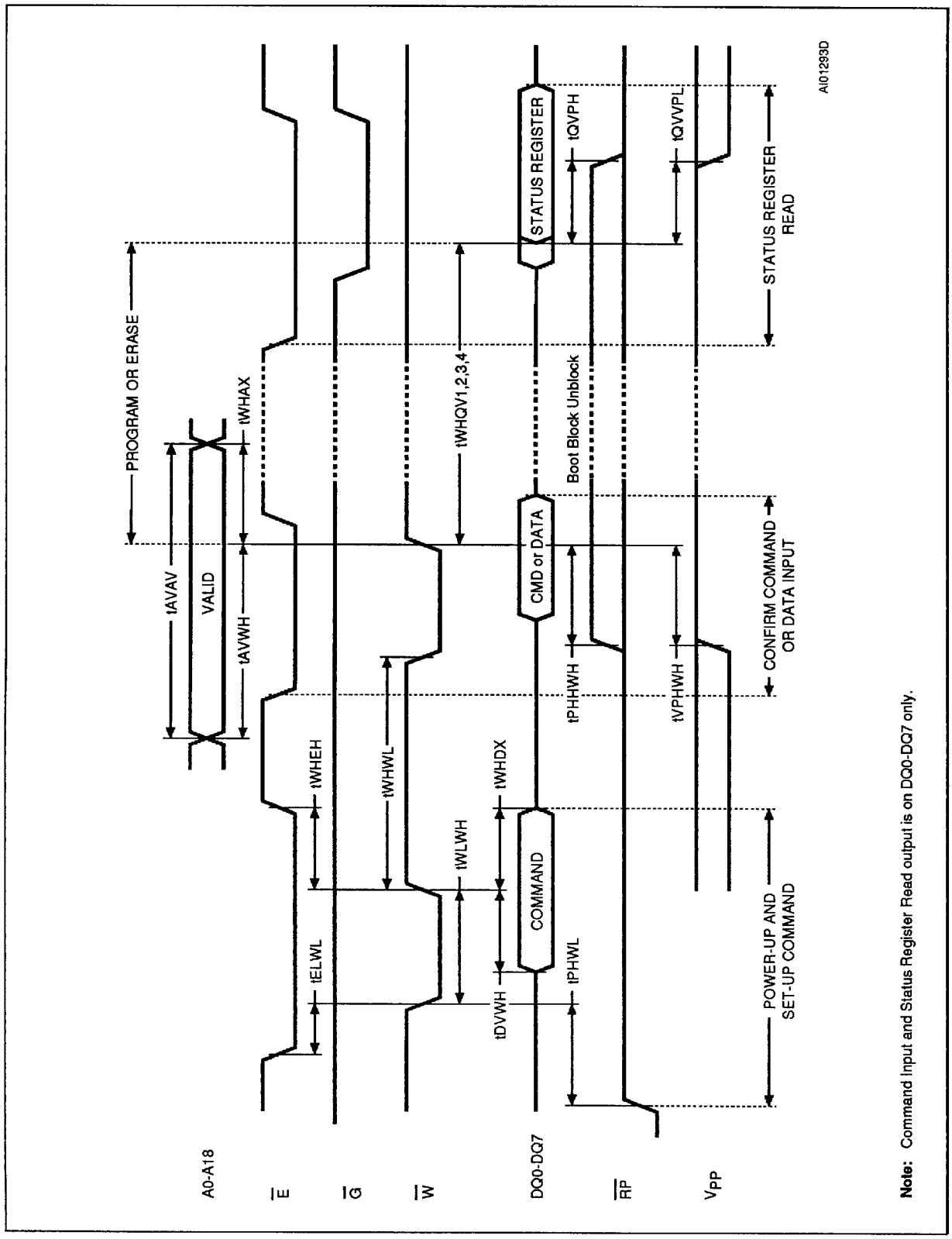


Table 17A. Write AC Characteristics, Chip Enable Controlled (1)
(T_A = 0 to 70°C, −20 to 85°C or −40 to 85°C; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28F411 / 421				Unit
			-70		-80		
			V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		
			SRAM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	70		80		ns
t_{PHEL}	t_{PS}	Power Down High to Chip Enable Low	210		210		ns
t_{WLEL}	t_{CS}	Write Enable Low to Chip Enable Low	0		0		ns
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High	50		50		ns
t_{DVEH}	t_{DS}	Data Valid to Chip Enable High	50		50		ns
t_{EHDX}	t_{DH}	Chip Enable High to Data Transition	0		0		ns
t_{EHWH}	t_{CH}	Chip Enable High to Write Enable High	10		10		ns
t_{EHEL}	t_{WPH}	Chip Enable High to Chip Enable Low	20		30		ns
t_{AVEH}	t_{AS}	Address Valid to Chip Enable High	50		50		ns
t_{PHHEH} (5)	t_{PHS}	Power Down V_{HH} (Boot Block Unlock) to Chip Enable High	100		100		ns
t_{VPHEH} (5)	t_{VPS}	V_{PP} High to Chip Enable High	100		100		ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition	10		10		ns
t_{EHQV1} (2, 3)		Chip Enable High to Output Valid	6		6		µs
t_{EHQV2} (2, 3)		Chip Enable High to Output Valid (Boot Block Erase)	0.3		0.3		sec
t_{EHQV3} (2)		Chip Enable High to Output Valid (Parameter Block Erase)	0.3		0.3		sec
t_{EHQV4} (2)		Chip Enable High to Output Valid (Main Block Erase)	0.6		0.6		sec
t_{QVPH} (5)	t_{PHH}	Output Valid to Reset/Power Down High	0		0		ns
t_{QVVPL} (5)		Output Valid to V_{PP} Low	0		0		ns
t_{PHBR} (4, 5)		Reset/Power Down High to Boot Block Relock		100		100	ns

Notes: 1. See Figure 3 and Table 8 for timing measurements.
2. Time is measured to Status Register Read giving bit b7 = '1'.
3. For Program or Erase of the Boot Block $\overline{RP}$ must be at V_{HH}.
4. Time required for Relocking the Boot Block.
5. Sampled only, not 100% tested.

Table 17B. Write AC Characteristics, Chip Enable Controlled (1)
(T_A = 0 to 70°C, −20 to 85°C or −40 to 85°C; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28F411 / 421				Unit
			-100		-120		
			V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	100		120		ns
t_{PHEL}	t_{PS}	Power Down High to Chip Enable Low	210		210		ns
t_{WLEL}	t_{CS}	Write Enable Low to Chip Enable Low	0		0		ns
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High	60		70		ns
t_{DVEH}	t_{DS}	Data Valid to Chip Enable High	60		60		ns
t_{EHDX}	t_{DH}	Chip Enable High to Data Transition	0		0		ns
t_{EHWH}	t_{CH}	Chip Enable High to Write Enable High	10		10		ns
t_{EHEL}	t_{WPH}	Chip Enable High to Chip Enable Low	40		50		ns
t_{AVEH}	t_{AS}	Address Valid to Chip Enable High	60		60		ns
t_{PHHEH} (5)	t_{PHS}	Power Down V_{HH} (Boot Block Unlock) to Chip Enable High	100		100		ns
t_{VPHEH} (5)	t_{VPS}	V_{PP} High to Chip Enable High	100		100		ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition	10		10		ns
t_{EHQV1} (2, 3)		Chip Enable High to Output Valid	7		7		µs
t_{EHQV2} (2, 3)		Chip Enable High to Output Valid (Boot Block Erase)	0.4		0.4		sec
t_{EHQV3} (2)		Chip Enable High to Output Valid (Parameter Block Erase)	0.4		0.4		sec
t_{EHQV4} (2)		Chip Enable High to Output Valid (Main Block Erase)	0.7		0.7		sec
t_{QVPH} (5)	t_{PHH}	Output Valid to Reset/Power Down High	0		0		ns
t_{QVVPL} (5)		Output Valid to V_{PP} Low	0		0		ns
t_{PHBR} (4, 5)		Reset/Power Down High to Boot Block Relock		100		100	ns

Notes: 1. See Figure 3 and Table 8 for timing measurements.
2. Time is measured to Status Register Read giving bit b7 = '1'.
3. For Program or Erase of the Boot Block $\overline{RP}$ must be at V_{HH}.
4. Time required for Relocking the Boot Block.
5. Sampled only, not 100% tested.

Table 18A. Write AC Characteristics, Chip Enable Controlled (1)
(T_A = −40 to 125°C; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28F411 / 421				Unit
			-80		-90		
			V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		
			SRAM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	80		90		ns
t_{PHEL}	t_{PS}	Power Down High to Chip Enable Low	210		210		ns
t_{WLEL}	t_{CS}	Write Enable Low to Chip Enable Low	0		0		ns
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High	50		60		ns
t_{DVEH}	t_{DS}	Data Valid to Chip Enable High	50		60		ns
t_{EHDX}	t_{DH}	Chip Enable High to Data Transition	0		0		ns
t_{EHWH}	t_{CH}	Chip Enable High to Write Enable High	10		10		ns
t_{EHEL}	t_{WPH}	Chip Enable High to Chip Enable Low	30		40		ns
t_{AVEH}	t_{AS}	Address Valid to Chip Enable High	50		60		ns
t_{PHHEH} (5)	t_{PHS}	Power Down V_{HH} (Boot Block Unlock) to Chip Enable High	100		100		ns
t_{VPHEH} (5)	t_{VPS}	V_{PP} High to Chip Enable High	100		100		ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition	10		10		ns
t_{EHQV1} (2, 3)		Chip Enable High to Output Valid	6		7		µs
t_{EHQV2} (2, 3)		Chip Enable High to Output Valid (Boot Block Erase)	0.3		0.4		sec
t_{EHQV3} (2)		Chip Enable High to Output Valid (Parameter Block Erase)	0.3		0.4		sec
t_{EHQV4} (2)		Chip Enable High to Output Valid (Main Block Erase)	0.6		0.7		sec
t_{QVPH} (5)	t_{PHH}	Output Valid to Reset/Power Down High	0		0		ns
t_{QVVPL} (5)		Output Valid to V_{PP} Low	0		0		ns
t_{PHBR} (4, 5)		Reset/Power Down High to Boot Block Relock		100		100	ns

Notes: 1. See Figure 3 and Table 8 for timing measurements.
2. Time is measured to Status Register Read giving bit b7 = '1'.
3. For Program or Erase of the Boot Block RP must be at V_{HH}.
4. Time required for Relocking the Boot Block.
5. Sampled only, not 100% tested.

Table 18B. Write AC Characteristics, Chip Enable Controlled (1)
(T_A = -40 to 125°C; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28F411 / 421				Unit
			-100		-120		
			V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	100		120		ns
t_{PHEL}	t_{PS}	Power Down High to Chip Enable Low	210		210		ns
t_{WLEL}	t_{CS}	Write Enable Low to Chip Enable Low	0		0		ns
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High	60		70		ns
t_{DVEH}	t_{DS}	Data Valid to Chip Enable High	60		60		ns
t_{EHDX}	t_{DH}	Chip Enable High to Data Transition	0		0		ns
t_{EHWH}	t_{CH}	Chip Enable High to Write Enable High	10		10		ns
t_{EHEL}	t_{WPH}	Chip Enable High to Chip Enable Low	40		50		ns
t_{AVEH}	t_{AS}	Address Valid to Chip Enable High	60		60		ns
t_{PHHEH} (5)	t_{PHS}	Power Down V_{HH} (Boot Block Unlock) to Chip Enable High	100		100		ns
t_{VPHEH} (5)	t_{VPS}	V_{PP} High to Chip Enable High	100		100		ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition	10		10		ns
t_{EHQV1} (2, 3)		Chip Enable High to Output Valid	7		7		µs
t_{EHQV2} (2, 3)		Chip Enable High to Output Valid (Boot Block Erase)	0.4		0.4		sec
t_{EHQV3} (2)		Chip Enable High to Output Valid (Parameter Block Erase)	0.4		0.4		sec
t_{EHQV4} (2)		Chip Enable High to Output Valid (Main Block Erase)	0.7		0.7		sec
t_{QVPH} (5)	t_{PHH}	Output Valid to Reset/Power Down High	0		0		ns
t_{QVVPL} (5)		Output Valid to V_{PP} Low	0		0		ns
t_{PHBR} (4, 5)		Reset/Power Down High to Boot Block Relock		100		100	ns

Notes: 1. See Figure 3 and Table 8 for timing measurements.
2. Time is measured to Status Register Read giving bit b7 = '1'.
3. For Program or Erase of the Boot Block RP must be at V_{HH}.
4. Time required for Relocking the Boot Block.
5. Sampled only, not 100% tested.

Figure 7. Program & Erase AC Waveforms, E Controlled

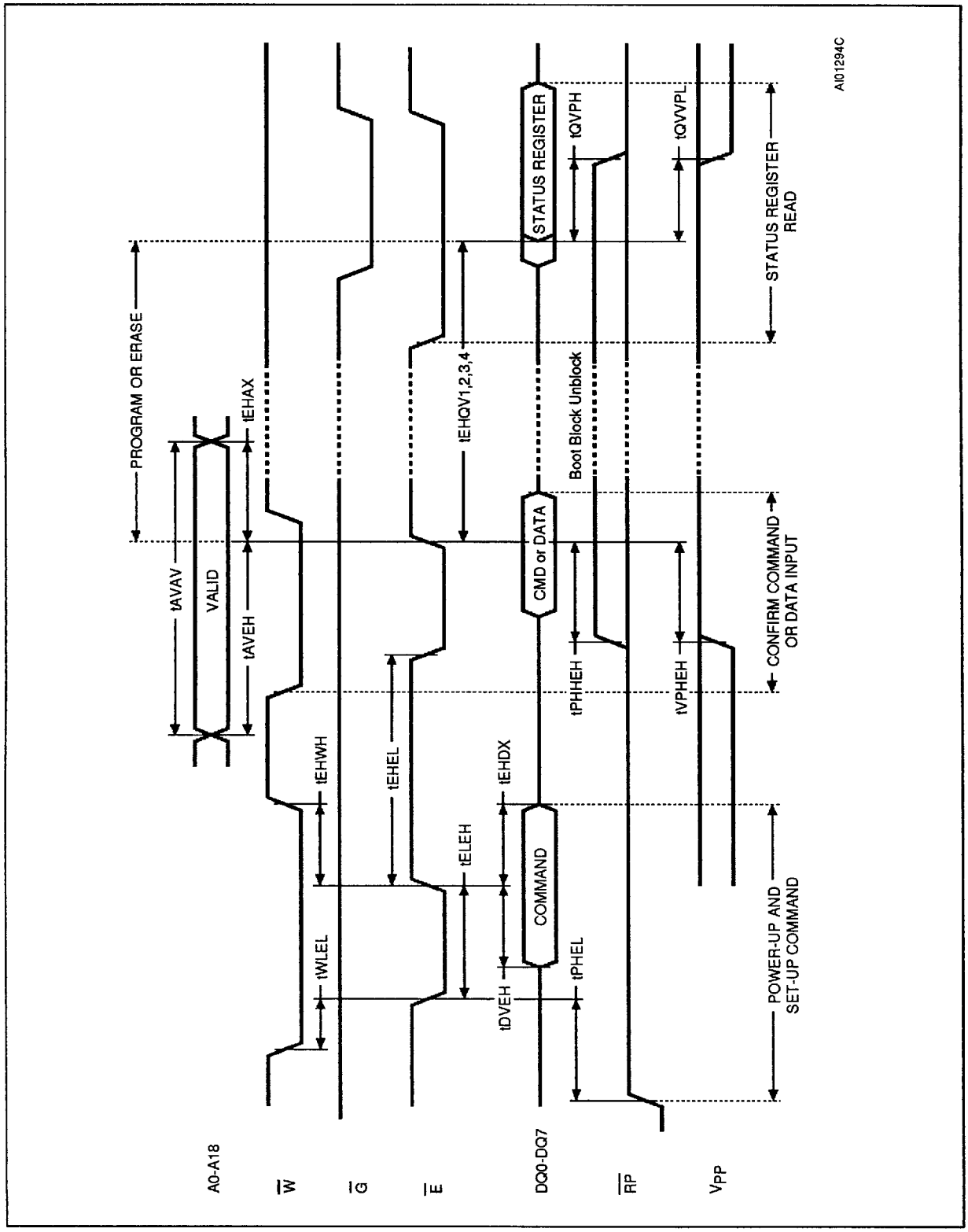


Table 19. Byte Program, Erase Times
(T_A = 0 to 70°C; V_{CC} = 5V ± 10% or 5V ± 5%)

Parameter	Test Conditions	M28F411 / 421			Unit
		Min	Typ	Max	
Main Block Program	V_{PP} = 12V ±5%		1.2	4.2	sec
Boot or Parameter Block Erase	V_{PP} = 12V ±5%		1	7	sec
Main Block Erase	V_{PP} = 12V ±5%		2.4	14	sec

Table 20. Byte Program, Erase Times
(T_A = -20 to 85°C, --40 to 85°C or -40 to 125°C; V_{CC} = 5V ± 10% or 5V ± 5%)

Parameter	Test Conditions	M28F411 / 421			Unit
		Min	Typ	Max	
Main Block Program	V_{PP} = 12V ±5%		1.4	5	sec
Boot or Parameter Block Erase	V_{PP} = 12V ±5%		1.5	10.5	sec
Main Block Erase	V_{PP} = 12V ±5%		3	18	sec

DEVICE OPERATION (cont'd)

Output Disable. The data outputs are high impedance when the Output Enable $\overline{G}$ is High with Write Enable $\overline{W}$ High.

Standby. The memory is in standby when the Chip Enable $\overline{E}$ is High. The power consumption is reduced to the standby level and the outputs are high impedance, independent of the Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

Power Down. The memory is in Power Down when $\overline{RP}$ is low. The power consumption is reduced to the Power Down level, and Outputs are in high impedance, independant of the Chip Enable $\overline{E}$, Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

Electronic Signature. Two codes identifying the manufacturer and the device can be read from the memories, the manufacturer code for SGS-THOMSON is 20h, and the device codes are 0F6h for the M28F411 (Top Boot Block) and 0FEh for the M28F421 (Bottom Boot Block). These codes allow programming equipment or applications to automatically match their interface to the characteristics of the particular manufacturer's product.

The Electronic Signature is output by a Read Array operation when the voltage applied to A9 is at V_{ID}, the manufacturer code is output when the Address input A0 is Low and the device code when this input is High. Other Address inputs are ignored.

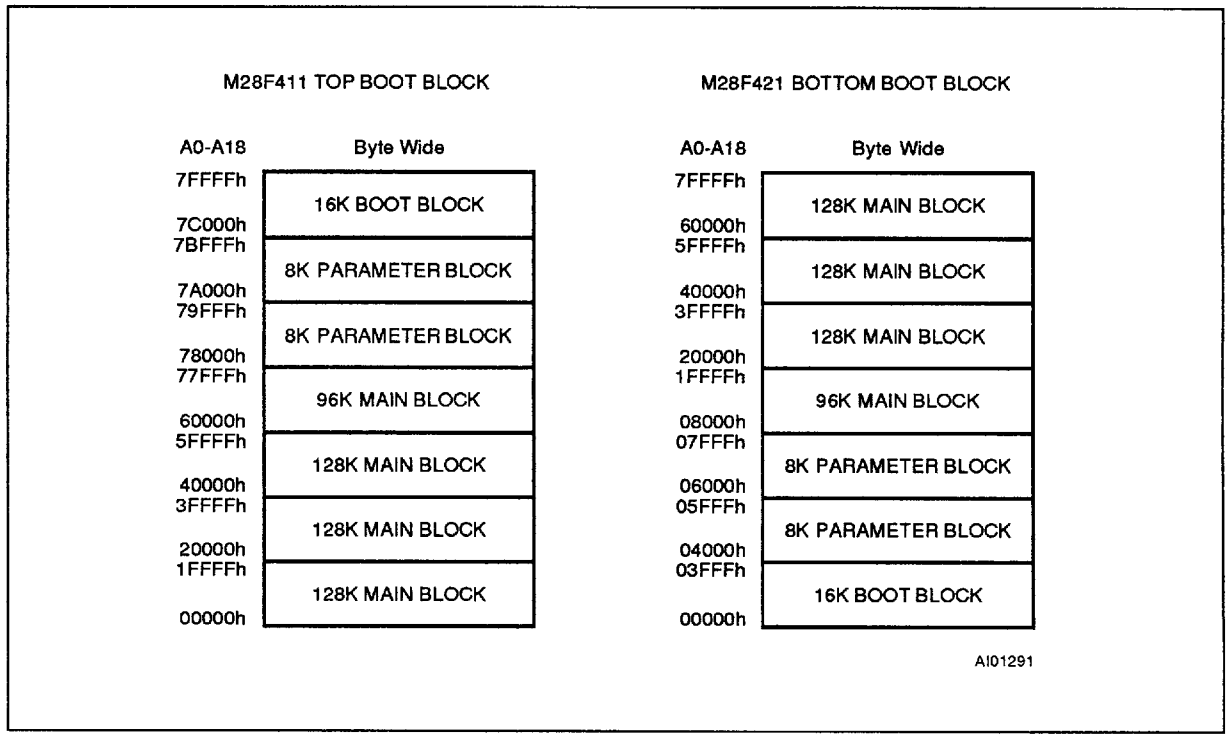
Instructions and Commands

The memories include a Command Interface (C.I.) which latches commands written to the memory. Instructions are made up from one or more commands to perform memory Read, Read Status Register, Read Electronic Signature, Erase, Program, Clear Status Register, Erase Suspend and Erase Resume. These instructions require from 1 to 3 operations, the first of which is always a write operation and is followed by either a further write operation to confirm the first command or a read operation(s) to output data.

A Status Register indicates the P/E.C. status Ready or Busy, the suspend/in-progress status of erase operations, the failure/success of erase and program operations and the low/correct value of the Program Supply voltage V_{PP}.

The P/E.C. automatically sets bits b3 to b7 and clears bit b6 & b7. It cannot clear bits b3 to b5. The register can be read by the Read Status Register (RSR) instruction and cleared by the Clear Status Register (CLRS) instruction. The meaning of the bits b3 to b7 is shown in Table 7. Bits b0 to b2 are reserved for future use (and should be masked out during status checks).

Figure 8. Memory Map, Byte-wide Addresses



Read (RD) instruction. The Read instruction consists of one write operation giving the command 0FFh. Subsequent read operations will read the addressed memory array content.

Read Status Register (RSR) instruction. The Read Status Register instruction may be given at any time, including while the Program/Erase Controller is active. It consists of one write operation giving the command 70h. Subsequent Read operations output the contents of the Status Register. The contents of the status register are latched on the falling edge of $\overline{E}$ or $\overline{G}$ signals, and can be read until $\overline{E}$ or $\overline{G}$ returns to its initial high level. Either $\overline{E}$ or $\overline{G}$ must be toggled to V_{IH} to update the latch. Additionally, any read attempt during program or erase operation will automatically output the contents of the Status Register.

Read Electronic Signature (RSIG) instruction. This instruction uses 3 operations. It consists of one write operation giving the command 90h followed by two read operations to output the manufacturer and device codes. The manufacturer code, 20h, is output when the address line A0 is Low, and the device code, 0F6h for the M28F411 or 0FEh for the M28F421, when A0 is High.

Erase (EE) instruction. This instruction uses two write operations. The first command written is the Erase Set-up command 20h. The second command is the Erase Confirm command 0D0h. During the input of the second command an address of the block to be erased is given and this is latched into the memory. If the second command given is not the Erase Confirm command then the status register bits b4 and b5 are set and the instruction aborts. Read operations output the status register after erasure has started.

During the execution of the erase by the P/E.C., the memory accepts only the RSR (Read Status Register) and ES (Erase Suspend) instructions. Status Register bit b7 returns '0' while the erasure is in progress and '1' when it has completed. After completion the Status Register bit b5 returns '1' if there has been an Erase Failure because erasure has not been verified even after the maximum number of erase cycles have been executed. Status Register bit b3 returns '1' if V_{PP} does not remain at V_{PPH} level when the erasure is attempted and/or proceeding.

V_{PP} must be at V_{PPH} when erasing, erase should not be attempted when $V_{PP} < V_{PPH}$ as the results will be uncertain. If V_{PP} falls below V_{PPH} or $\overline{RP}$ goes Low the erase aborts and must be repeated, after having cleared the Status Register (CLRS). The Boot Block can only be erased when $\overline{RP}$ is also at V_{HH}.

Program (PG) instruction. This instruction uses two write operations. The first command written is the Program Set-up command 40h (or 10h). A second write operation latches the Address and the Data to be written and starts the P/E.C. Read operations output the status register after the programming has started.

Memory programming is only made by writing '0' in place of '1' in a byte.

During the execution of the programming by the P/E.C., the memory accepts only the RSR (Read Status Register) instruction. The Status Register bit b7 returns '0' while the programming is in progress and '1' when it has completed. After completion the Status register bit b4 returns '1' if there has been a Program Failure. Status Register bit b3 returns a '1' if V_{PP} does not remain at V_{PPH} when programming is attempted and/or during programming. V_{PP} must be at V_{PPH} when programming, programming should not be attempted when $V_{PP} < V_{PPH}$ as the results will be uncertain. Programming aborts if V_{PP} drops below V_{PPH} or $\overline{RP}$ goes Low. If aborted the data may be incorrect. Then after having cleared the Status Register (CLRS), the memory must be erased and re-programmed.

The Boot Block can only be programmed when $\overline{RP}$ is at V_{HH}.

Clear Status Register (CLRS) instruction. The Clear Status Register uses a single write operation which clears bits b3, b4 and b5, if latched to '1' by the P/E.C., to '0'. Its use is necessary before any new operation when an error has been detected.

Erase Suspend (ES) instruction. The Erase operation may be suspended by this instruction which consists of writing the command 0B0h. The Status Register bit b6 indicates whether the erase has actually been suspended, b6 = '1', or whether the P/E.C. cycle was the last and the erase is completed, b6 = '0'. During the suspension the memory will respond only to Read (RD), Read Status Register (RSR) or Erase Resume (ER) instructions. Read operations initially output the status register while erase is suspended but, following a Read instruction, data from other blocks of the memory can be read. V_{PP} must be maintained at V_{PPH} while erase is suspended. If V_{PP} does not remain at V_{PPH} or the $\overline{RP}$ signal goes Low while erase is suspended then erase is aborted while bits b5 and b3 of the status register are set. Erase operation must be repeated after having cleared the status register, to be certain to erase the block.

Erase Resume (ER) instruction. If an Erase Suspend instruction was previously executed, the erase operation may be resumed by giving the command 0D0h. The status register bit b6 is cleared when erasure resumes. Read operations output the status register after the erase is resumed. The suggested flow charts for programs that use the programming, erasure and erase suspend/resume features of the memories are shown in Figure 9 to Figure 11.

Programming. The memory can be programmed byte-by-byte. The Program Supply voltage V_{PP} must be applied before program instructions are given, and if the programming is in the Boot Block, $\overline{RP}$ must also be raised to V_{HH} to unlock the Boot Block. The Program Supply voltage may be applied continuously during programming. The program sequence is started by writing a Program Set-up command (40h) to the Command Interface, this is followed by writing the address and data byte or word to the memory. The Program/Erase Controller automatically starts and performs the programming after the second write operation, providing that the V_{PP} voltage (and $\overline{RP}$ voltage if programming the Boot Block) are correct. During the programming the memory status is checked by reading the status register bit b7 which shows the status of the P/E.C. Bit b7 = '1' indicates that programming is completed.

A full status check can be made after each byte/word or after a sequence of data has been programmed. The status check is made on bit b3 for any possible V_{PP} error and on bit b4 for any possible programming error.

Erase. The memory can be erased by blocks. The Program Supply voltage V_{PP} must be applied before the Erase instruction is given, and if the Erase is of the Boot Block $\overline{RP}$ must also be raised to V_{HH} to unlock the Boot Block. The Erase sequence is started by writing an Erase Set-up command (20h) to the Command Interface, this is followed by an address in the block to be erased and the Erase Confirm command (0D0h). The Program/Erase Controller automatically starts and performs the block erase, providing the V_{PP} voltage (and the $\overline{RP}$ voltage if the erase is of the Boot Block) is correct. During the erase the memory status is checked by reading the status register bit b7 which shows the status of the P/E.C. Bit b7 = '1' indicates that erase is completed.

A full status check can be made after the block erase by checking bit b3 for any possible V_{PP} error, bits b5 and b6 for any command sequence errors (erase suspended) and bit b5 alone for an erase error.

Reset. Note that after any program or erase instruction has completed with an error indication or after any V_{PP} transitions down to V_{PPL} the Command Interface must be reset by a Clear Status Register Instruction before data can be accessed.

Automatic Power Saving

The M28F411 and M28F421 memories place themselves in a lower power state when not being accessed. Following a Read operation, after a delay equal to the memory access time, the Supply Current is reduced from a typical read current of 25mA (CMOS inputs) to less than 2mA.

Power Down

The memories provide a power down control input $\overline{RP}$. When this signal is taken to below V_{SS} + 0.2V all internal circuits are switched off and the supply current drops to typically 0.2µA and the program current to typically 0.1µA. If $\overline{RP}$ is taken low during a memory read operation then the memory is de-selected and the outputs become high impedance. If $\overline{RP}$ is taken low during a program or erase sequence then it is aborted and the memory content is no longer valid.

Recovery from deep power down requires 300ns to a memory read operation, or 210ns to a command write. On return from power down the status register is cleared to 00h.

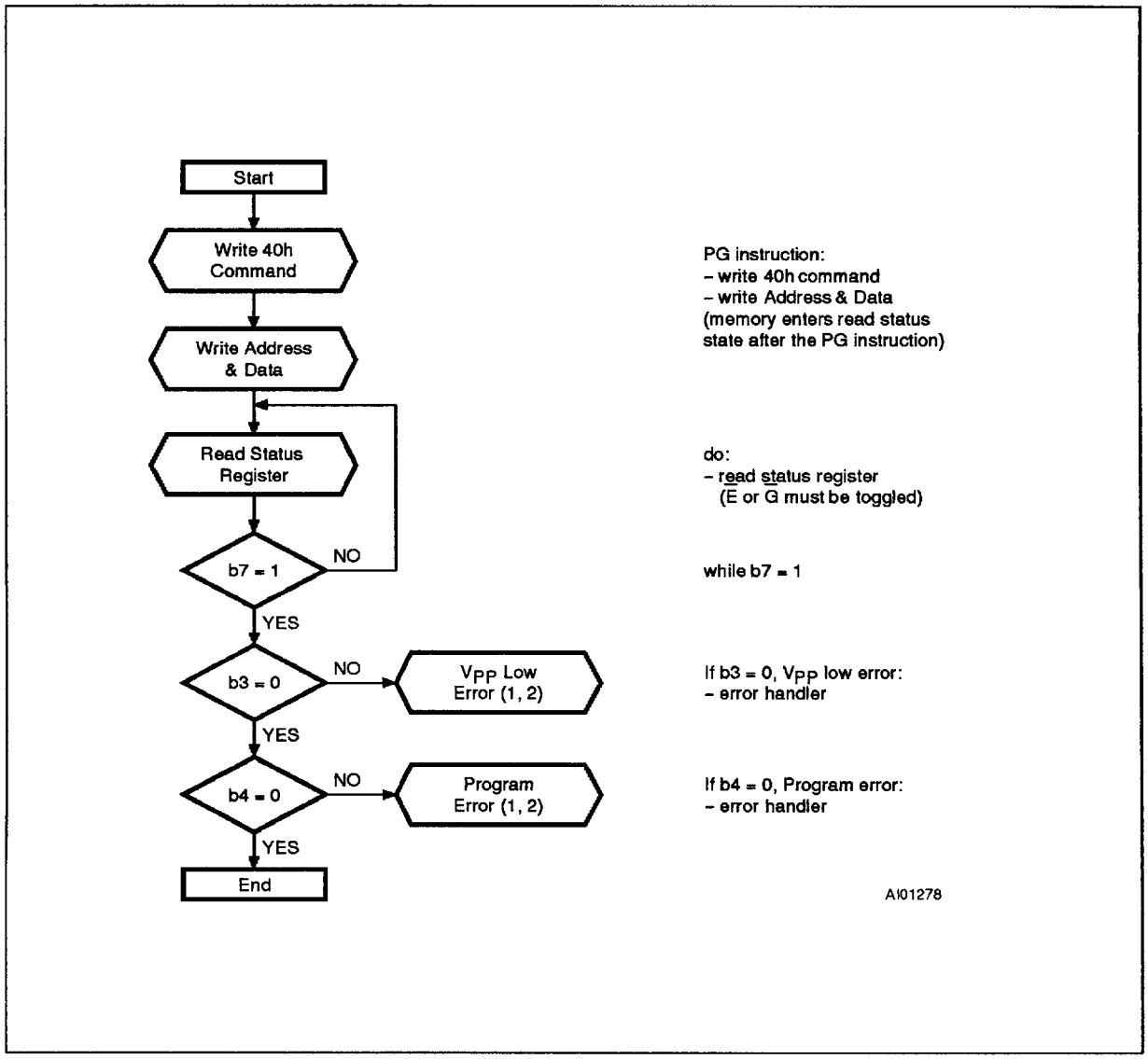
Power Up

The Supply voltage V_{CC} and the Program Supply voltage V_{PP} can be applied in any order. The memory Command Interface is reset on power up to Read Memory Array, but a negative transition of Chip Enable $\overline{E}$ or a change of the addresses is required to ensure valid data outputs. Care must be taken to avoid writes to the memory when V_{CC} is above V_{LKO} and V_{PP} powers up first. Writes can be inhibited by driving either $\overline{E}$ or $\overline{W}$ to V_{IH}. The memory is disabled until $\overline{RP}$ is up to V_{IH}.

Supply Rails

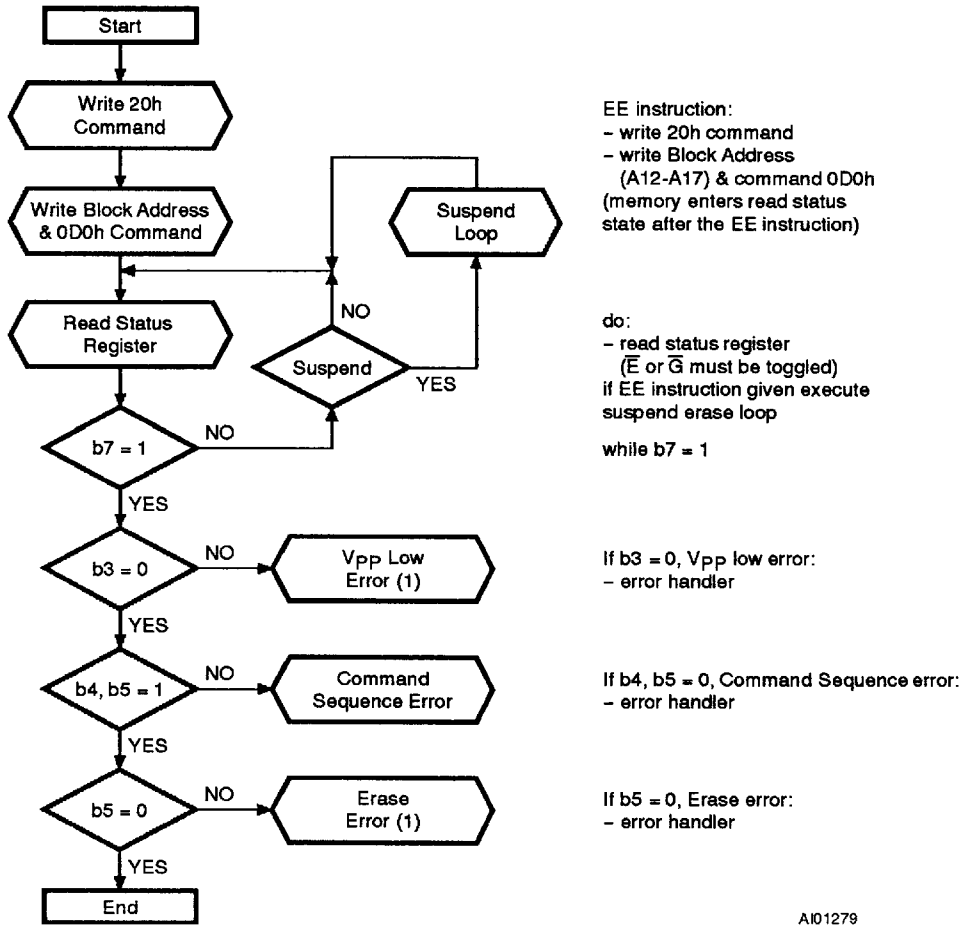
Normal precautions must be taken for supply voltage decoupling, each device in a system should have the V_{CC} and V_{PP} rails decoupled with a 0.1µF capacitor close to the V_{CC} and V_{SS} pins. The PCB trace widths should be sufficient to carry the V_{PP} program and erase currents required.

Figure 9. Program Flow-chart and Pseudo Code



Notes: 1. Status check of b3 (V_{PP} Low) and b4 (Program Error) can be made after each byte/word programming or after a sequence.
2. If a V_{PP} Low or Program Erase is found, the Status Register must be cleared (CLRS instruction) before further P/E.C. operations.

Figure 10. Erase Flow-chart and Pseudo Code



Note: 1. If V_{PP} Low or Erase Error is found, the Status Register must be cleared (CLRS instruction) before further P/E.C. operations.

Figure 11. Erase Suspend & Resume Flow-chart and Pseudo Code

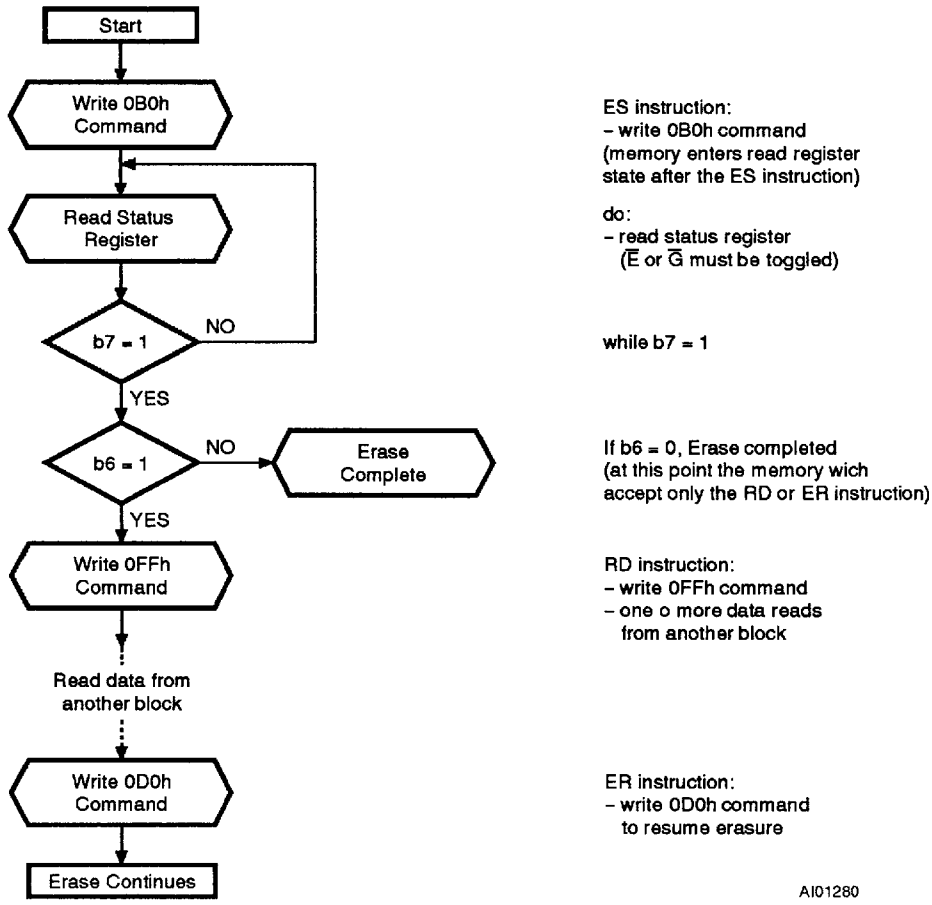
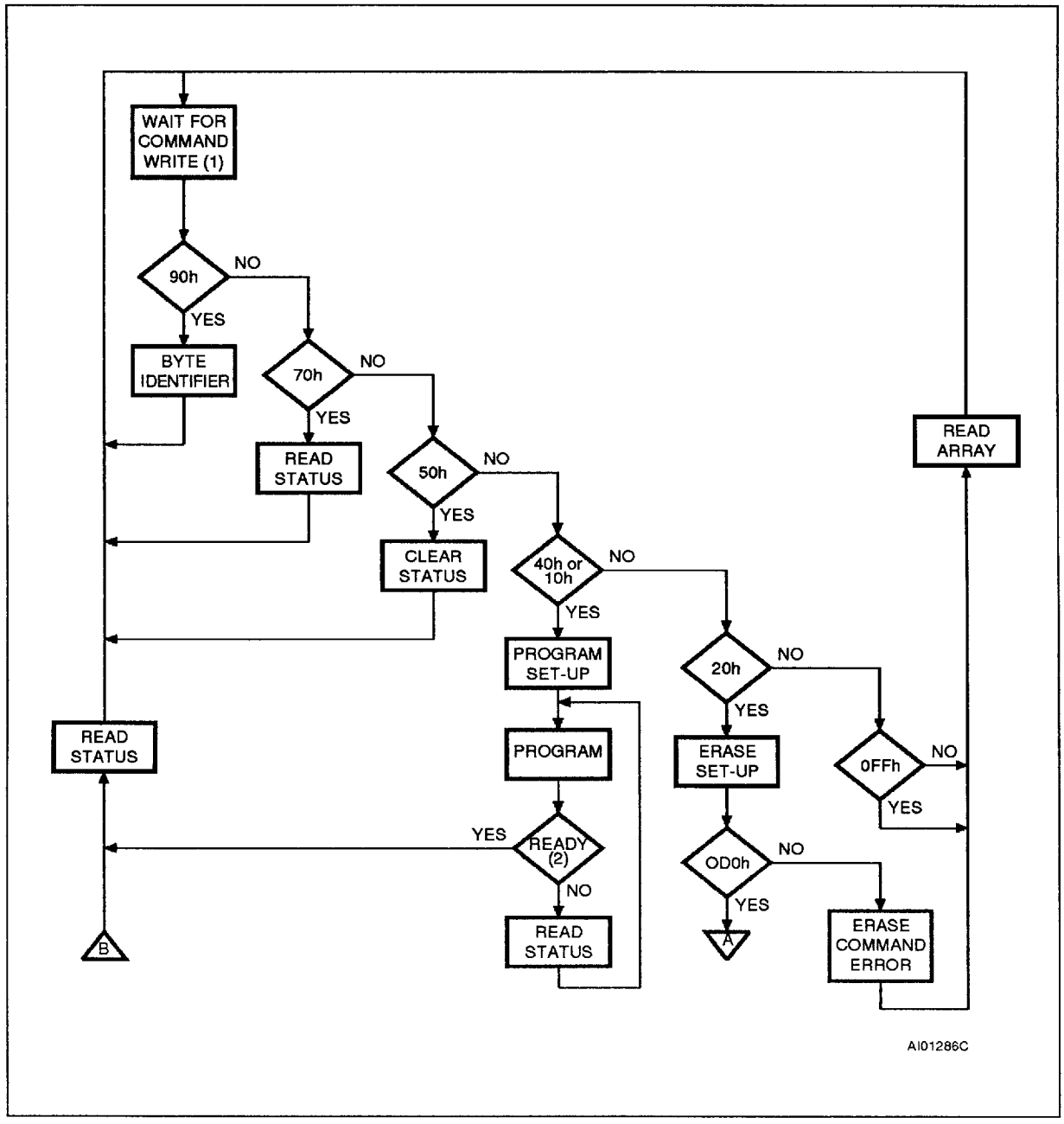
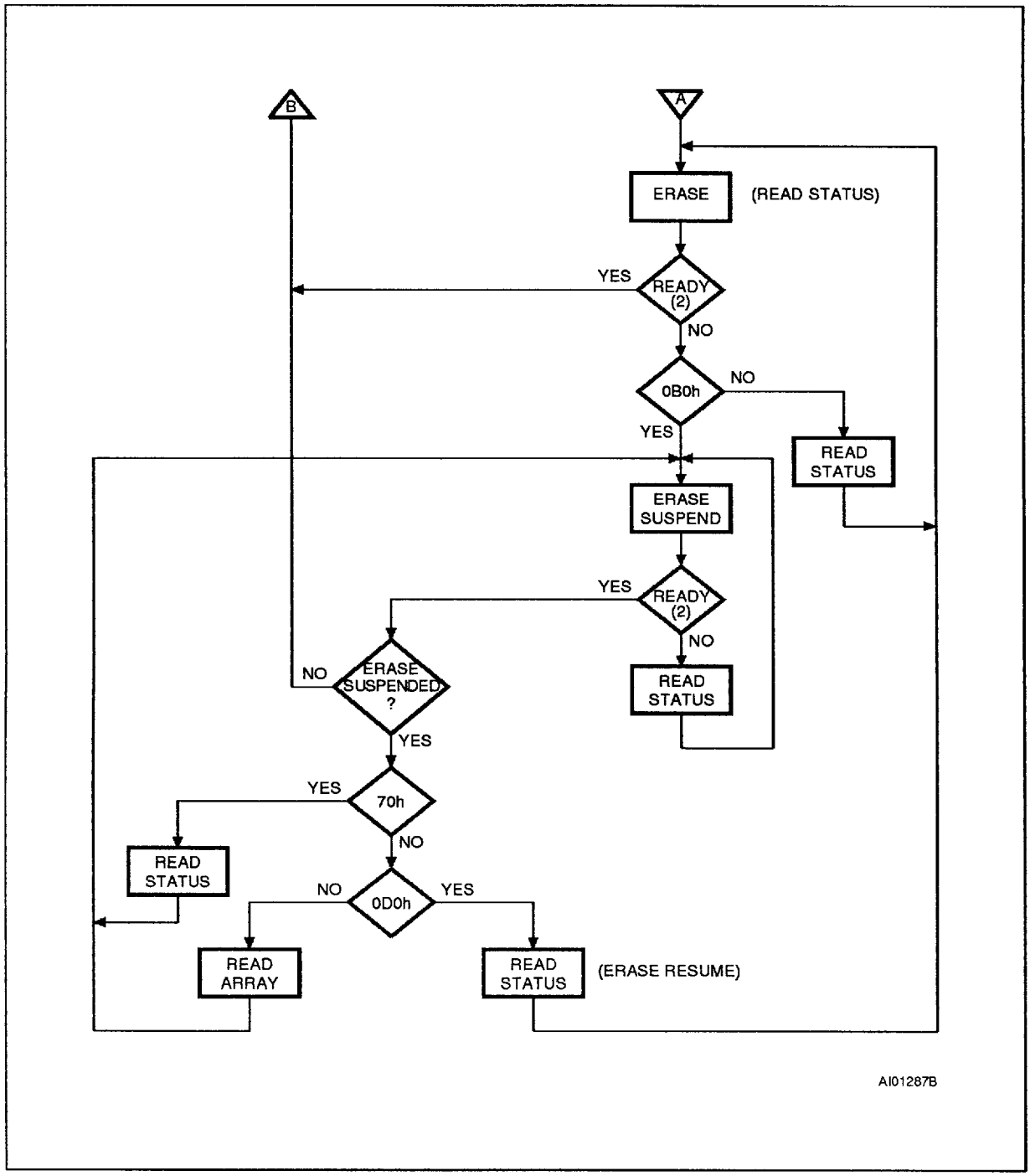


Figure 12. Command Interface and Program Erase Controller Flow-diagram (a)



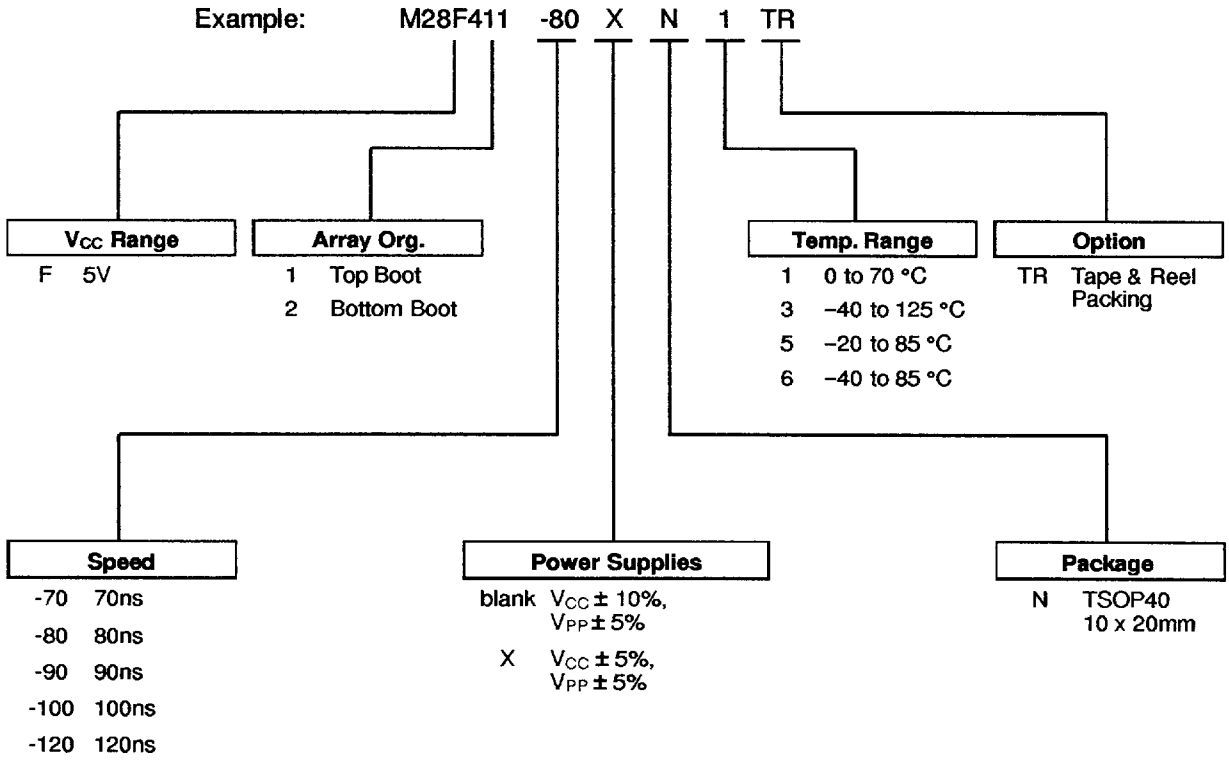
Notes: 1. If no command is written, the Command Interface remains in its previous valid state. Upon power-up, on exit from power-down or if V_{CC} falls below V_{LKO}, the Command Interface defaults to Read Array mode.
2. P/E.C. status (Ready or Busy) is read on Status Register bit 7.

Figure 13. Command Interface and Program Erase Controller Flow-diagram (b)



Note: 2. P/E.C. status (Ready or Busy) is read on Status Register bit 7.

ORDERING INFORMATION SCHEME



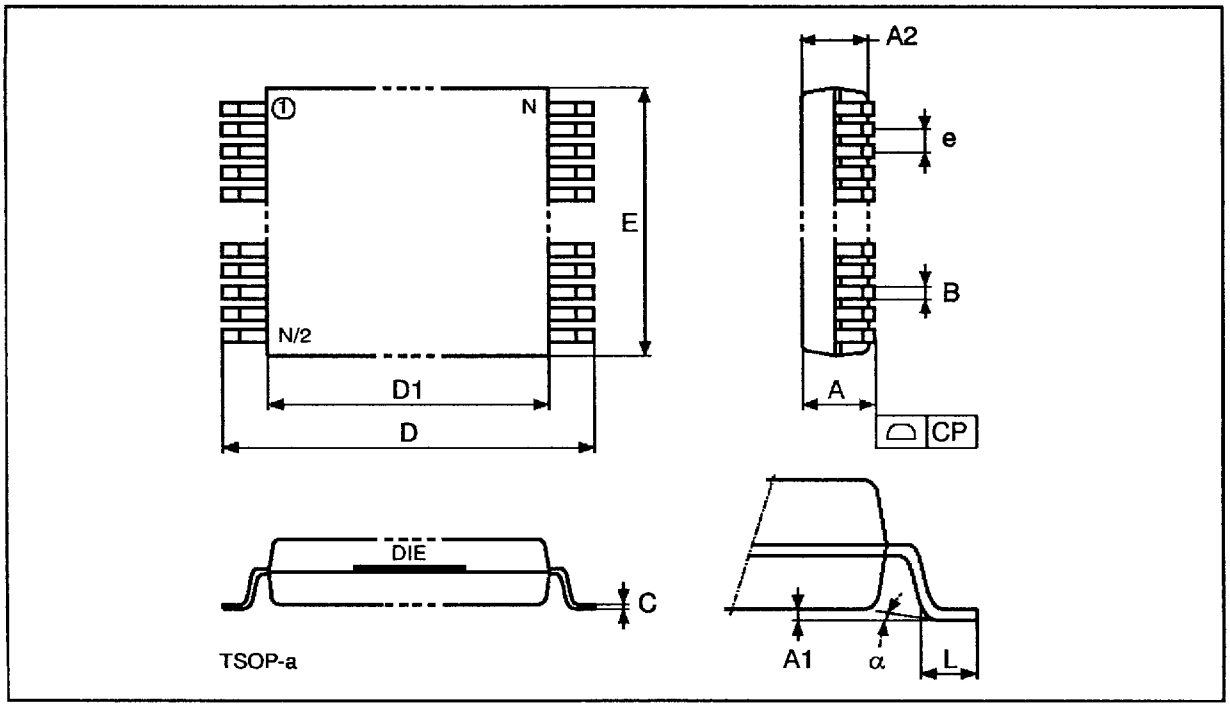
For a list of available options (V_{CC} Range, Array Organisation, Speed, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

TSOP40 - 40 lead Plastic Thin Small Outline, 10 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.15		0.002	0.006
A2		0.95	1.05		0.037	0.041
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		9.90	10.10		0.390	0.398
e	0.50	-	-	0.020	-	-
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N		40			40	
CP			0.10			0.004

TSOP40



TSOP-a

Drawing is not to scale