CML Semiconductor Products

PRODUCT INFORMATION

FX631 Low-Voltage SPM Detector

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Features

- Detects 12kHz and 16kHz SPM Frequencies
- Low Power (3.0 $Volt_{MIN}$ <1.0mA) Operation
- High Speechband Rejection Properties
- Tone-Follower and Packet Mode Outputs
- Applications
  - Complex and/or Simple Telephone Systems
  - Call-Charge/-Logging Systems

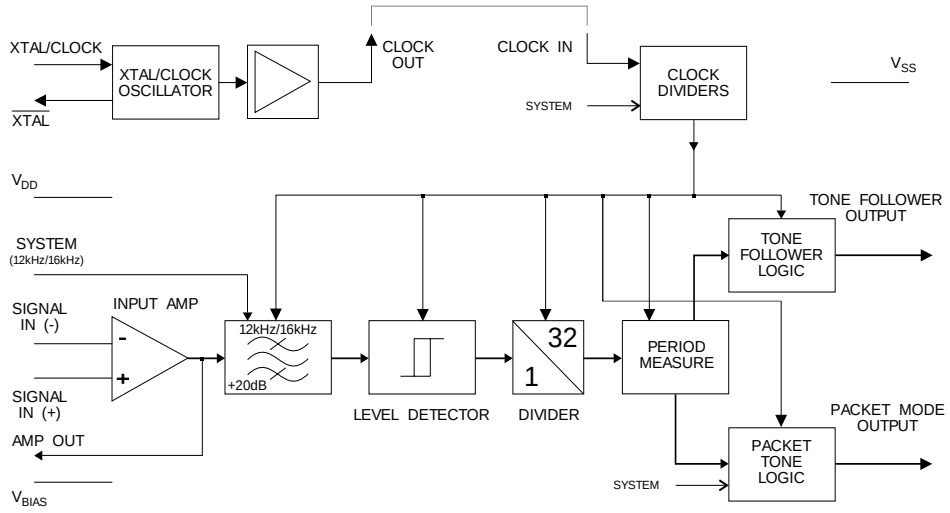


Fig.1 Functional Block Diagram

FX631

Brief Description

The FX631 is a low-power, system-selectable Subscriber Pulse Metering (SPM) detector to indicate the presence, on a telephone line, of both 12kHz and 16kHz telephone call-charge frequencies.

Deriving its input directly from the telephone line, input amplitude/sensitivities are component adjustable to the user's national 'Must/Must-Not Decode' specifications via an on-chip input amplifier, whilst the 12kHz and 16kHz frequency limits are accurately defined by the use of an external 3.579545MHz telephone-system Xtal or clock-pulse input.

The FX631, which demonstrates high 12kHz and 16kHz performance in the presence of both voice and noise, can operate from either a single or differential analogue signal input from which it will produce two individual logic outputs.

1. Tone Follower Output - A 'tone-following' logic output producing a "Low" level for the period of a correct decode and a "High" level for a bad decode or NOTONE.
2. Packet (Cumulative Tone) Mode Output - To respond and de-respond after a cumulative 40ms of good tone (or NOTONE) in any 48ms period. This process will ignore small fluctuations or fades of a valid frequency input and is available for µProcessor 'Wake-Up', Minimum tone detection, NOTONE indication or transient avoidance.

This system (12kHz/16kHz) selectable microcircuit, which may be line-powered, is available in 16-pin plastic DIL and surface mount SOIC and 24-pin plastic SSOP packages.

Pin Number		Function
FX631 D5	**FX631 DW/P**	
1	**1**	**Xtal/Clock:** The input to the on-chip clock oscillator; for use with a 3.579545MHz Xtal in conjunction with the $\overline{\text{Xtal}}$ output (see Figure 2); circuit components are on chip. Using this mode of clock operation, the Clock Out pin should be connected directly to the Clock In pin. If a clock pulse input is employed to the Clock In pin, this pin must be connected directly to V_{DD} (see Figure 2).
4	**2**	**$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator inverter.
5	**3**	**Clock Out:** The buffered output of the on-chip clock oscillator inverter. If a Xtal input is employed this output should be connected directly to the Clock In pin.
6	**4**	**Clock In:** The 3.579545MHz clock pulse input to the internal clock-dividers. If a clock pulse input is employed, the Xtal/Clock input (Pin 1) should be connected to V_{DD}. See Figure 2.
8	**7**	**V_{BIAS}:** The output of the on-chip analogue bias circuitry. Held internally at $V_{DD}/2$, this pin should be decoupled to V_{SS} (see Figure 2).
12	**8**	**V_{SS}:** Negative supply rail (GND).
13	**9**	**Signal In (+):** The positive and negative signal inputs to, and the output from, the input gain adjusting signal amplifier. Refer to the graph in Figure 4 for guidance on setting level sensitivities to national specifications, and the selection of gain adjusting components.
17	**10**	**Signal In (-):**
18	**11**	**Amp Out:**
19	**13**	**Tone Follower Output:** This output provides a logic “0” (Low) for the period of a detected tone, and a logic “1” (High) for NOTONE detection. See Figure 7.
20	**14**	**Packet Mode Output:** A logic output that will be available after a cumulation of 40ms of 'good' tone has been received. This packet mode tone follower will only respond when a tone frequency of sufficient quality has been received for sufficient time, i.e. a cumulation of 40ms in any 48ms, short tone bursts or breaks will be ignored. This output provides a logic “0” (Low) for a detected tone and a logic “1” (High) for NOTONE detection. See Figure 7.
21	**15**	**System:** The logic input to select device operation to either 12kHz (logic “1” - High) or 16kHz (logic “0” - Low) SPM systems. This input has an internal 1MΩ pullup resistor (12kHz).
24	**16**	**V_{DD}:** Positive supply rail. A single, stable power supply is required. Critical levels and voltages within the FX631 are dependant upon this supply. This pin should be decoupled to V_{SS} by a capacitor mounted close to the pin. Note that if this device is ‘line’ powered, the resulting supply must be stable. See notes on Microcircuit Protection from high and spurious line voltages.
2, 3, 7, 9, 10, 11, 14, 15, 16, 22, 23	5, 6, 12	No internal connection, leave open circuit.

Application Information
External Components

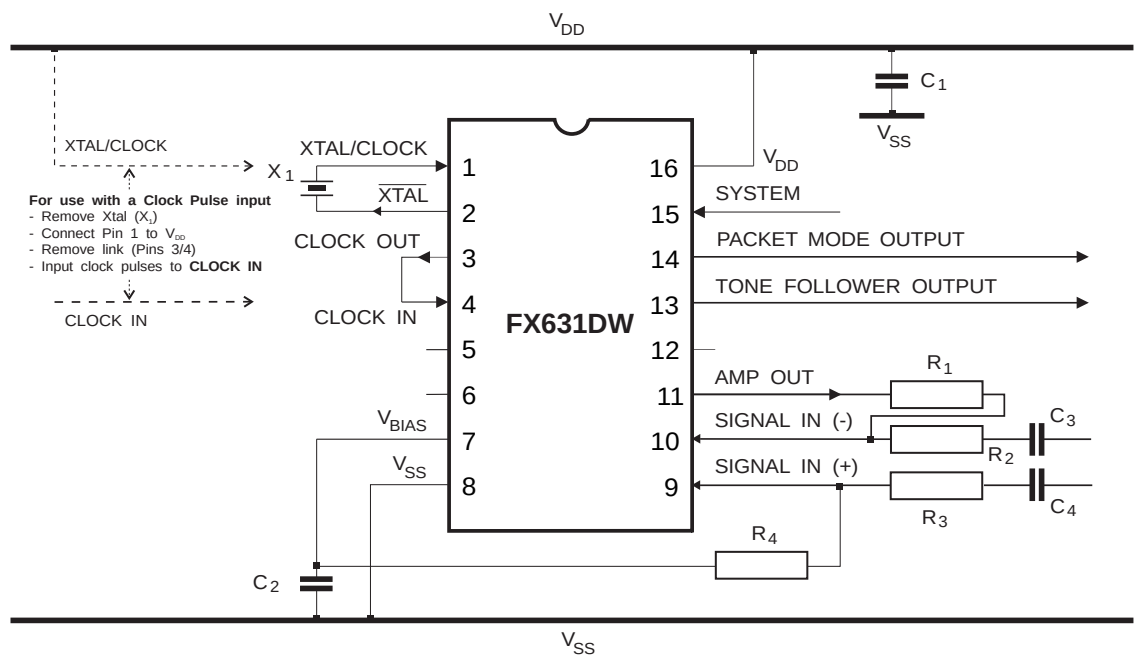


Fig.2 Recommended External Components - Differential Input Mode

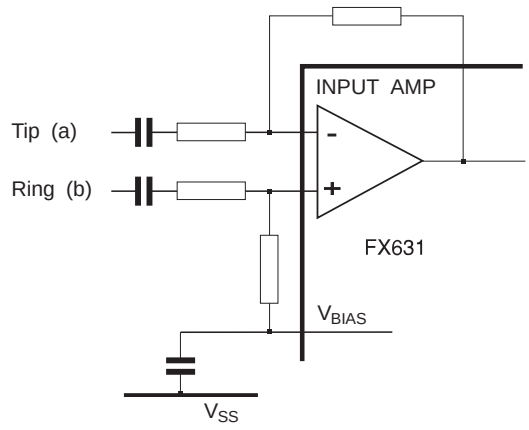
Component	Value
R_1	$R_{FEEDBACK}$
R_2	$R_{IN\ (-)}$
R_3	$R_{IN\ (+)}$
R_4	R_{BIAS}
C_1	1.0µF ±20%
C_2	1.0µF ±20%
C_3	$C_{IN\ (-)}$
C_4	$C_{IN\ (+)}$
X_1	3.579545MHz

External Components

1. The values of the Input Amp gain components illustrated are calculated using the Input Gain Calculation Graphs (Figures 4 and 5). Whilst calculating input gain components, for correct operation, it is recommended that the values of resistors R_1 and R_4 are always greater than, or equal to, 33kΩ.

2. Refer to following pages for advice on Microcircuit Protection from high and spurious line voltages.

Differential Input



Common Mode Input

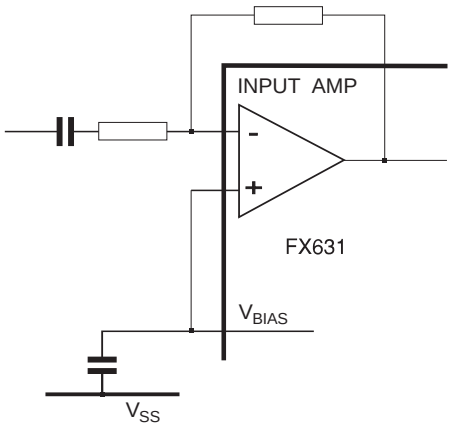


Fig.3 Example Input Configurations

Application Information .....

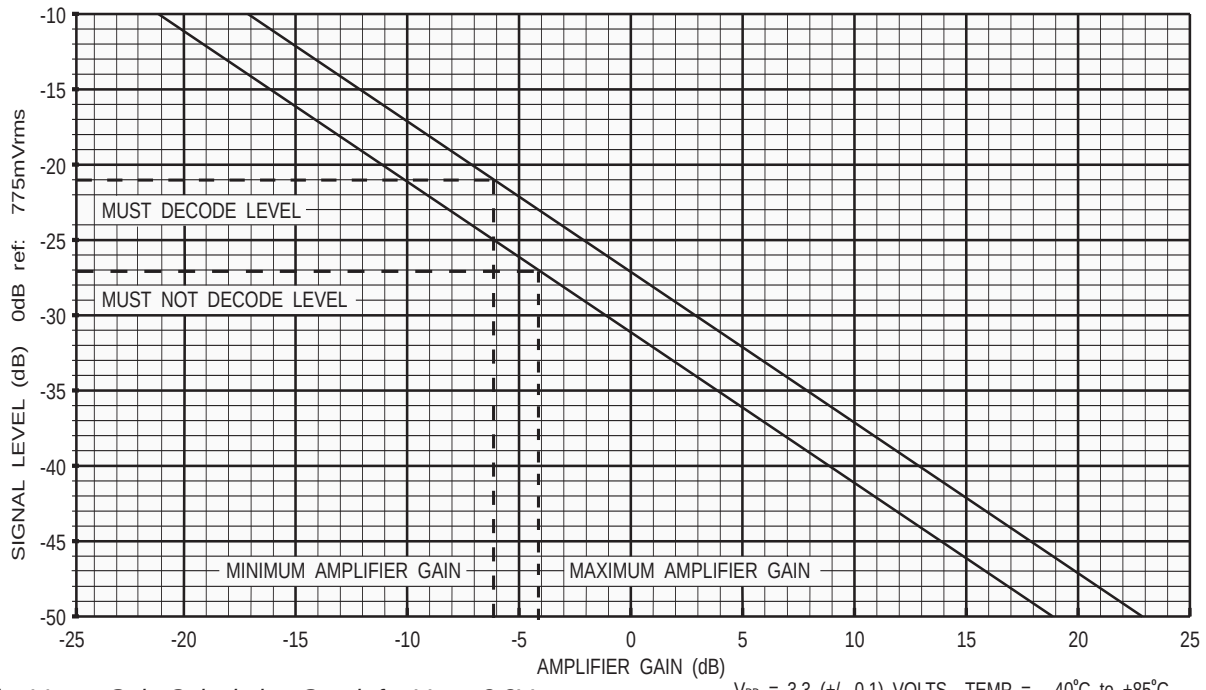


Fig.4 Input Gain Calculation Graph for V_{DD} = 3.3V

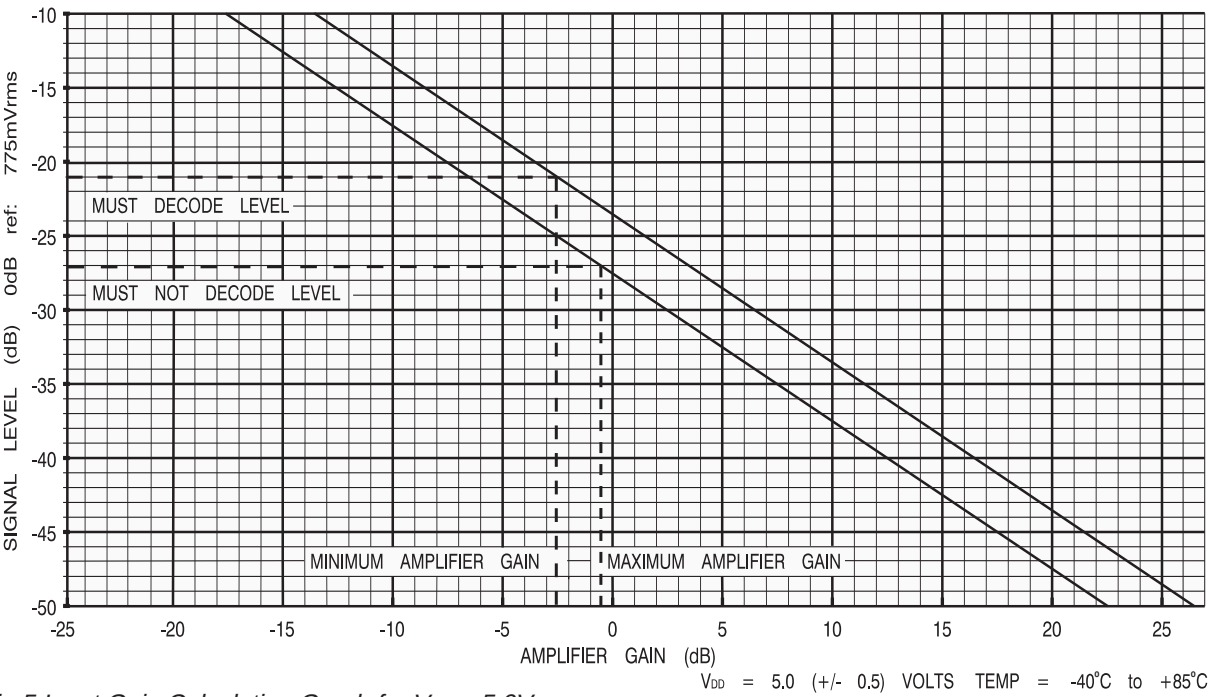


Fig.5 Input Gain Calculation Graph for V_{DD} = 5.0V

Application Information .....

Input Gain Calculation

The input amplifier, with its external circuitry, is provided on-chip to set the sensitivity of the FX631 to conform to the user's national level specification with regard to 'Must' and 'Must-Not' decode signal levels.

With reference to the graphs in Figures 4 and 5, the following steps will assist in the determination of the required gain/attenuation.

Step 1

Draw two horizontal lines from the Y-axis (Signal Levels (dB)).
The upper line will represent the required 'Must' decode level.
The lower line will represent the required 'Must-Not' decode level.

Step 2

Mark the intersection of the upper horizontal line and the upper sloping line; drop a vertical line from this point to the X-axis (Amplifier Gain (dB)).
The point where the vertical line meets the X-axis will indicate the MINIMUM Input Amp gain required for reliable decoding of valid signals.

Step 3

Mark the intersection of the lower horizontal line and the lower sloping line; drop a vertical line from this point to the X-axis.
The point where the vertical line meets the X-axis will indicate the MAXIMUM allowable Input Amp gain.
Input signals at or below the 'Must-Not' decode level will not be detected as long as the amplifier gain is no higher than this level.
Select the gain components as described opposite.

Input Gain Components

With reference to the gain components shown in Figures 2 and 3.

The user should calculate and select external components (R_1, R_2/C_3, R_3/C_4, R_4) to provide an amplifier gain within the limits obtained in Steps 2 and 3.

Component tolerances should not move the gain-figure outside these limits.

It is recommended that the designed gain is near the centre of the calculated range. The graphs in Figures 4 and 5 are for the calculation of input gain components for an FX631 using a V_{DD} of 3.3 (±0.1) or 5.0 (±0.5) volts respectively.

Use this area to keep a permanent record of your calculated gains and components

Implementation Notes

Aliasing

Due to the switched-capacitor filters employed in the FX631, care should be taken, with the chosen external components, to avoid the effects of alias distortion.

Possible Alias Frequencies:
12kHz Mode = 52kHz
16kHz Mode = 69kHz

If these alias frequencies are liable to cause problems and/or interference, it is recommended that anti-alias capacitors are employed across input resistors R_1 and R_4.

Values of anti-alias capacitors should be chosen so as to provide a highpass cutoff frequency, in conjunction with R_1 (R_4) of approximately 20kHz to 25kHz (12kHz system) or 25kHz to 30kHz (16kHz system).

$$\text{i.e. } C = \frac{1}{2 \times \pi \times f_0 \times R_1}$$

When anti-alias capacitors are used, allowance must be made for reduced gain at the SPM frequency (12kHz or 16kHz).

Microcircuit Protection

Telephone systems may have high d.c. and a.c. voltages present on the line. If the FX631 is part of a host equipment that has its own signal input protection circuitry, there will be no need for further protection as long as the voltage on any pin is limited to within V_{DD} + 0.3V and V_{SS} -0.3V.

If the host system does not have input protection, or there are signals present outside the device's specified limits, the FX631 will require protection diodes at its signal inputs (+ and -). The breakdown voltage of capacitors and the peak inverse voltage of the diodes must be sufficient to withstand the sum of the d.c. voltages plus all expected signal peaks.

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)		-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)		+/- 30mA
(other pins)		+/- 20mA
Total device dissipation (DW/P) @ T_{AMB} 25°C		800mW Max.
(D5) @ T_{AMB} 25°C		550mW Max.
Derating (DW/P)		10mW/°C
(D5)		9mW/°C
Operating Temperature (T_{OP}):	**FX631DW/D5/P**	-40°C to +85°C
Storage temperature range (T_{ST}):	**FX631DW/D5/P**	-40°C to +85°C

Functional Limits .....

	Min.	Max.	Unit	
Supply Voltage (V_{DD})	3.0	5.5	V	at 25°C

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 3.3V to 5.0V T_{OP} = -40 to +85 °C. Audio Level 0dB ref: = 775mVrms. Noise Bandwidth = 50kHz. Xtal/Clock or 'Clock In' Frequency = 3.579545MHz. 12kHz or 16kHz System Setting.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Supply Current	1	-	-	1.0	mA
	2	-	-	2.0	mA
Input Logic "1" (High)		70	-	-	%V_{DD}
Input Logic "0" (Low)		-	-	30	%V_{DD}
Output Logic "1" (High)		90	-	-	%V_{DD}
Output Logic "0" (Low)		-	-	10	%V_{DD}
Xtal/Clock or Clock In Frequency		3.558918	–	3.589368	MHz
"High" External Clock Pulse Width		100	-	-	ns
"Low" External Clock Pulse Width		100	-	-	ns
Input Amp					
D.C. Gain		60.0	-	-	dB
Bandwidth (-3dB)		-	100	-	Hz
Input Impedance		-	1.0	-	MΩ
Logic Impedances					
Input (System)		0.7	-	3.8	MΩ
(Clock In)		10.0	-	-	MΩ
Output		-	14.0	30.0	kΩ
Overall Performance					
12kHz Detect Bandwidth	3	11.820		12.180	kHz
12kHz Not-Detect Frequencies (below 12kHz)	3	-	-	11.520	kHz
12kHz Not-Detect Frequencies (above 12kHz)	3	12.480	-	-	kHz
16kHz Detect Bandwidth	3	15.760		16.240	kHz
16kHz Not-Detect Frequencies (below 16kHz)	3	-	-	15.360	kHz
16kHz Not-Detect Frequencies (above 16kHz)	3	16.640	-	-	kHz
Sensitivity	4	7.8	10.0	15.5	mVp-p
Tone Operation Characteristics					
Signal-to-Noise Requirements (Amp Input)	5, 6, 7, 8	22.0	20.0	-	dB
Signal-to-Voice Requirements (Amp Input)	5, 6, 7, 9	-36.0	-40.0	-	dB
Signal-to-Voice Requirements (Amp Output)	7, 8	-25.0	-	-29.0	dB
Tone Follower Output					
Response and De-Response Times	3, 10	-	-	10.0	ms
Packet Mode Output					
Response and De-Response Times	3, 10	40.0	-	48.0	ms

Notes .. ..

Specification .....

Notes

1. V_{DD} = 3.3V
2. V_{DD} = 5.0V
3. With adherence to Signal-to-Voice and Signal-to Noise specifications.
4. With Input Amp gain setting: $15.5dB_{MIN}$/$18.0dB_{MAX}$.
5. Common Mode SPM and balanced voice signal.
6. Immune to false responses.
7. Immune to false de-responses
8. With SPM and voice signal amplitudes balanced; To avoid false de-responses due to saturation, the peak-to-peak voice+noise level at the output of the Input Amp (12/16kHz Filter Input) should be no greater than the dynamic range of the device.
9. Maximum voice frequencies = 3.4kHz
10. Response, De-Response and Power-up Response Timing.

Application Information .....

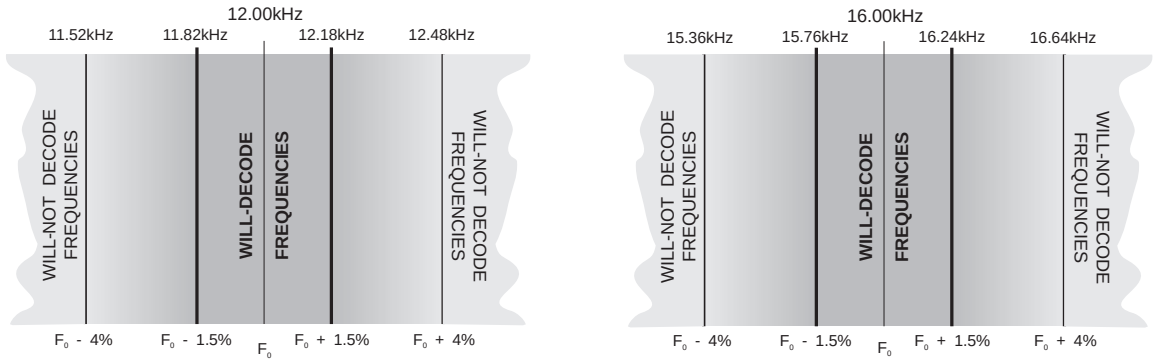


Fig.6 Will/Will-Not Decode Frequencies

System Timing

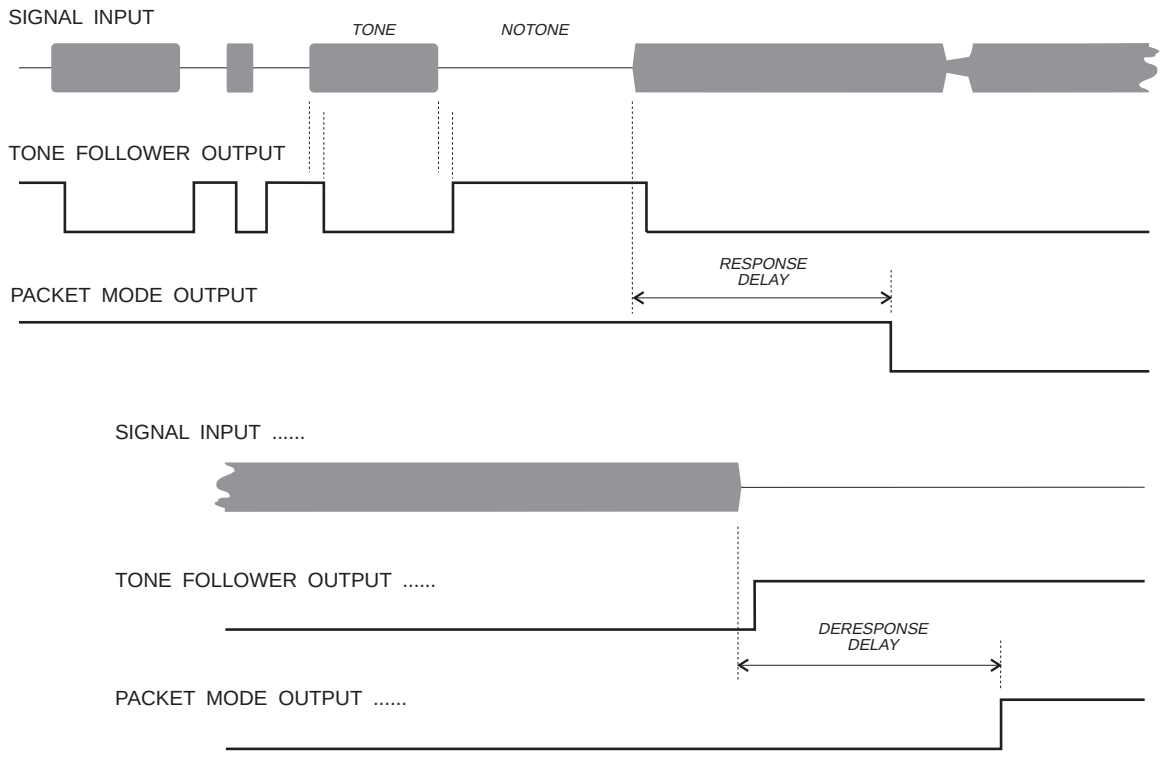


Fig.7 Examples of Input and Output Relationships

Package Outlines

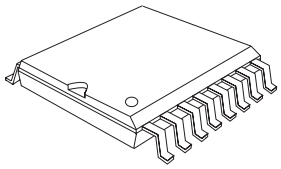
The FX631 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

Handling Precautions

The FX631 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX631DW 16-pin plastic S.O.I.C. **(D4)**

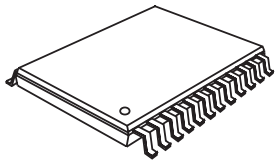
NOT TO SCALE



Max. Body Length	10.49mm
Max. Body Width	7.59mm

FX631D5 24-pin plastic S.S.O.P.

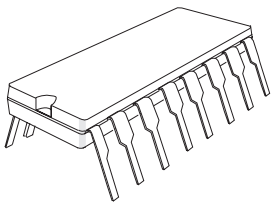
NOT TO SCALE



Max. Body Length	8.33mm
Max. Body Width	5.38mm

FX631P 16-pin plastic DIL **(P3)**

NOT TO SCALE



Max. Body Length	20.57mm
Max. Body Width	6.60mm

Ordering Information

FX631DW	16-pin plastic S.O.I.C.	**(D4)**
FX631D5	24-pin plastic S.S.O.P.	
FX631P	16-pin plastic DIL	**(P3)**