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# HM6287, HM6287H Series

65536-word  $\times$  1-bit High Speed CMOS Static RAM

**HITACHI**

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## Description

The Hitachi HM6287/HM6287H is a high speed 64 k static RAM organized as 64-kword  $\times$  1-bit. It realizes high speed access time (25/35/45/55/70 ns) and low power consumption, employing CMOS process technology and high speed circuit design technology. It is most advantageous for high speed and high density memory, such as cache memory for mainframes or 32-bit MPUs. The HM6287/HM6287H is packaged in a 300-mil plastic DIP and SOJ, and is available for high density mounting. The low power version retains data with battery backup.

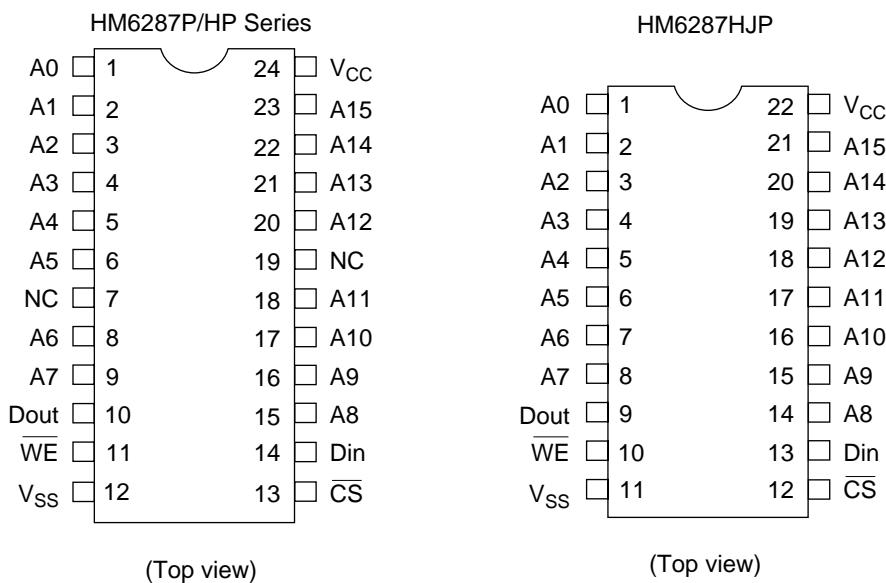
## Features

- Single 5 V supply and high density 22-pin DIP and 24-pin SOJ
- High speed: Fast access time 25/35/45/55/70 ns (max)
- Low power
  - Operation: 300 mW (typ)
  - Standby: 100  $\mu$ W (typ)/10  $\mu$ W (typ) (L-version)
- Completely static memory
- No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible: All inputs and outputs
- Battery backup capability (L-version)

## Ordering Information

Type No.	Access Time	Package
HM6287P-45	45 ns	300-mil, 22-pin plastic DIP (DP-22N)
HM6287P-55	55 ns	
HM6287P-70	70 ns	
HM6287LP-45	45 ns	
HM6287LP-55	55 ns	
HM6287LP-70	70 ns	
HM6287HP-25	25 ns	300-mil, 22-pin plastic DIP (DP-22NB)
HM6287HP-35	35 ns	
HM6287HLP-25	25 ns	
HM6287HLP-35	35 ns	
HM6287HJP-25	25 ns	300-mil, 24-pin SOJ (CP-24D)
HM6287HJP-35	35 ns	
HM6287HLJP-25	25 ns	
HM6287HLJP-35	35 ns	

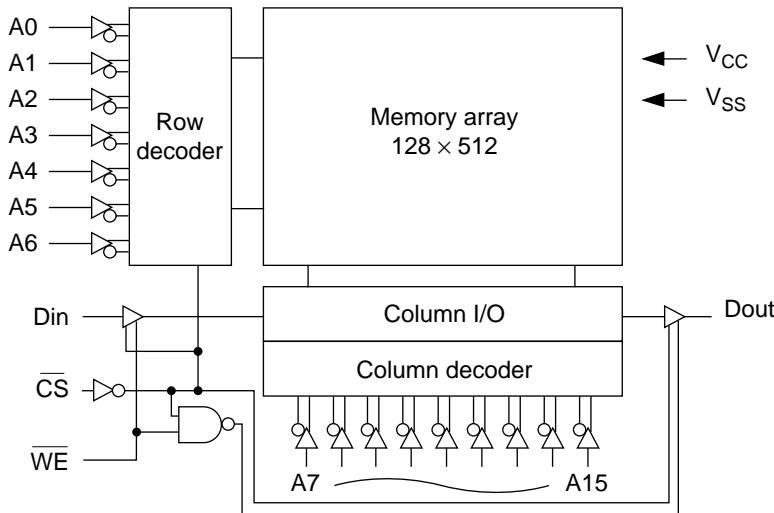
## Pin Arrangement



## Pin Description

Pin Name	Function
A0–A15	Address
Din	Input
Dout	Output
CS	Chip select
WE	Write enable
V <sub>cc</sub>	Power supply
V <sub>ss</sub>	Ground

## Block Diagram



## Truth Table

CS	WE	Mode	V <sub>cc</sub> current	Dout pin	Ref. Cycle
H	×	Standby	I <sub>SB</sub> , I <sub>SB1</sub>	High-Z	—
L	H	Read	I <sub>cc</sub>	Dout	Read cycle 1, 2
L	L	Write	I <sub>cc</sub>	High-Z	Write cycle 1, 2

Note: ×: Don't care.

## Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage any pin relative to $V_{ss}$	$V_T$	-0.5° to +7.0	V
Power dissipation	$P_T$	1.0	W
Operating temperature	$Topr$	0 to +70	°C
Storage temperature	$Tstg$	-55 to +125	°C
Storage temperature under bias	$Tbias$	-10 to +85	°C

Note:  $V_T$  min: -3.5 V for pulse width  $\leq$  20 ns (HM6287 Series)

$V_T$  min: -2.0 V for pulse width  $\leq$  10 ns (HM6287H Series)

## Recommended DC Operating Conditions ( $Ta = 0$ to $+70^\circ\text{C}$ )

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{cc}$	4.5	5.0	5.5	V
	$V_{ss}$	0	0	0	V
Input high (logic 1) voltage	$V_{ih}$	2.2	—	6.0	V
Input low (logic 0) voltage	$V_{il}$	-0.5° <sup>1</sup>	—	0.8	V

Note: 1.  $V_{il}$  min: -3.0 V for pulse width  $\leq$  20 ns (HM6287 Series)

$V_{il}$  min: -2.0 V for pulse width  $\leq$  10 ns (HM6287H Series)

## DC Characteristics ( $Ta = 0$ to $+70^\circ\text{C}$ , $V_{cc} = 5 \text{ V} \pm 10\%$ , $V_{ss} = 0 \text{ V}$ )

Parameter	Symbol	HM6287			HM6287H			Unit	Test Conditions
		Min	Typ <sup>*1</sup>	Max	Min	Typ <sup>*1</sup>	Max		
Input leakage current	$ I_{ul} $	—	—	2.0	—	—	2.0	μA	$V_{cc} = \text{Max}$ $V_{in} = V_{ss}$ to $V_{cc}$
Output leakage current	$ I_{ol} $	—	—	2.0	—	—	2.0	μA	$\overline{CS} = V_{ih}$ , $V_{io} = V_{ss}$ to $V_{cc}$
Operating $V_{cc}$ current	$I_{cc}$	—	60	100	—	60	120	mA	$\overline{CS} = V_{il}$ , $I_{out} = 0 \text{ mA}$ , min cycle
Standby $V_{cc}$ current	$I_{sb}$	—	10	30	—	15	30	mA	$\overline{CS} = V_{ih}$ , min. cycle
Standby $V_{cc}$ current (1)	$I_{sb1}$	—	0.02	2.0	—	0.02	2.0	mA	$\overline{CS} \geq V_{cc} - 0.2 \text{ V}$
		—	0.02 <sup>*2</sup>	0.1 <sup>*2</sup>	—	0.02 <sup>*2</sup>	0.1 <sup>*2</sup>	mA	$0 \text{ V} \leq V_{in} \leq 0.2 \text{ V}$ or $V_{cc} - 0.2 \text{ V} \leq V_{in}$
Output low voltage	$V_{ol}$	—	—	0.4	—	—	0.4	V	$I_{ol} = 8 \text{ mA}$
Output high voltage	$V_{oh}$	2.4	—	—	2.4	—	—	V	$I_{oh} = -4.0 \text{ mA}$

Notes: 1. Typical values are at  $V_{cc} = 5.0 \text{ V}$ ,  $Ta = +25^\circ\text{C}$  and not guaranteed.

2. These characteristics are guaranteed only for L-version.

Capacitance (Ta = 25°C, f = 1.0 MHz)<sup>\*1</sup>

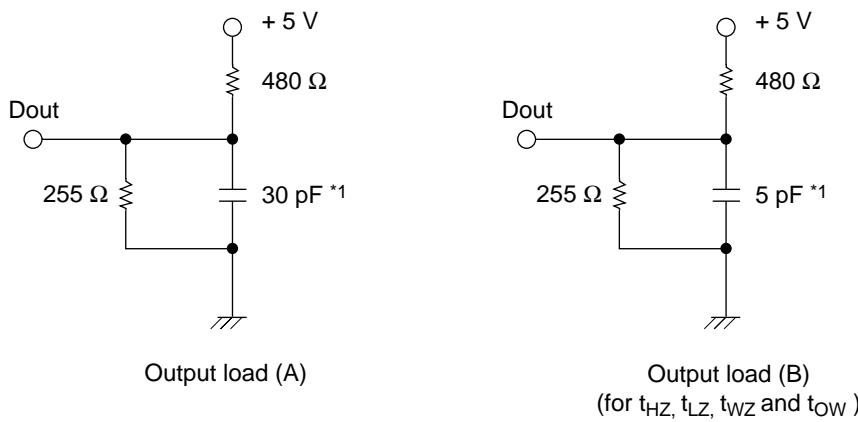
Parameter	Symbol	HM6287		HM6287H		Unit	Test Conditions
		Min	Max	Min	Max		
Input capacitance	Cin	—	5	—	6	pF	Vin = 0 V
Output capacitance	Cout	—	7.5	—	8	pF	Vout = 0 V

Note: 1. These parameters are sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V<sub>CC</sub> = 5 V ± 10%, unless otherwise noted.)

### Test Conditions

- Input pulse levels: V<sub>SS</sub> to 3.0 V
- Input and output timing reference levels: 1.5 V
- Input rise and fall time: 5 ns
- Output load: See figure



Note: 1. Including scope and jig

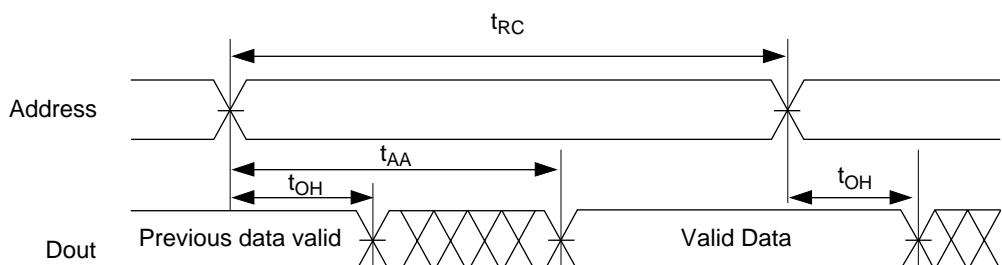
## Read Cycle

Parameter	Symbol	HM6287H-25		HM6287H-35		HM6287-45		HM6287-55		HM6287-70		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read cycle time	$t_{RC}$	25	—	35	—	45	—	55	—	70	—	ns	2
Address access time	$t_{AA}$	—	25	—	35	—	45	—	55	—	70	ns	
Chip select access time	$t_{ACS}$	—	25	—	35	—	45	—	55	—	70	ns	
Output hold from address change	$t_{OH}$	3	—	5	—	5	—	5	—	5	—	ns	
Chip selection to output in low-Z	$t_{LZ}$	5	—	5	—	5	—	5	—	5	—	ns	1, 3, 4
Chip deselection to output in high-Z	$t_{HZ}$	0	12	0	20	0	30	0	30	0	30	ns	1, 3, 4
Chip selection to power-up time	$t_{PU}$	0	—	0	—	0	—	0	—	0	—	ns	4
Chip deselection to power-down time	$t_{PD}$	—	25	—	30	—	40	—	40	—	40	ns	4

Notes:

1. Transition is measured +200 mV from steady state voltage with load (B).
2. All read cycle timing is referenced from last valid address to the first transitioning address.
3. At any given temperature and voltage condition,  $t_{HZ}$  max, is less the  $t_{LZ}$  min both for a given device and from device to device.
4. These parameters are sampled and not 100% tested.

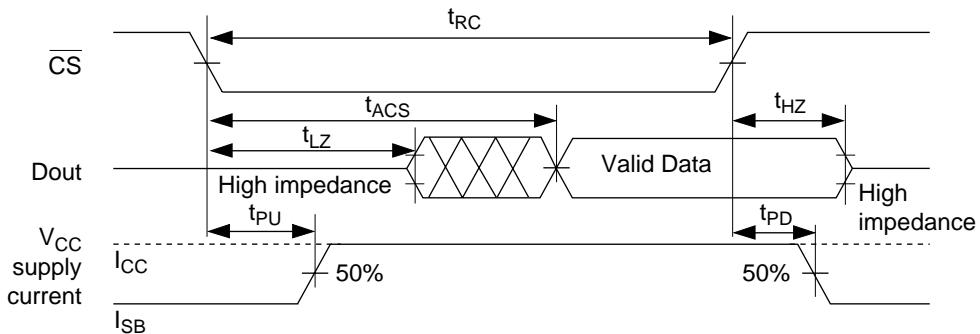
## Read Timing Waveform (1)



Notes:

1.  $\overline{WE}$  is high for read cycle.
2. Device is continuously selected,  $\overline{CS} = V_{IL}$ .
3. All read cycle timing is referred from last valid address to the first transitioning address.

## Read Timing Waveform (2)



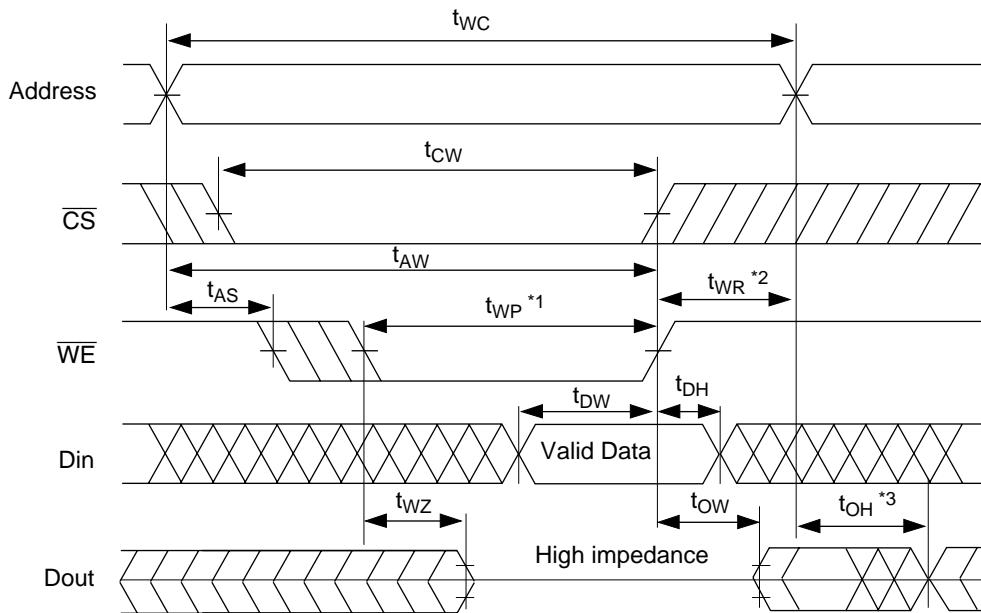
Notes: 1.  $\overline{WE}$  is high for read cycle.  
 2. Address valid prior to or coincident with  $\overline{CS}$  transition low.

## Write Cycle

Parameter	Symbol	HM6287H- 25		HM6287H- 35		HM6287- 45		HM6287- 55		HM6287- 70		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write cycle time	$t_{WC}$	25	—	35	—	45	—	55	—	70	—	ns	1
Chip selection to end of write	$t_{CW}$	20	—	30	—	40	—	50	—	55	—	ns	
Address valid to end of write	$t_{AW}$	20	—	30	—	40	—	50	—	55	—	ns	
Address setup time	$t_{AS}$	0	—	0	—	0	—	0	—	0	—	ns	
Write pulse width	$t_{WP}$	20	—	30	—	25	—	35	—	40	—	ns	
Write recovery time	$t_{WR}$	0	—	0	—	0	—	0	—	0	—	ns	
Data valid to end of write	$t_{DW}$	15	—	20	—	25	—	25	—	30	—	ns	
Data hold time	$t_{DH}$	0	—	0	—	0	—	0	—	0	—	ns	
Write enabled to output in high-Z	$t_{WZ}$	0	8	0	10	0	25	0	25	0	30	ns	2
Output active from end of write	$t_{OW}$	5	—	5	—	0	—	0	—	0	—	ns	2

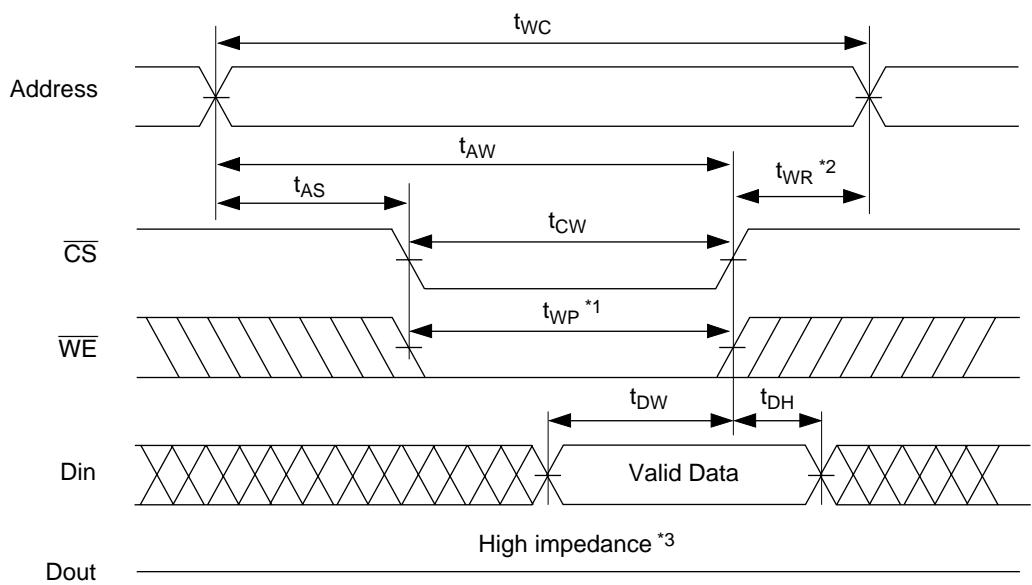
Notes: 1. All write cycle timing is referenced from the last valid address to first transitioning address.  
 2. Transition is measured  $\pm 200$  mV from steady state voltage with load B. These parameters are sampled and not 100% tested.

## Write Timing Waveform (1) ( $\overline{WE}$ Controlled)



Notes:

1. A write occurs during the overlap of a low  $\overline{CS}$  and a low  $\overline{WE}$  ( $t_{WP}$ ).
2.  $t_{WR}$  is measured from the earlier of  $\overline{CS}$  or  $\overline{WE}$  going high to the end of the write cycle.
3. Dout is the same phase of write data of this write cycle, if  $t_{WR}$  is long enough.

Write Timing Waveform (2) ( $\overline{\text{CS}}$  Controlled)

Notes:

1. A write occurs during the overlap of a low  $\overline{\text{CS}}$  and a low  $\overline{\text{WE}}$  ( $t_{WP}$ ).
2.  $t_{WR}$  is measured from the earlier of  $\overline{\text{CS}}$  or  $\overline{\text{WE}}$  going high to the end of the write cycle.
3. If  $\overline{\text{CS}}$  low transition occurs simultaneously with the  $\overline{\text{WE}}$  low transition or after the  $\overline{\text{WE}}$  transition, the output buffers remain in a high impedance state.

## Low $V_{CC}$ Data Retention Characteristics ( $T_a = 0$ to $+70^\circ C$ )

These specifications are guaranteed only for L-version.

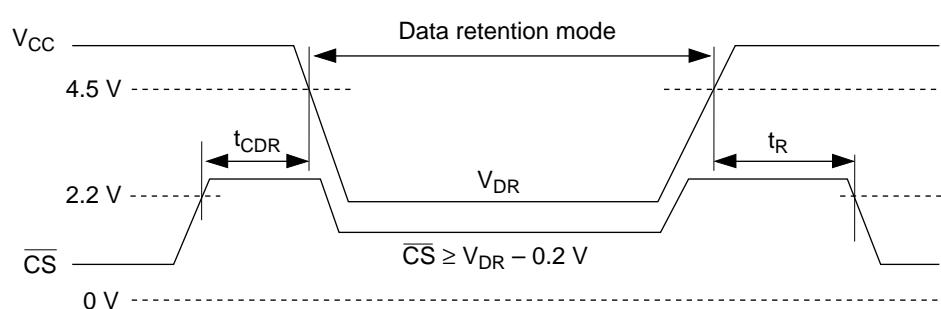
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
$V_{CC}$ for data retention	$V_{DR}$	2.0	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V, 0 V $\geq$ $V_{in} - 0.2$ V, or 0 V $\leq$ $V_{in} \leq 0.2$ V
Data retention current	$I_{CCDR}$	—	—	$50^{*2}$	$\mu A$	
		—	—	$35^{*3}$	$\mu A$	
Chip deselect to data retention time	$t_{CDR}$	0	—	—	ns	See retention waveform
Operation recovery time	$t_R$	$t_{RC}^{*1}$	—	—	ns	

Notes: 1.  $t_{RC}$  = Read cycle time

2.  $V_{CC} = 3.0$  V

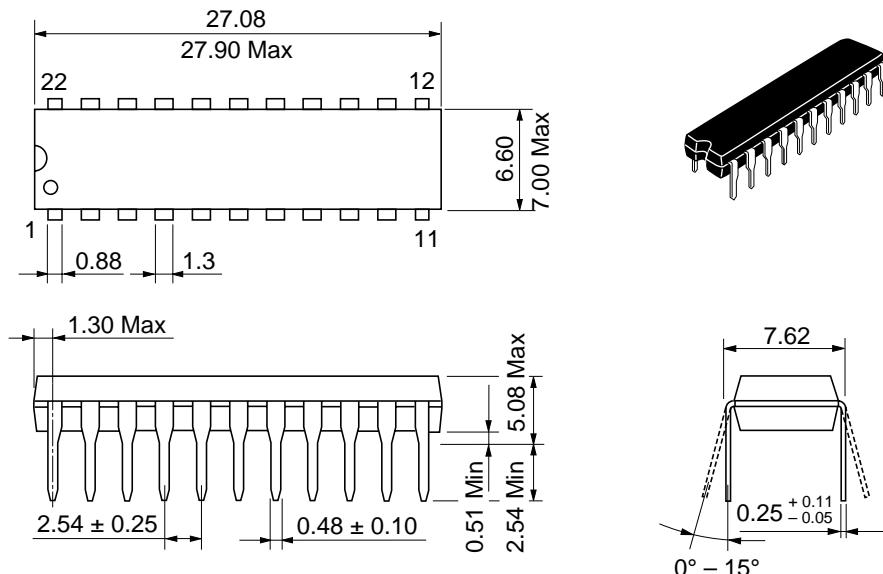
3.  $V_{CC} = 2.0$  V

## Low $V_{CC}$ Data Retention Waveform

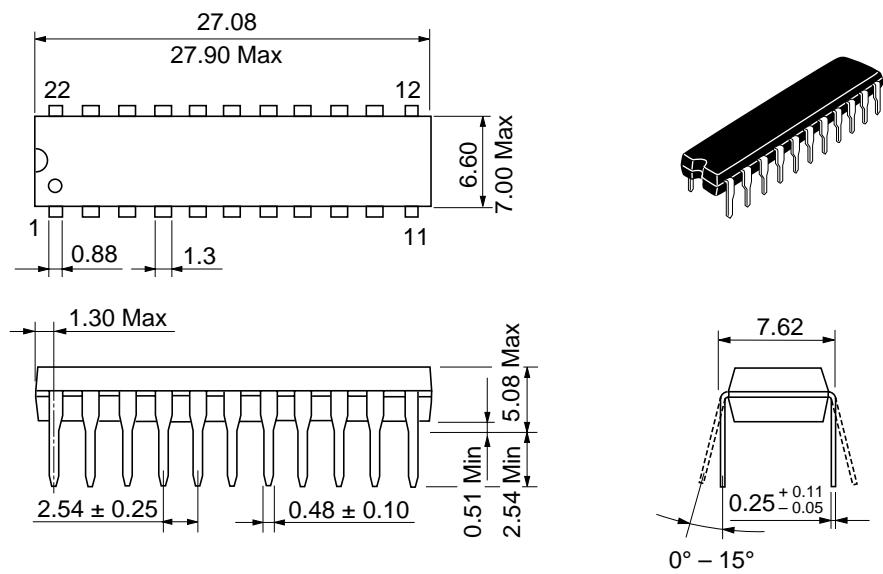


**Package Dimensions****HM6287P/LP Series (DP-22N)**

Unit: mm

**HM6287HP/HLP Series (DP-22NB)**

Unit: mm



# HM6287, HM6287H Series

## HM6287HJP/HLJP Series (CP-24D)

Unit: mm

