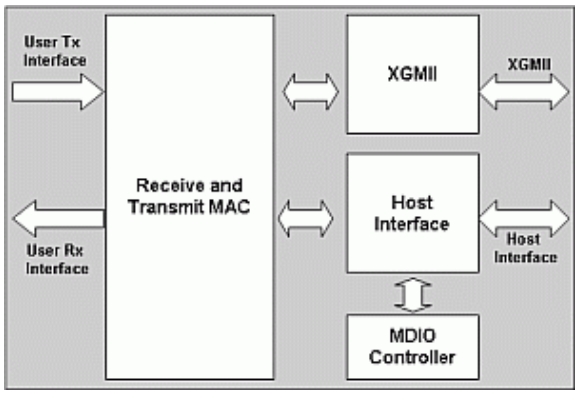
10Gb+ Ethernet MAC

Overview

The **10Gb+ Ethernet Media Access Controller** (MAC) transmits and receives data between a host processor and an Ethernet network. The main function of the 10Gb+ Ethernet MAC is to ensure that the Media Access rules specified in the IEEE802.3ae standard are met while transmitting a frame of data over Ethernet. On the receive side, the Ethernet MAC extracts the different components of a frame and transfers them to higher applications through a FIFO interface.



Features

- Compliant to IEEE 802.3-2005 standard, successfully passed University of New Hampshire InterOperability Laboratory(UNH-IOL) 10GbE MAC hardware tests
- Supports standard 10Gbps Ethernet link layer data rate
- Supports rates up to 12Gbps by over-clocking
- 64-bit wide internal data path operating at 156.25MHz to 187.5MHz
- XGMII interface to the PHY layer (using IODDR external to the core)
- XAUI interface to the PHY layer (using PCS/SERDES external to the core)
- Simple FIFO interface with user's application
- Optional Multicast address filtering
- Transmit and receive statistics vector
- Optional statistics counters of length from 16 to 40 bits for all devices (statistic counters are external to the core)
- Programmable Inter Frame Gap
- Supports:
  - Full duplex operation
  - Flow control using PAUSE frames
  - VLAN tagged frames
  - Automatic padding of short frames
  - Optional FCS generation during transmission
  - Optional FCS stripping during reception
  - Jumbo frames up to 16k
  - Inter frame Stretch Mode during transmission
  - Deficit Idle Count

Data rates up to 12Gbps are supported by increasing the 10 Gb+ Ethernet MAC system clock rate from the standard frequency of 156.25MHz used for processing 10Gbps data up to frequencies as high as 187.50MHz.

Performance and Resource Utilization

LatticeECP3[1]

Mode	SLICEs	LUTs	Registers	External Pins[2]	sysMEM EBRs	f_{MAX} (MHz)
Multicast Address Filtering	3239	4024	2833	78	4	160

1. Performance and utilization data are generated using an LFE3-35EA-8FN672C device with Lattice's Diamond 1.1 software with Synplify Pro D-2010.03L-SP1 synthesis. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP3 family.

2. The 10 Gb+ Ethernet MAC core itself does not use any external pins. However, in an application the core is used together IODDR and I/O Buffers integrated in the LatticeECP3 series FPGA. Thus the application implementing the 10 Gb+ Ethernet MAC specification will utilize I/O pins.

LatticeECP2M / S[1]

Mode	SLICEs	LUTs	Registers	External Pins[2]	sysMEM EBRs	f_{MAX} (MHz)
Multicast Address Filtering	3153	4370	2777	78	4	181

1. Performance and utilization data are generated using an LFE2M35E-7F672C device with Lattice's Diamond 1.1 software with Synplify Pro D-2010.03L-SP1 synthesis. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP2M/S family.
2. The 10 Gb+ Ethernet MAC core itself does not use any external pins. However, in an application the core is used together IODDR and I/O Buffers integrated in the LatticeECP2M series FPGA. Thus the application implementing the 10 Gb+ Ethernet MAC specification will utilize I/O pins.

LatticeECP2 / S[1]

Mode	SLICEs	LUTs	Registers	External Pins[2]	sysMEM EBRs	f_{MAX} (MHz)
Multicast Address Filtering	3153	4022	2777	78	4	170

1. Performance and utilization data are generated using an LFE2-35E-7F672C device with Lattice's Diamond 1.1 software with Synplify Pro D-2010.03L-SP1 synthesis. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP2/S family.
2. The 10 Gb+ Ethernet MAC core itself does not use any external pins. However, in an application the core is used together IODDR and I/O Buffers integrated in the LatticeECP2 series FPGA. Thus the application implementing the 10 Gb+ Ethernet MAC specification will utilize I/O pins.

LatticeSC / M[1]

Mode	SLICEs	LUTs	Registers	External Pins[2]	sysMEM EBRs	f_{MAX} (MHz)
Multicast Address Filtering	2961	4370	2764	78	4	205

1. Performance and utilization data are generated using an LFSC3GA25E-5F900C device with Lattice's Diamond 1.1 software with Synplify Pro D-2010.03L-SP1 synthesis. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeSC family.
2. The 10 Gb+ Ethernet MAC core itself does not use any external pins. However, in an application the core is used together IODDR and I/O Buffers integrated in the LatticeSC series FPGA. Thus the application implementing the 10 Gb+ Ethernet MAC specification will utilize I/O pins.

Ordering Information

Family	Part Numbers
LatticeECP3	ETHER-10G-E3-U4
LatticeECP2M	ETHER-10G-PM-U4
LatticeECP2	ETHER-10G-P2-U4
LatticeSC/M	ETHER-10G-SC-U4

IP Version: 4.3

Evaluate: To download a full evaluation version of this IP, go to the IPexpress tool and click the IP Server button in the toolbar. All LatticeCORE IP cores and modules available for download will be visible. For more information on viewing/downloading IP please read the **IP Express Quick Start Guide**.

Purchase: To find out how to purchase the IP Core, please contact your **local Lattice Sales Office**.