# Single/Dual/Quad 18MHz, Low Noise, Rail-to-Rail Output, CMOS Op Amps

## FEATURES

- **0.1Hz to 10Hz Noise: 550nV$_{P-P}$**
- **Input Bias Current:**
  **0.2pA (Typ at 25°C)**
  **1pA Max (LTC6240)**
- **Low Offset Voltage: 125µV Max**
- Low Offset Drift: 2.5µV/°C Max
- Gain Bandwidth Product: 18MHz
- Output Swings Rail-to-Rail
- Supply Operation:
  2.8V to 6V LTC6240/LTC6241/LTC6242
  2.8V to ±5.5V LTC6240HV/LTC6241HV/LTC6242HV
- Low Input Capacitance
- H-Grade Temperature Range: –40°C to 125°C
- Single LTC6240 in 5-Pin Low Profile (1mm) ThinSOT™ Package and 8-Pin SO for PCB Guard Ring
- Dual LTC6241 in 8-Pin SO and Tiny DFN Packages
- Quad LTC6242 in 16-Pin SSOP and 5mm × 3mm DFN Packages

## APPLICATIONS

- Photo Diode Amplifiers
- Charge Coupled Amplifiers
- Low Noise Signal Processing
- Medical Instrumentation
- High Impedance Transducer Amplifier

## DESCRIPTION

The LTC®6240/6241/LTC6242 are single, dual and quad low noise, low offset, rail-to-rail output, unity gain stable CMOS op amps that feature 1pA of input bias current. Input bias current is guaranteed to be 1pA max on the single LTC6240. The 0.1Hz to 10Hz noise of only 550nV$_{P-P}$, along with an offset of just 125µV are significant improvements over traditional CMOS op amps. Additionally, noise is guaranteed to be less than 10nV/√Hz at 1kHz. An 18MHz gain bandwidth, and 10V/µs slew rate, along with the wide supply range and low input capacitance, make them perfect for use as fast signal processing amplifiers.

These op amps have an output stage that swings within 30mV of either supply rail to maximize the signal dynamic range in low supply applications. The input common mode range extends to the negative supply. They are fully specified on 3V and 5V, and an HV version guarantees operation on supplies up to ±5V.

The LTC6240 is available in the 8-pin SO and the 5-pin SOT-23 packages. The LTC6241 is available in the 8-pin SO, and for compact designs it is packaged in a tiny dual fine pitch leadless (DFN) package. The LTC6242 is available in the 16-pin SSOP as well as the 5mm × 3mm DFN package.

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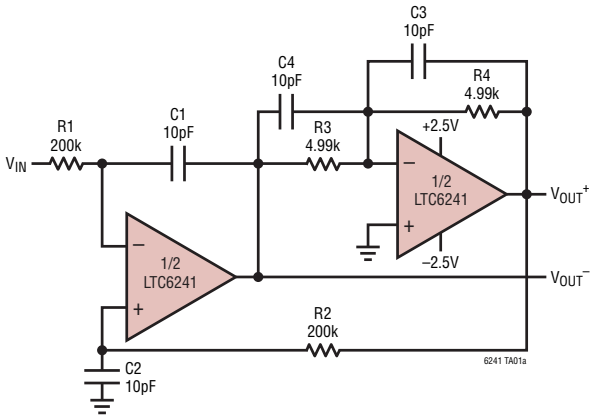
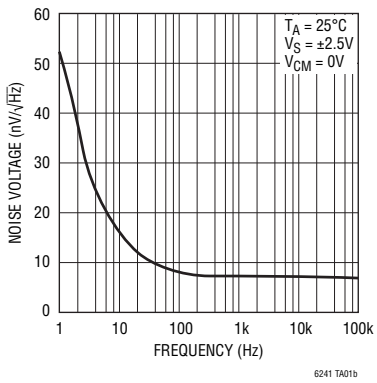
## TYPICAL APPLICATION

**Low Noise Single-Ended Input to Differential Output Amplifier**




**Noise Voltage vs Frequency**



## ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage ($V^+$ to $V^-$)
- LTC6240/LTC6241/LTC6242 ..... 7V
- LTC6240HV/LTC6241HV/LTC6242HV ..... 12V

Input Voltage ..... ($V^+$ + 0.3V) to ($V^-$ – 0.3V)
Input Current ..... ±10mA
Output Short-Circuit Duration (Note 2) ..... Indefinite
Operating Temperature Range
- LTC6240C/LTC6241C/LTC6242C ..... –40°C to 85°C
- LTC6240I/LTC6241I/LTC6242I ..... –40°C to 85°C
- LTC6240H/LTC6241H/LTC6242H ..... –40°C to 125°C

Specified Temperature Range (Note 3)
- LTC6240C/LTC6241C/LTC6242C ..... 0°C to 70°C
- LTC6240I/LTC6241I/LTC6242I ..... –40°C to 85°C
- LTC6240H/LTC6241H/LTC6242H ..... –40°C to 125°C

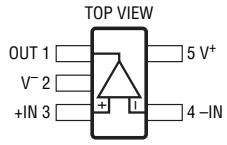
Junction Temperature ..... 150°C
- DHC, DD Package ..... 125°C

Storage Temperature Range ..... –65°C to 150°C
- DHC, DD Package ..... –65°C to 125°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

## PIN CONFIGURATION

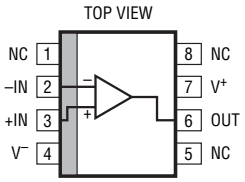
LTC6240




S5 PACKAGE
5-LEAD PLASTIC TSOT-23

$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 250°C/W

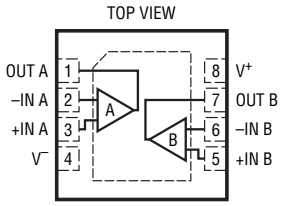
LTC6240




S8 PACKAGE
8-LEAD PLASTIC SO

$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 190°C/W

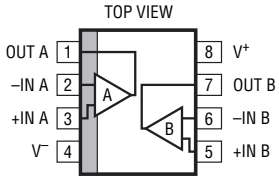
LTC6241




DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN

$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 43°C/W
UNDERSIDE METAL CONNECTED TO $V^-$
(PCB CONNECTION OPTIONAL)

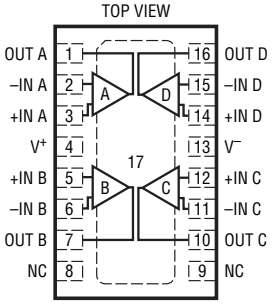
LTC6241




S8 PACKAGE
8-LEAD PLASTIC SO

$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 190°C/W

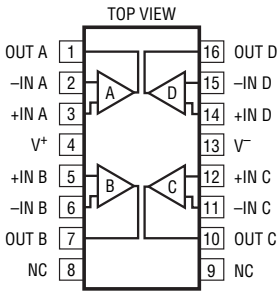
LTC6242




DHC PACKAGE
16-LEAD (5mm × 3mm) PLASTIC DFN

$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 43°C/W
UNDERSIDE METAL CONNECTED TO $V^-$ (PCB CONNECTION OPTIONAL)

LTC6242




GN PACKAGE
16-LEAD PLASTIC SSOP

$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 135°C/W

## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC6240CS5#PBF | LTC6240CS5#TRPBF | LTCRR | 5-Lead Plastic TSOT-23 | 0°C to 70°C |
| LTC6240HVCS5#PBF | LTC6240HVCS5#TRPBF | LTCRS | 5-Lead Plastic TSOT-23 | 0°C to 70°C |
| LTC6240IS5#PBF | LTC6240IS5#TRPBF | LTCRR | 5-Lead Plastic TSOT-23 | –40°C to 85°C |
| LTC6240HVIS5#PBF | LTC6240HVIS5 #TRPBF | LTCRS | 5-Lead Plastic TSOT-23 | –40°C to 85°C |
| LTC6240HS5#PBF | LTC6240HS5#TRPBF | LTCRR | 5-Lead Plastic TSOT-23 | –40°C to 125°C |
| LTC6240HVHS5#PBF | LTC6240HVHS5#TRPBF | LTCRS | 5-Lead Plastic TSOT-23 | –40°C to 125°C |
| LTC6240CS8#PBF | LTC6240CS8#TRPBF | 6240 | 8-Lead Plastic SO | 0°C to 70°C |
| LTC6240HVCS8#PBF | LTC6240HVCS8#TRPBF | 6240HV | 8-Lead Plastic SO | 0°C to 70°C |
| LTC6240IS8#PBF | LTC6240IS8#TRPBF | 6240I | 8-Lead Plastic SO | –40°C to 85°C |
| LTC6240HVIS8#PBF | LTC6240HVIS8#TRPBF | 240HVI | 8-Lead Plastic SO | –40°C to 85°C |
| LTC6240HS8#PBF | LTC6240HS8#TRPBF | 6240H | 8-Lead Plastic SO | –40°C to 125°C |
| LTC6240HVHS8#PBF | LTC6240HVHS8#TRPBF | 240HVH | 8-Lead Plastic SO | –40°C to 125°C |
| LTC6241CDD#PBF | LTC6241CDD#TRPBF | LBPD | 8-Lead (3mm × 3mm) Plastic DFN | 0°C to 70°C |
| LTC6241HVCDD#PBF | LTC6241HVCDD#TRPBF | LBRR | 8-Lead (3mm × 3mm) Plastic DFN | 0°C to 70°C |
| LTC6241IDD#PBF | LTC6241IDD#TRPBF | LBPD | 8-Lead (3mm × 3mm) Plastic DFN | –40°C to 85°C |
| LTC6241HVIDD#PBF | LTC6241HVIDD#TRPBF | LBRR | 8-Lead (3mm × 3mm) Plastic DFN | –40°C to 85°C |
| LTC6241CS8#PBF | LTC6241CS8#TRPBF | 6241 | 8-Lead Plastic SO | 0°C to 70°C |
| LTC6241HVCS8#PBF | LTC6241HVCS8#TRPBF | 6241HV | 8-Lead Plastic SO | 0°C to 70°C |
| LTC6241IS8#PBF | LTC6241IS8#TRPBF | 6241I | 8-Lead Plastic SO | –40°C to 85°C |
| LTC6241HVIS8#PBF | LTC6241HVIS8#TRPBF | 241HVI | 8-Lead Plastic SO | –40°C to 85°C |
| LTC6241HS8#PBF | LTC6241HS8#TRPBF | 6241H | 8-Lead Plastic SO | –40°C to 125°C |
| LTC6241HVHS8#PBF | LTC6241HVHS8#TRPBF | 241HVH | 8-Lead Plastic SO | –40°C to 125°C |
| LTC6242CDHC#PBF | LTC6242CDHC#TRPBF | 6242 | 16-Lead (5mm × 3mm) Plastic DFN | 0°C to 70°C |
| LTC6242HVCDHC#PBF | LTC6242HVCDHC#TRPBF | 6242HV | 16-Lead (5mm × 3mm) Plastic DFN | 0°C to 70°C |
| LTC6242IDHC#PBF | LTC6242IDHC#TRPBF | 6242 | 16-Lead (5mm × 3mm) Plastic DFN | –40°C to 85°C |
| LTC6242HVIDHC#PBF | LTC6242HVIDHC#TRPBF | 6242HV | 16-Lead (5mm × 3mm) Plastic DFN | –40°C to 85°C |
| LTC6242CGN#PBF | LTC6242CGN#TRPBF | 6242 | 16-Lead Plastic SSOP | 0°C to 70°C |
| LTC6242HVCGN#PBF | LTC6242HVCGN#TRPBF | 6242HV | 16-Lead Plastic SSOP | 0°C to 70°C |
| LTC6242IGN#PBF | LTC6242IGN#TRPBF | 6242I | 16-Lead Plastic SSOP | –40°C to 85°C |
| LTC6242HVIGN#PBF | LTC6242HVIGN#TRPBF | 242HVI | 16-Lead Plastic SSOP | –40°C to 85°C |
| LTC6242HGN#PBF | LTC6242HGN#TRPBF | 6242H | 16-Lead Plastic SSOP | –40°C to 125°C |
| LTC6242HVHGN#PBF | LTC6242HVHGN#TRPBF | 242HVH | 16-Lead Plastic SSOP | –40°C to 125°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

## AVAILABLE OPTIONS

| PART NUMBER | AMPS/PACKAGE | SPECIFIED TEMP RANGE | SPECIFIED SUPPLY VOLTAGE | PACKAGE | PART MARKING |
|---|---|---|---|---|---|
| LTC6240CS5 | 1 | 0°C to 70°C | 3V, 5V | SOT-23 | LTCRR |
| LTC6240CS8 | 1 | 0°C to 70°C | 3V, 5V | SO-8 | 6240 |
| LTC6240HVCS5 | 1 | 0°C to 70°C | 3V, 5V, ±5V | SOT-23 | LTCRS |
| LTC6240HVCS8 | 1 | 0°C to 70°C | 3V, 5V, ±5V | SO-8 | 6240HV |
| LTC6240IS5 | 1 | –40°C to 85°C | 3V, 5V | SOT-23 | LTCRR |
| LTC6240IS8 | 1 | –40°C to 85°C | 3V, 5V | SO-8 | 6240I |
| LTC6240HVIS5 | 1 | –40°C to 85°C | 3V, 5V, ±5V | SOT-23 | LTCRS |
| LTC6240HVIS8 | 1 | –40°C to 85°C | 3V, 5V, ±5V | SO-8 | 240HVI |
| LTC6240HS5 | 1 | –40°C to 125°C | 3V, 5V | SOT-23 | LTCRR |
| LTC6240HS8 | 1 | –40°C to 125°C | 3V, 5V | SO-8 | 6240H |
| LTC6240HVHS5 | 1 | –40°C to 125°C | 3V, 5V, ±5V | SOT-23 | LTCRS |
| LTC6240HVHS8 | 1 | –40°C to 125°C | 3V, 5V, ±5V | SO-8 | 240HVH |
| LTC6241CS8 | 2 | 0°C to 70°C | 3V, 5V | SO-8 | 6241 |
| LTC6241CDD | 2 | 0°C to 70°C | 3V, 5V | DD | LBPD |
| LTC6241HVCS8 | 2 | 0°C to 70°C | 3V, 5V, ±5V | SO-8 | 6241HV |
| LTC6241HVCDD | 2 | 0°C to 70°C | 3V, 5V, ±5V | DD | LBRR |
| LTC6241IS8 | 2 | –40°C to 85°C | 3V, 5V | SO-8 | 6241I |
| LTC6241IDD | 2 | –40°C to 85°C | 3V, 5V | DD | LBPD |
| LTC6241HVIS8 | 2 | –40°C to 85°C | 3V, 5V, ±5V | SO-8 | 241HVI |
| LTC6241HVIDD | 2 | –40°C to 85°C | 3V, 5V, ±5V | DD | LBRR |
| LTC6241HS8 | 2 | –40°C to 125°C | 3V, 5V | SO-8 | 6241H |
| LTC6241HVHS8 | 2 | –40°C to 125°C | 3V, 5V, ±5V | SO-8 | 241HVH |
| LTC6242CGN | 4 | 0°C to 70°C | 3V, 5V | GN | 6242 |
| LTC6242CDHC | 4 | 0°C to 70°C | 3V, 5V | DHC | 6242 |
| LTC6242HVCGN | 4 | 0°C to 70°C | 3V, 5V, ±5V | GN | 6242HV |
| LTC6242HVCDHC | 4 | 0°C to 70°C | 3V, 5V, ±5V | DHC | 6242HV |
| LTC6242IGN | 4 | –40°C to 85°C | 3V, 5V | GN | 6242I |
| LTC6242IDHC | 4 | –40°C to 85°C | 3V, 5V | DHC | 6242 |
| LTC6242HVIGN | 4 | –40°C to 85°C | 3V, 5V, ±5V | GN | 242HVI |
| LTC6242HVIDHC | 4 | –40°C to 85°C | 3V, 5V, ±5V | DHC | 6242HV |
| LTC6242HGN | 4 | –40°C to 125°C | 3V, 5V | GN | 6242H |
| LTC6242HVHGN | 4 | –40°C to 125°C | 3V, 5V, ±5V | GN | 242HVH |

## ELECTRICAL CHARACTERISTICS

**(LTC6240C/I, LTC6240HVC/I, LTC6241C/I, LTC6241HVC/I, LTC6242C/I, LTC6242HVC/I) The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_S$ = 5V, 0V, $V_{CM}$ = 2.5V unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage (Note 4) | LTC6241 S8 | | | 40 | 125 | µV |
| | | 0°C to 70°C | ● | | | 250 | µV |
| | | –40°C to 85°C | ● | | | 300 | µV |
| | | LTC6242 GN | | | 50 | 150 | µV |
| | | 0°C to 70°C | ● | | | 275 | µV |
| | | –40°C to 85°C | ● | | | 300 | µV |
| | | LTC6240 | | | 50 | 175 | µV |
| | | 0°C to 70°C | ● | | | 300 | µV |
| | | –40°C to 85°C | ● | | | 350 | µV |
| | | LTC6241 DD, LTC6242 DHC | | | 100 | 550 | µV |
| | | 0°C to 70°C | ● | | | 650 | µV |
| | | –40°C to 85°C | ● | | | 725 | µV |
| | $V_{OS}$ Match Channel-to-Channel (Note 5) | LTC6241 S8 | | | 40 | 160 | µV |
| | | 0°C to 70°C | ● | | | 300 | µV |
| | | –40°C to 85°C | ● | | | 375 | µV |
| | | LTC6242 GN | | | 50 | 185 | µV |
| | | 0°C to 70°C | ● | | | 325 | µV |
| | | –40°C to 85°C | ● | | | 400 | µV |
| | | LTC6241 DD, LTC6242 DHC | | | 150 | 650 | µV |
| | | 0°C to 70°C | ● | | | 700 | µV |
| | | –40°C to 85°C | ● | | | 750 | µV |
| TC $V_{OS}$ | Input Offset Voltage Drift (Note 6) | | ● | | 0.7 | 2.5 | µV/°C |
| $I_B$ | Input Bias Current (Notes 4, 7) | LTC6241, LTC6242 | | | 0.2 | | pA |
| | | | ● | | | 75 | pA |
| | | LTC6240 | | | 0.2 | 1 | pA |
| | | | ● | | | 75 | pA |
| $I_{OS}$ | Input Offset Current (Notes 4, 7) | LTC6241, LTC6242 | | | 0.2 | | pA |
| | | | ● | | | 75 | pA |
| | | LTC6240 | | | 0.2 | 1 | pA |
| | | | ● | | | 75 | pA |
| | Input Noise Voltage | 0.1Hz to 10Hz | | | 550 | | $nV_{P-P}$ |
| $e_n$ | Input Noise Voltage Density | f = 1kHz | | | 7 | 10 | $nV/\sqrt{Hz}$ |
| $i_n$ | Input Noise Current Density (Note 8) | | | | 0.56 | | $fA/\sqrt{Hz}$ |
| $R_{IN}$ | Input Resistance | Common Mode | | | $10^{12}$ | | Ω |
| $C_{IN}$ | Input Capacitance | f = 100kHz | | | | | |
| | Differential Mode | | | | 3.5 | | pF |
| | Common Mode | | | | 3 | | pF |
| $V_{CM}$ | Input Voltage Range | Guaranteed by CMRR | ● | 0 | | 3.5 | V |
| CMRR | Common Mode Rejection | $0V \le V_{CM} \le 3.5V$ | ● | 80 | 105 | | dB |
| | CMRR Match Channel-to-Channel (Note 5) | | ● | 76 | 95 | | dB |

## ELECTRICAL CHARACTERISTICS

**(LTC6240C/I, LTC6240HVC/I, LTC6241C/I, LTC6241HVC/I, LTC6242C/I, LTC6242HVC/I) The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_S$ = 5V, 0V, $V_{CM}$ = 2.5V unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $A_{VOL}$ | Large Signal Voltage Gain | $V_O$ = 1V to 4V<br>$R_L$ = 10k to $V_S$/2<br>0°C to 70°C<br>–40°C to 85°C | <br><br>●<br>● | <br>425<br>300<br>200 | <br>1600 | | <br>V/mV<br>V/mV<br>V/mV |
| | | $V_O$ = 1.5V to 3.5V<br>$R_L$ = 1k to $V_S$/2<br>0°C to 70°C<br>–40°C to 85°C | <br><br>●<br>● | <br>90<br>60<br>50 | <br>215 | | <br>V/mV<br>V/mV<br>V/mV |
| $V_{OL}$ | Output Voltage Swing Low (Note 9) | No Load<br>$I_{SINK}$ = 1mA<br>$I_{SINK}$ = 5mA | ●<br>●<br>● | | 7<br>40<br>190 | 30<br>75<br>325 | mV<br>mV<br>mV |
| $V_{OH}$ | Output Voltage Swing High (Note 9) | No Load<br>$I_{SOURCE}$ = 1mA<br>$I_{SOURCE}$ = 5mA | ●<br>●<br>● | | 11<br>45<br>190 | 30<br>75<br>325 | mV<br>mV<br>mV |
| PSRR | Power Supply Rejection | $V_S$ = 2.8V to 6V, $V_{CM}$ = 0.2V | ● | 80 | 104 | | dB |
| | PSRR Match Channel-to-Channel (Note 5) | | ● | 74 | 100 | | dB |
| | Minimum Supply Voltage (Note 10) | | ● | 2.8 | | | V |
| $I_{SC}$ | Short-Circuit Current | | ● | 15 | 30 | | mA |
| $I_S$ | Supply Current per Amplifier | LTC6241, LTC6242<br>0°C to 70°C<br>–40°C to 85°C | <br>●<br>● | | 1.8 | 2.2<br>2.3<br>2.4 | mA<br>mA<br>mA |
| | | LTC6240<br>0°C to 70°C<br>–40°C to 85°C | <br>●<br>● | | 2 | 2.4<br>2.5<br>2.6 | mA<br>mA<br>mA |
| GBW | Gain Bandwidth Product | Frequency = 20kHz, $R_L$ = 1kΩ | ● | 13 | 18 | | MHz |
| SR | Slew Rate (Note 11) | $A_V$ = –2, $R_L$ = 1kΩ | ● | 5 | 10 | | V/µs |
| FPBW | Full Power Bandwidth (Note 12) | $V_{OUT}$ = $3V_{P-P}$, $R_L$ = 1kΩ | ● | 0.53 | 1.06 | | MHz |
| $t_s$ | Settling Time | $V_{STEP}$ = 2V, $A_V$ = –1, $R_L$ = 1kΩ, 0.1% | | | 1100 | | ns |

## ELECTRICAL CHARACTERISTICS

**(LTC6240C/I, LTC6240HVC/I, LTC6241C/I, LTC6241HVC/I, LTC6242C/I, LTC6242HVC/I) The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_S$ = 3V, 0V, $V_{CM}$ = 1.5V unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage (Note 4) | LTC6241 S8 | | | 40 | 175 | µV |
| | | 0°C to 70°C | ● | | | 275 | µV |
| | | –40°C to 85°C | ● | | | 325 | µV |
| | | LTC6242 GN | | | 60 | 200 | µV |
| | | 0°C to 70°C | ● | | | 275 | µV |
| | | –40°C to 85°C | ● | | | 325 | µV |
| | | LTC6240 | | | 50 | 200 | µV |
| | | 0°C to 70°C | ● | | | 325 | µV |
| | | –40°C to 85°C | ● | | | 375 | µV |
| | | LTC6241 DD, LTC6242 DHC | | | 100 | 550 | µV |
| | | 0°C to 70°C | ● | | | 650 | µV |
| | | –40°C to 85°C | ● | | | 725 | µV |
| | $V_{OS}$ Match Channel-to-Channel (Note 5) | LTC6241 S8 | | | 40 | 200 | µV |
| | | 0°C to 70°C | ● | | | 325 | µV |
| | | –40°C to 85°C | ● | | | 400 | µV |
| | | LTC6242 GN | | | 60 | 225 | µV |
| | | 0°C to 70°C | ● | | | 325 | µV |
| | | –40°C to 85°C | ● | | | 400 | µV |
| | | LTC6241 DD, LTC6242 DHC | | | 150 | 650 | µV |
| | | 0°C to 70°C | ● | | | 700 | µV |
| | | –40°C to 85°C | ● | | | 750 | µV |
| TC $V_{OS}$ | Input Offset Voltage Drift (Note 6) | | ● | | 0.7 | 2.5 | µV/°C |
| $I_B$ | Input Bias Current (Notes 4, 7) | LTC6241, LTC6242 | | | 0.2 | | pA |
| | | | ● | | | 75 | pA |
| | | LTC6240 | | | 0.2 | 1 | pA |
| | | | ● | | | 75 | pA |
| $I_{OS}$ | Input Offset Current (Notes 4, 7) | LTC6241, LTC6242 | | | 0.2 | | pA |
| | | | ● | | | 75 | pA |
| | | LTC6240 | | | 0.2 | 1 | pA |
| | | | ● | | | 75 | pA |
| $V_{CM}$ | Input Voltage Range | Guaranteed by CMRR | ● | 0 | | 1.5 | V |
| CMRR | Common Mode Rejection | 0V ≤ $V_{CM}$ ≤ 1.5V | ● | 78 | 100 | | dB |
| | CMRR Match Channel-to-Channel (Note 5) | | ● | 76 | 95 | | dB |
| $A_{VOL}$ | Large Signal Voltage Gain | $V_O$ = 1V to 2V | | | | | |
| | | $R_L$ = 10k to $V_S$/2 | | 140 | 600 | | V/mV |
| | | 0°C to 70°C | ● | 100 | | | V/mV |
| | | –40°C to 85°C | ● | 75 | | | V/mV |
| $V_{OL}$ | Output Voltage Swing Low (Note 9) | No Load | ● | | 3 | 30 | mV |
| | | $I_{SINK}$ = 1mA | ● | | 65 | 110 | mV |
| $V_{OH}$ | Output Voltage Swing High (Note 9) | No Load | ● | | 4 | 30 | mV |
| | | $I_{SOURCE}$ = 1mA | ● | | 70 | 120 | mV |
| PSRR | Power Supply Rejection | $V_S$ = 2.8V to 6V, $V_{CM}$ = 0.2V | ● | 80 | 104 | | dB |
| | PSRR Match Channel-to-Channel (Note 5) | | ● | 74 | 100 | | dB |
| | Minimum Supply Voltage (Note 10) | | ● | 2.8 | | | V |
| $I_{SC}$ | Short-Circuit Current | | ● | 3 | 6 | | mA |

## ELECTRICAL CHARACTERISTICS

**(LTC6240C/I, LTC6240HVC/I, LTC6241C/I, LTC6241HVC/I, LTC6242C/I, LTC6242HVC/I) The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_S$ = 3V, 0V, $V_{CM}$ = 1.5V unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $I_S$ | Supply Current per Amplifier | LTC6241, LTC6242 | | | 1.4 | 1.7 | mA |
| | | 0°C to 70°C | ● | | | 1.8 | mA |
| | | –40°C to 85°C | ● | | | 1.9 | mA |
| | | LTC6240 | | | 1.5 | 1.9 | mA |
| | | 0°C to 70°C | ● | | | 2 | mA |
| | | –40°C to 85°C | ● | | | 2.1 | mA |
| GBW | Gain Bandwidth Product | Frequency = 20kHz, $R_L$ = 1kΩ | ● | 12 | 17 | | MHz |

**(LTC6240HVC/I, LTC6241HVC/I, LTC6242HVC/I) The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_S$ = ±5V, 0V, $V_{CM}$ = 0V unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage (Note 4) | LTC6241 S8 | | | 50 | 175 | µV |
| | | 0°C to 70°C | ● | | | 275 | µV |
| | | –40°C to 85°C | ● | | | 325 | µV |
| | | LTC6242 GN | | | 60 | 200 | µV |
| | | 0°C to 70°C | ● | | | 275 | µV |
| | | –40°C to 85°C | ● | | | 325 | µV |
| | | LTC6240 | | | 60 | 250 | µV |
| | | 0°C to 70°C | ● | | | 350 | µV |
| | | –40°C to 85°C | ● | | | 400 | µV |
| | | LTC6241 DD, LTC6242 DHC | | | 100 | 550 | µV |
| | | 0°C to 70°C | ● | | | 650 | µV |
| | | –40°C to 85°C | ● | | | 725 | µV |
| | $V_{OS}$ Match Channel-to-Channel (Note 5) | LTC6241 S8 | | | 50 | 200 | µV |
| | | 0°C to 70°C | ● | | | 325 | µV |
| | | –40°C to 85°C | ● | | | 400 | µV |
| | | LTC6242 GN | | | 60 | 225 | µV |
| | | 0°C to 70°C | ● | | | 325 | µV |
| | | –40°C to 85°C | ● | | | 400 | µV |
| | | LTC6241 DD, LTC6242 DHC | | | 150 | 650 | µV |
| | | 0°C to 70°C | ● | | | 700 | µV |
| | | –40°C to 85°C | ● | | | 750 | µV |
| TC $V_{OS}$ | Input Offset Voltage Drift (Note 6) | | ● | | 0.7 | 2.5 | µV/°C |
| $I_B$ | Input Bias Current (Notes 4, 7) | LTC6241, LTC6242 | | | 0.5 | | pA |
| | | | ● | | | 75 | pA |
| | | LTC6240 | | | 0.5 | 1 | pA |
| | | | ● | | | 75 | pA |
| $I_{OS}$ | Input Offset Current (Notes 4, 7) | LTC6241, LTC6242 | | | 0.2 | | pA |
| | | | ● | | | 75 | pA |
| | | LTC6240 | | | 0.2 | 1 | pA |
| | | | ● | | | 75 | pA |
| | Input Noise Voltage | 0.1Hz to 10Hz | | | 550 | | $nV_{P-P}$ |

## ELECTRICAL CHARACTERISTICS

**(LTC6240HVC/I, LTC6241HVC/I, LTC6242HVC/I) The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_S$ = ±5V, 0V, $V_{CM}$ = 0V unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $e_n$ | Input Noise Voltage Density | f = 1kHz | | | 7 | 10 | nV/√Hz |
| $i_n$ | Input Noise Current Density (Note 8) | | | | 0.56 | | fA/√Hz |
| $R_{IN}$ | Input Resistance | Common Mode | | | $10^{12}$ | | Ω |
| $C_{IN}$ | Input Capacitance<br>Differential Mode<br>Common Mode | f = 100kHz | | | <br>3.5<br>3 | | <br>pF<br>pF |
| $V_{CM}$ | Input Voltage Range | Guaranteed by CMRR | ● | –5 | | 3.5 | V |
| CMRR | Common Mode Rejection | –5V ≤ $V_{CM}$ ≤ 3.5V | ● | 83 | 105 | | dB |
| | CMRR Match<br>Channel-to-Channel (Note 5) | | ● | 76 | 95 | | dB |
| $A_{VOL}$ | Large Signal Voltage Gain | $V_O$ = –3.5V to 3.5V<br>$R_L$ = 10k<br>0°C to 70°C<br>–40°C to 85°C | <br><br>●<br>● | <br>775<br>600<br>500 | <br>2700<br><br> | <br><br><br> | <br>V/mV<br>V/mV<br>V/mV |
| | | $R_L$ = 1k<br>0°C to 70°C<br>–40°C to 85°C | <br>●<br>● | 150<br>90<br>75 | 360<br><br> | <br><br> | V/mV<br>V/mV<br>V/mV |
| $V_{OL}$ | Output Voltage Swing Low (Note 9) | No Load<br>$I_{SINK}$ = 1mA<br>$I_{SINK}$ = 10mA | ●<br>●<br>● | | 15<br>45<br>360 | 30<br>75<br>550 | mV<br>mV<br>mV |
| $V_{OH}$ | Output Voltage Swing High (Note 9) | No Load<br>$I_{SOURCE}$ = 1mA<br>$I_{SOURCE}$ = 10mA | ●<br>●<br>● | | 15<br>45<br>360 | 30<br>75<br>550 | mV<br>mV<br>mV |
| PSRR | Power Supply Rejection | $V_S$ = 2.8V to 11V, $V_{CM}$ = 0.2V | ● | 85 | 110 | | dB |
| | PSRR Match<br>Channel-to-Channel (Note 5) | | ● | 82 | 106 | | dB |
| | Minimum Supply Voltage (Note 10) | | ● | 2.8 | | | V |
| $I_{SC}$ | Short-Circuit Current | | ● | 15 | 35 | | mA |
| $I_S$ | Supply Current per Amplifier | LTC6241, LTC6242<br>0°C to 70°C<br>–40°C to 85°C | <br>●<br>● | | 2.5<br><br> | 3.2<br>3.3<br>3.7 | mA<br>mA<br>mA |
| | | LTC6240<br>0°C to 70°C<br>–40°C to 85°C | <br>●<br>● | | 2.7<br><br> | 3.3<br>3.4<br>3.8 | mA<br>mA<br>mA |
| GBW | Gain Bandwidth Product | Frequency = 20kHz, $R_L$ = 1kΩ | ● | 13 | 18 | | MHz |
| SR | Slew Rate (Note 11) | $A_V$ = –2, $R_L$ = 1kΩ | ● | 5.5 | 10 | | V/µs |
| FPBW | Full Power Bandwidth (Note 12) | $V_{OUT}$ = $3V_{P-P}$, $R_L$ = 1kΩ | ● | 0.58 | 1.06 | | MHz |
| $t_s$ | Settling Time | $V_{STEP}$ = 2V, $A_V$ = –1, $R_L$ = 1kΩ, 0.1% | | | 900 | | ns |

## ELECTRICAL CHARACTERISTICS

**(LTC6240H/LTC6240HVH, LTC6241H/LTC6241HVH, LTC6242H/LTC6242HVH)**

**The ● denotes the specifications which apply from –40°C to 125°C, otherwise specifications are at $T_A$ = 25°C. $V_S$ = 5V, 0V, $V_{CM}$ = 2.5V unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage (Note 4) | LTC6241 S8 | <br>● | | 40 | 125<br>400 | µV<br>µV |
| | | LTC6242 GN | <br>● | | 50 | 150<br>400 | µV<br>µV |
| | | LTC6240 | <br>● | | 50 | 175<br>450 | µV<br>µV |
| | $V_{OS}$ Match Channel-to-Channel (Note 5) | LTC6241 S8 | <br>● | | 40 | 160<br>400 | µV<br>µV |
| | | LTC6242 GN | <br>● | | 50 | 185<br>400 | µV<br>µV |
| TC $V_{OS}$ | Input Offset Voltage Drift (Note 6) | | ● | | 0.7 | 2.5 | µV/°C |
| $I_B$ | Input Bias Current (Notes 4, 7) | LTC6241, LTC6242 | <br>● | | 0.2 | <br>1.5 | pA<br>nA |
| | | LTC6240 | <br>● | | 0.2 | 1<br>2.5 | pA<br>nA |
| $I_{OS}$ | Input Offset Current (Notes 4, 7) | LTC6241, LTC6242 | <br>● | | 0.2 | <br>150 | pA<br>pA |
| | | LTC6240 | <br>● | | 0.2 | 1<br>750 | pA<br>pA |
| $V_{CM}$ | Input Voltage Range | Guaranteed by CMRR | ● | 0 | | 3.5 | V |
| CMRR | Common Mode Rejection | 0V ≤ $V_{CM}$ ≤ 3.5V | ● | 78 | | | dB |
| | CMRR Match Channel-to-Channel (Note 5) | | ● | 74 | | | dB |
| $A_{VOL}$ | Large Signal Voltage Gain | $V_O$ = 1V to 4V<br>$R_L$ = 10k to $V_S$/2 | <br>● | 425<br>200 | 1600 | | V/mV<br>V/mV |
| | | $V_O$ = 1.5V to 3.5V<br>$R_L$ = 1k to $V_S$/2 | <br>● | 90<br>40 | 215 | | V/mV<br>V/mV |
| $V_{OL}$ | Output Voltage Swing Low (Note 9) | No Load<br>$I_{SINK}$ = 1mA<br>$I_{SINK}$ = 5mA | ●<br>●<br>● | | | 30<br>85<br>325 | mV<br>mV<br>mV |
| $V_{OH}$ | Output Voltage Swing High (Note 9) | No Load<br>$I_{SOURCE}$ = 1mA<br>$I_{SOURCE}$ = 5mA | ●<br>●<br>● | | | 30<br>85<br>325 | mV<br>mV<br>mV |
| PSRR | Power Supply Rejection | $V_S$ = 2.8V to 6V, $V_{CM}$ = 0.2V | ● | 78 | | | dB |
| | PSRR Match Channel-to-Channel (Note 5) | | ● | 74 | | | dB |
| | Minimum Supply Voltage (Note 10) | | ● | 2.8 | | | V |
| $I_{SC}$ | Short-Circuit Current | | ● | 15 | | | mA |
| $I_S$ | Supply Current per Amplifier | LTC6241, LTC6242 | <br>● | | 1.8 | 2.2<br>2.4 | mA<br>mA |
| | | LTC6240 | <br>● | | 2 | 2.4<br>2.8 | mA<br>mA |
| GBW | Gain Bandwidth Product | Frequency = 20kHz, $R_L$ = 1kΩ | ● | 12 | | | MHz |
| SR | Slew Rate (Note 11) | $A_V$ = –2, $R_L$ = 1kΩ | ● | 4.5 | | | V/µs |
| FPBW | Full Power Bandwidth (Note 12) | $V_{OUT}$ = $3V_{P-P}$, $R_L$ = 1kΩ | ● | 0.48 | | | MHz |

## ELECTRICAL CHARACTERISTICS

**(LTC6240H/LTC6240HVH, LTC6241H/LTC6241HVH, LTC6242H/LTC6242HVH)**

**The ● denotes the specifications which apply from –40°C to 125°C, otherwise specifications are at $T_A$ = 25°C. $V_S$ = 3V, 0V, $V_{CM}$ = 1.5V unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage (Note 4) | LTC6241 S8 | <br>● | | 40 | 175<br>400 | µV<br>µV |
| | | LTC6242 GN | <br>● | | 60 | 200<br>400 | µV<br>µV |
| | | LTC6240 | <br>● | | 50 | 200<br>450 | µV<br>µV |
| | $V_{OS}$ Match Channel-to-Channel (Note 5) | LTC6241 S8 | <br>● | | 40 | 200<br>400 | µV<br>µV |
| | | LTC6242 GN | <br>● | | 60 | 225<br>400 | µV<br>µV |
| TC $V_{OS}$ | Input Offset Voltage Drift (Note 6) | | ● | | 0.7 | 2.5 | µV/°C |
| $I_B$ | Input Bias Current (Notes 4, 7) | LTC6241, LTC6242 | <br>● | | 0.2 | <br>1.5 | pA<br>nA |
| | | LTC6240 | <br>● | | 0.2 | 1<br>2.5 | pA<br>nA |
| $I_{OS}$ | Input Offset Current (Notes 4, 7) | LTC6241, LTC6242 | <br>● | | 0.2 | <br>150 | pA<br>pA |
| | | LTC6240 | <br>● | | 0.2 | 1<br>750 | pA<br>pA |
| $V_{CM}$ | Input Voltage Range | Guaranteed by CMRR | ● | 0 | | 1.5 | V |
| CMRR | Common Mode Rejection | 0V ≤ $V_{CM}$ ≤ 1.5V | ● | 75 | | | dB |
| | CMRR Match Channel-to-Channel (Note 5) | | ● | 74 | | | dB |
| $A_{VOL}$ | Large Signal Voltage Gain | $V_O$ = 1V to 2V<br>$R_L$ = 10k to $V_S$/2 | <br>● | 140<br>65 | 600 | | V/mV<br>V/mV |
| $V_{OL}$ | Output Voltage Swing Low (Note 9) | No Load<br>$I_{SINK}$ = 1mA | ●<br>● | | | 30<br>130 | mV<br>mV |
| $V_{OH}$ | Output Voltage Swing High (Note 9) | No Load<br>$I_{SOURCE}$ = 1mA | ●<br>● | | | 30<br>130 | mV<br>mV |
| PSRR | Power Supply Rejection | $V_S$ = 2.8V to 6V, $V_{CM}$ = 0.2V | ● | 78 | | | dB |
| | PSRR Match Channel-to-Channel (Note 5) | | ● | 74 | | | dB |
| | Minimum Supply Voltage (Note 10) | | ● | 2.8 | | | V |
| $I_{SC}$ | Short-Circuit Current | | ● | 2.5 | | | mA |
| $I_S$ | Supply Current per Amplifier | LTC6241, LTC6242 | <br>● | | 1.4 | 1.7<br>1.9 | mA<br>mA |
| | | LTC6240 | <br>● | | 1.5 | 1.9<br>2.1 | mA<br>mA |
| GBW | Gain Bandwidth Product | Frequency = 20kHz, $R_L$ = 1kΩ | ● | 10 | | | MHz |

## ELECTRICAL CHARACTERISTICS

**(LTC6240HVH/LTC6241HVH/LTC6242HVH) The ● denotes the specifications which apply from –40°C to 125°C, otherwise specifications are at $T_A$ = 25°C. $V_S$ = ±5V, $V_{CM}$ = 0V unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage (Note 4) | LTC6241 S8 | <br>● | | 50 | 175<br>400 | µV<br>µV |
| | | LTC6242 GN | <br>● | | 60 | 200<br>400 | µV<br>µV |
| | | LTC6240 | <br>● | | 60 | 250<br>450 | µV<br>µV |
| | $V_{OS}$ Match Channel-to-Channel (Note 5) | LTC6241 S8 | <br>● | | 50 | 200<br>400 | µV<br>µV |
| | | LTC6242 GN | <br>● | | 60 | 225<br>400 | µV<br>µV |
| TC $V_{OS}$ | Input Offset Voltage Drift (Note 6) | | ● | | 0.7 | 2.5 | µV/°C |
| $I_B$ | Input Bias Current (Notes 4, 7) | LTC6241, LTC6242 | <br>● | | 0.5 | <br>1.5 | pA<br>nA |
| | | LTC6240 | <br>● | | 0.5 | 1<br>2.5 | pA<br>nA |
| $I_{OS}$ | Input Offset Current (Notes 4, 7) | LTC6241, LTC6242 | <br>● | | 0.2 | <br>150 | pA<br>pA |
| | | LTC6240 | <br>● | | 0.2 | 1<br>750 | pA<br>pA |
| $V_{CM}$ | Input Voltage Range | Guaranteed by CMRR | ● | –5 | | 3.5 | V |
| CMRR | Common Mode Rejection | –5V ≤ $V_{CM}$ ≤ 3.5V | ● | 80 | | | dB |
| | CMRR Match Channel-to-Channel (Note 5) | | ● | 76 | | | dB |
| $A_{VOL}$ | Large Signal Voltage Gain | $V_O$ = –3.5V to 3.5V<br>$R_L$ = 10k | <br>● | 775<br>350 | 2700 | | V/mV<br>V/mV |
| | | $R_L$ = 1k | <br>● | 150<br>60 | 360 | | V/mV<br>V/mV |
| $V_{OL}$ | Output Voltage Swing Low (Note 9) | No Load<br>$I_{SINK}$ = 1mA<br>$I_{SINK}$ = 10mA | ●<br>●<br>● | | | 30<br>85<br>600 | mV<br>mV<br>mV |
| $V_{OH}$ | Output Voltage Swing High (Note 9) | No Load<br>$I_{SOURCE}$ = 1mA<br>$I_{SOURCE}$ = 10mA | ●<br>●<br>● | | | 30<br>85<br>600 | mV<br>mV<br>mV |
| PSRR | Power Supply Rejection | $V_S$ = 2.8V to 11V, $V_{CM}$ = 0.2V | ● | 83 | | | dB |
| | PSRR Match Channel-to-Channel (Note 5) | | ● | 82 | | | dB |
| | Minimum Supply Voltage (Note 10) | | ● | 2.8 | | | V |
| $I_{SC}$ | Short-Circuit Current | | ● | 15 | | | mA |
| $I_S$ | Supply Current per Amplifier | LTC6241, LTC6242 | <br>● | | 2.5 | 3.2<br>3.7 | mA<br>mA |
| | | LTC6240 | <br>● | | 2.7 | 3.3<br>3.8 | mA<br>mA |
| GBW | Gain Bandwidth Product | Frequency = 20kHz, $R_L$ = 1kΩ | ● | 12 | | | MHz |
| SR | Slew Rate (Note 11) | $A_V$ = –2, $R_L$ = 1kΩ | ● | 5 | | | V/µs |
| FPBW | Full Power Bandwidth (Note 12) | $V_{OUT}$ = $3V_{P-P}$, $R_L$ = 1kΩ | ● | 0.53 | | | MHz |

## ELECTRICAL CHARACTERISTICS

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

**Note 3:** The LTC6240C/LTC6240HVC/LTC6241C/LTC6241HVC, LTC6242C/LTC6242HVC are guaranteed to meet specified performance from 0°C to 70°C. They are designed, characterized and expected to meet specified performance from –40°C to 85°C, but are not tested or QA sampled at these temperatures. The LTC6240I/LTC6240HVI, LTC6241I/LTC6241HVI, LTC6242I/LTC6242HVI are guaranteed to meet specified performance from –40°C to 85°C. All versions of the LTC6240H/LTC6241H/LTC6242H are guaranteed to meet specified performance from –40°C to 125°C.

**Note 4:** ESD (Electrostatic Discharge) sensitive device. ESD protection devices are used extensively internal to the LTC6240/LTC6241/LTC6242; however, high electrostatic discharge can damage or degrade the device. Use proper ESD handling precautions.

**Note 5:** Matching parameters are the difference between the two amplifiers A and D and between B and C of the LTC6242; between the two amplifiers of the LTC6241. CMRR and PSRR match are defined as follows: CMRR and PSRR are measured in µV/V on the matched amplifiers. The difference is calculated between the matching sides in µV/V. The result is converted to dB.

**Note 6:** This parameter is not 100% tested.

**Note 7:** Bias current at $T_A$ = 25°C is 100% tested and guaranteed for the LTC6240 in the S8 package. The LTC6240S5, LTC6241 and LTC6242 are expected to achieve the same performance as the LTC6240S8. All parts are guaranteed to meet specifications over temperature.

**Note 8:** Current noise is calculated from the formula: $i_n = (2qI_B)^{1/2}$ where $q = 1.6 \times 10^{-19}$ coulomb. The noise of source resistors up to 50GΩ dominates the contribution of current noise. See also Typical Performance Characteristics curve Noise Current vs Frequency.

**Note 9:** Output voltage swings are measured between the output and power supply rails.

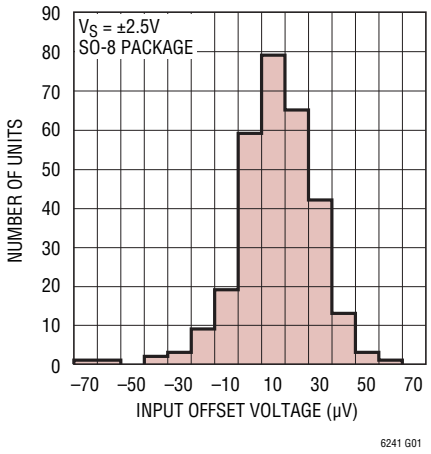
**Note 10:** Minimum supply voltage is guaranteed by the power supply rejection ratio test.

**Note 11:** Slew rate is measured in a gain of –2 with $R_F$ = 1k and $R_G$ = 500Ω. On the LTC6240/LTC6241/LTC6242, $V_S$ = ±2.5V, $V_{IN}$ is ±1V and $V_{OUT}$ slew rate is measured between –1V and +1V. On the LTC6240HV/LTC6241HV/LTC6242HV, $V_{IN}$ is ±2V and $V_{OUT}$ slew rate is measured between –2V and +2V.

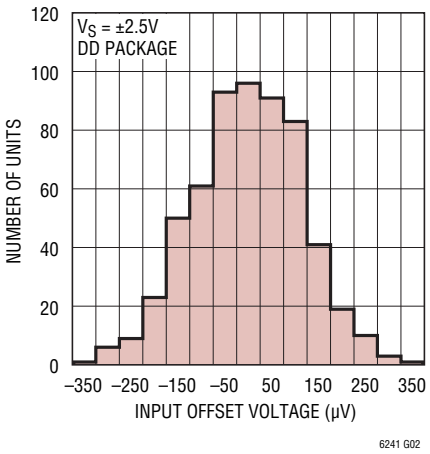
**Note 12:** Full-power bandwidth is calculated from the slew rate:
$FPBW = SR/\pi V_{P-P}$.

## TYPICAL PERFORMANCE CHARACTERISTICS

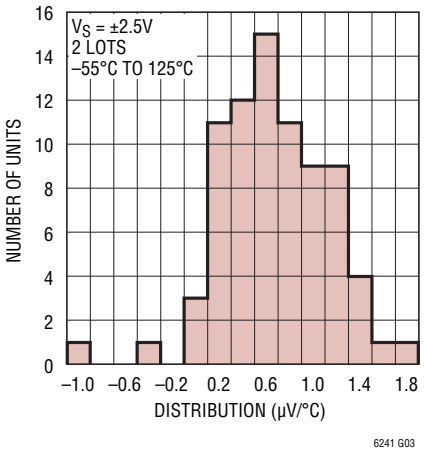
**$V_{OS}$ Distribution LTC6241**



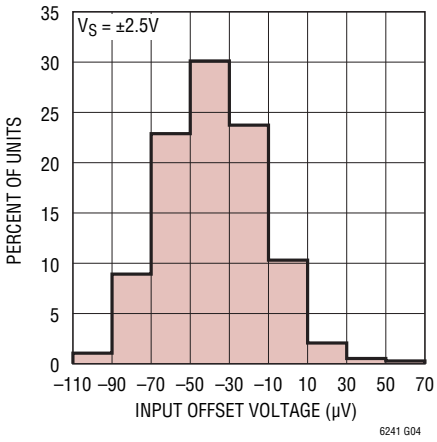

**$V_{OS}$ Distribution LTC6241**



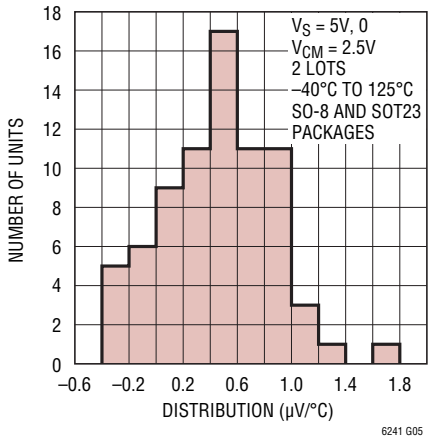

**$V_{OS}$ Temperature Coefficient Distribution LTC6241**



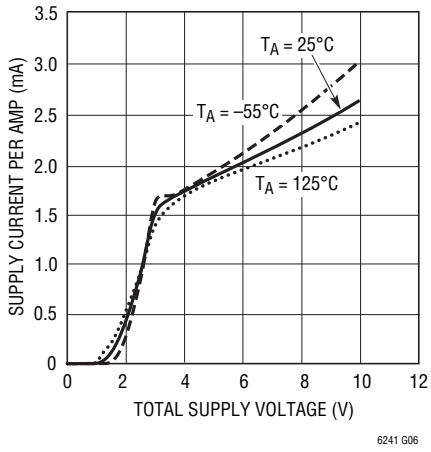

**$V_{OS}$ Distribution LTC6240**



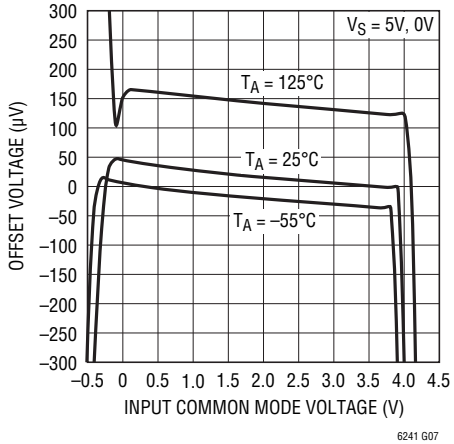

**$V_{OS}$ Temperature Coefficient Distribution LTC6240**



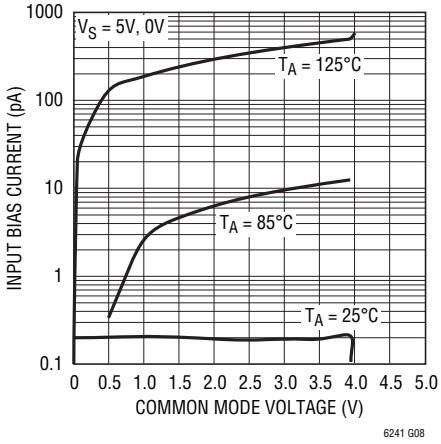

**Supply Current vs Supply Voltage**



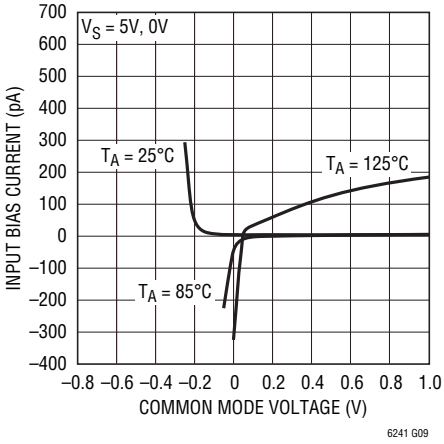

**Offset Voltage vs Input Common Mode Voltage**




**Input Bias Current vs Common Mode Voltage**

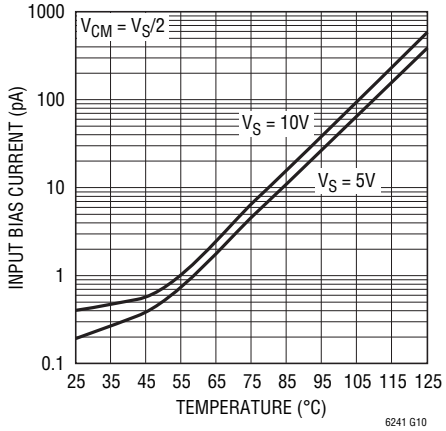



**Input Bias Current vs Common Mode Voltage**

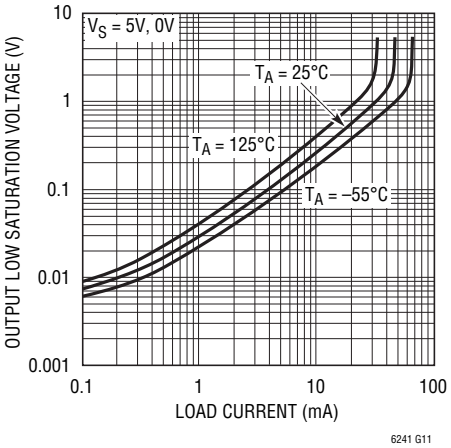


# TYPICAL PERFORMANCE CHARACTERISTICS

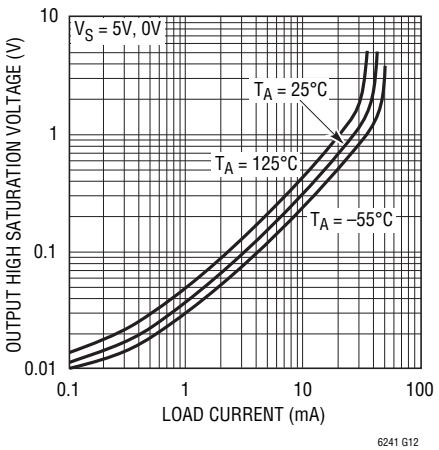
### Input Bias Current vs Temperature



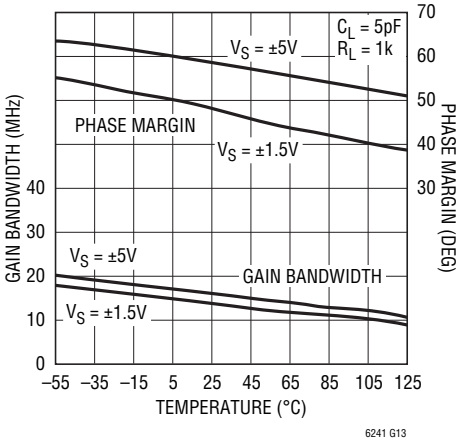

### Output Saturation Voltage vs Load Current (Output Low)



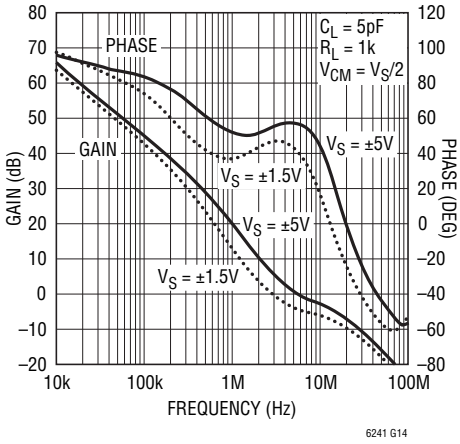

### Output Saturation Voltage vs Load Current (Output High)



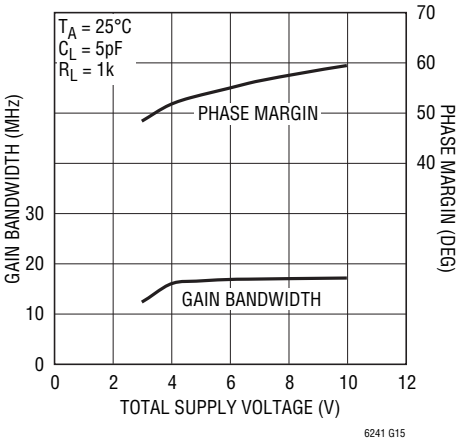

### Gain Bandwidth and Phase Margin vs Temperature



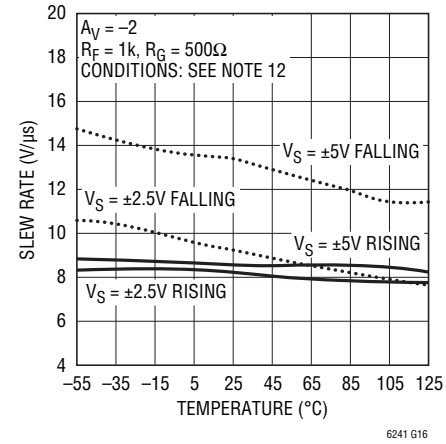

### Open Loop Gain vs Frequency



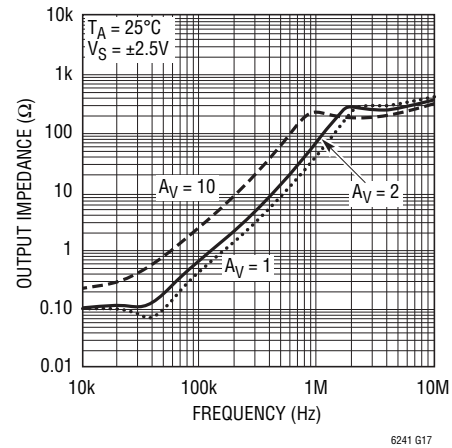

### Gain Bandwidth and Phase Margin vs Supply Voltage



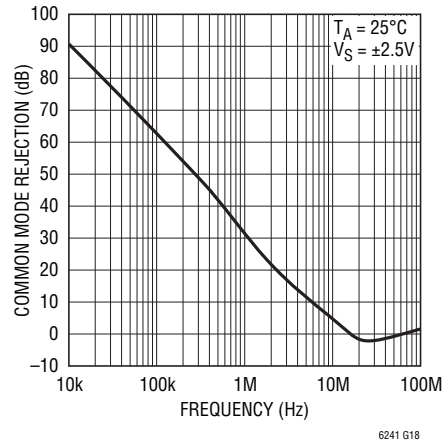

### Slew Rate vs Temperature




### Output Impedance vs Frequency

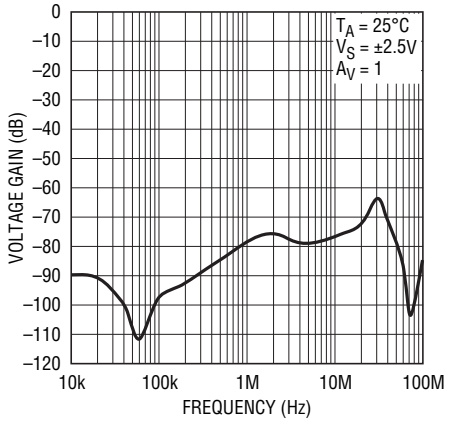



### Common Mode Rejection Ratio vs Frequency



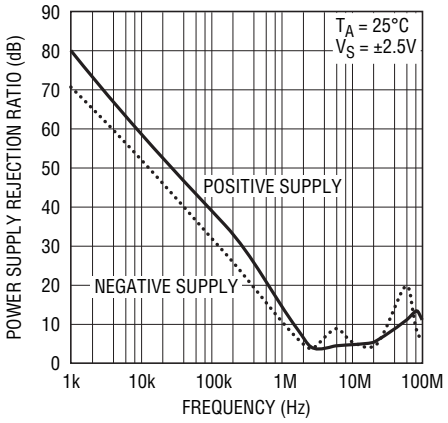
## TYPICAL PERFORMANCE CHARACTERISTICS

### Channel Separation vs Frequency



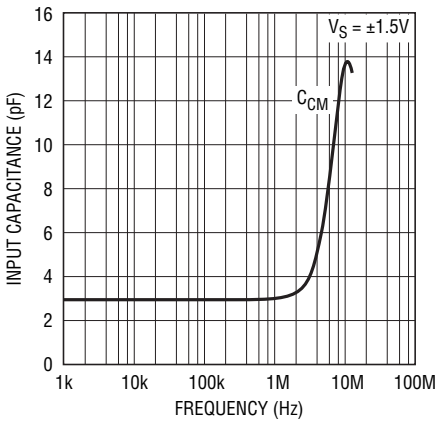

6241 G19

### Power Supply Rejection Ratio vs Frequency



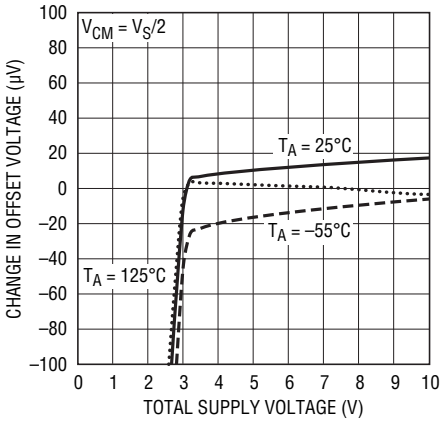

6241 G20

### Input Capacitance vs Frequency



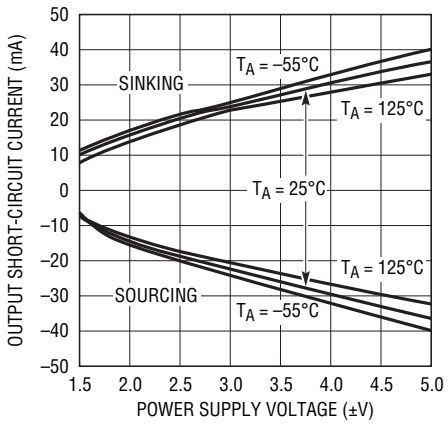

6241 G21

### Minimum Supply Voltage



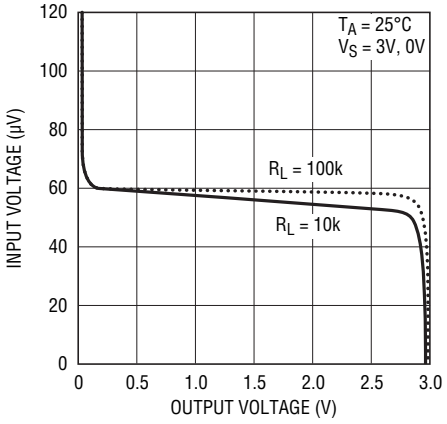

6241 G22

### Output Short-Circuit Current vs Power Supply Voltage



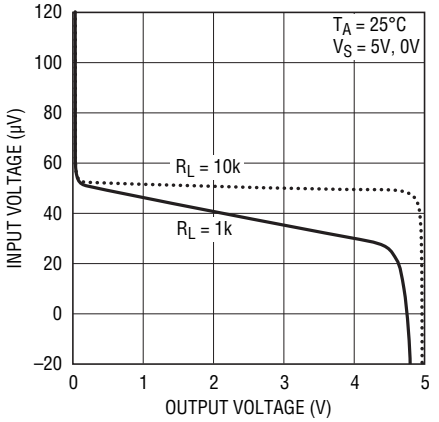

6241 G23

### Open Loop Gain



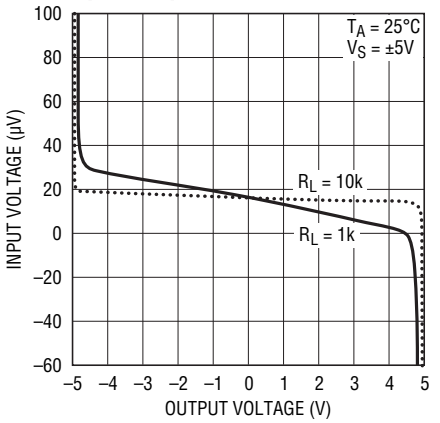

6241 G24

### Open Loop Gain



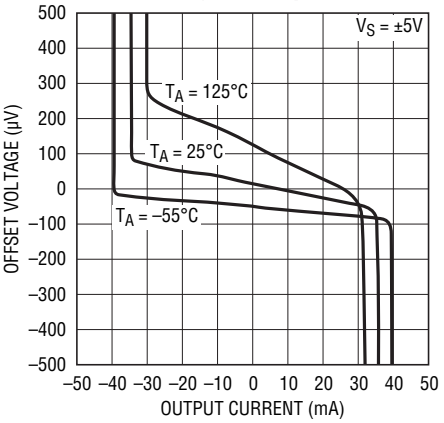

6241 G25

### Open Loop Gain




6241 G26

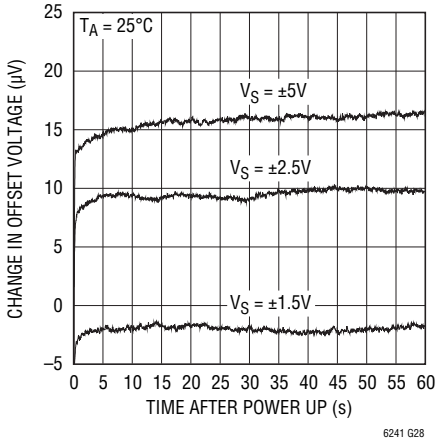
### Offset Voltage vs Output Current



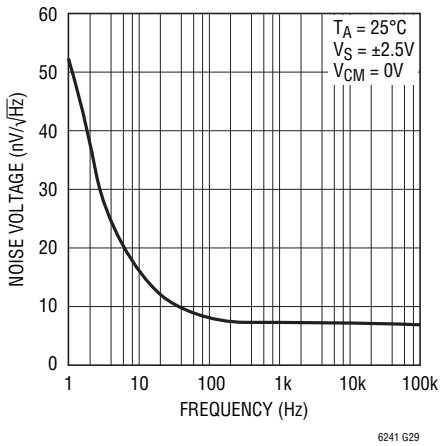

6241 G27

## TYPICAL PERFORMANCE CHARACTERISTICS

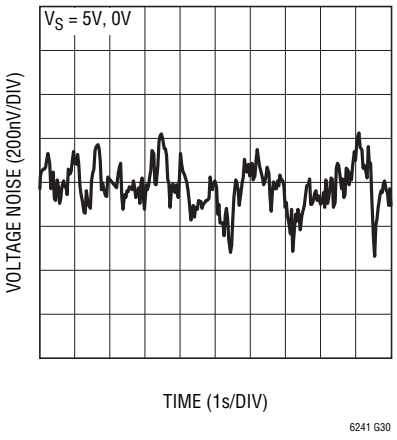
### Warm-Up Drift vs Time



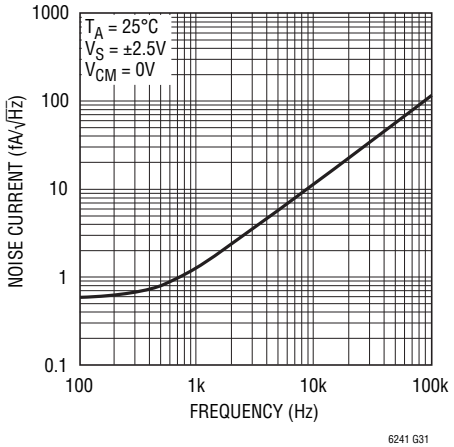

### Noise Voltage vs Frequency



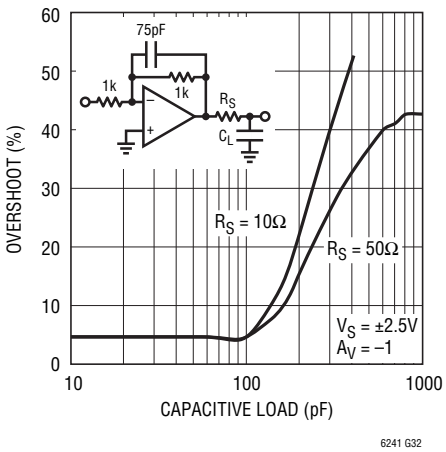

### 0.1Hz to 10Hz Voltage Noise



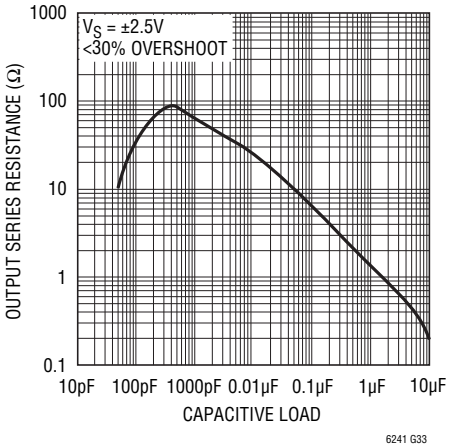

### Noise Current vs Frequency



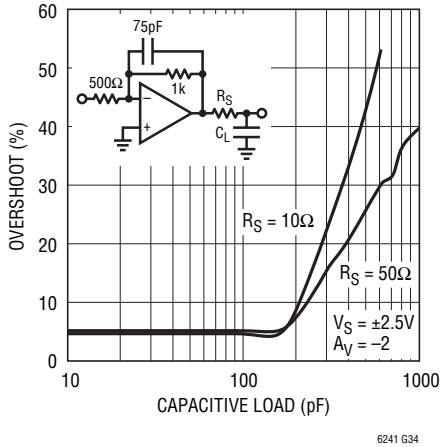

### Series Output Resistance and Overshoot vs Capacitive Load



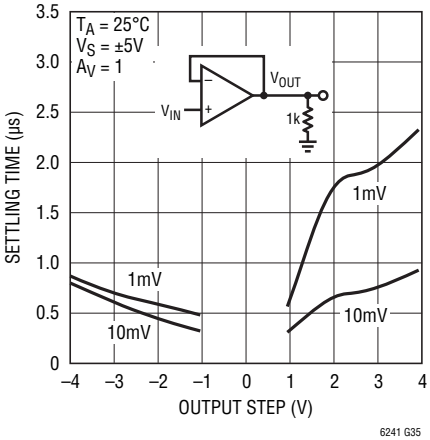

### Minimum Output Series Resistance vs Capacitive Load



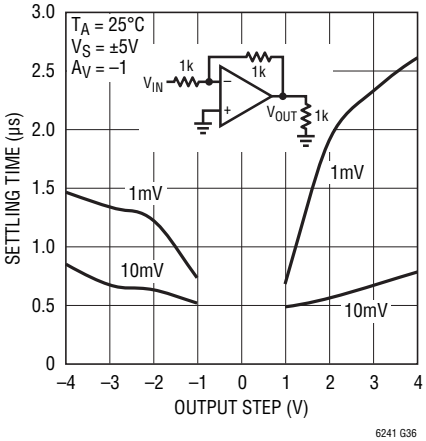

### Series Output Resistance and Overshoot vs Capacitive Load




### Settling Time vs Output Step (Non-Inverting)

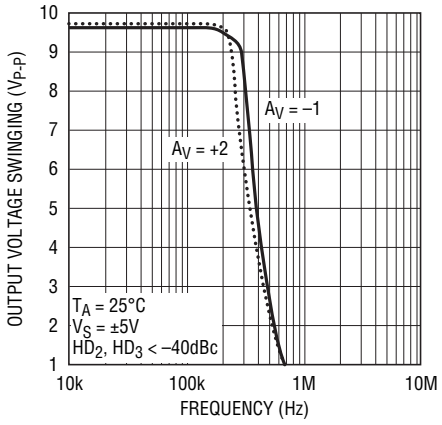



### Settling Time vs Output Step (Inverting)

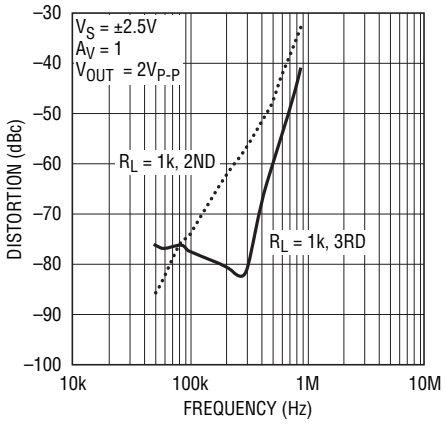


## TYPICAL PERFORMANCE CHARACTERISTICS

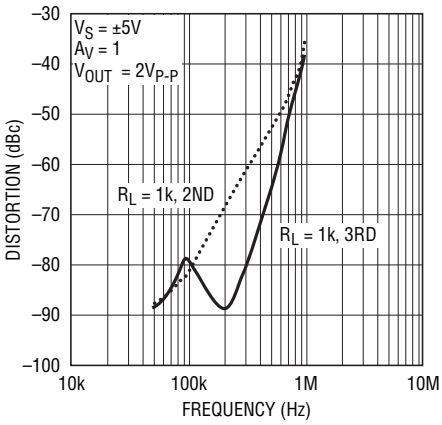
### Maximum Undistorted Output Signal vs Frequency



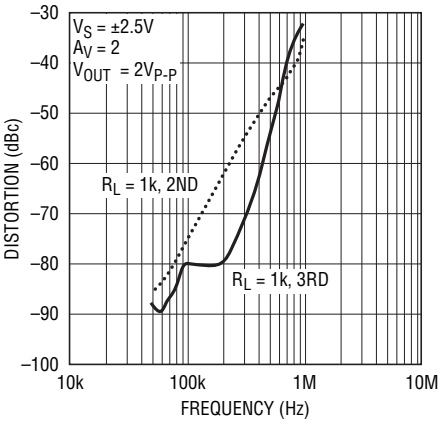

### Distortion vs Frequency



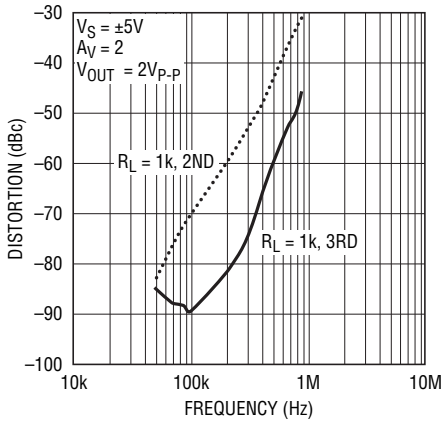

### Distortion vs Frequency



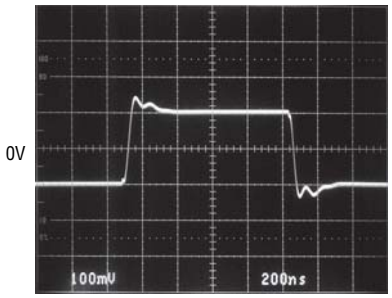

### Distortion vs Frequency




### Distortion vs Frequency

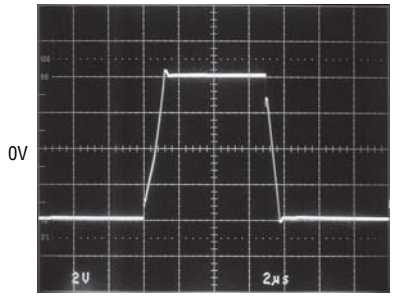



### Small Signal Response



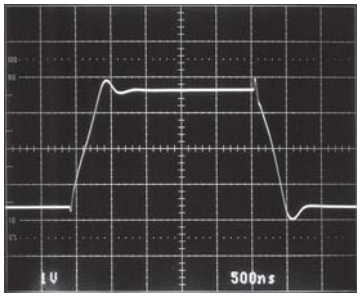

VS = ±2.5V
AV = 1
RL = ∞

### Large Signal Response



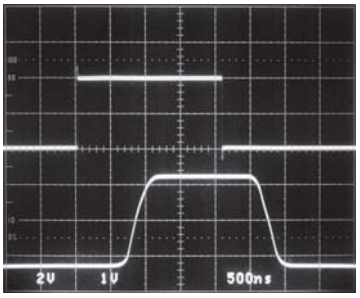

VS = ±5V
AV = 1
RL = ∞

### Large Signal Response




VS = ±2.5V
AV = –1
RL = 1k

### Output Overdrive Recovery




VS = ±2.5V
AV = 3
RL = ∞
500ns/DIV

## APPLICATIONS INFORMATION

### Amplifier Characteristics

Figure 1 is a simplified schematic of the amplifier, which has a pair of low noise input transistors M1 and M2. A simple folded cascode Q1, Q2 and R1, R2 allow the input stage to swing to the negative rail, while performing level shift to the differential drive generator. Low offset voltage is accomplished by laser trimming the input stage.

Capacitor C1 reduces the unity cross frequency and improves the frequency stability without degrading the gain bandwidth of the amplifier. Capacitor CM sets the overall amplifier gain bandwidth. The differential drive generator supplies signals to transistors M3 and M4 that swing the output from rail-to-rail.

The photo of Figure 2 shows the output response to an input overdrive with the amplifier connected as a voltage follower. If the negative going input signal is less than a diode drop below $V^–$, no phase inversion occurs. For input signals greater than a diode drop below $V^–$, limit the current to 3mA with a series resistor $R_S$ to avoid phase inversion.

### ESD

The LTC6240/LTC6241/LTC6242 have reverse-biased ESD protection diodes on all input and outputs as shown in Figure 1. If these pins are forced beyond either supply, unlimited current will flow through these diodes. If the current is transient and limited to one hundred milliamps or less, no damage to the device will occur.

The amplifier input bias current is the leakage current of these ESD diodes. This leakage is a function of the temperature and common mode voltage of the amplifier, as shown in the Typical Performance Characteristics curves.

### Noise

The LTC6240/LTC6241/LTC6242 exhibit exceptionally low 1/f noise in the 0.1Hz to 10Hz region. This 550nV$_{P-P}$ noise allows these op amps to be used in a wide variety of high impedance low frequency applications, where zero-drift amplifiers might be inappropriate due to their charge injection.

In the frequency region above 1kHz the LTC6240/LTC6241/LTC6242 also show good noise voltage performance. In this frequency region, noise can easily be dominated by the total source resistance of the particular application. Specifically, these amplifiers exhibit the noise of a 3.1kΩ resistor, meaning it is desirable to keep the source and feedback resistance at or below this value, i.e. $R_S + R_G||R_{FB} \leq 3.1k\Omega$. Above this total source impedance, the noise voltage is not dominated by the amplifier.

Noise current can be estimated from the expression $i_n = \sqrt{2qI_B}$, where $q = 1.6 \bullet 10^{-19}$ coulombs. Equating $\sqrt{4kTR\Delta f}$ and $R\sqrt{2qI_B\Delta f}$ shows that for source resistors below 50GΩ the amplifier noise is dominated by the source resistance. See the Typical Performance Characteristics curve Noise Current vs Frequency.

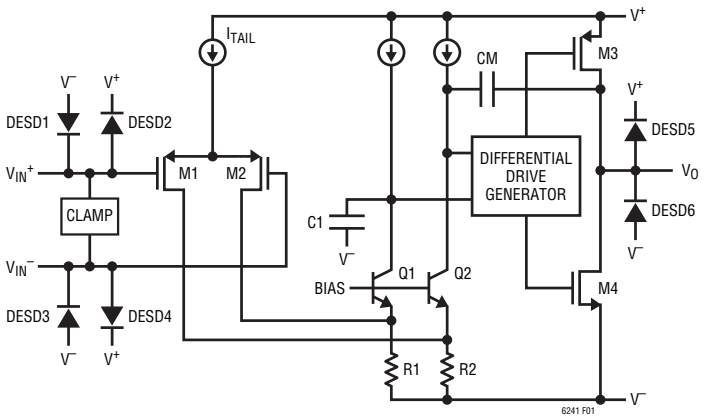
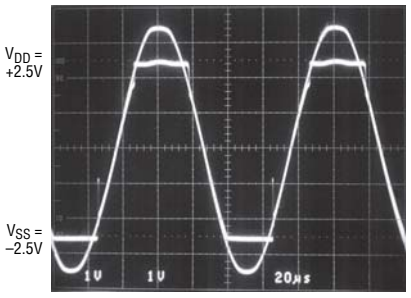



**Figure 1. Simplified Schematic**




VOUT AND VIN OF FOLLOWER WITH LARGE INPUT OVERDRIVE

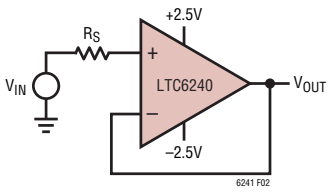



**Figure 2. Unity Gain Follower Test Circuit**

## APPLICATIONS INFORMATION

Proprietary design techniques are used to obtain simultaneous low 1/f noise and low input capacitance. Low input capacitance is important when the amplifier is used with high value source and feedback resistors. High frequency noise from the amplifier tail current source, $I_{TAIL}$ in Figure 1, couples through the input capacitance and appears across these large source and feedback resistors. As an example, the photodiode amplifier of Figure 15 on the last page of this data sheet shows the noise results from the LTC6241 and the results of a competitive CMOS amplifier. The LTC6241 output is the ideal noise of a 1MΩ resistor at room temperature, 130nV$\sqrt{Hz}$.

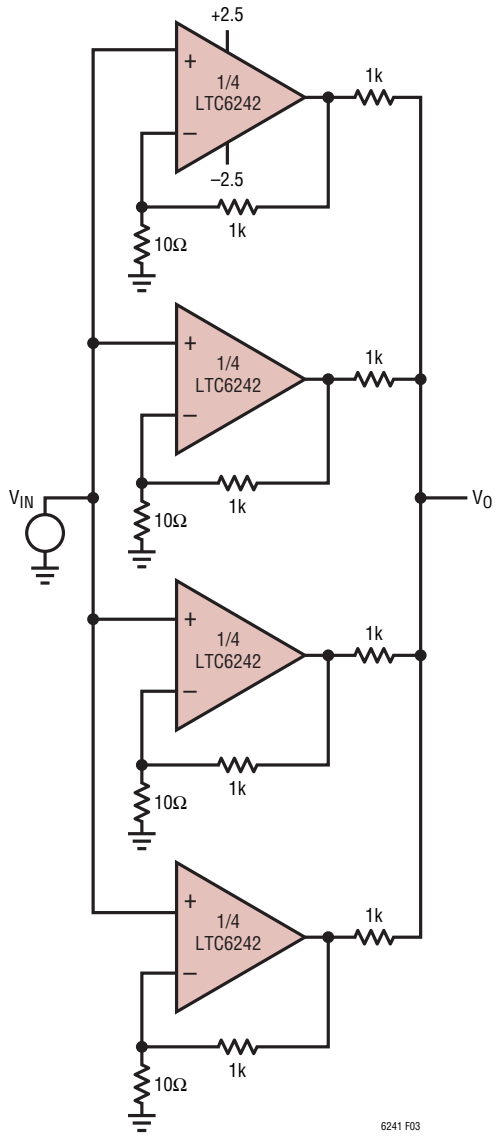



Figure 3. Parallel Amplifier Lowers Noise by 2x

### Half the Noise

The circuit shown in Figure 3 can be used to achieve even lower noise voltage. By paralleling 4 amplifiers the noise voltage can be lowered by $\sqrt{4}$, or half as much noise. The $\sqrt{}$ comes about from an RMS summing of uncorrelated noise sources. This circuit maintains extremely high input resistance, and has a 250Ω output resistance. For lower output resistance, a buffer amplifier can be added without influencing the noise.

### Stability

The good noise performance of these op amps can be attributed to large input devices in the differential pair. Above several hundred kilohertz, the input capacitance rises and can cause amplifier stability problems if left unchecked. When the feedback around the op amp is resistive ($R_F$), a pole will be created with $R_F$, the source resistance, source capacitance ($R_S$, $C_S$), and the amplifier input capacitance. In low gain configurations and with $R_F$ and $R_S$ in even the kilohm range (Figure 4), this pole can create excess phase shift and possibly oscillation. A small capacitor $C_F$ in parallel with $R_F$ eliminates this problem.

### Low Noise Single-Ended Input to Differential Output Amplifier

The circuit on the first page of the data sheet is a low noise single-ended input to differential output amplifier, with a 200k input impedance. The very low input bias current of the LTC6241 allows for these large input and feedback resistors. The 200k resistors, R1 and R2, along with C1 and C2 set the –3dB bandwidth to 80kHz. Capacitor C3 is used to cancel effects of input capacitance, while C4 adds phase lead to compensate the phase lag of the second amplifier.

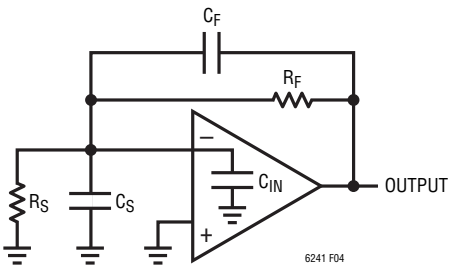



Figure 4. Compensating Input Capacitance

## APPLICATIONS INFORMATION

The op amp's good input offset voltage match and low input bias current means that the typical differential output offset voltage is less than 40µV. A noise spectrum plot of the differential output is shown in Figure 5.

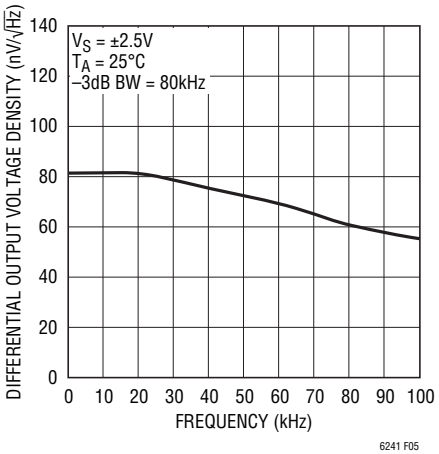



**Figure 5. Differential Output Noise**

### Achieving Low Input Bias Current

The DD package is leadless and makes contact to the PCB beneath the package. Solder flux used during the attachment of the part to the PCB can create leakage current paths and can degrade the input bias current performance of the part. All inputs are susceptible because the backside paddle is connected to V⁻ internally. As the input voltage changes or if V⁻ changes, a leakage path can be formed and alter the observed input bias current. For lowest bias current, use the LTC6240/LTC6241 in the SO-8 and provide a guard ring around the inputs that are tied to a potential near the input voltage.

### Layout Considerations and a PCB Guard Ring

In high source impedance applications such as pH probes, photodiodes, strain gauges, et cetera, the low input bias current of these parts requires a clean board layout to minimize additional leakage current into a high impedance signal node. A mere 100GΩ of PC board resistance between a 5V supply trace and an input trace adds 50pA of leakage current, far greater then the input bias current of the operational amplifier. A guard ring around the high impedance input traces driven by a low impedance source equal to the input voltage prevents such leakage problems.

The guard ring should extend as far as necessary to shield the high impedance signal from any and all leakage paths. Figure 6 shows the use of a guard ring on the LTC6241 in a unity gain configuration. In this case the guard ring is connected to the output and is shielding the high impedance noninverting input from V⁻. Figure 7 shows the inverting gain configuration.

### A Digitally Programmable AC Difference Amplifier

The LTC6241 configured as a difference amplifier, can be combined with a programmable gain amplifier (PGA) to obtain a low noise high speed programmable difference amplifier. Figure 8 shows the LTC6241 based as a single-supply AC amplifier. One LTC6241 op amp is used at the circuit's input as a standard four resistor difference amplifier.

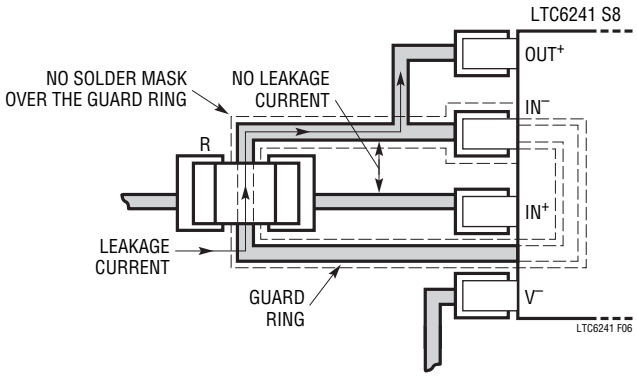



**Figure 6. Sample Layout. Unity Gain Configuration, Using Guard Ring to Shield High Impedance Input from Board Leakage**

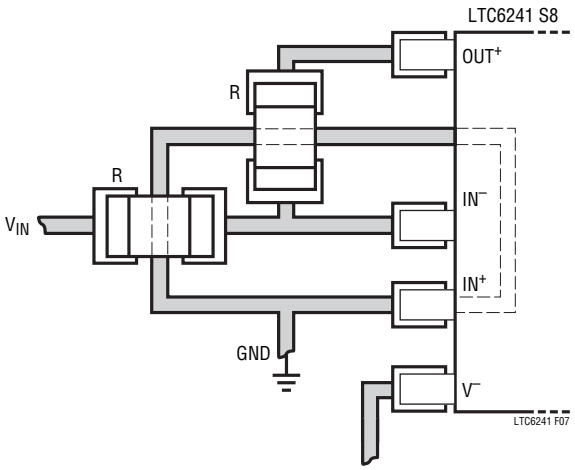
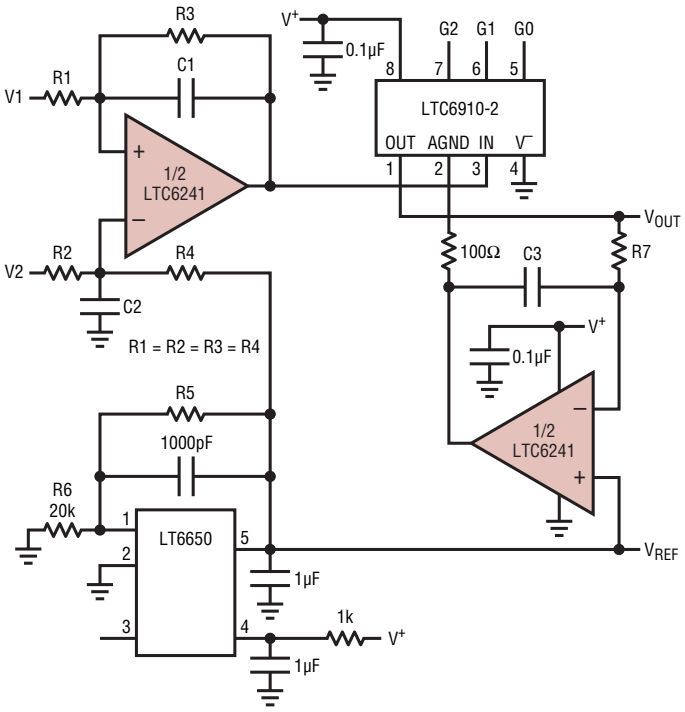



**Figure 7. Sample Layout. Inverting Gain Configuration, Using Guard Ring to Shield High Impedance Input from Board Leakage**

## APPLICATIONS INFORMATION




| DIGITAL INPUTS G2 | G1 | G0 | GAIN |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | –1 |
| 0 | 1 | 0 | –2 |
| 0 | 1 | 1 | –4 |
| 1 | 0 | 0 | –8 |
| 1 | 0 | 1 | –16 |
| 1 | 1 | 0 | –32 |
| 1 | 1 | 1 | –64 |

$V_{OUT} = (V1 - V2)\ GAIN + V_{REF}$

$V_{REF} = 0.4 \bullet \left(\frac{R5}{R6} + 1\right)$

$R5 = 10k \bullet (5 \bullet V_{REF} - 2)$ $R6 = 20k$

$-3d\ BANDWIDTH = (f_{HIGH} - f_{LOW})$

$f_{HIGH} = \frac{1}{2 \bullet \pi \bullet R3 \bullet C1}$ $f_{LOW} = \frac{GAIN}{2 \bullet \pi \bullet R7 \bullet C3}$

6241 F08

**Figure 8. Wideband Difference Amplifier with High Input Impedance and Digitally Programmable Gain**

The low bias current and current noise of the LTC6241 allow the use of high valued input resistors, 100k or greater. Resistors R1, R2, R3 and R4 are equal and the gain of the difference amplifier is one. An LTC6910-2 PGA amplifies the difference amplifier output with inverting gains of –1, –2, –4, –8, –16, –32 and –64. The second LTC6241 op amp is used as an integrator to set the DC output voltage equal to the LT6650 reference voltage $V_{REF}$. The integrator drives the PGA analog ground to provide a feedback loop, in addition to blocking any DC voltage through the PGA. The reference voltage of the LT6650 can be set to a voltage from 400mV to $V^+$ – 350mV with resistors R5 and R6. If R6 is 20k or less, the error due to the LT6650 op amp bias current is negligible. The low voltage offset and drift of the LTC6241 integrator will not contribute any significant error to the LT6650 reference voltage. The LT6650 $V_{REF}$ voltage has a maximum error of ±2% with 1% resistors. The upper –3dB frequency of the amplifier is set by resistor R3 and capacitor C1 and is limited by the bandwidth of the PGA when operated at a gain of 64. Capacitor C2 is equal to C1 and is added to maintain good common mode rejection at high frequency. The lower –3dB frequency is set by the integrator resistor R7, capacitor C3, and the gain setting of the LTC6910-2 PGA. This lower –3dB zero frequency is multiplied by the PGA gain. The rail-to-rail output of the LTC6910-2 PGA allows for a maximum output peak-to-peak voltage equal to twice the $V_{REF}$ voltage. At the maximum gain setting of 64, the maximum peak-to-peak difference between inputs V1 and V2 is equal to twice $V_{REF}$ divided by 64.

**Example Design:** Design a programmable gain AC difference amplifier, with a bandwidth of at least 10Hz to 100kHz, an input impedance equal to or greater than 100kΩ, and an output DC reference equal to 1V.

a. Select input resistors R1, R2, R3 and R4 equal to 100k.

b. If the upper –3dB frequency is 100kHz then C1 = 1/(2π • R2 • f3dB) = 1/(6.28 • 100kΩ • 100kHz) = 15pF (to the nearest 5% value) and C2 = C1 = 15pF.

c. Select R7 equal to one 1M and set the lower –3dB frequency to 10Hz at the highest PGA gain of 64, then C3 = Gain/(2π • R7 • f3dB) = 64/(6.28 • 100kΩ • 10Hz) = 1µF. Lower gains settings will give a lower f3dB.

d. Calculate the value of R5 to set the LT6650 reference equal to 1V;

$V_{REF}$ = 0.4(R5/R6 + 1), so R5 = R6(2.5$V_{REF}$ – 1). For R6 = 20kΩ, R5 = 30kΩ

With $V_{REF}$ = 1V the maximum input difference voltage is equal to 2V/64 = 31.2mV.

### 40nVpp Noise, 0.05µV/°C Drift, Chopped FET Amplifier

Figure 9's circuit combines the ±5V rail-to-rail performance of the LTC6241HV with a pair of extremely low noise JFETs configured in a chopper based carrier modulation scheme

## APPLICATIONS INFORMATION

to achieve an extraordinarily low noise and low DC drift. The performance of this circuit is suited for the demanding transducer signal conditioning situations such as high resolution scales and magnetic search coils.

The LTC1799's output is divided down to form a 2-phase 925Hz square wave clock. This frequency, harmonically unrelated to 60Hz, provides excellent immunity to harmonic beating or mixing effects which could cause instabilities. S1 and S2 receive complementary drive, causing A1 to see a chopped version of the input voltage. A1's square wave output is synchronously demodulated by S3 and S4. Because these switches are synchronously driven with the input chopper, proper amplitude and polarity information is presented to A2, the DC output amplifier. This stage integrates the square wave into a DC voltage, providing the output. The output is divided down (R2 and R1) and fed back to the input chopper where it serves as a zero signal reference. Gain, in this case 1000, is set by the R1-R2 ratio. Because A1 is AC coupled, its DC offset and drift do not affect the overall circuit offset, resulting in the extremely low offset and drift noted. The JFETs have an input RC damper that minimizes offset voltage contribution due to parasitic switch behavior, resulting in the 1μV offset specification.

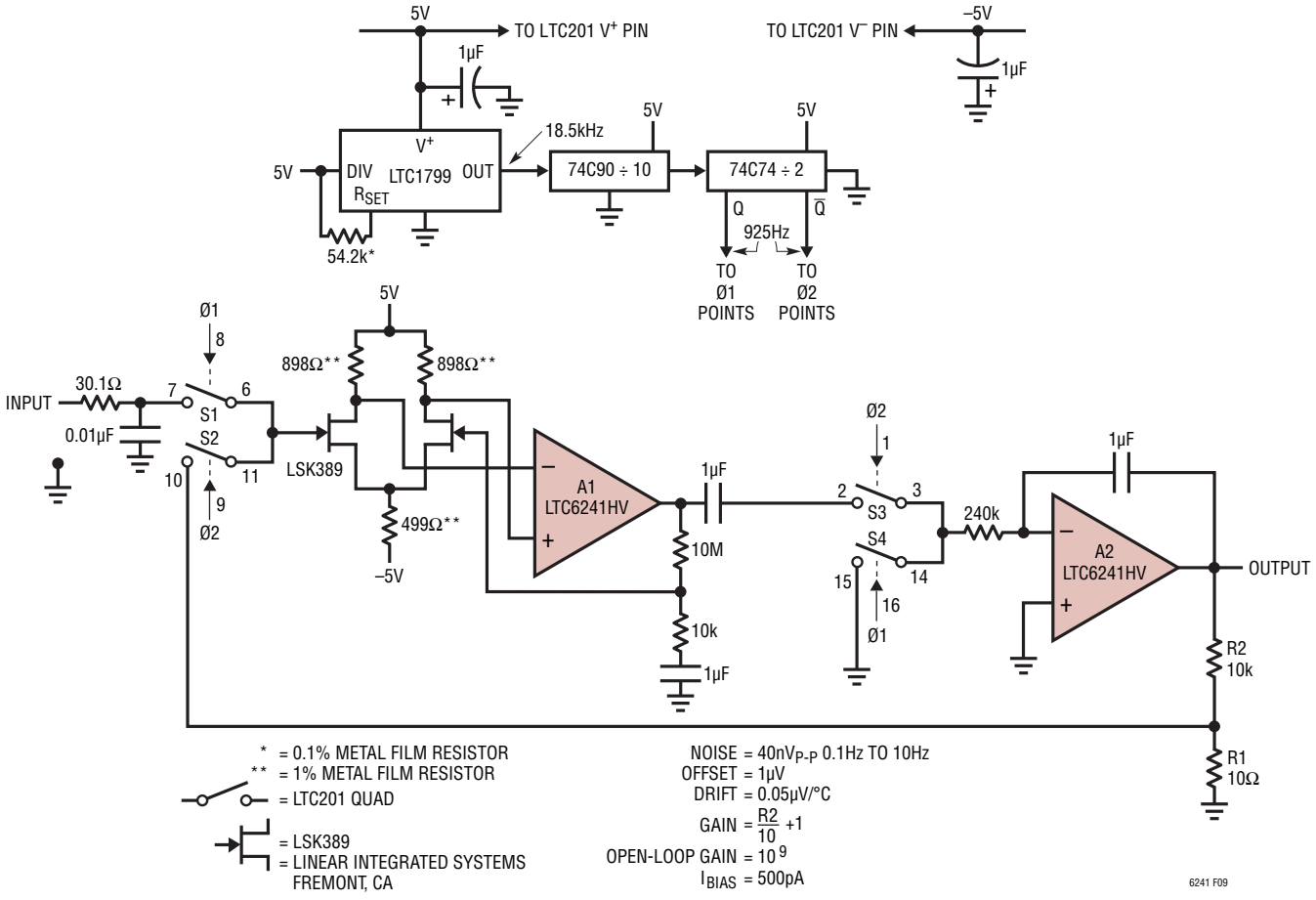



**Figure 9. Ultralow Noise Chopper Amplifier**

## APPLICATIONS INFORMATION

The noise measured over a 50 second interval, in Figure 10, is 40nV in a 0.1Hz to 10Hz bandwidth. This low noise is attributed to the input JFET's die size and current density.

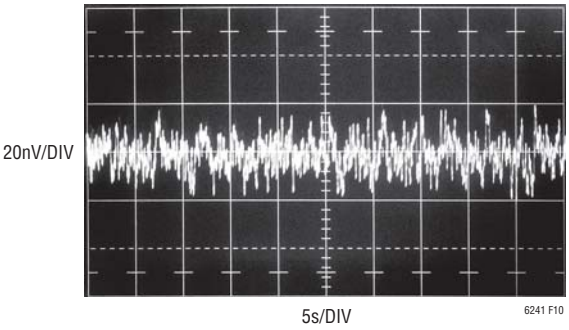



**Figure 10. Noise in a 0.1Hz to 10Hz Bandwidth**

### Low Noise Shock Sensor Amplifiers

Figures 11 and 12 show the amplifiers realizing two different approaches to amplifying signals from a capacitive sensor. The sensor in both cases is a 770pF piezoelectric shock sensor accelerometer, which generates charge under physical acceleration.

Figure 11 shows the classical "charge amplifier" approach. The LTC6240 is in the inverting configuration so the sensor looks into a virtual ground. All of the charge generated by the sensor is forced across the feedback capacitor by the op amp action. Because the feedback capacitor is 100 times smaller than the sensor, it will be forced to 100 times what would have been the sensor's open circuit voltage. So the circuit gain is 100. The benefit of this approach is that the signal gain of the circuit is independent of any cable capacitance introduced between the sensor and the amplifier. Hence this circuit is favored for remote accelerometers where the cable length may vary. Difficulties with the circuit are inaccuracy of the gain setting with the small capacitor, and low frequency cutoff due to the bias resistor working into the small feedback capacitor.

Figure 12 shows a noninverting amplifier approach. This approach has many advantages. First of all, the gain is set accurately with resistors rather than with a small capacitor. Second, the low frequency cutoff is dictated by the bias resistor working into the large 770pF sensor, rather than into a small feedback capacitor, for lower frequency response. Third, the noninverting topology can be paralleled and summed (as shown) for scalable reductions in voltage noise. The only drawback to this circuit is that the parasitic capacitance at the input reduces the gain slightly. This circuit is favored in cases where parasitic input capacitances such as traces and cables will be relatively small and invariant.

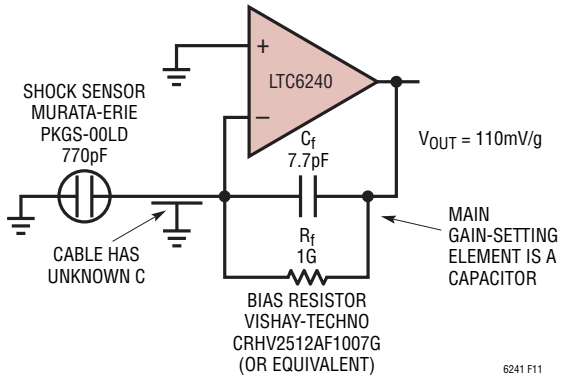



**Figure 11. Classical Inverting Charge Amplifier**

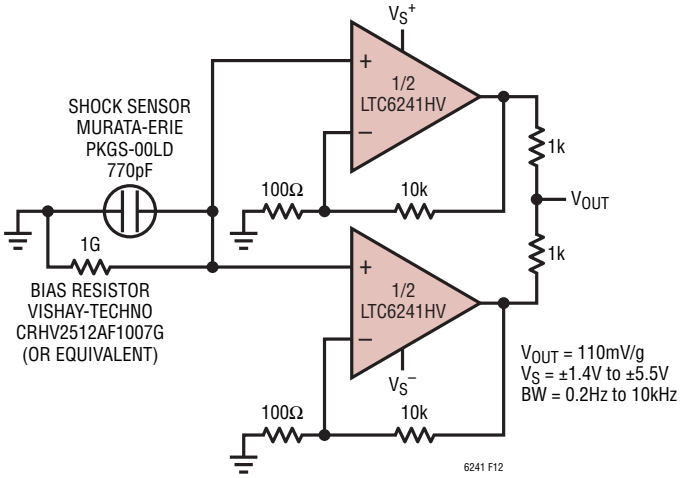



**Figure 12. Low Noise Noninverting Shock Sensor Amplifier**

## APPLICATIONS INFORMATION

### 1M Transimpedance Amplifier with 43nV/√Hz Output Noise

In a normal 1M transimpedance amplifier, like that shown on the back page of this data sheet, the output noise density must be at least 130nV/√Hz at room temperature. This is true even should the op amp be perfectly noiseless, because the 1M resistor provides 130nV/√Hz of voltage noise at room temperature independently of the op amp.

The circuit of Figure 13 provides an overall transimpedance gain of 1MΩ, but it has an output noise density of only 43nV/√Hz, about 1/3 of the normal transimpedance amplifier. It does this by taking a higher initial transimpedance gain of 10M and then attenuating by a factor of 10. The transistor section provides voltage gain and works on a 54V supply voltage to guarantee adequate output swing.

By achieving an output swing of 50V before attenuation, the circuit provides an output swing to 5V after attenuation. The 10M resistor sets the gain of the TIA stage and has a noise density of 400nV/√Hz. After attenuation, the effective TIA gain drops to 1M while the noise floor drops to 40nV/√Hz, which clearly dominates the observed 43nV/√Hz. Note the additional benefit that the offset voltage of the op amp is divided by 10. Worst-case output offset for this circuit is 150µV over temperature.

### Reference Buffer

Figure 14 shows the LTC6240 being utilized as a buffer in conjunction with the LT1019 reference. The passive R-C filter attenuates the reference noise and the LTC6240 provides a low noise buffer, resulting in an output noise of 8nV/√Hz.

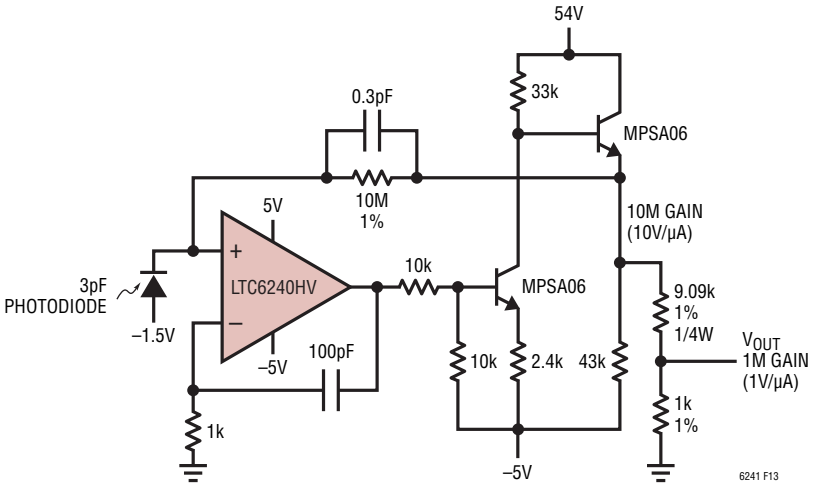



**Figure 13. 1M Transimpedance Amplifier with 43nV/√Hz Output Noise**

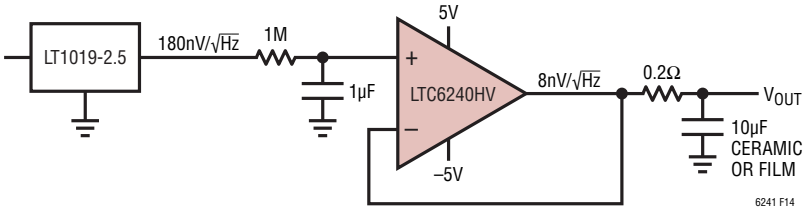
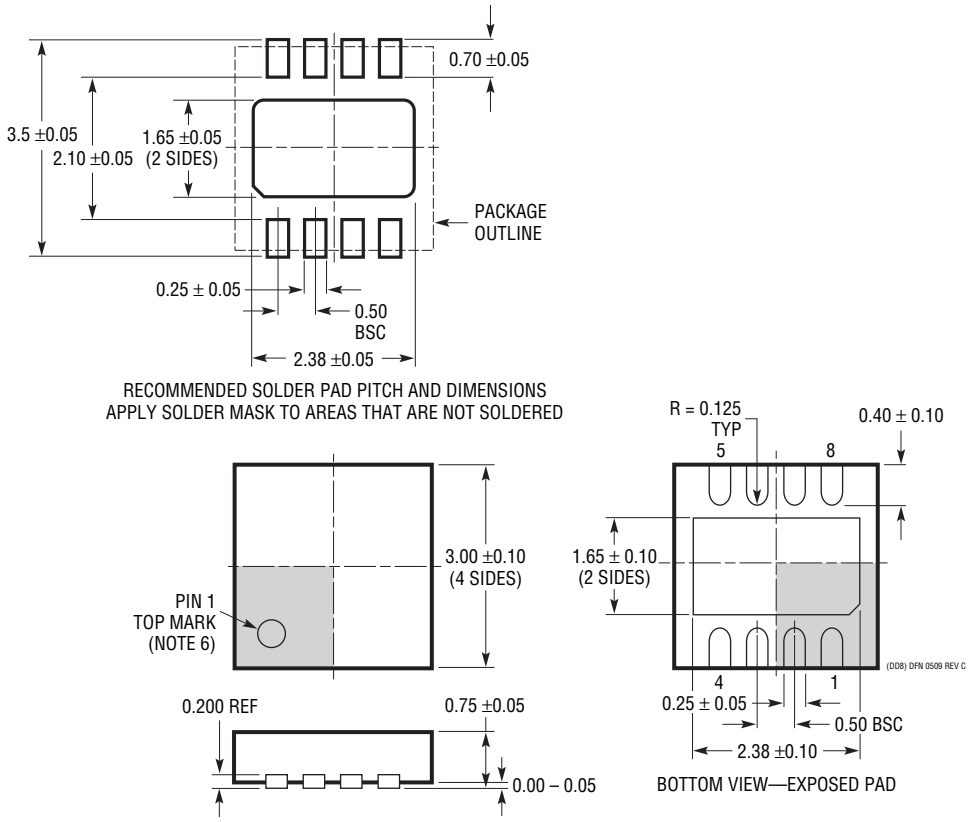



**Figure 14. Low Noise Reference Buffer**

## PACKAGE DESCRIPTION

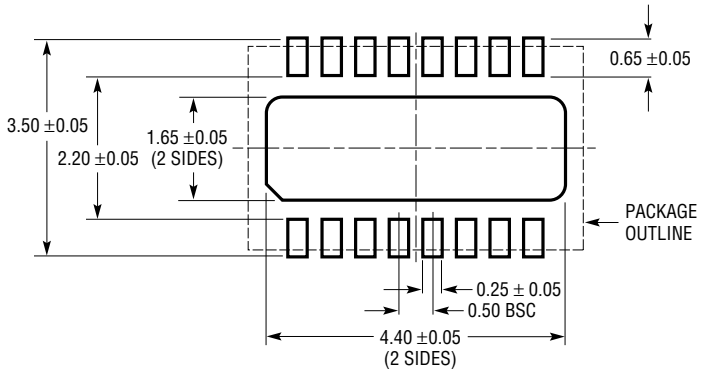
**DD Package**
**8-Lead Plastic DFN (3mm × 3mm)**
(Reference LTC DWG # 05-08-1698)



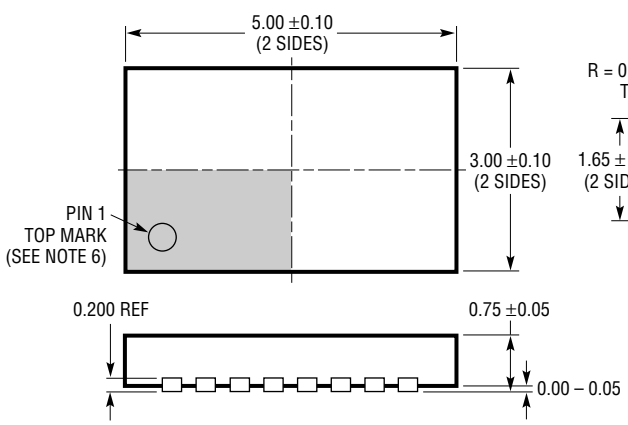

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

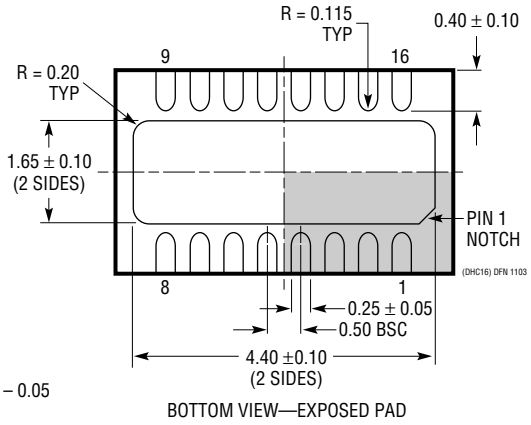
# PACKAGE DESCRIPTION

**DHC Package**
**16-Lead Plastic DFN (5mm × 3mm)**
(Reference LTC DWG # 05-08-1706)




**RECOMMENDED** SOLDER PAD PITCH AND DIMENSIONS



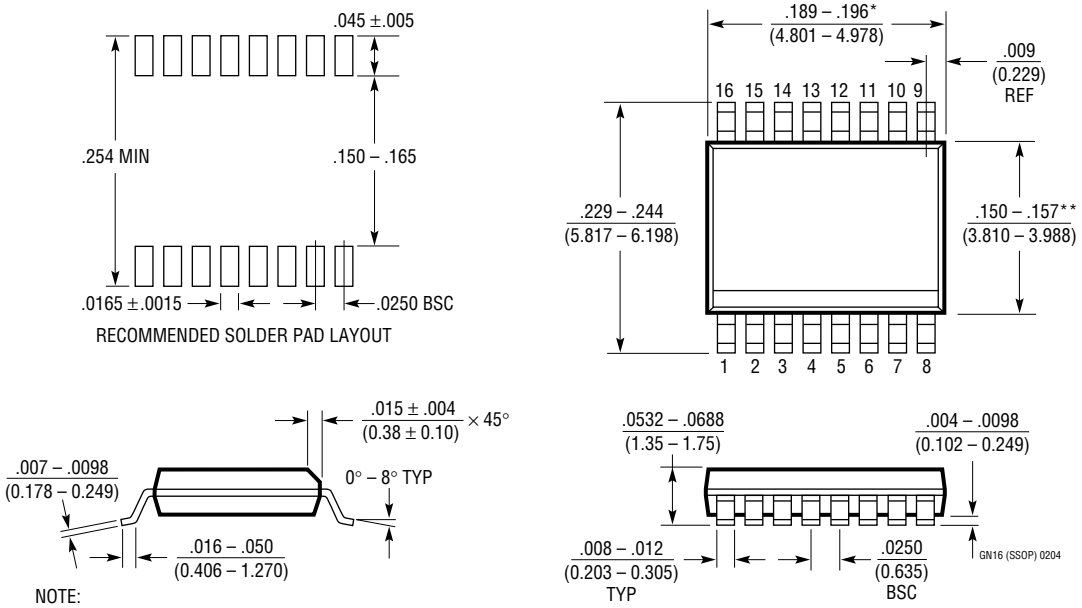




BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJED-1) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

# PACKAGE DESCRIPTION

**GN Package**
**16-Lead Plastic SSOP (Narrow .150 Inch)**
(Reference LTC DWG # 05-08-1641)



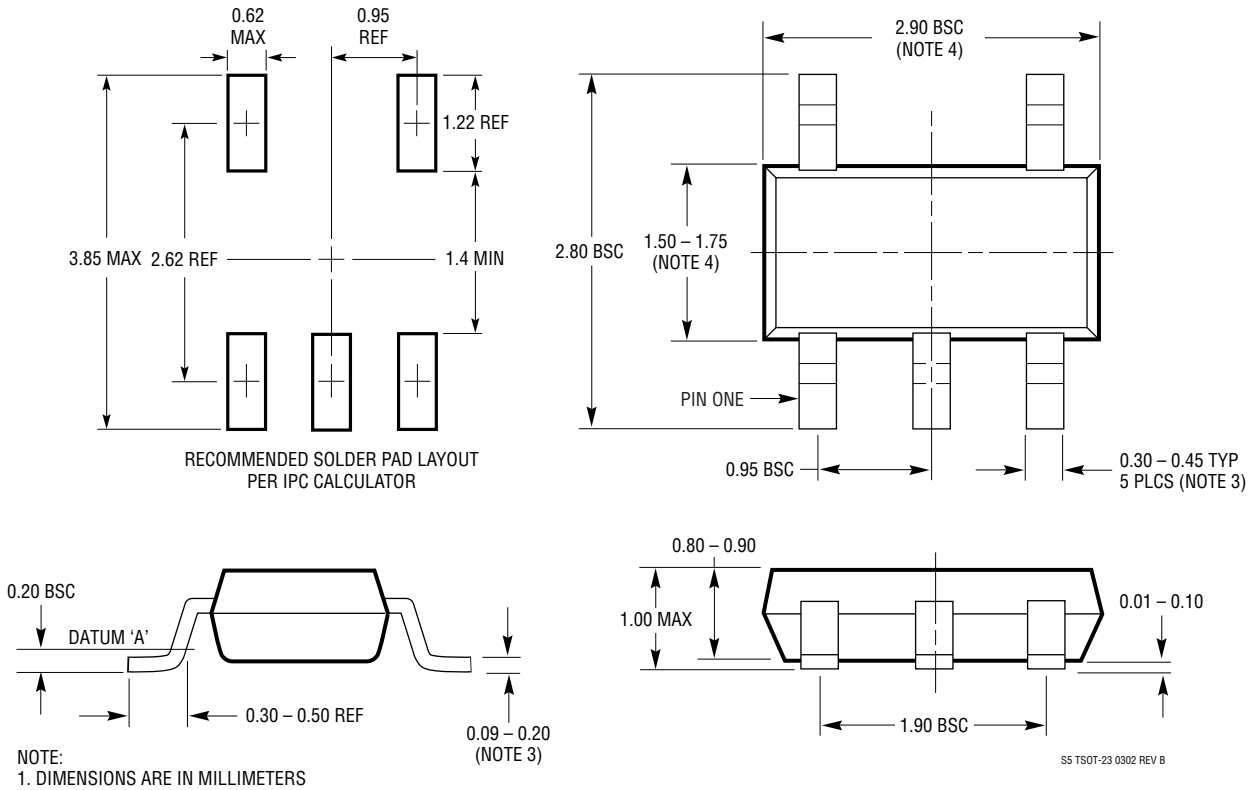

NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

# PACKAGE DESCRIPTION

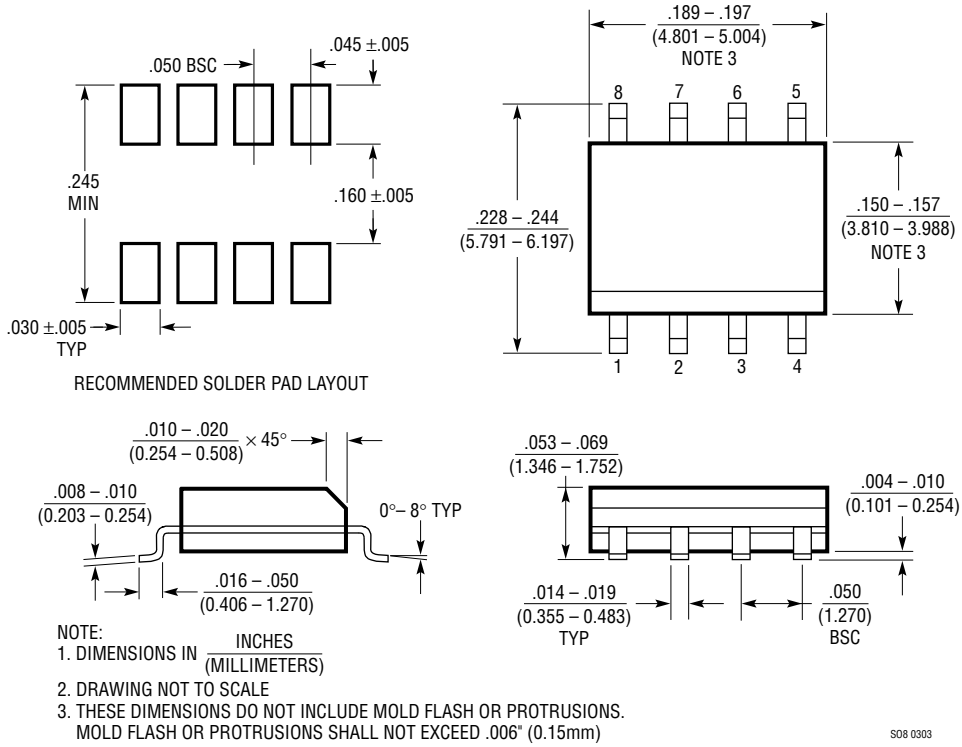
**S5 Package**
**5-Lead Plastic TSOT-23**
(Reference LTC DWG # 05-08-1635 Rev B)




NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

## PACKAGE DESCRIPTION

**S8 Package**
**8-Lead Plastic Small Outline (Narrow .150 Inch)**
(Reference LTC DWG # 05-08-1610)




NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

SO8 0303

## REVISION HISTORY (Revision history begins at Rev E)

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| E | 07/10 | Update to Simplified Schematic (Figure 1) | 19 |



LINEAR TECHNOLOGY

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

## TYPICAL APPLICATION

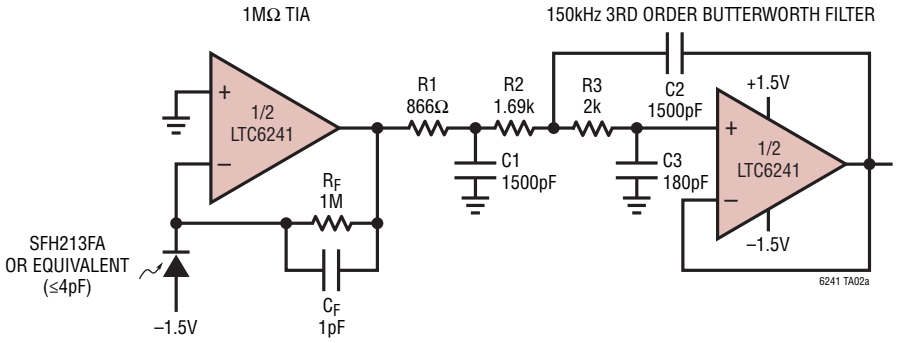
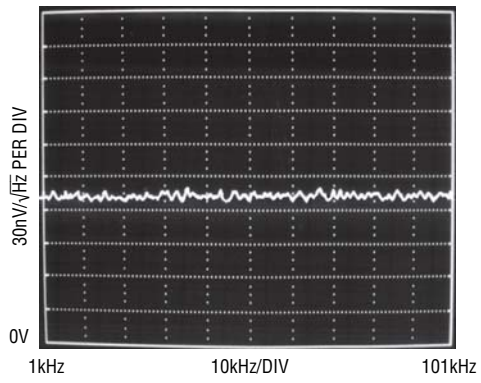
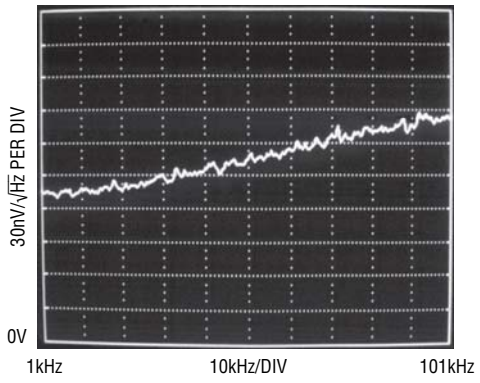



**Figure 15. Ultralow Noise 1MΩ 150kHz Photodiode Amplifier**

**LTC6241 Output Noise Spectrum. 1MΩ Resistor Noise Dominates; Ideal Performance**




**Competition Output Noise Spectrum. Op Amp Noise Dominates; Performance Compromised**




## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC1151 | ±15V Zero-Drift Op Amp | Dual High Voltage Operation ±18V |
| LT1792 | Low Noise Precision JFET Op Amp | 6nV/√Hz Noise, ±15V Operation |
| LTC2050 | Zero-Drift Op Amp | 2.7 Volt Operation, SOT-23 |
| LTC2051/LTC2052 | Dual/Quad Zero-Drift Op Amp | Dual/Quad Version of LTC2050 in MS8/GN16 Packages |
| LTC2054/LTC2055 | Single/Dual Zero-Drift Op Amp | Micropower Version of the LTC2050/LTC2051 in SOT-23 and DD Packages |
| LTC6244 | Dual 50MHz Rail-to-Rail Op Amp | 100μV $V_{OS(MAX)}$, 1pA $I_{BIAS}$, 40V/μV, Slew Rate |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